Design of Digital Systems

# Lab Instructions

**General Instructions:**

* Lab assignment submission due date are announced on Canvas.
* All lab assignments should be submitted electronically through Canvas.
* Lab submitted after due date are penalized 5% for every day submitted past the due date.
* Labs not turned in after 7 days of due date are given a grade of 0.
* No labs will be dropped.
* Many labs are interdependent, so you should try to be on time for all labs.
* If there are special circumstances involved with late labs, talk to the professor and/or TA as early as possible.
* Submit four files in the canvas submission. Any missing file will not be graded.
  + Design source code VHDL file
  + Simulation source code VHDL file
  + Constraint source code XDC file
  + Lab report PDF file following lab

**Point Distributions:**

70%: Source code. The source codes should be contained in 3 files.

* Copy all design source code into one .vdh file
* Copy all simulation source code into one .vhd file
* Copy all constraint source code into one .xdc file

30%: Lab report

* Written professionally
* Follows the format written on page 2
* Assignments with missing cover page will NOT be graded

**Lab Report Format:**

Lab reports must include the following sections.

1. Cover page on the first page: A sample cover page is provided on canvas. The cover page **MUST** include the following notice unmodified with your signature or full name placed in the signature field. The assignment will not be graded if this notice is missing in the cover page.

By submitting this report, you attest that you neither have given nor have received any assistance (including writing, collecting data, plotting figures, tables, or graphs, or using previous student assignments as a reference), and you further acknowledge that giving or receiving such assistance will result in a failing grade for this course.

|  |  |
| --- | --- |
| Your Signature: | <FULL NAME OR SIGNATURE> |

1. Simulation results:
   * Screenshot of waveforms with explanation
2. Area implementation results in tabulated form. Area results must show
   * Look-up tables (LUT)
   * Flip-flops (FF)
3. Timing implementation results in tabulated form.
   * Worst negative slack
   * Critical path delay
   * Maximum Frequency
4. FPGA Demo. Must cover every case to receive the full grade. You have multiple options to demo the results in an FPGA:
   * Take pictures of the FPGA covering every case. Make sure to explain each picture in a couple of sentences.
   * Same as above without taking pictures. Instead, you will need to explain how the FPGA will behave.
   * A link to a video recording (streamable.com, youtube.com, …) showing the design running on the FPGA. This is the recommended method for later labs.