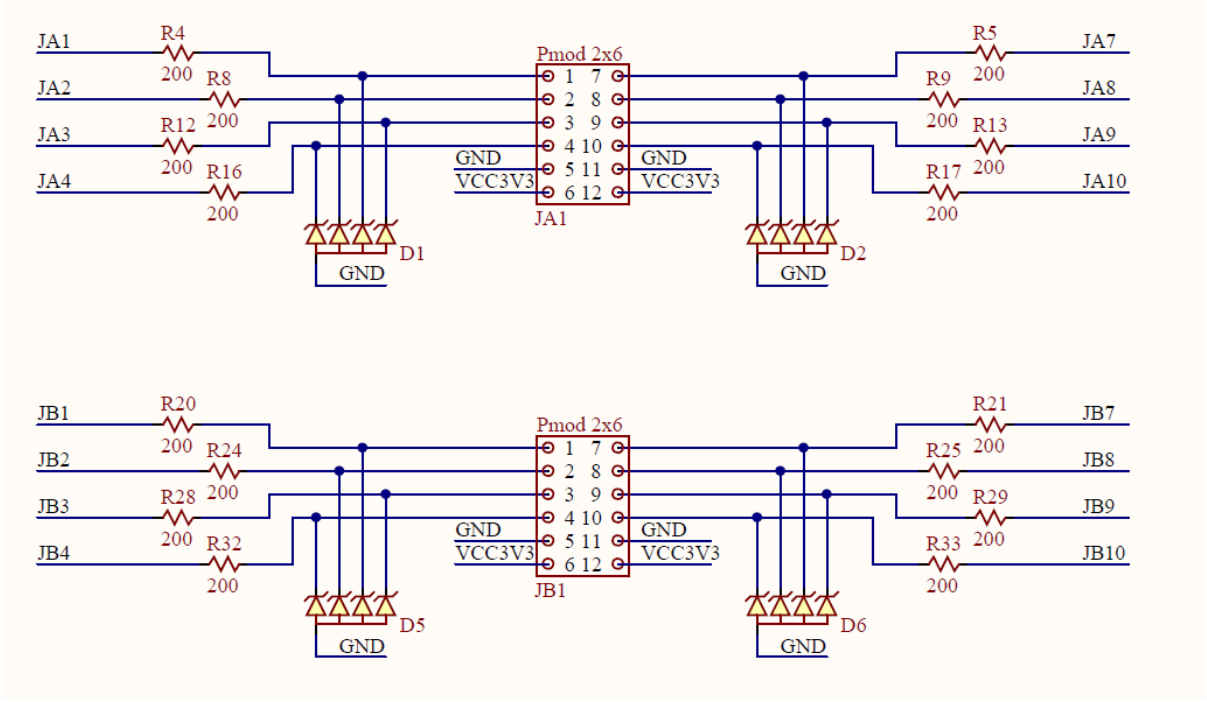
| Signal | Type | Description |
|---|---|---|
| checker_states[2:0] | Status Output | It indicates the current state of the Checker Control Unit.<br><br>0: IDLE<br>1: CHECK STATUS<br>2: CHECKPOINT_FROM_BOTH_CORES<br>3: ROLLBACK<br>4: WAKE_UP_CORES<br>5: WAIT_FOR_STANDBY<br>6: CHECKPOINT_FROM_ONE_CORE<br>7: ROLLFORWARD |
| core_standbywfe[1:0] | Status Output | It reflects the corresponding event_standbywfe status output signals from PS (synchronized to the checker clock) |
| core_parity_error[1:0] | Status Output | It indicates whether the cores have parity error. The signals are cleared when the check state enters WAKE_UP_CORES state. |
| watchdog_timer_expiration | Pulse Output | It indicates that the watchdog timer expired |
| forced_standby_status[1:0] | Status Output | It reflects the corresponding interrupt signal outputs to the PS, one for each APU core to put on demand a core in standby mode, in case one of the two cores is not in standby state. The IRQs can be asserted when checker state is in WAIT_FOR_STANDBY state and they are cleared to all the others states. |
| checkpoint_error_after_boot | Status Output | It indicates the comparison error during the first checkpoint operation (CHECKPOINT_FROM_BOTH_CORES) after system boot. The signal is cleared with the checker's reset |

**Zedboard JA/JB Pinout**

| PMOD PIN | Signal |
|---|---|
| JA1 | checker_state[0] |
| JA2 | checker_state[1] |
| JA3 | checker_state[2] |
| JA4 | core_standbywfe[0] |
| JA7 | core_standbywfe[1] |
| JA8 | forced_standby_status[0] |
| JA9 | forced_standby_status[1] |
| JA10 | watchdog_timer_expiration |
| JB1 | core_parity_error[0] |
| JB2 | core_parity_error[1] |
| JB3 | checkpoint_error_after_boot |


JA1
JA2
JA3
JA4
R4
R8
R12
R16
200
Pmod 2x6
1 7
2 8
3 9
4 10
GND
VCC3V3
5 11
6 12
GND
VCC3V3
JA1
R5
R9
R13
R17
JA7
JA8
JA9
JA10
D1
D2
GND
JB1
JB2
JB3
JB4
R20
R24
R28
R32
JB7
JB8
JB9
JB10
R21
R25
R29
R33
D5
D6