

Features

- Low Voltage and Standard Voltage Operation
 - 5.0 ($V_{CC} = 4.5V$ to $5.5V$)
 - 2.7 ($V_{CC} = 2.7V$ to $5.5V$)
 - 2.5 ($V_{CC} = 2.5V$ to $5.5V$)
 - 1.8 ($V_{CC} = 1.8V$ to $5.5V$)
- Internally Organized 2048 x 8 (16K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 KHz (1.8V, 2.5V, 2.7V) and 400 KHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- Cascadable Feature Allows for Extended Densities
- 16-Byte Page Write Mode
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
 - ESD Protection: >3,000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin JEDEC SOIC and 8-Pin PDIP Packages

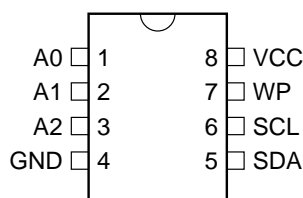
Description

The AT24C164 provides 16,384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 2048 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C164 is available in space saving 8-pin PDIP and 8-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, this device is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

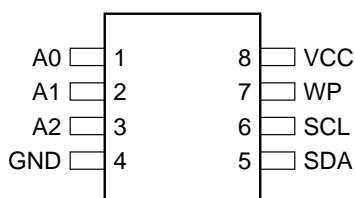
Pin Configurations

Pin Name	Function
A0 to A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

8-Pin PDIP



8-Pin SOIC



2-Wire Serial EEPROM

16K (2048 x 8)

AT24C164



Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage.....	6.25V
DC Output Current.....	5.0 mA

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The block diagram illustrates the internal architecture of the 24C02. It features several key components and their interconnections:

- Inputs:** V_{CC} , GND, WP (Write Protect), SCL (Serial Clock), SDA (Serial Data), and address lines A_2 , A_1 , and A_0 .
- START STOP LOGIC:** Receives SCL and SDA inputs and provides control signals to the SERIAL CONTROL LOGIC.
- SERIAL CONTROL LOGIC:** Manages data flow between the SDA line and internal components. It receives EN (Enable) from the H.V. PUMP/TIMING block and provides LOAD and INC signals to the DATA WORD ADDR/COUNTER.
- DEVICE ADDRESS COMPARATOR:** Receives address inputs A_2 , A_1 , and A_0 (with A_1 inverted). It provides a COMP (Compare) signal to the SERIAL CONTROL LOGIC and an R/W (Read/Write) signal to the DATA WORD ADDR/COUNTER.
- DATA WORD ADDR/COUNTER:** Receives LOAD and INC signals. It provides an X DEC (X Decrement) signal to the E²PROM and a Y DEC (Y Decrement) signal to the SERIAL MUX.
- H.V. PUMP/TIMING:** Provides the EN signal to the SERIAL CONTROL LOGIC.
- DATA RECOVERY:** Receives signals from the SERIAL CONTROL LOGIC and the SERIAL MUX.
- E²PROM:** The non-volatile memory array, receiving X DEC and Y DEC signals.
- SERIAL MUX:** Routes data between the E²PROM and the D_{OUT}/ACK LOGIC.
- D_{OUT}/ACK LOGIC:** Manages data output (D_{OUT}) and acknowledgment (ACK) signals. It receives D_{IN} (Data Input) and provides D_{OUT} to the output pin.

DEVICE SELECT (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that may be hardwired or actively driven to V_{DD} or V_{SS} . These inputs allow the selection for

The AT24C164 is internally organized with 256 pages of 8 bytes each. Random word addressing requires an 11 bit data word address.

Pin Capacitance⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +1.8\text{V}$.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
C_{IN}	Input Capacitance (A_0 , A_1 , A_2 , SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: $T_{AI} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $T_{AC} = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.5		5.5	V
V_{CC3}	Supply Voltage		2.7		5.5	V
V_{CC4}	Supply Voltage		4.5		5.5	V
I_{CC}	Standby Current $V_{CC} = 5.0\text{V}$	READ at 100 KHz		0.4	1.0	mA
I_{CC}	Standby Current $V_{CC} = 5.0\text{V}$	WRITE at 100 KHz		2.0	3.0	mA
I_{SB1}	Standby Current $V_{CC} = 1.8\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		0.6	3.0	μA
I_{SB2}	Standby Current $V_{CC} = 2.5\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.4	4.0	μA
I_{SB3}	Standby Current $V_{CC} = 2.7\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		1.6	4.0	μA
I_{SB4}	Standby Current $V_{CC} = 5.0\text{V}$	$V_{IN} = V_{CC}$ or V_{SS}		8.0	18.0	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or V_{SS}		0.10	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or V_{SS}		0.05	3.0	μA
V_{IL}	Input Low Level ⁽¹⁾		-0.6		$V_{CC} \times 0.3$	V
V_{IH}	Input High Level ⁽¹⁾		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level $V_{CC} = 3.0\text{V}$	$I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OL1}	Output Low Level $V_{CC} = 1.8\text{V}$	$I_{OL} = 0.15\text{ mA}$			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $CL = 1$ TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7-, 2.5-, 1.8-volt		5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	KHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		μs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		μs
t_I	Noise Suppression Time ⁽¹⁾		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	μs
t_{BUF}	Time the bus must be free before a new transmission can start ⁽¹⁾	4.7		1.2		μs
$t_{HD,STA}$	Start Hold Time	4.0		0.6		μs
$t_{SU,STA}$	Start Set-up Time	4.7		0.6		μs
$t_{HD,DAT}$	Data In Hold Time	0		0		μs
$t_{SU,DAT}$	Data In Set-up Time	200		100		ns
t_R	Inputs Rise Time ⁽¹⁾		1.0		0.3	μs
t_F	Inputs Fall Time ⁽¹⁾		300		300	ns
$t_{SU,STO}$	Stop Set-up Time	4.7		0.6		μs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance ⁽¹⁾	5.0V, 25°C, Page Mode	1M		1M		Write cycles

Notes: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

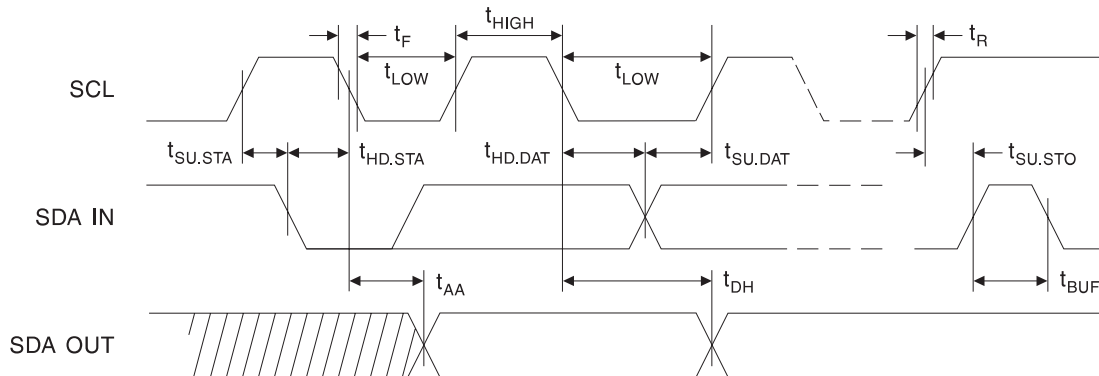
STANDBY MODE: The AT24C164 features a low power standby mode which is enabled: a) upon power-up and b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, the AT24C164 can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

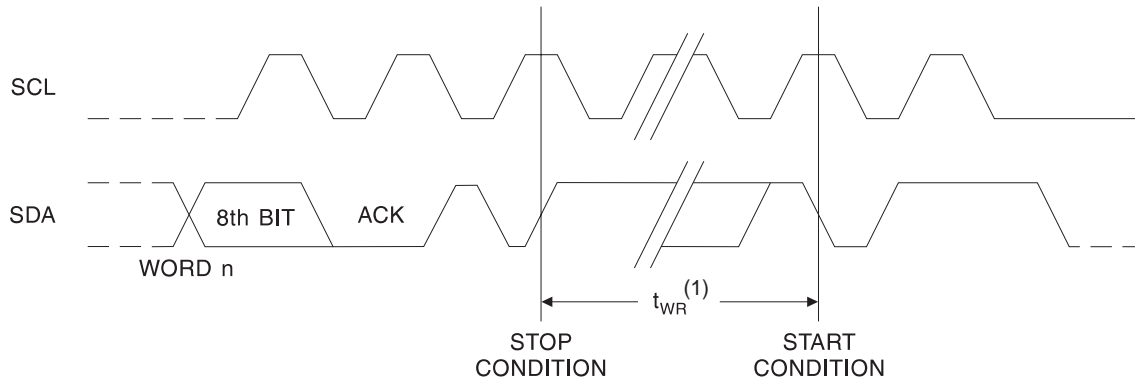
Bus Timing

SCL: Serial Clock, SDA: Serial Data I/O



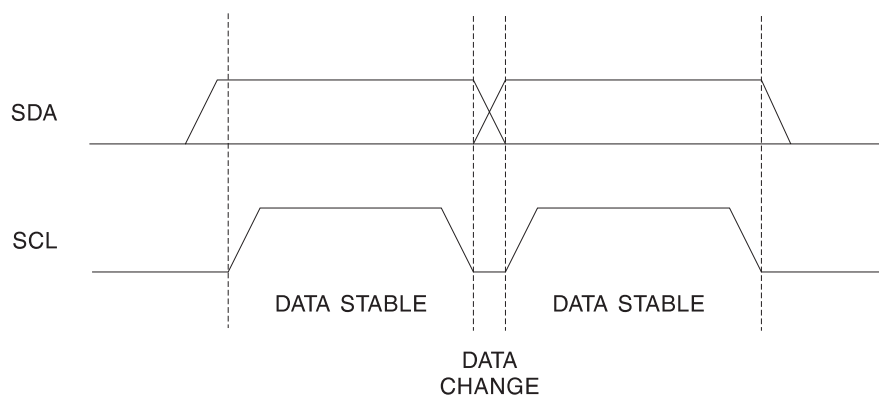
Write Cycle Timing

SCL: Serial Clock, SDA: Serial Data I/O

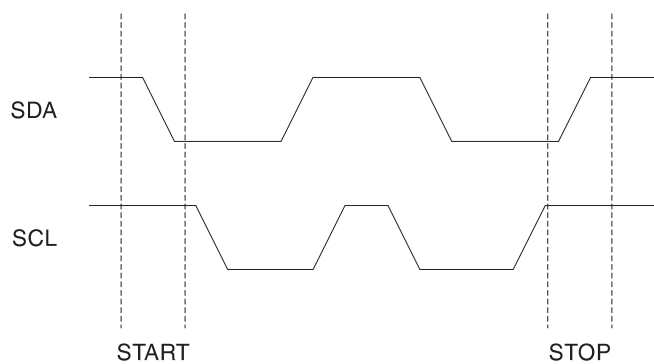


Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

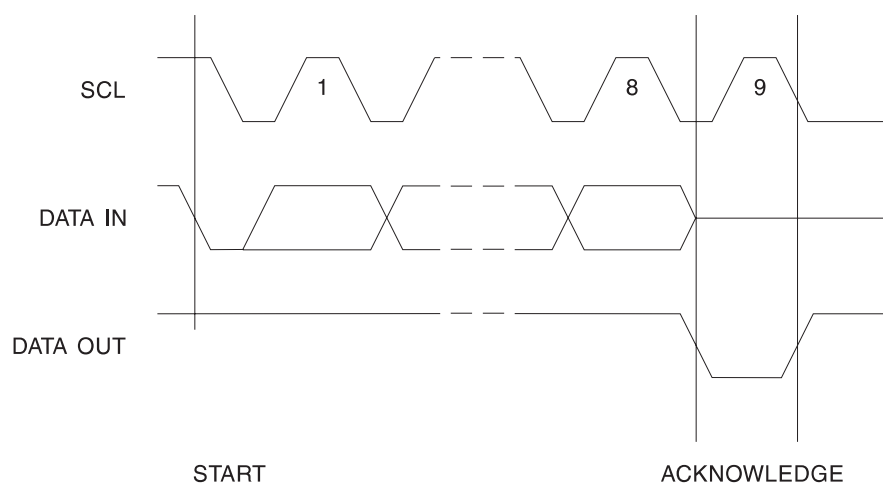
Data Validity



Start and Stop Definition



Output Acknowledge



Device Addressing

The AT24C164 requires an 8-bit device address word following a start condition to enable the chip for read or write operations (refer to Figure 1). The most significant bit must be a one followed by the A2, A1 and A0 device select bits (the A1 bit must be the compliment of the A1 input pin signal). The next 3 bits are used for memory block addressing and select one of the eight 256 x 8 memory blocks. These bits should be considered the three most significant bits of the data word address. The eighth bit of the device address is the read/write select bit. A read operation is selected if this bit is high or a write operation is selected if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Write Operations

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 2).

PAGE WRITE: The AT24C164 is capable of a 16-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 3).

The data word address lower 4 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 4).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 5).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 6).

Figure 1. Device Address

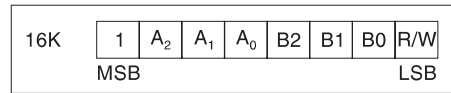


Figure 2. Byte Write

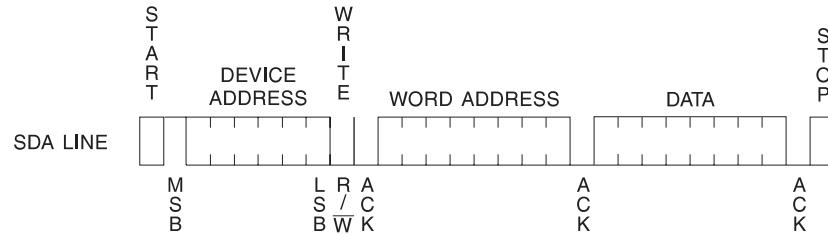


Figure 3. Page Write

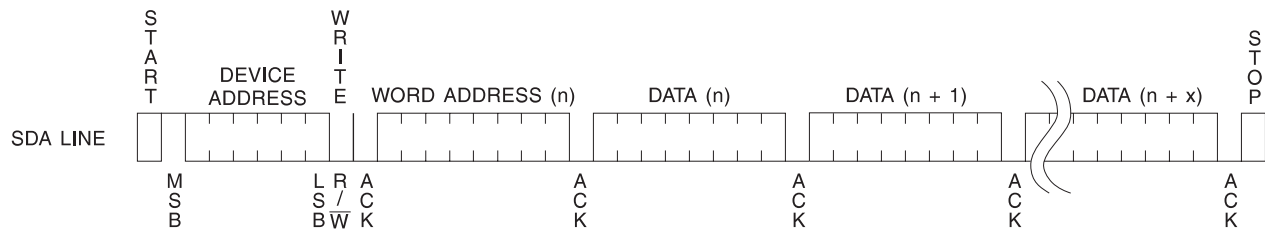


Figure 4. Current Address Read

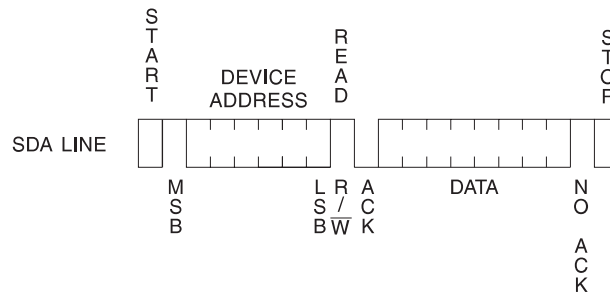


Figure 5. Random Read

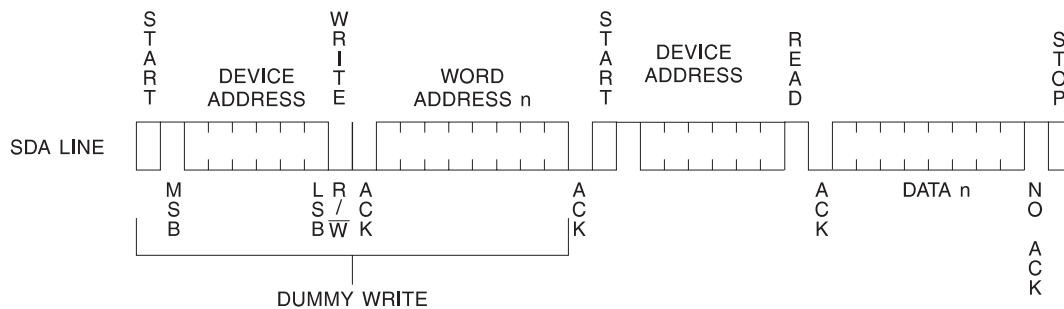
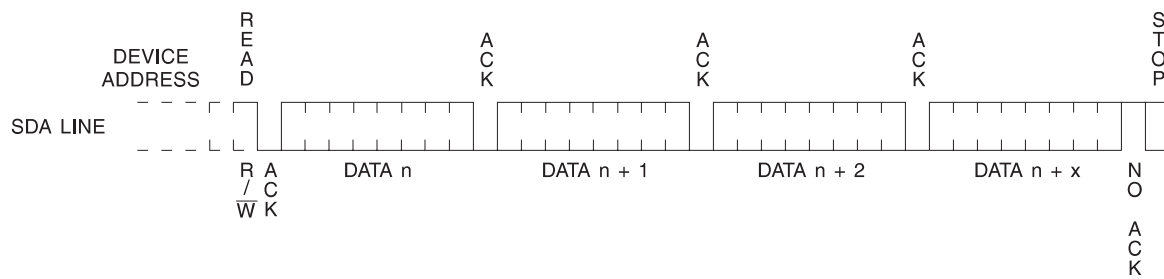


Figure 6. Sequential Read





Ordering Information

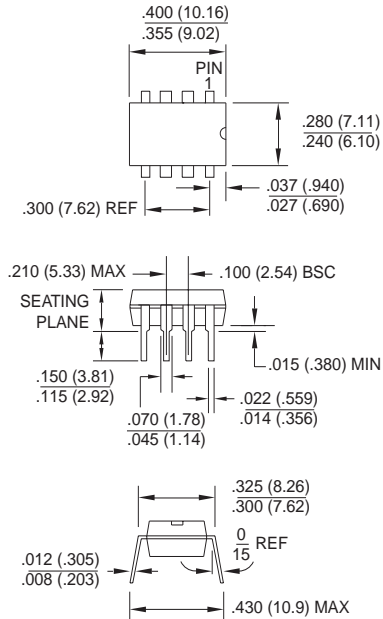
t_{WR} (max) (ms)	I_{CC} (max) (μ A)	I_{SB} (max) (μ A)	f_{MAX} (KHz)	Ordering Code	Package	Operation Range
10	3000	18	400	AT24C164-10PC AT24C164-10SC	8P3 8S1	Commercial (0°C to 70°C)
	3000	18	400	AT24C164-10PI AT24C164-10SI	8P3 8S1	Industrial (-40°C to 85°C)
10	1500	4	100	AT24C164-10PC-2.7 AT24C164-10SC-2.7	8P3 8S1	Commercial (0°C to 70°C)
	1500	4	100	AT24C164-10PI-2.7 AT24C164-10SI-2.7	8P3 8S1	Industrial (-40°C to 85°C)
10	1000	4	100	AT24C164-10PC-2.5 AT24C164-10SC-2.5	8P3 8S1	Commercial (0°C to 70°C)
	1000	4	100	AT24C164-10PI-2.5 AT24C164-10SI-2.5	8P3 8S1	Industrial (-40°C to 85°C)
10	800	4	100	AT24C164-10PC-1.8 AT24C164-10SC-1.8	8P3 8S1	Commercial (0°C to 70°C)
	800	4	100	AT24C164-10PI-1.8 AT24C164-10SI-1.8	8P3 8S1	Industrial (-40°C to 85°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
Options	
Blank	Standard Operation (4.5V to 5.5V)
-2.7	Low-Voltage (2.7V to 5.5V)
-2.5	Low-Voltage (2.5V to 5.5V)
-1.8	Low-Voltage (1.8V to 5.5V)

Packaging Information

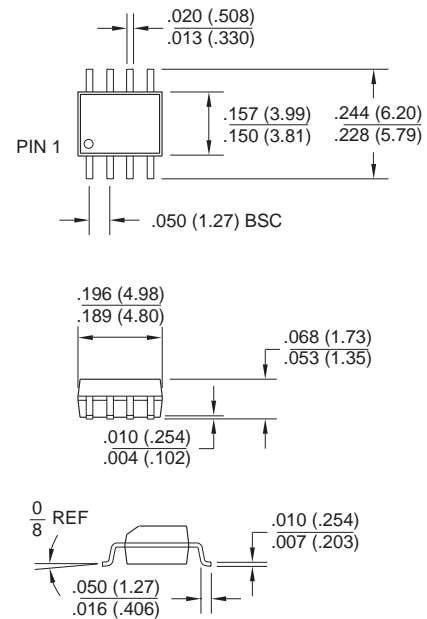
8P3, 8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)

Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



8S1, 8-Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)

Dimensions in Inches and (Millimeters)



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