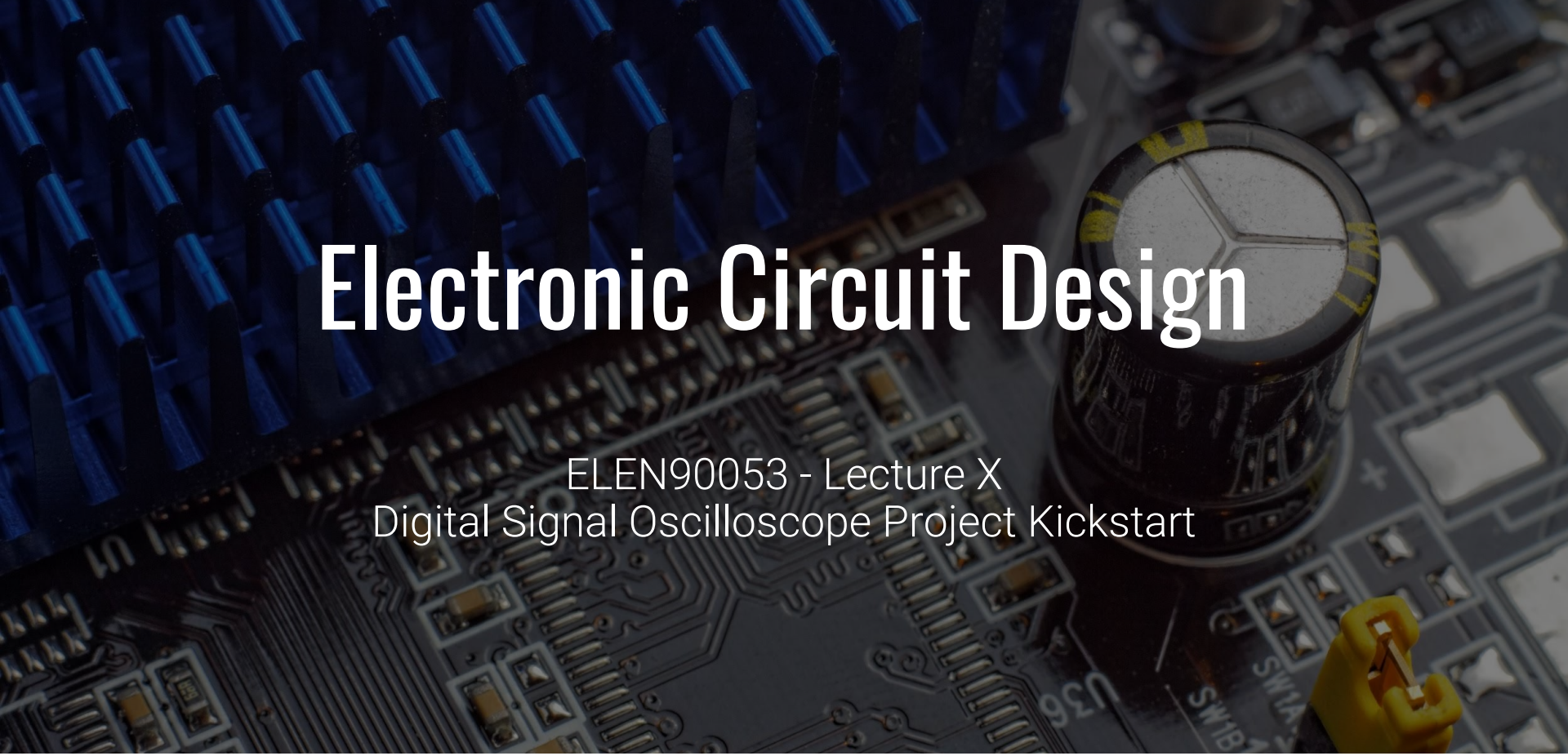


Electronic Circuit Design

ELEN90053 - Lecture X
Digital Signal Oscilloscope Project Kickstart

THE UNIVERSITY OF MELBOURNE

Bryce Widdicombe
Email: bryce.widdicombe@unimelb.edu.au

Summary

- Timeline and Assessment Points
- Project Basics
- Specification Review
- Nyquist Rate
- Antialiasing Filters
- Front End and ADC
- Level Shifting
- DAC
- Bit Banging
- Voltage Referencing
- Triggering
- ATMega16 Introduction
- Phased Locked Loops (PLL)
- DSO Clock
- ATMega Counters and Timers
- Voltage Clamping and Protection
- Power Domains
- Supply Labels
- Power Filtering
- Passive Component Values
- CPLD, FPGA and Discrete ICs
- Advanced Track
- Questions
- Reference Material

Timeline and Assessment Points

Top Level Schematics and Simulation Report - September 1 2018

Gerber Files, Schematics and Bill of Materials (BoM) - September 15 2018

Final Presentation - Last week and Exam Period (TBA)

Reference: https://goo.gl/SxpcLk

Project Basics

- Design, build, program, and test a 20MHz USB Digital Storage Oscilloscope (DSO).
- The project will be made up of:
  - Filters & Signal conditioning
  - Amplifiers
  - A DAC and ADC
  - Clock
  - Glue Logic
  - Data Storage
  - Comparators
  - A microcontroller
  - Power supply components
  - Isolation

Project Specifications

- Refer to the Workshop Manual for full details:
- Points of specific interest based upon the functional spec:
  - 1.0.3 – Input can accept a maximum input of ±5V (Clamping)
  - 2.0.6 – The device will be galvanically isolated from the PC (Power and Data Isolation)
  - 2.0.8 – The +5V and USB 5V rail will not be connected (Power Isolation)
  - 4.0.2 – When the input rises across a trigger threshold, and the device has been instructed to sample, the device will store 65536 8 bit samples in RAM (Comparator)
  - 4.0.3 – The value of the trigger threshold will be set by the PC (DAC, SPI)
  - 6.0.4 – The device will support the following sampling rates: 25ns, 50ns (PLL frequency multiplication, Nyquist Rate)

Nyquist Rate

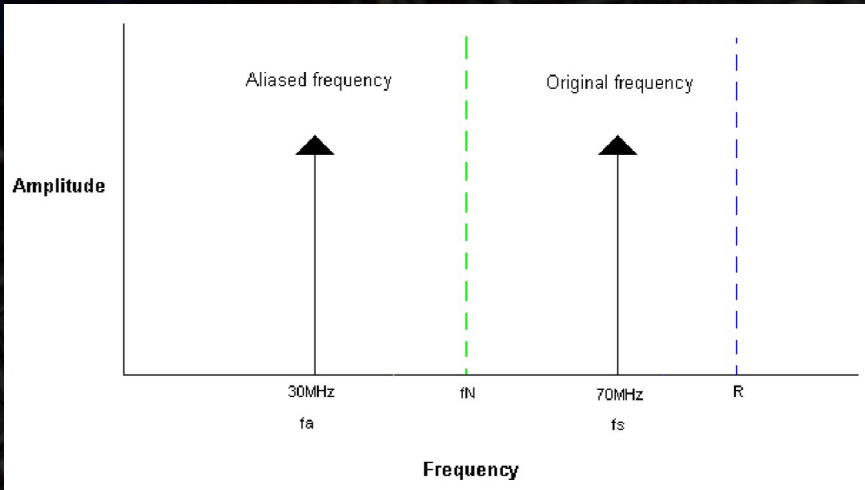
The Nyquist rate is the un-aliased frequency achievable by a given sampling rate such that under perfect conditions this signal could be replicated exactly.

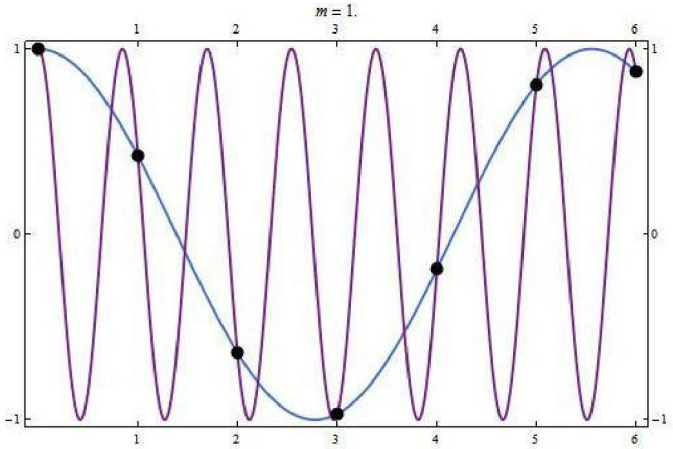
$$F_{NYQUIST} = F_{sample\text{-}rate}/2$$

Any frequency which is above the Nyquist frequency will be folded into the spectrum of interest and as such is said to be “aliased”.

Antialiasing Filters

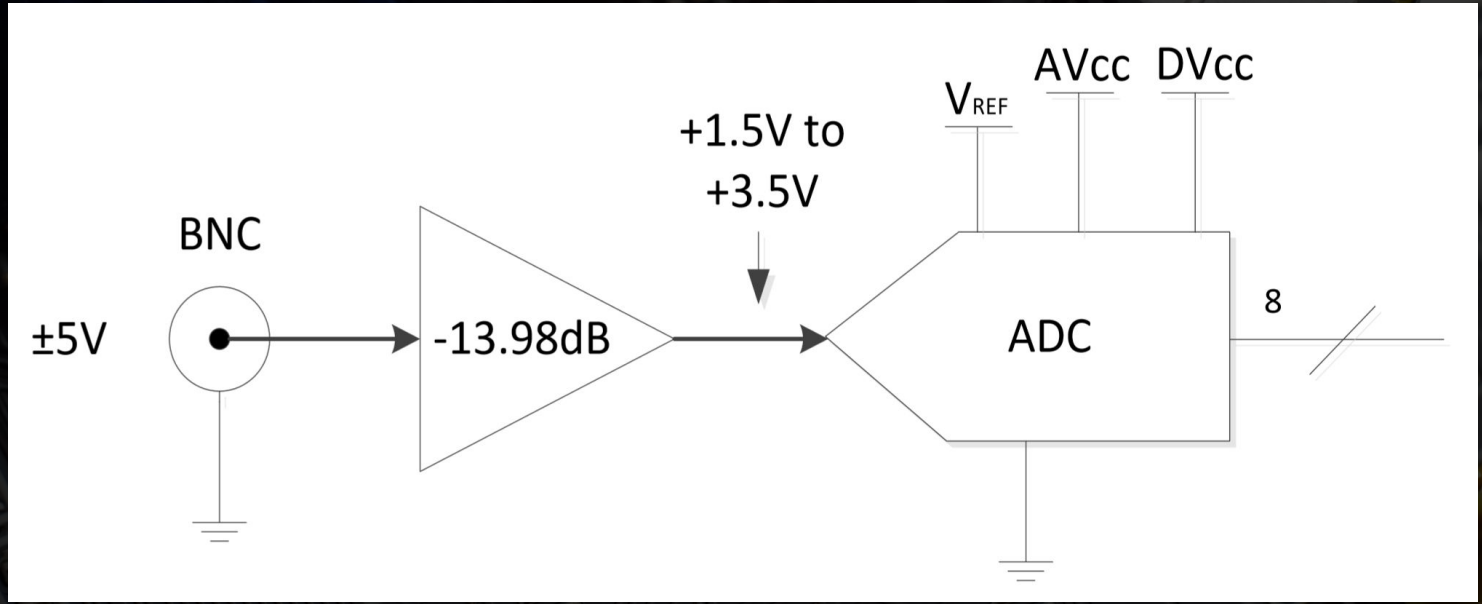
An antialiasing filter removes the components in the analog spectrum of your input signal which would otherwise be aliased into your range of digital input equivalent signals. The corner frequency of your filter needs to be at or below half your sampling frequency and the order is dependent on allowable frequency components within the transition region.





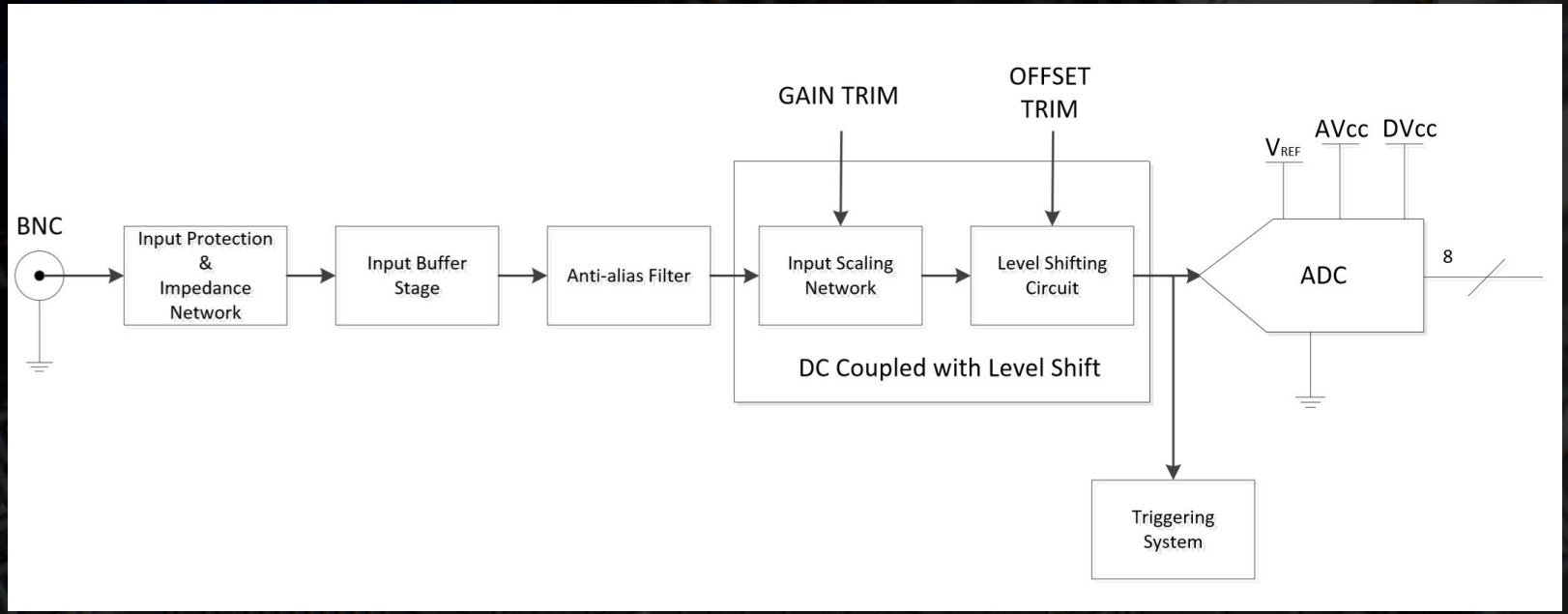
Front End and ADC

The combined analog cascade stage gain and voltage ranges:



Front End and ADC

Full DSO Front End Block Diagram:

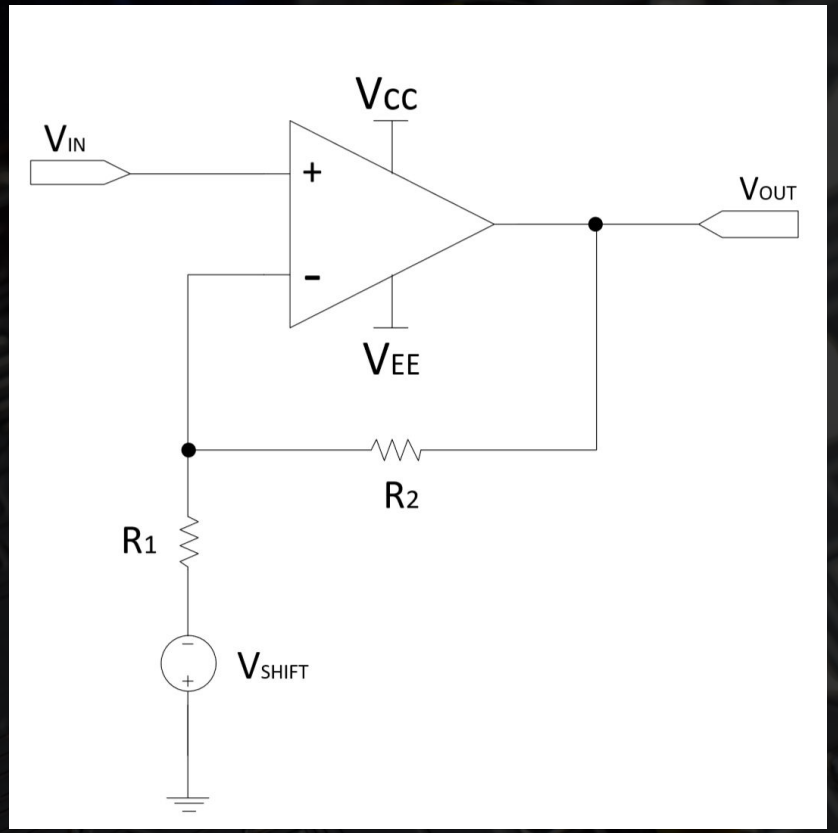


Level Shifting

Let $A = (R_2/R_1) + 1$

$V_{OUT} = A \cdot V_{IN} + (A - 1) \cdot V_{SHIFT}$

NOTE: Ideally V_{SHIFT} holds constant voltage across it's terminals independent of the current through it



DAC

		MIN		MAX		
(All inputs/outputs)	C_{OUT}					f_{CLK} = 1 MHz **(Note 1)**
Clock Frequency	F_{CLK}	—	—	20	MHz	T_A = +25°C **(Note 1)**
Clock High Time	t_{HI}	15	—	—	ns	**Note 1**
Clock Low Time	t_{LO}	15	—	—	ns	**Note 1**
$\overline{CS}$ Fall to First Rising CLK	t_{CSSR}	40	—	—	ns	Applies only when $\overline{CS}$ falls with

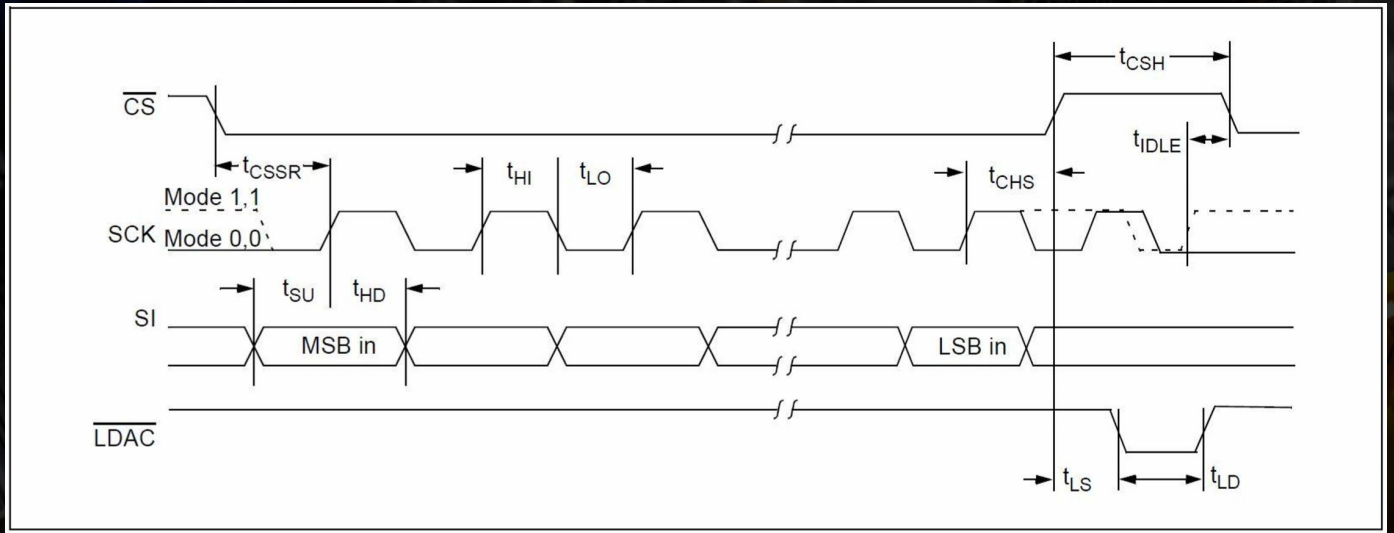


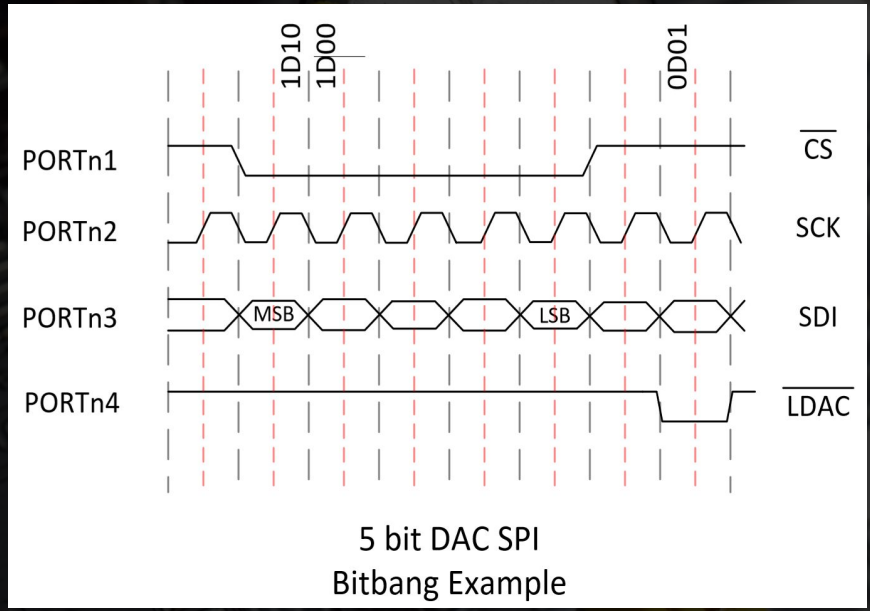
FIGURE 1-1: *SPI Input Timing Data.*

Bit Banging

- Bit banging is a method of sending bits to the GPIO pins of a microcontroller enabling you to emulate communication protocols in software that would otherwise require dedicated microcontroller hardware logic blocks.
- Some of the standard digital communications interfaces implemented within software include:
  - SPI
  - TWI (Two-Wire Interface)
  - TTL RS232 or USART (Universal Serial Asynchronous Receive and Transmit)
  - USB

Bit Banging Waveform

- There is no minimum transfer rate for the DAC.
- Our application doesn't require high transfer rates therefore bitbanging is an acceptable method of data transfer.
- Waveform timing can be driven by a counter interrupt event within the microcontroller.



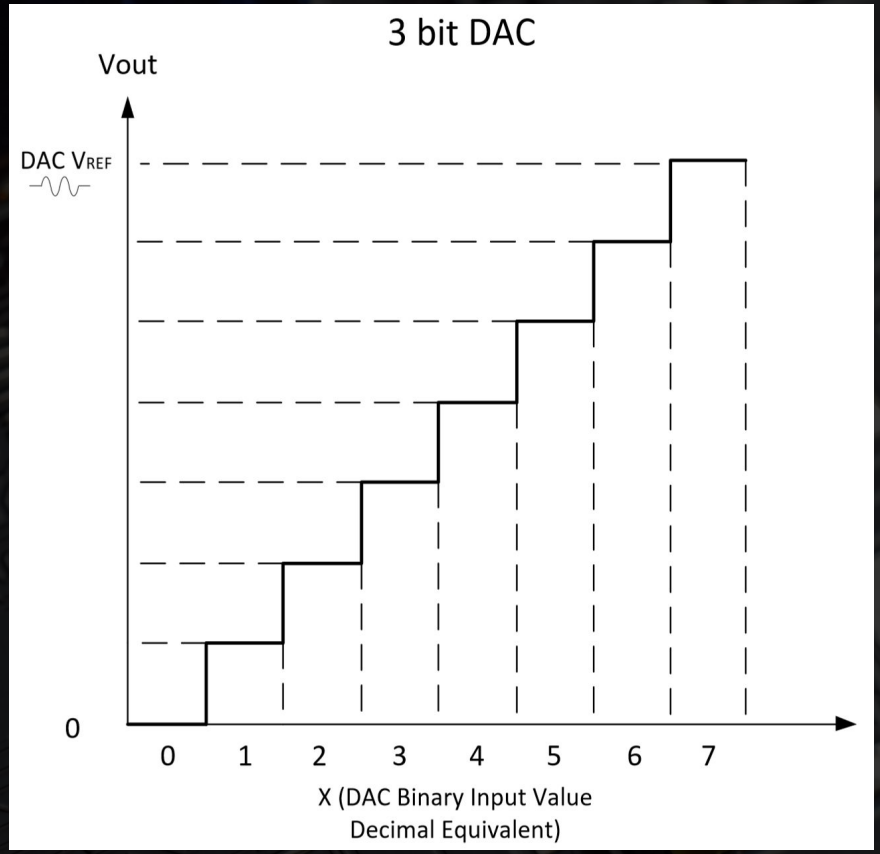
5 bit DAC SPI
Bitbang Example

Voltage Referencing

- $0 \leq X \leq (2^N - 1)$ Where N is the resolution in bits (DAC or ADC)
- For a DAC:

$$V_{REF} = (X \bullet V_{REF}) / (2^N - 1)$$

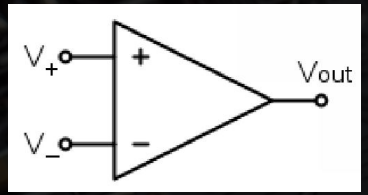
In both the ADC and DAC, variation in V_{REF} will scale quantisation proportional to this reference voltage and therefore error and noise is introduced into the digitised signal if this reference contains noise. **VREF needs to be filtered !!!**

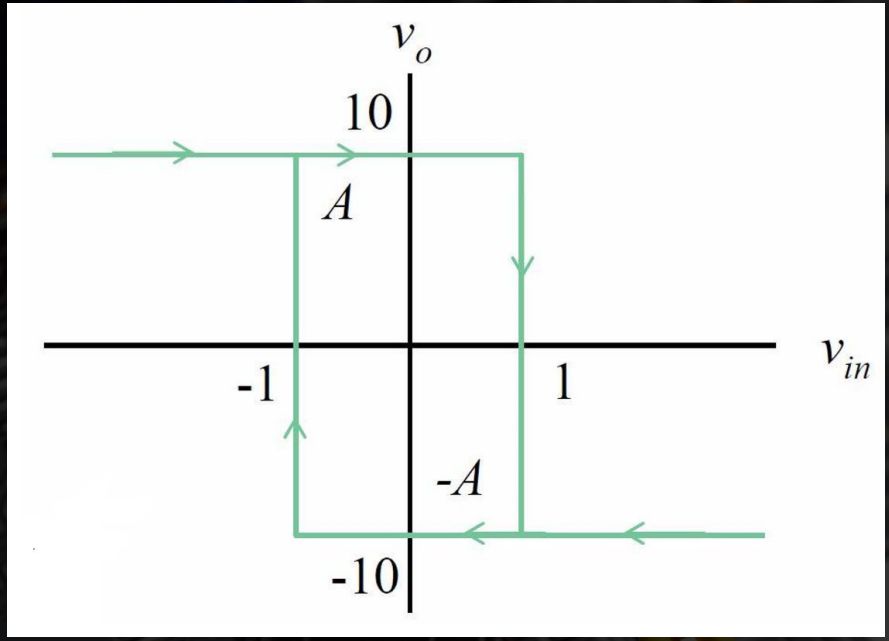


Triggering

All **comparators** aim to have the following properties:

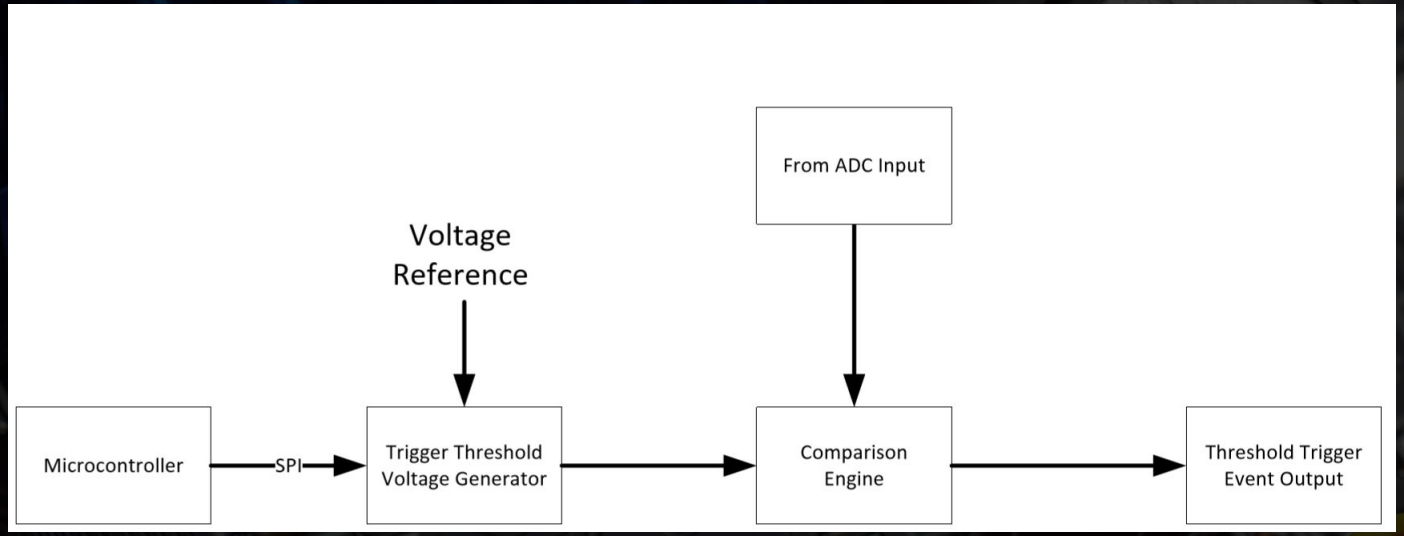
- High slew rate
- Low propagation delay
- Input Hysteresis
- High CMMR





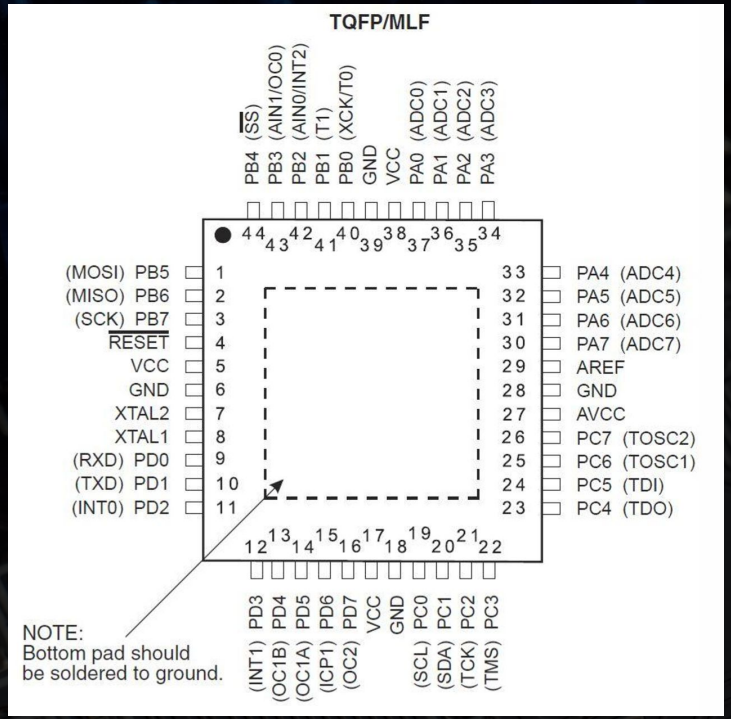
INPUT Voltages	OUTPUT State
V- > V+	Negative Rail Voltage or Ground
V+ > V-	Positive Rail Voltage or Floating

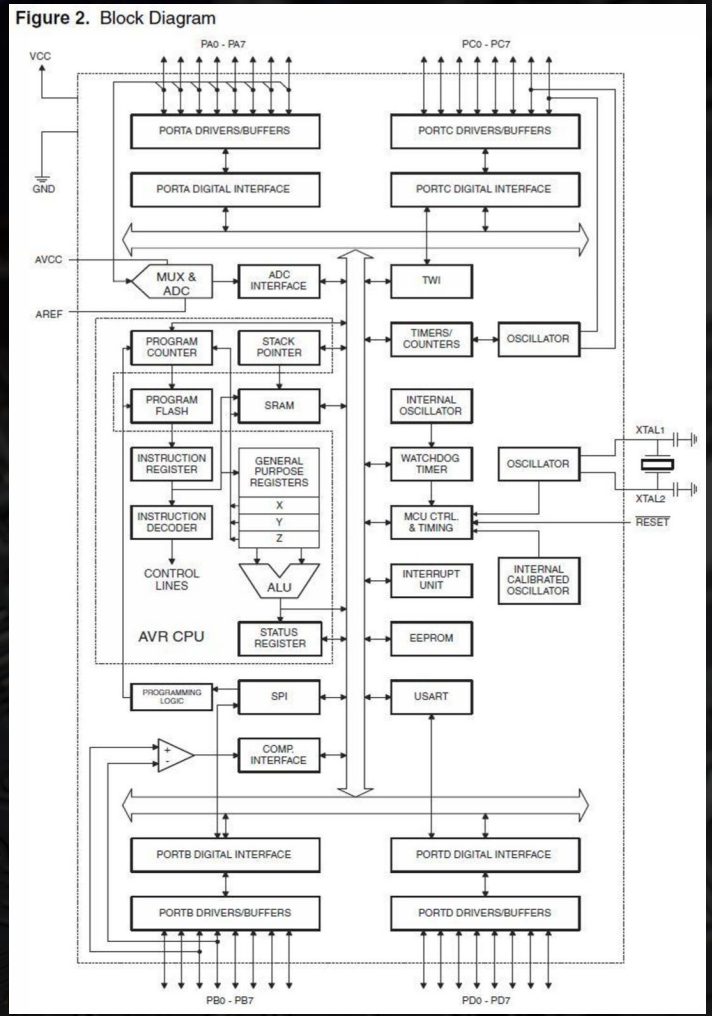
Triggering Block Diagram



A basic block diagram of a non-specific DSO triggering section

ATMega16 Introduction





Phased Locked Loops (PLL)

A PLL circuit can perform four primary functions:

1. Clock Multiplication/Division
2. Clock recovery
3. FM Demodulation
4. Jitter rejection

- In your project we will be using the PLL for clock multiplication and division functionality only.
- The PLL input clock is derived from the system crystal via a prescaler and counter within the microcontroller.

PLL Basic Blocks

In its most basic form a PLL can often be thought of as simply a digital or analog frequency modifier, abstracting away from the method by which this is achieved.

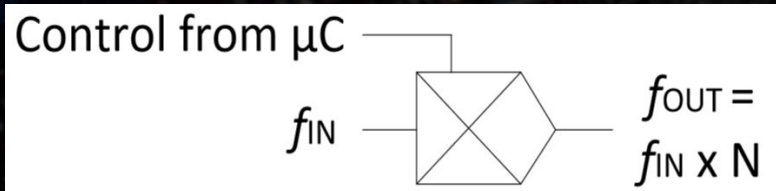


Fig 1: PLL as N clock multiplier.

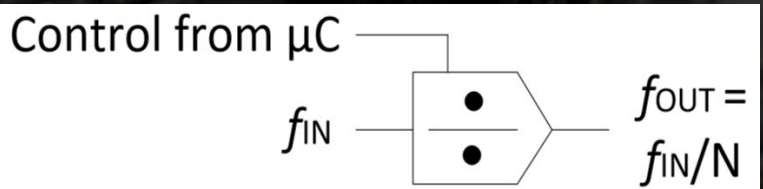
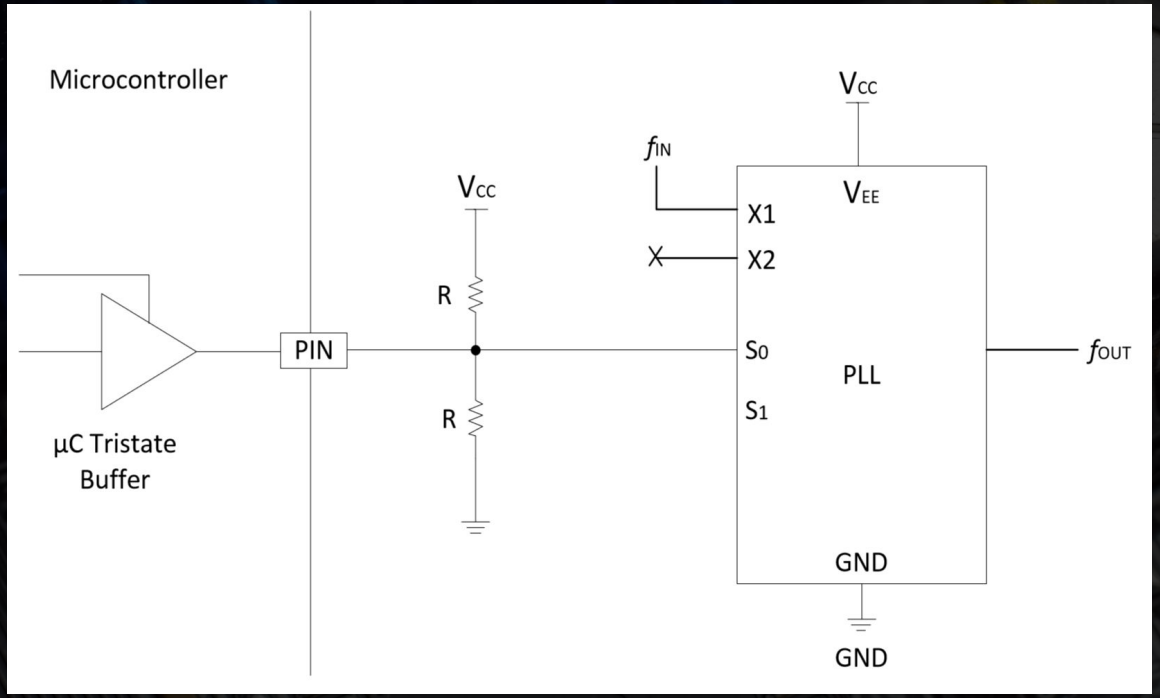


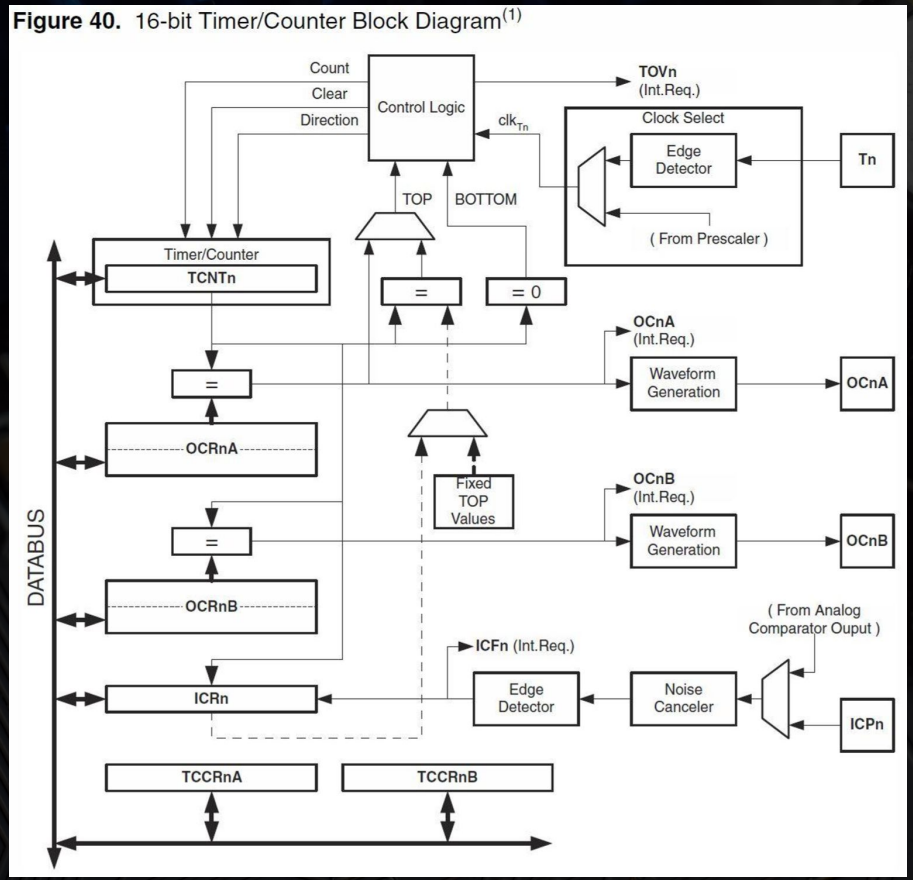
Fig 2: PLL as N clock divider.

DSO Clock

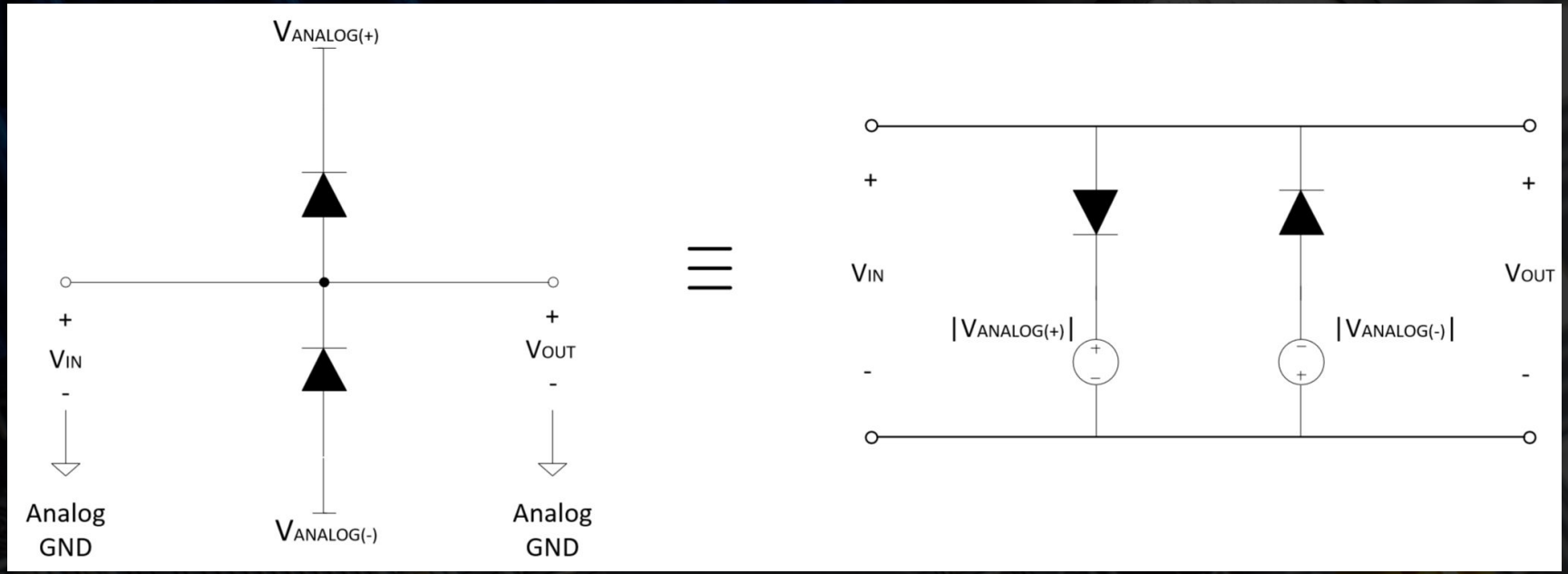


An example of microcontroller drive for a PLL ICs frequency modifier control.

ATMega Counters and Timers

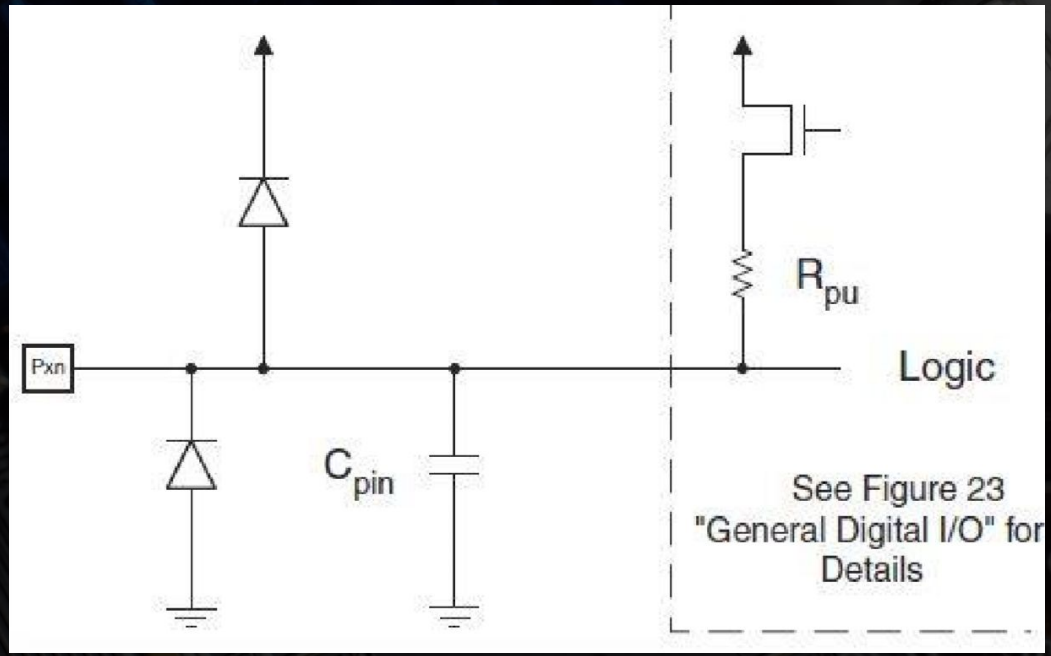


Voltage Clamping and Detection



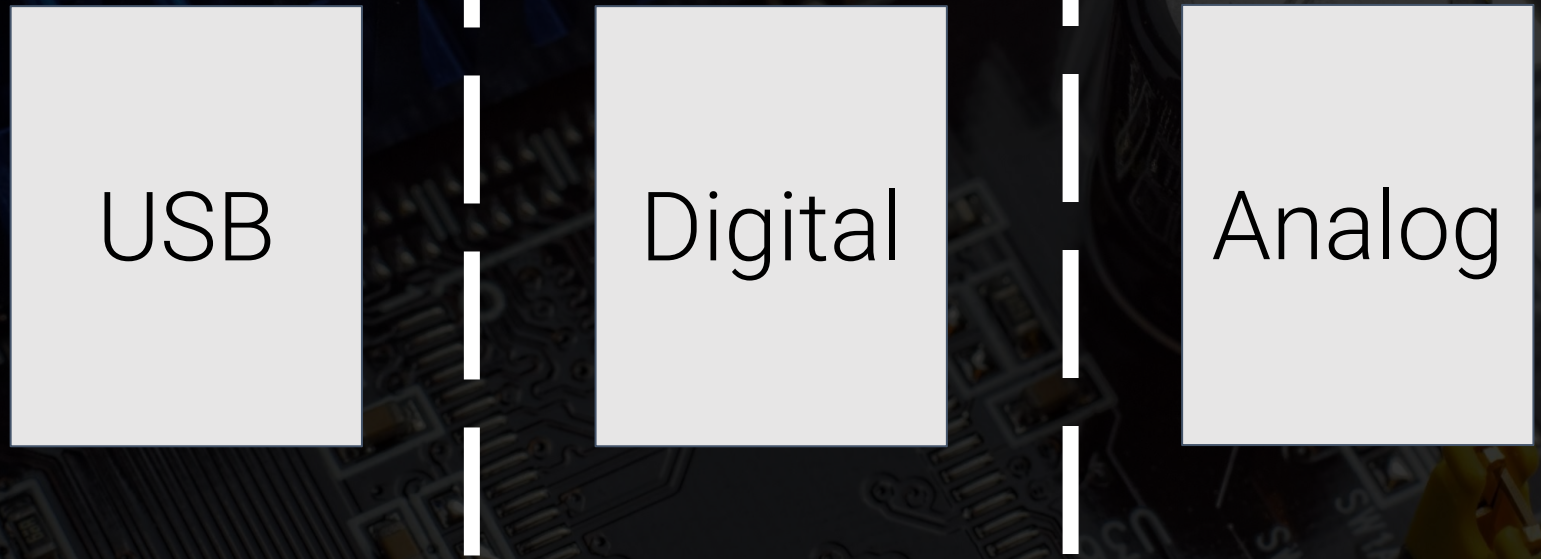
Example of equivalent voltage clamping circuitry

ATMega GPIO and Clamping



GPIO – General Purpose Input Output (p.4849 Atmega16 Datasheet)

Power Domains



Ground planes should be split at domain boundaries
(Net Tie or stacked PCB design)

Supply Labels

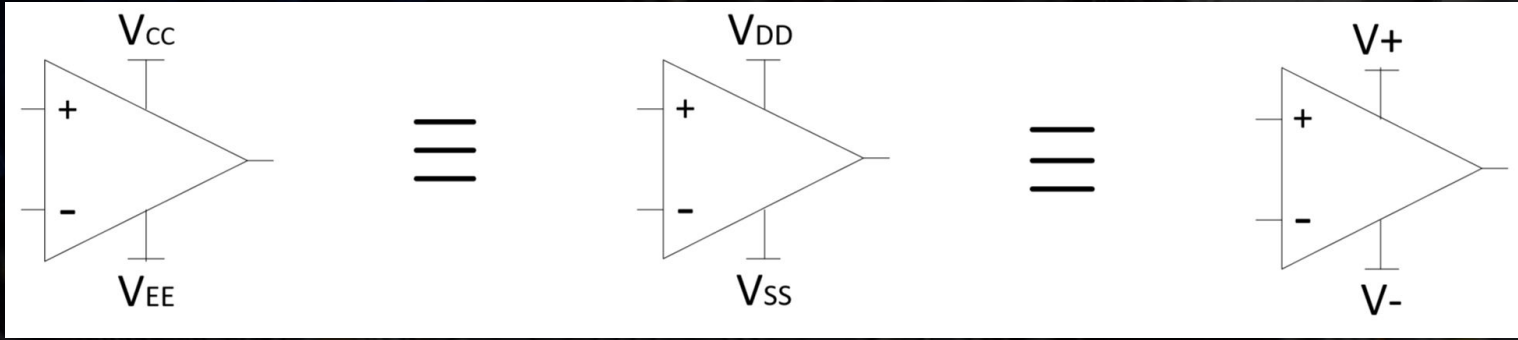
Power net labels in both the digital and analog domains are used in pairs relating to the transistor type traditionally used in the underlying circuitry. i.e. C -> collector, D -> Drain, etc.

Typical Supply Pin Labeling			
BJT	**FET**	**Generic**	
V_{CC}	V_{DD}	V_{+}	Positive Supply
V_{EE}	V_{SS}	V_{-}	Negative Supply
		GND, AGND	Ground Supply

Ground reference labelling can be split many times within a complex design to assist in digital and analog circuitry noise isolation. AGND -> Analog Ground.

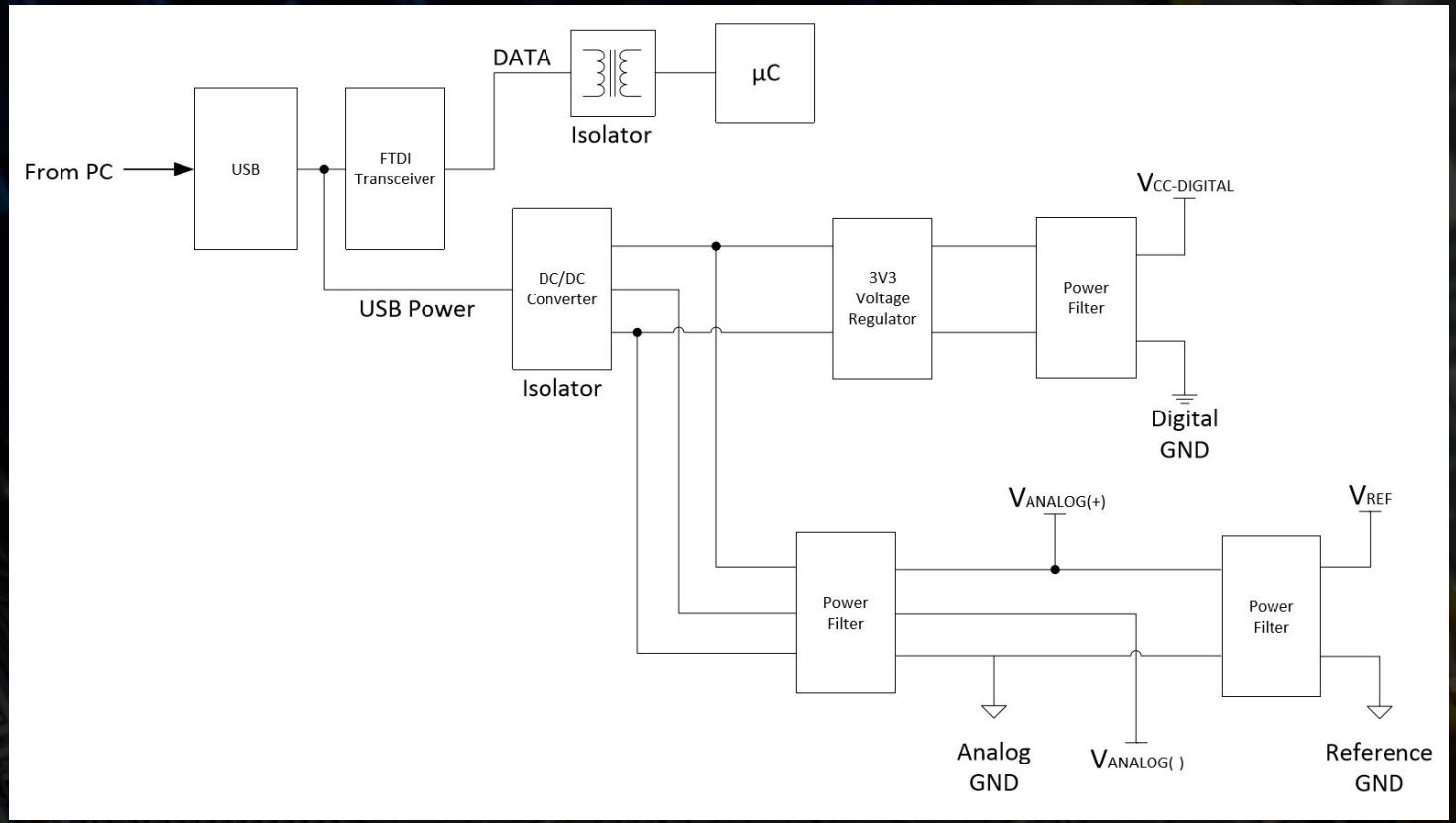
Supply Labeling Example

The three labelling schemes below are equivalent but it is important to note that the polarity and pairing should be consistent within your schematics.



If you require multiple net labels for different power domains then it is recommended that you add a number postfix such as V_{DD1} or V_{EE-2}

Power Filters



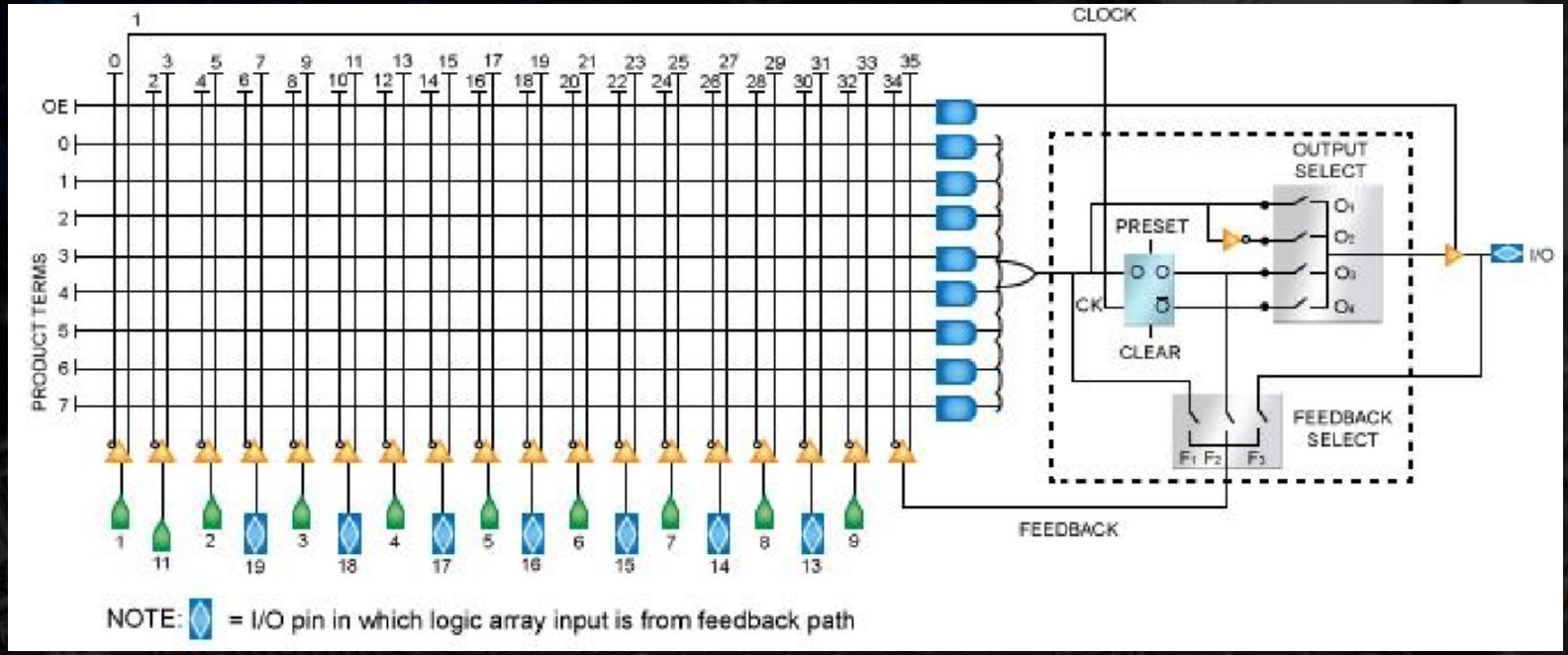
Power Filters

Consider the following when constructing your power supply filtering:

- **PI Filtering** for PLL and Analog V_{CC}
- Supply decoupling at each IC power pin in both the digital and analog sections
- Large capacitive supply decoupling at the Recom isolated supply
- Paralleling larger capacitance with smaller (C/100) capacitors to improve wide-band RF filtering across the PCB

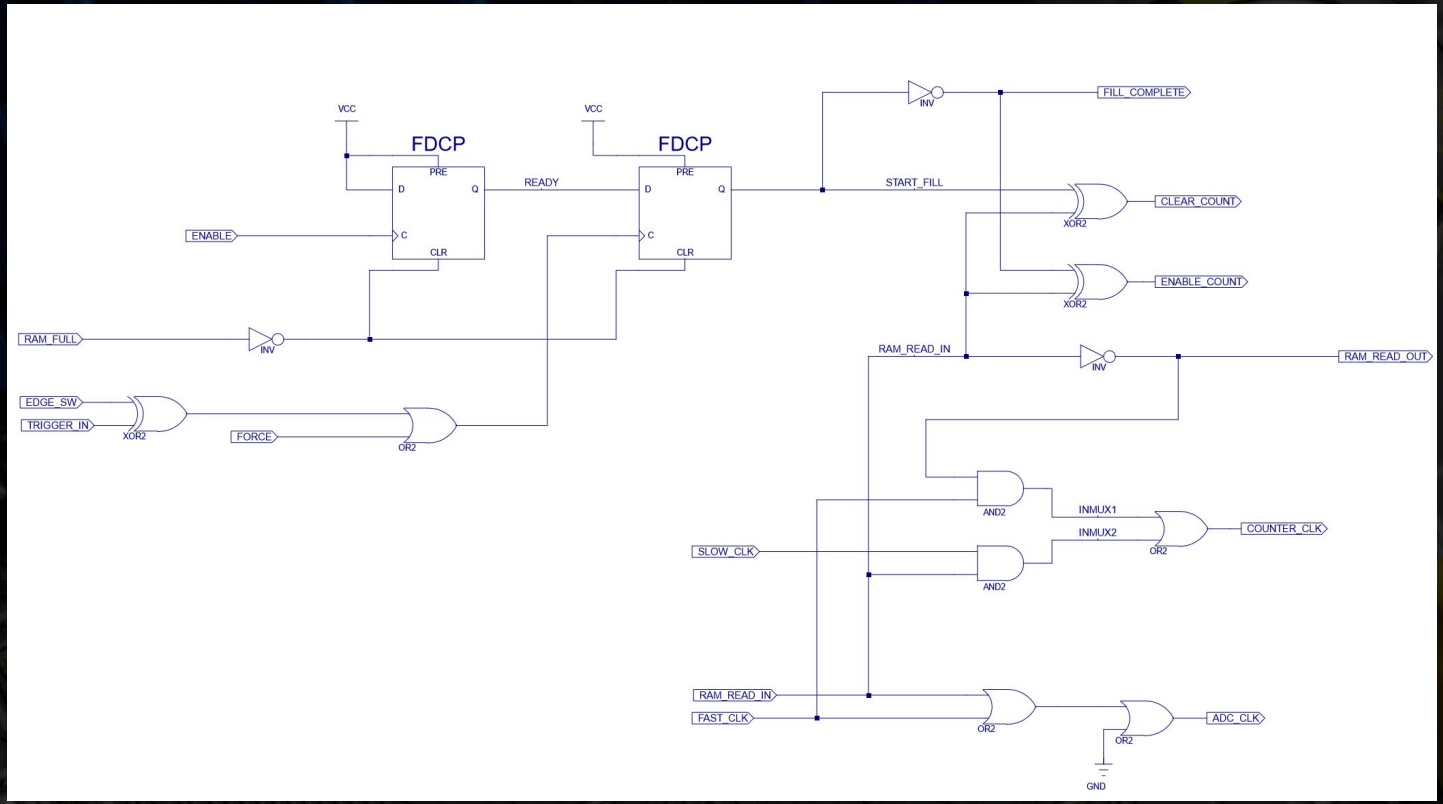
CPLD Implementation

A **CPLD** or Complex Programmable Logic Device is a collection of state machine modules called **macrocells** and an underlying interconnection fabric which allows for **non-volatile** implementation of software defined combination logic.



This diagram shows one of eight basic macrocells within an early model Altera EP300/EP310 CPLD

CPLD Implementation



What is happening inside our CPLD for the DSO to function

CPLD, FPGA and Discrete ICs

	Discrete	CPLD	FPGA
Cost	Very Low	Low	Medium to High
Design Complexity	Low	Medium	High
Max Speed	Low to Medium – 100MHz	Medium – 100MHz to 300MHz	Low to High - 50
Configurability	None	High	High
Volatility	Non-volatile	Non-volatile	Volatile
Density	NA	Low	High
Number of Gates	1 to 8	1K to 20K	10K to 5G
Number of IO	1 to 14	20 to 100	20 to 900+
Example Peripheral Modules	None	SPI	Multiple LVDS Transceivers, Ethernet PHY
Maximum Voltage	5V	3V3	3V3

Additional Project Requirements

- Schematic notation for PCB fiducials, labels, and mounting holes
- User Interface -> User adjustable potentiometer to control trigger level
- Creation of footprints and schematic symbols with supplier information
- Bill of Materials required with documentation
- Gerber files must also be exported

Questions to Answer

- What is the DC/DC converter ripple and how will this effect the ADC reference voltage?
- What is the maximum current supply of the DC/DC converter?
- What order of antialiasing filter does this design require?
- How do we define and calculate input impedance?

References

- Read and understand **EVERY. SINGLE. DATASHEET.**
- Application notes from the manufacturer generally will tell you everything you need to know to design a circuit
- Examine the specification closely
- Refer to the Art of Electronics (Third Edition preferred) for thourough circuit design explanations
- Don’t spend too much time on the front end and ADC circuits - you will run out of time if you don’t follow the timeline!