Core Schematics and Simulation Report Checklist

Your report should include:

- ❏ A title page and table of contents
- ❏ A picture of your LTSpice schematics embedded within the report
- ❏ A frequency response graph from 0Hz to 50MHz measured at the ADC input
- ❏ A phase response graph from 0Hz to 50MHz measured at the ADC input ????
- ❏ The frequency and phase responses should be presented for the following points:
  - ❏ Prior to your filter stage
  - ❏ At the input to the ADC
- ❏ An input impedance graph from 0Hz to 50MHz measured at the BNC
- ❏ Power dissipation table. A tabulated collection of DC bias and power dissipation ??? simulation results taken at various important points throughout your front end. Net labels should be utilised to identify each point in the schematics and table entries.
- ❏ A time domain plot for a 10Mhz input signal taken at the input to the ADC
- ❏ A short observation on each of your results reflecting on whether core specification criteria have been met and what (if any) issues might exist with your front-end design. If there are notable features of your results a clear description of possible reasons for these variations would be advisable.
- ❏ A summary outlining expected performance of the final design.

Your submission should include:

- ❏ Altium Designer Analog Front-End Schematics complete,
  - ❏ DSO_Top.SchDoc,
  - ❏ DSO_Front.SchDoc,
  - ❏ DSO_ADC.SchDoc,
  - ❏ DSO_Trigger.SchDoc,
- ❏ All remaining schematics completed to the best of your ability
- ❏ Files Zipped with a filename format as per submission guide (on LMS) including only:
  - ❏ All DSO project schematics, *.SchDoc
  - ❏ A DSO PCB project file, *.PrjPCB
  - ❏ Report in PDF format
  - ❏ Your LTSpice schematic design, *.asc