University of Melbourne
ELEN90053 Electronic System Design
WORKSHOP

SIMULATION REPORT

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Contents

I Over whole Front-End Schematics

The whole circuit built as figure 1.

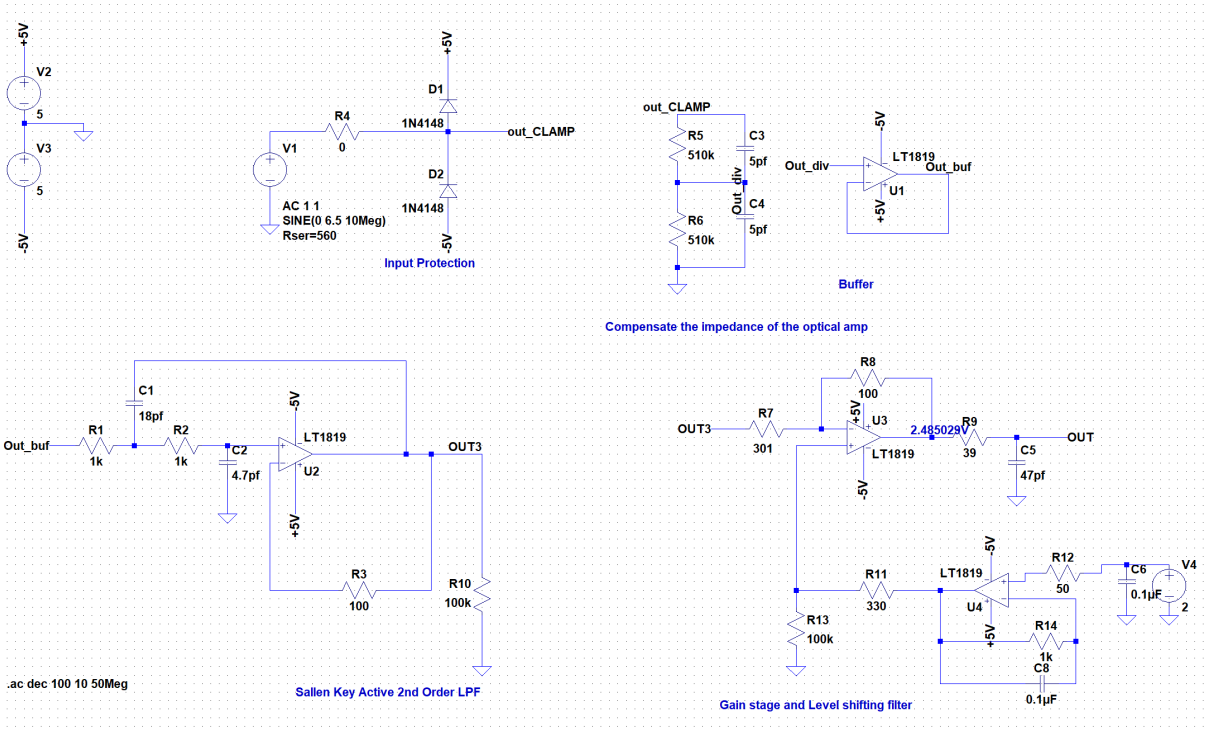


Figure 1: The front end circuit designed

Each part will be discussed respectively at the sections

II Frequency and phase response graphs

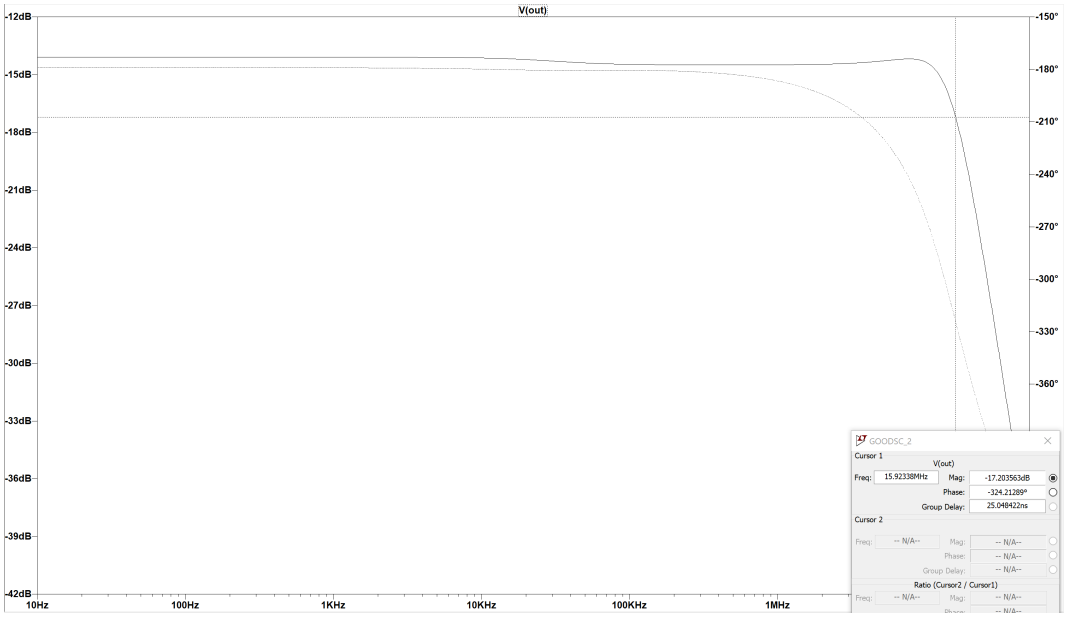


Figure 2: Frequency and phase response at the ADC input

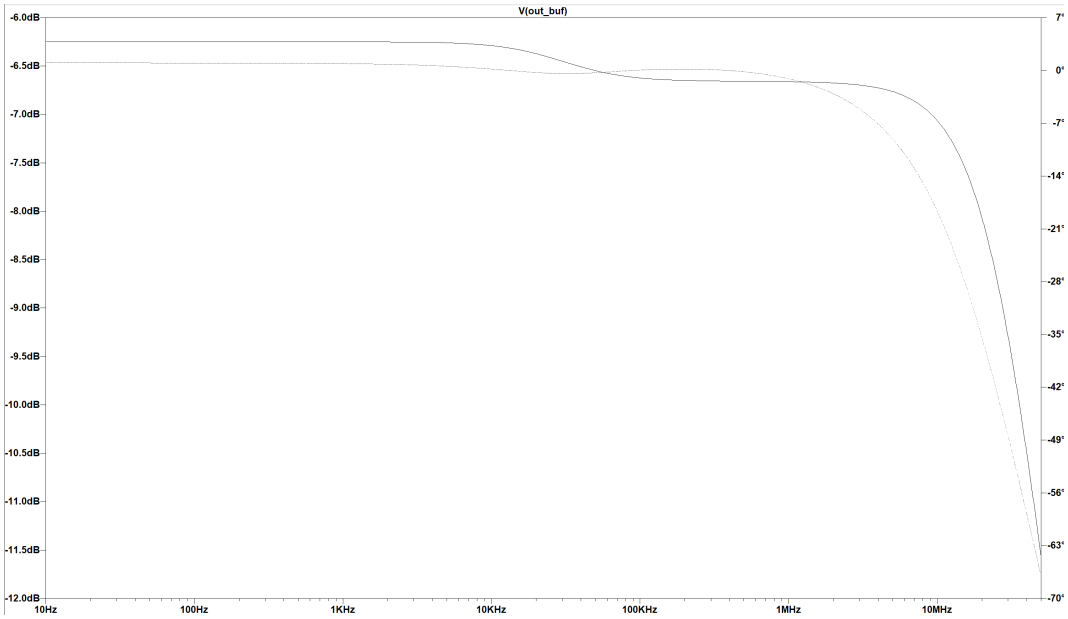


Figure 3: Frequency and phase prior to the filter stage

From the figures above, the amplitude sent to adc has been decreased by $-14dB$, which is 0.199. This is designed intentionally as we want to shrink our amplitude from 10 V peak-to-peak to 2 V peak-to-peak. **While the phase has a 180 degree shift due to the feedback loop of the low pass filter, this can also be verified in figure 3**. The $-6dB$ amplitude decrease in figure 3 is discussed in section VI.

III Input impedance graph

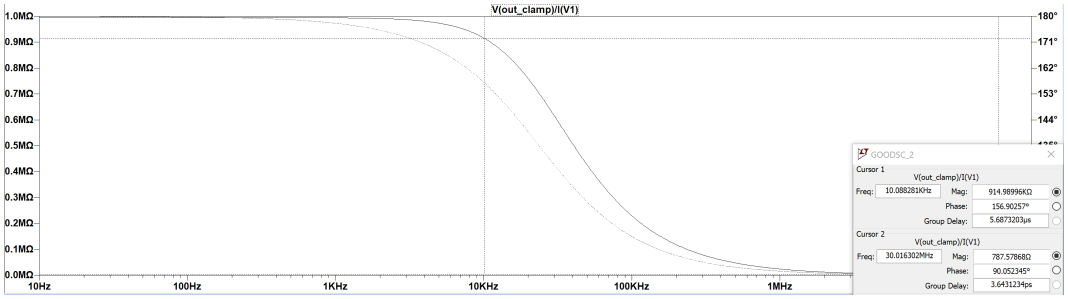


Figure 4: Input impedance measured at the BNC

From two cursors, the input impedance requirement is satisfied by the design.

IV Power dissipation table and DC bias

The power consumption at each point collected as below:

Component	U1	U2	U3	U4
Average power	90.462mW	100.94mW	95.222mW	89.953mW

Table 1: power consumption table

Although all components' power seems in a reasonable range from the data sheet, to ensure all operational amplifiers running well in the real circuit, currents of those amplifiers are measured as below:

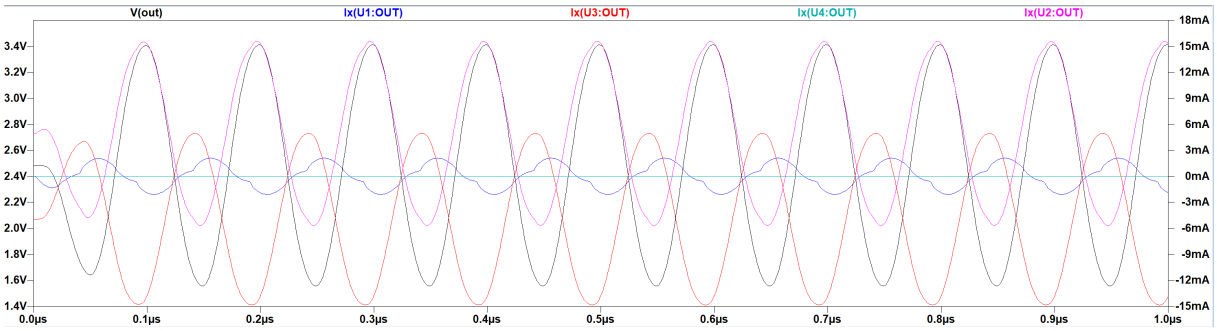


Figure 5: Output current of each amplifier

From data sheet, the maximum output current is $\pm 50mA$, from this circumstance, our design is safe as all the currents are within this range.
The measured DC bias table is as below:

Interested point	Out_Clamp	Out_Buf	Out_3	OUT
Bias DC	540uV	497mV	500mV	2.49V

Figure 6: DC bias point of each stage.

V Time domain plot for a 10Mhz input

When a 10Mhz input signal with 5V amplitude is implemented, the output signal is as below:

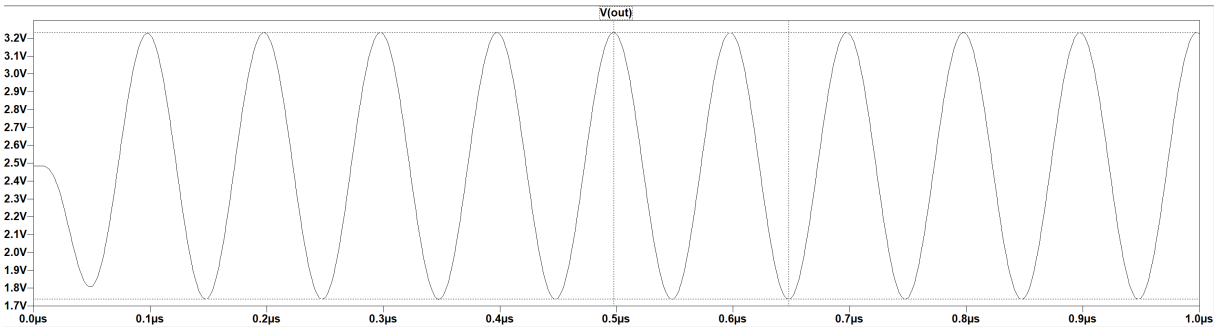


Figure 7: Input to the ADC when apply a 10Mhz input with 5V amplitude.

From the figure below, we can state the peak voltage of the output signal is from 1.7 to 3.3 centring around 2.5V. The amplitude is intentionally scale more than needed for the scenario when a large signal is clamped. This scenario is simulated as below:

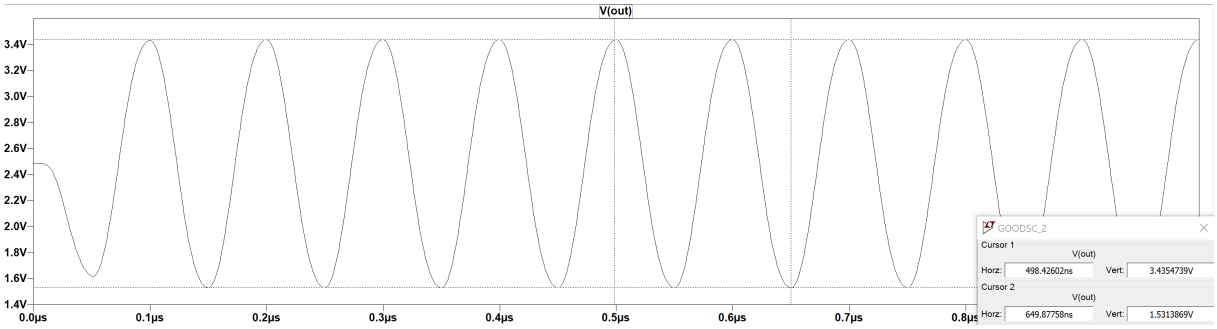


Figure 8: Input to the ADC when apply a 10Mhz input with 7V amplitude.

From the figure above, the amplitude is still in control when a unproperly large signal is implemented.

VI Circuits analysing and specification criteria

VI.1 Input Protection

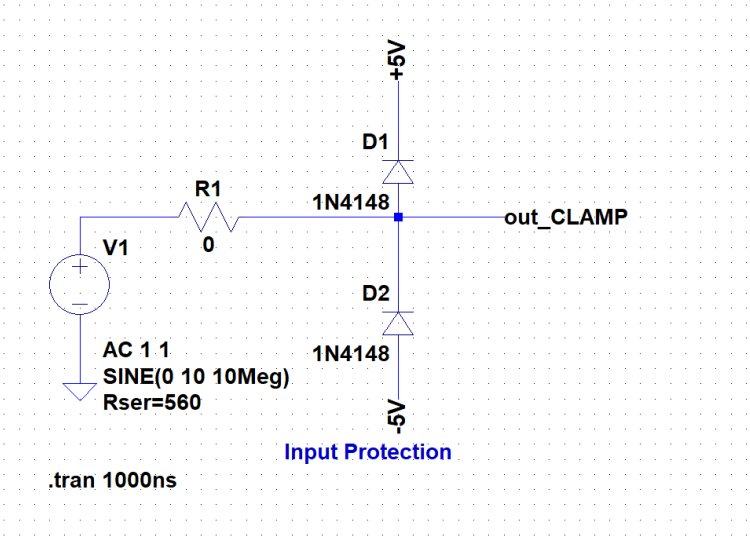


Figure 9: Input protection circuit

To test the input amplitude protection, a $10V$ AC input is implemented. The output signal is shown as below. **The input signal is limited by two diode, and the maximum amplitudes are $5\mathrm{V} + \mathrm{V_{on}}$ and $-5\mathrm{V} - \mathrm{V_{on}}$, which from the plot is about ± 5.6V.**

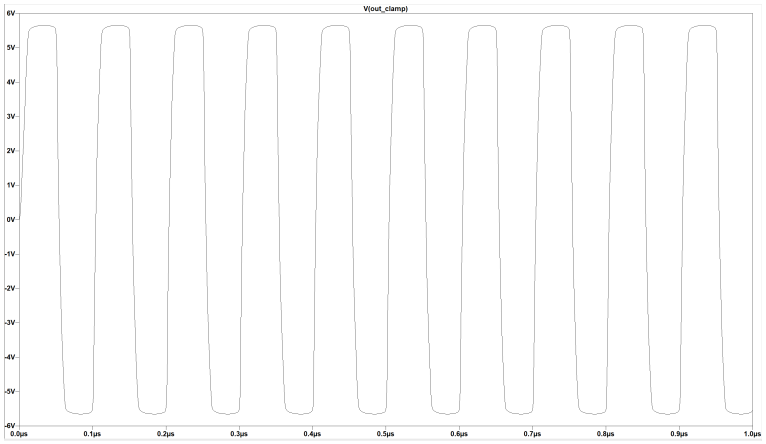


Figure 10: Output signal after the protection circuit

VI.2 Input impedance and buffer

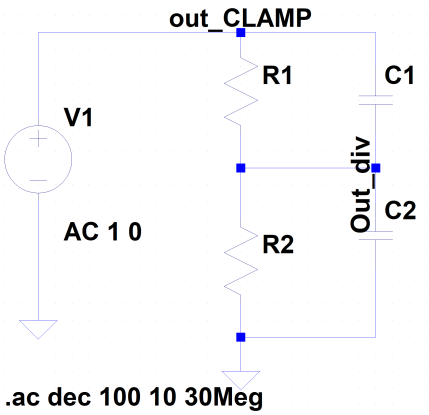


Figure 11: Impedance components for the Front end circuit

Since the construction above is between the protection circuit and the buffer, we can state this part is mainly used to provide a proper impedance for the circuit as the buffer isolate the impedance. Based on our functional specifications, **we need a 1MΩ ± 10% input impedance from DC to 10kHz, and greater than 100ohms between 10 kHz and 30 MHz.** Firstly, when a DC is implemented, C1 and C2 are open, hence we have $R1 + R2 = 1M\Omega \pm 10\%$. Another factor we need to consider is the frequency response:

$$\begin{aligned} \frac{V_{out-div}}{V_{out-CLAMP}} &= \frac{Z_2}{Z_1 + Z_2} \\ &= \frac{R_2 || \frac{1}{2\pi f C_2}}{R_1 || \frac{1}{2\pi f C_1} + R_2 || \frac{1}{2\pi f C_2}} \\ &= \frac{R_1(1 + sR_2C_2)}{R_1(1 + SR_2C_2) + R_2(1 + SR_1C_1)} \end{aligned} \tag{1}$$

From the equation above, we have one zero and one poles. As zero brings 20dB increase per decade and poles brings 20dB decrease per decade, to get a flatter frequency response at all band, there are two possible ways. **One is that we need our pole and zero far bigger than 30Mhz**, which means $R_1C_1 << 3 \times 10^{-7}$. However, since the smallest capacitor we have is $1nf$ and the two impedance requirements make this method impossible. Another possible way is we put zero and poles locate at the same position. **Although this will still cause phase oscillation at some frequency, the overall frequency response is relevant stable** Hence:

$$\frac{-1}{R_1C_1} = -\frac{R_1 + R_2}{R_1 \cdot R_2(C_1 + C_2)} \tag{2}$$

$$R_1 \cdot C_1 = R_2 \cdot C_2 \tag{3}$$

To simplify the calculation. we assume $R_1 = R_2$, so we can state $C_1 = C_2$, the discussed part is a half divider. Hence $R_1 = R_2 \approx 500K\Omega$. **The closet value available is 510kΩ**. When the frequency affects the circuit, we have:

$$Z_{in} = 2 \times (R||\frac{1}{2\pi fC}) \qquad R_1 = R_2 = R; \quad C_1 = C_2 = C \tag{4}$$

$$= \frac{2R}{1 + 2\pi fCR}$$

From the equation above, to achieve the functional specification, we need:

$$\frac{2R}{1 + 2\pi fCR} \geq 100 \qquad R = 510k\Omega \quad f = 30 \times 10^6 \tag{5}$$

$$C \leq 106pf \tag{6}$$

Another requirement here is **out input capacitance should be less than or equal to 60pF**. Under this condition, I put two $5pf$ small capacitors. Another reason is to guarantee the input impedance. Implement those parameter and plot the impedance as below:

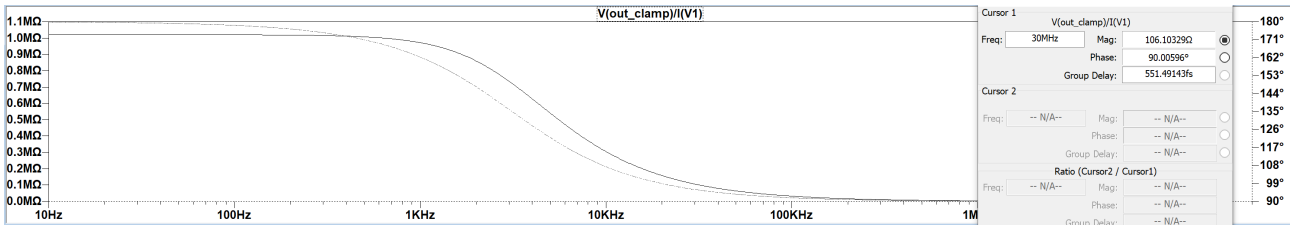


Figure 12: Input impedance simulation

From the figures above, **we can state our design satisfies the impedance requirements.** Besides these, the slightly phase can be seen as below:

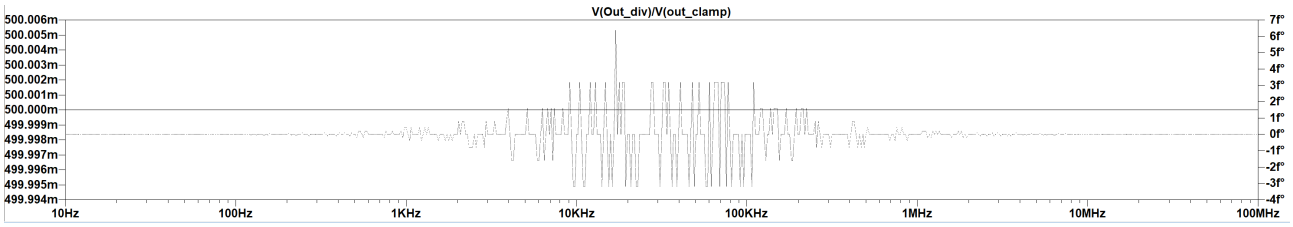
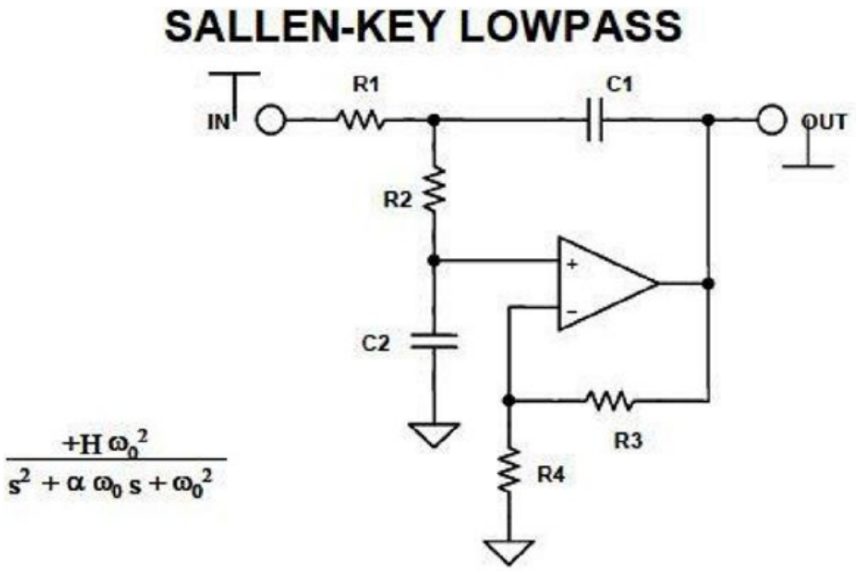


Figure 13: Constant gain and slightly oscillated phase

VI.3 Low pass filter

The designed LPF is as below:
Concretely, since the requirement 'An anti-aliasing filter appropriate to the $40MSPS$ maximum sample rate must be implemented with a minimum of a first-order $20dB$ per decade response and $\pm 2dB$ maximum ripple in the pass band' is expected to be meet. A second order Sallen Key Active Low Pass Filter then is used with reference circuit as figure 11. textbfSince the gain is expected to be normal, the R4 is open. Besides, based on sampling theorem, the cut-off frequency should be $20Mhz$, hence f_0 is set to $20Mhz$ to guarantee the bandwidth, and a is set to 1.



$$\frac{V_O}{V_{IN}} = \frac{H\,\frac{1}{R1\,R2\,C1\,C2}}{s^2 + s\left[\left(\frac{1}{R1}+\frac{1}{R2}\right)\frac{1}{C1}+\frac{(1-H)}{R2\,C2}\right] + \frac{1}{R1\,R2\,C1\,C2}}$$

CHOOSE: C1 R3

THEN:

$$k = 2\pi F_O\,C1 \qquad R4 = \frac{R3}{(H-1)}$$

$$m = \frac{\alpha^2}{4} + (H-1)$$

$$C2 = m\,C1$$

$$R1 = \frac{2}{\alpha k}$$

$$R2 = \frac{\alpha}{2mk}$$

Figure 14: Given reference circuit and equation

After calculating based on the equations above, we built our LPF as below:

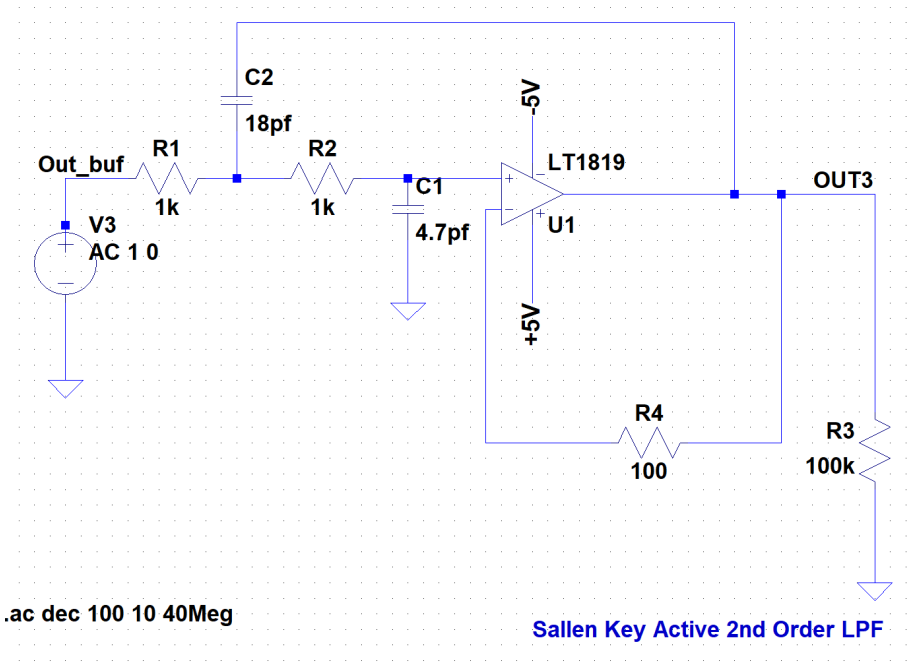


Figure 15: Built low pass filter

To test the frequency response, a 1V AC input is plugged and the bode plot as below, although a much more larger bandwidth is generated, the final bandwidth is just a little bit more than we need as shown in figure 2:

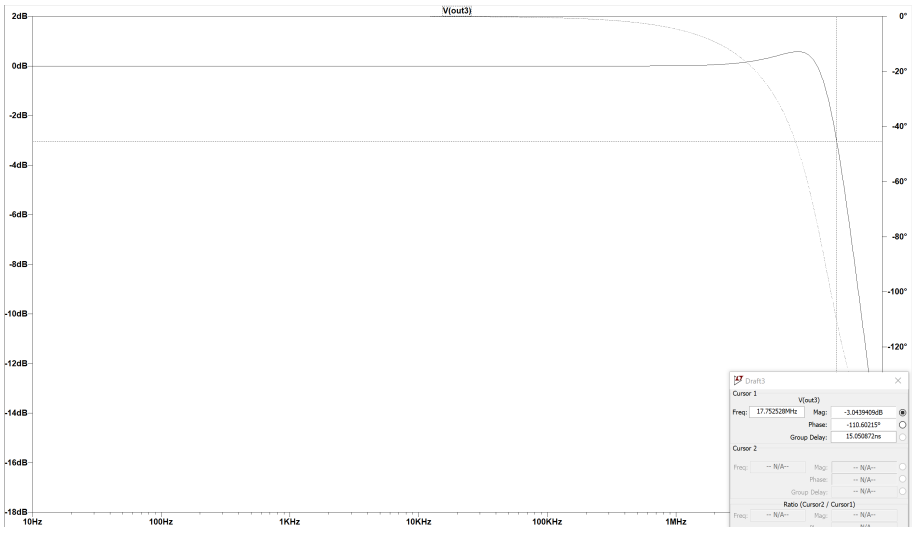


Figure 16: Bode plot of the low pass filter

VI.4 Gain stage and level shifting filter

In this part, the circuit is divided to three part based on functions as comments illustrate below:

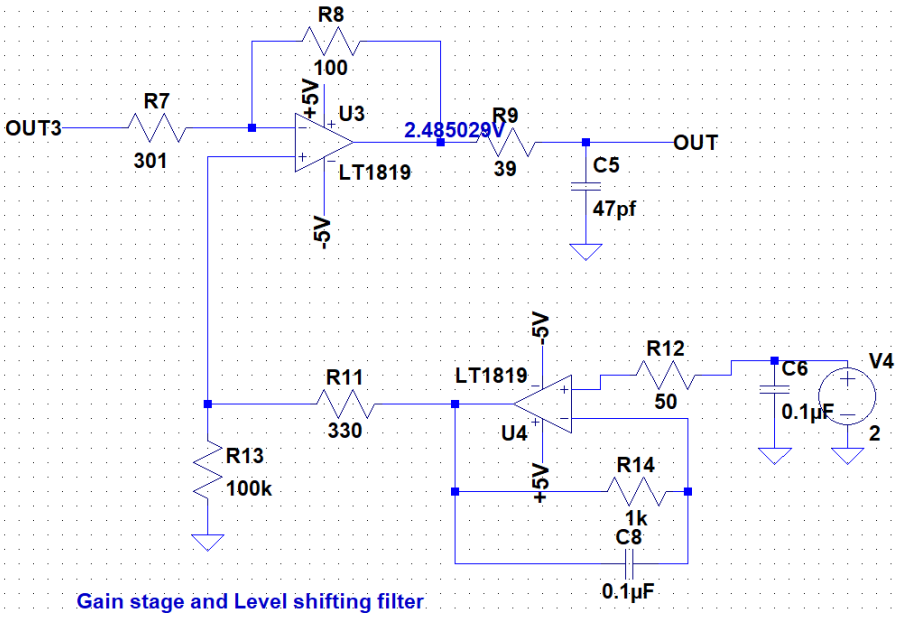


Figure 17: Gain stage and level shifting filter

From the bottom right to top left, a buffer is firstly used make sure our reference. Two resistors are used to bias our signals' center point to $5V$. However, this part is also affected by the gain stage, where we can scale the signal by changing resistor R_1 and R_2.
Yielding, the R_2 and R_3 is first calibrated to get a $\frac{2}{5.6}$ gain from outClamp to output3 in the figure 1 (The previous stages shrink the signal to a half as discussed above). Secondly, we change the level shifting to make central voltage at $2.5V$. As we have to select components form values supplied, the closet central point gotten is 2.48V. Then a $10Mhz$ test signal with 10V peak-to-peak is implemented to test the performance and the output is as figure 5.

VII Specifications Summary

In conclusion, as discussed, we have meet the requirements below:

- **The input impedance is above 9MΩ from 0 to 10hHz and above 100 between 10 kHz and 30 MHz.**
- **The input capacitance is less than 60pF**
- **The input signal can be champed to ±5.6V**
- **The signal path from the BNC input to the ADC shall be DC coupled.**
- **The lpf is anti-aliasing which support maximum 35MSPS sample rate, with a minimum of a first-order 20dB per decade response and ±2dB maximum ripple in the pass band**
- **All passive components are selected based on values supplied.**