

Functional Specifications

The device must meet the following specifications. Modification to the specification must be provided in detail by the student, and must be approved by a demonstrator or coordinator.

Input

- 1.0 The device will have one analogue input.
- 1.0.1 The input will be through a BNC connector
- 1.0.2 The input will have a $1\text{M}\Omega \pm 10\%$ input impedance from DC to 10kHz.
- 1.0.3 The input must have impedance between 10 kHz and 30 MHz of greater than 100 ohms.
- 1.0.4 The input will have an input capacitance of less than or equal to 60pF
- 1.0.5 The BNC input can accept a maximum input of $\pm 5.6\text{V}$ after which the input voltage is clamped.
- 1.0.6 The signal path from the BNC input to the ADC shall be DC coupled.
- 1.0.7 An anti-aliasing filter appropriate to the 40MSPS maximum sample rate must be implemented with a minimum of a first-order 20dB per decade response and $\pm 2\text{dB}$ maximum ripple in the pass band.
- 1.0.8 All passive components must be selected from the values supplied in the passive components list to achieve the closest possible match to desired filter response.

Interface - Basic

- 2.0 The device will have one USB connector.
- 2.0.1 The USB device will be recognised as a Serial to USB adapter.
- 2.0.2 The device will connect using a virtual COM port.
- 2.0.3 The device will communicate at the default 38,400 baud.
- 2.0.4 The device will transmit digitised analogue signals to the PC.
- 2.0.5 The device will receive configuration information from the PC.
- 2.0.6 The device will be galvanically isolated from the PC.
- 2.0.7 The device will have 3 1.8mm input power pads, +5v, 0v and -5v.
- 2.0.8 The +5v and USB 5v rail will not be connected.
- 2.0.9 The device will be powered by the USB port. (Your device must draw less than 150mA per rail when running a maximum sampling rate)
- 2.0.10 A tactile pushbutton switch will be included to force triggering to begin

Interface – Advanced

- 3.0 The device will be powered by the USB port or by a battery source (Your device must draw less than 150mA per rail when running a maximum sampling rate)
- 3.0.1 The device will have buttons and knobs to also (not instead of the PC) control its configuration.
- 3.0.2 The device will have an LCD screen to also display the signal traces

- 3.0.3 The PCB will be fully enclosed (e.g. with laser cut acrylic or a 3D printed injection mould prototype) with considerations made for EMI/EMC compliance.

Triggering

- 4.0 The device will wait until the PC tells it to sample.
- 4.0.1 When the input rises across a trigger threshold, and the device has been instructed to sample, the device will store 65536 8 bit samples in RAM.
- 4.0.2 The value of the trigger threshold will be set by the PC.
- 4.0.3 Once the samples are stored in RAM the device will be instructed to send the data to the PC.
- 4.0.4 Once the device has transferred the data from RAM it waits to be instructed to sample again.

Triggering - Advanced

- 4.0.5 The trigger of 5.0 can be controlled by the PC to be on either rising or falling edge.

Sampling

- 5.0 Input 1.0 will be sampled and stored into RAM
- 5.0.1 Sampling will have 8 bit resolution
- 5.0.2 65536 samples will be stored in RAM
- 5.0.3 The sampling rate will be controlled by the PC.
- 5.0.4 The device will support the following sampling rates: 25ns (40MHz), 50ns (20MHz), 100ns (10MHz).

Presentation

- 6.0 The PCB layout will be constrained to a total shape of dimensions 110mm wide and 100mm high. This area must be inclusive of all components and panelised PCBs.
- 6.0.1 All components and their overlays are to lay within the board size.
- 6.0.2 Track width will be a minimum of 10 mil.
- 6.0.3 Clearance between tracks will be a minimum of 10mil.
- 6.0.4 Vias and Through Holes will conform to manufacturer's specifications
- 6.0.5 There will be four 3mm mounting screws 4mm from each edge at each corner and these will be represented on the schematics as Non-BOM components. These holes are for pick and place machinery and are standard for large scale manufacture.
- 6.0.6 Your student number will be placed on the top right of your PCB and a schematic symbol will represent the student number decal as a Non-BOM component.
- 6.0.7 Your name as it appears on the class list will be placed on the top left of your PCB
- 6.0.8 The device will have LEDs to display its status as follows.
- 6.0.8.1 A LED for +5 power good
- 6.0.8.2 A LED for -5 power good
- 6.0.8.3 LEDs for USB RX and TX
- 6.0.8.4 LEDs should be labelled indicating their purpose
- 6.0.9 There will be only 2 designator orientations throughout your PCB design

- 6.0.10 All via's should be tented on both Top and Bottom layers
- 6.0.11 USB differential lines must be laid out as a differential pair
- 6.0.12 All input and output connections must be clearly labelled
- 6.0.13 The top and bottom layers shall have a ground plain polygon pour
- 6.0.14 Tracks, components, and polygon pours, with the exception of the USB connector, will be kept a bare minimum of 50 mil from the boards edge.
- 6.0.15 The correct layer stack configuration for a 2-layer PCB must be set for a total PCB thickness of 1.6mm including the solder mask.
- 6.0.16 The submitted PCB must pass all design rules relating to the specification as listed above.
- 6.0.17 2 PCB fiducials positioned close to one corner of the CPLD and microcontroller, and represented on the schematics as non-BOM components. Fiducials are used by pick and place machinery with computer vision to align components with good precision and accuracy

Advanced PCB Features

- 7.0 The device will fit into an enclosure of your choosing (purchased by student)
- 7.0.1 The device will have LEDs which indicate the state of the system including,
 - 7.0.1.1 A LED for Triggered state, lit while the DSO is acquiring ADC data
 - 7.0.1.2 A LED for PC data streaming state, lit while the DSO is transferring
- 7.0.2 A rotary encoder to adjust trigger threshold or clock rate (purchased by student)

Software Interface Specifications

- 1.0 The device will operate at a default baud rate of 38400 bps.
- 1.1 When the device receives a 'v' it will respond with the string "DSO version *" where * is the firmware's version number.

Configuration

- 2.0 Configuration information will be sent to the device at start up and can be updated during runtime.
- 2.1 't' sets the trigger threshold values. The unsigned byte followed directly after 't' is the value of the trigger between 0 and 255.
- 2.2* 'i' sets the trigger source. The char after the 'i' will indicate the following:
 - 'r': rising edge on channel 1 (default)
 - 'f': falling edge on channel 1
- 2.3* 'o' sets the offset of the samples. The unsigned char proceeding directly after the 'o' is the offset * 256. (a value of 0 all samples are after the trigger, value of 4 is 1024

samples before and 64512 after, and 128 is 32768 samples before, 32768 samples after.)

- 2.4 'r' sets the sampling rate of the device. The unsigned byte followed directly after 'r' indicates the rate of sampling as follows:
- 1: 25ns
 - 2: 50ns
 - 3: 100ns
- 2.5* 'm' sets the number of samples to transfer back to the PC. The unsigned byte following directly after 'm' indicates how many samples to skip (a value of 1 will transfer every value (default) a value of 2 will transfer every second value, a value of 3 will transfer every third value etc.)
- 2.6* 'z' sets an offset of data to transfer. The unsigned byte following directly after 'z' indicates an offset *256 before the start of transferring samples.
- 2.7* 'Z' sets the length of data to transfer. The unsigned byte following directly after 'Z' indicates length * 256 samples to transfer.
- 2.8 'c' is a request to write back the configuration information. The device will return a string containing configuration information in conforming to the following format:

"t# T# s# o# r# a# A# m# z# Z# b#"

where # is the currently stored value for the corresponding setting (b is the baud rate).

Transferring Samples

- 3.1 'C' will instruct the device to start sampling at the next trigger event. The device will transmit 'C' when capture is complete.
- 3.2 'f' will instruct the device to start sampling immediately, overriding the trigger circuit. The device will transmit 'C' when capture is complete.
- 3.3 's' will instruct the device to send the samples collected on channel 1. The device will send a stream of 65,536 unsigned bytes to the PC.
- 3.3.1 If the device is transmitting data, 'n' will stop the current transfer. The device can then optionally be reconfigured and 'C' can be sent again to wait for the next trigger.
- 3.2 If 'm' in 2.5 and/or 'z' in 2.6 and/or 'Z' in 2.7 is set then the number of bytes will be reduced.

CPLD Design Summary

