1. Description

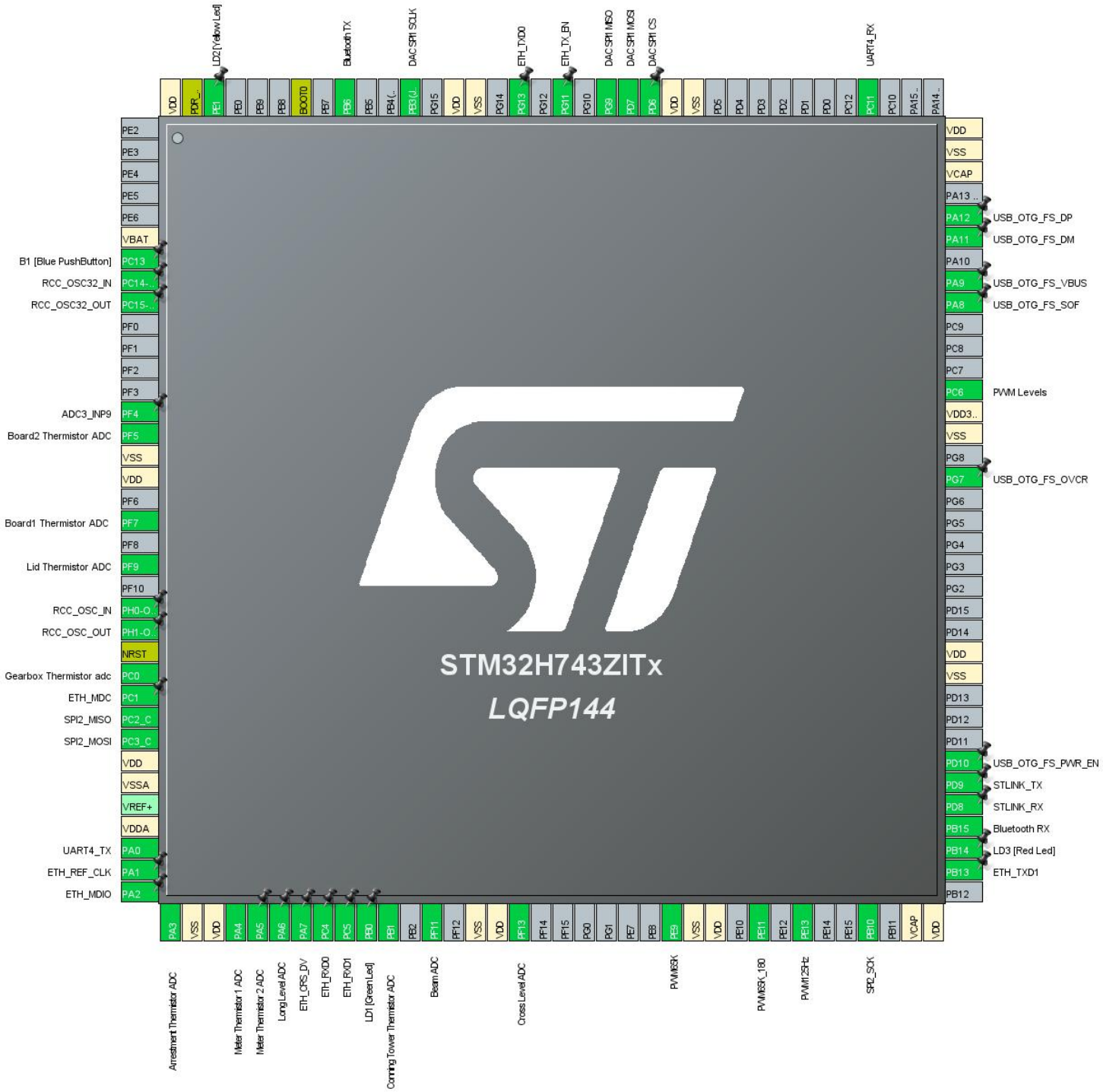
1.1. Project

Project Name	H743-ADC-Beam
Board Name	NUCLEO-H743ZI2
Generated with:	STM32CubeMX 5.2.0
Date	08/09/2019

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

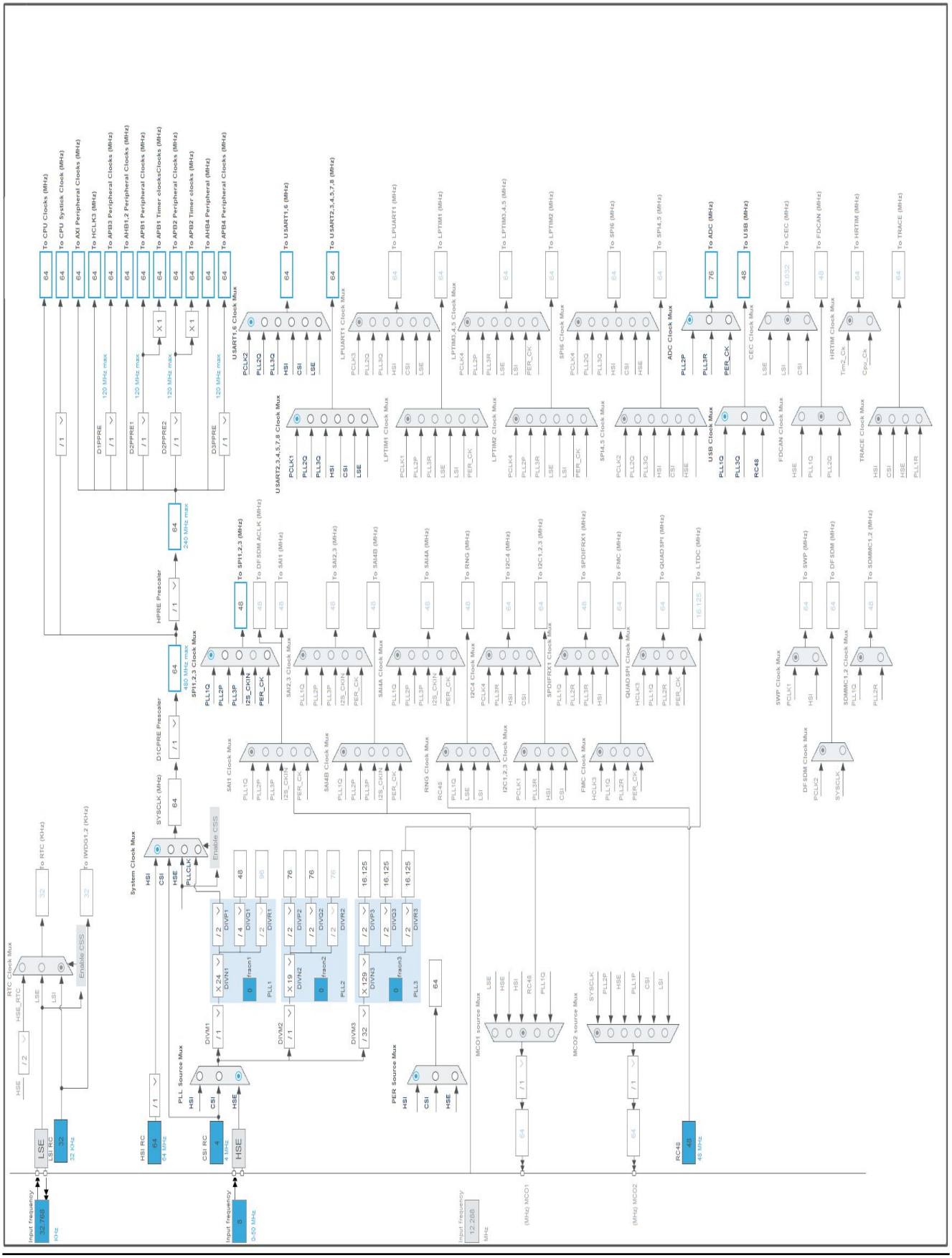
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	B1 [Blue PushButton]
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
14	PF4	I/O	ADC3_INP9	
15	PF5	I/O	ADC3_INP4	Board2 Thermistor ADC
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	ADC3_INP3	Board1 Thermistor ADC
21	PF9	I/O	ADC3_INP2	Lid Thermistor ADC
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC2_INP10	Gearbox Thermistor adc
27	PC1	I/O	ETH_MDC	
28	PC2_C	I/O	SPI2_MISO	
29	PC3_C	I/O	SPI2_MOSI	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	UART4_TX	
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
37	PA3	I/O	ADC2_INP15	Arrestment Thermistor ADC
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	ADC1_INP18, ADC2_INP18	Meter Thermistor 1 ADC
41	PA5	I/O	ADC1_INP19, ADC2_INP19	Meter Thermistor 2 ADC
42	PA6	I/O	ADC1_INP3, ADC2_INP3	Long Level ADC
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
46	PB0 *	I/O	GPIO_Output	LD1 [Green Led]

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
47	PB1	I/O	ADC1_INP5, ADC2_INP5	Conning Tower Thermistor ADC
49	PF11	I/O	ADC1_INP2	Beam ADC
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	Cross Level ADC
60	PE9	I/O	TIM1_CH1	PWM65K
61	VSS	Power		
62	VDD	Power		
64	PE11	I/O	TIM1_CH2	PWM65K_180
66	PE13	I/O	TIM1_CH3	PWM125Hz
69	PB10	I/O	SPI2_SCK	
71	VCAP	Power		
72	VDD	Power		
74	PB13	I/O	ETH_TXD1	
75	PB14 *	I/O	GPIO_Output	LD3 [Red Led]
76	PB15	I/O	USART1_RX	Bluetooth RX
77	PD8	I/O	USART3_TX	STLINK_RX
78	PD9	I/O	USART3_RX	STLINK_TX
79	PD10 *	I/O	GPIO_Output	USB_OTG_FS_PWR_EN
83	VSS	Power		
84	VDD	Power		
92	PG7	I/O	GPIO_EXTI7	USB_OTG_FS_OVCR
94	VSS	Power		
95	VDD33_USB	Power		
96	PC6	I/O	TIM3_CH1	PWM Levels
100	PA8	I/O	USB_OTG_FS_SOF	
101	PA9	I/O	USB_OTG_FS_VBUS	
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
112	PC11	I/O	UART4_RX	
120	VSS	Power		
121	VDD	Power		
122	PD6 *	I/O	GPIO_Output	DAC SPI1 CS
123	PD7	I/O	SPI1_MOSI	DAC SPI1 MOSI
124	PG9	I/O	SPI1_MISO	DAC SPI1 MISO

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
126	PG11	I/O	ETH_TX_EN	
128	PG13	I/O	ETH_TXD0	
130	VSS	Power		
131	VDD	Power		
133	PB3 (JTDO/TRACESWO)	I/O	SPI1_SCK	DAC SPI1 SCLK
136	PB6	I/O	USART1_TX	Bluetooth TX
138	BOOT0	Boot		
142	PE1 *	I/O	GPIO_Output	LD2 [Yellow Led]
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	H743-ADC-Beam
Project Folder	C:\Users\zls\STM32CubeIDE\workspace_1.0.0\H743-ADC-Beam
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.4.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN5: IN5 Single-ended

IN18: Single-ended

mode: IN19

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 19 ***
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN5: IN5 Single-ended

IN10: IN10 Single-ended

mode: IN15

IN18: Single-ended

mode: IN19

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

IN2: IN2 Single-ended

IN3: IN3 Single-ended

IN4: IN4 Single-ended

mode: IN9

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	**Channel 9 ***
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. CORTEX_M7

7.4.1. Parameter Settings:

Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.5. ETH

Mode: RMII

7.5.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 3

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

7.7. SPI1

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**24.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern

Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.8. SPI2

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**24.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.9. SYS

Timebase Source: SysTick

7.10. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: Output Compare CH3

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable

Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

7.11. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1

Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.12. UART4

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. USART1

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.14. USART3

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.15. USB_OTG_FS

Mode: Device_Only

Activate_VBUS: VBUS sensing

mode: Activate_SOF

7.15.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Low power	Disabled
Battery charging	Enabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Enabled
Signal start of frame	Enabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_INP18	Analog mode	No pull-up and no pull-down	n/a	Meter Thermistor 1 ADC
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	Meter Thermistor 2 ADC
	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	Long Level ADC
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	Conning Tower Thermistor ADC
	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	Beam ADC
ADC2	PC0	ADC2_INP10	Analog mode	No pull-up and no pull-down	n/a	Gearbox Thermistor adc
	PA3	ADC2_INP15	Analog mode	No pull-up and no pull-down	n/a	Arrestment Thermistor ADC
	PA4	ADC2_INP18	Analog mode	No pull-up and no pull-down	n/a	Meter Thermistor 1 ADC
	PA5	ADC2_INP19	Analog mode	No pull-up and no pull-down	n/a	Meter Thermistor 2 ADC
	PA6	ADC2_INP3	Analog mode	No pull-up and no pull-down	n/a	Long Level ADC
	PB1	ADC2_INP5	Analog mode	No pull-up and no pull-down	n/a	Conning Tower Thermistor ADC
	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	Cross Level ADC
ADC3	PF4	ADC3_INP9	Analog mode	No pull-up and no pull-down	n/a	
	PF5	ADC3_INP4	Analog mode	No pull-up and no pull-down	n/a	Board2 Thermistor ADC
	PF7	ADC3_INP3	Analog mode	No pull-up and no pull-down	n/a	Board1 Thermistor ADC
	PF9	ADC3_INP2	Analog mode	No pull-up and no pull-down	n/a	Lid Thermistor ADC
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_OUT (PH1)					
SPI1	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	DAC SPI1 MOSI
	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	DAC SPI1 MISO
	PB3 (JTDO/TRACESWO)	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	DAC SPI1 SCLK
SPI2	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC3_C	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM65K
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM65K_180
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM125Hz
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM Levels
UART4	PA0	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PB15	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	Bluetooth RX
	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	Bluetooth TX
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_TX
USB_OTG_FS	PA8	USB_OTG_FS_SOF	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green Led]
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red Led]
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_PWR_EN
	PG7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USB_OTG_FS_OVCR
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DAC SPI1 CS
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Yellow Led]

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
UART4 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FPU global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
USB On The Go FS global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		

*** User modified value**

9. Software Pack Report