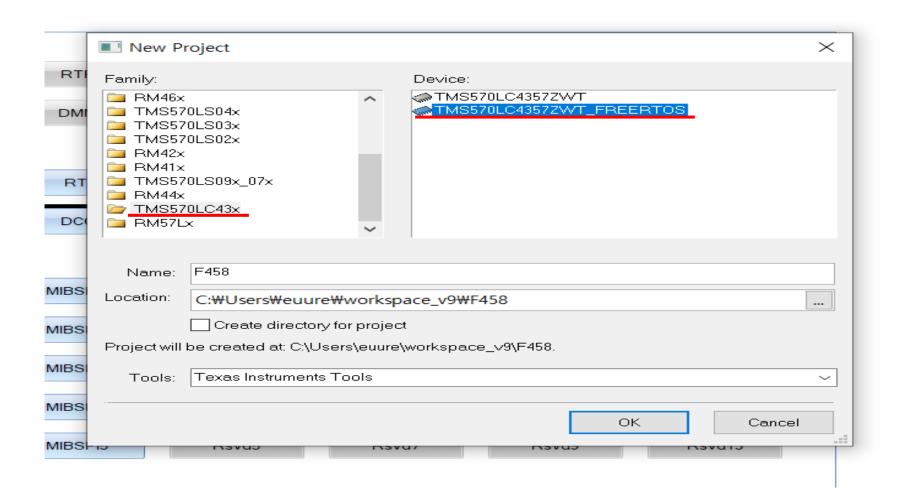
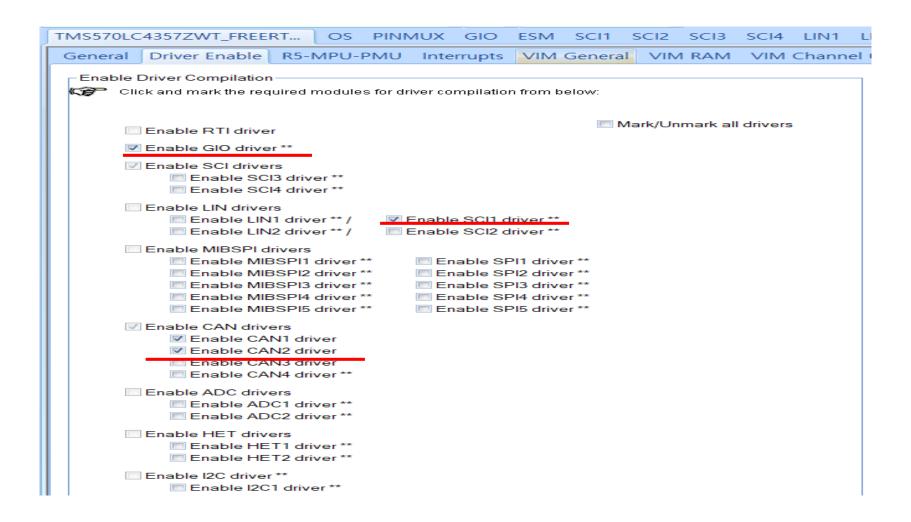
# TMDX570LC43 HDK

- HALCOGEN 설정 -

### - FREERTOS 운영체제를 사용 하기 위한 설정



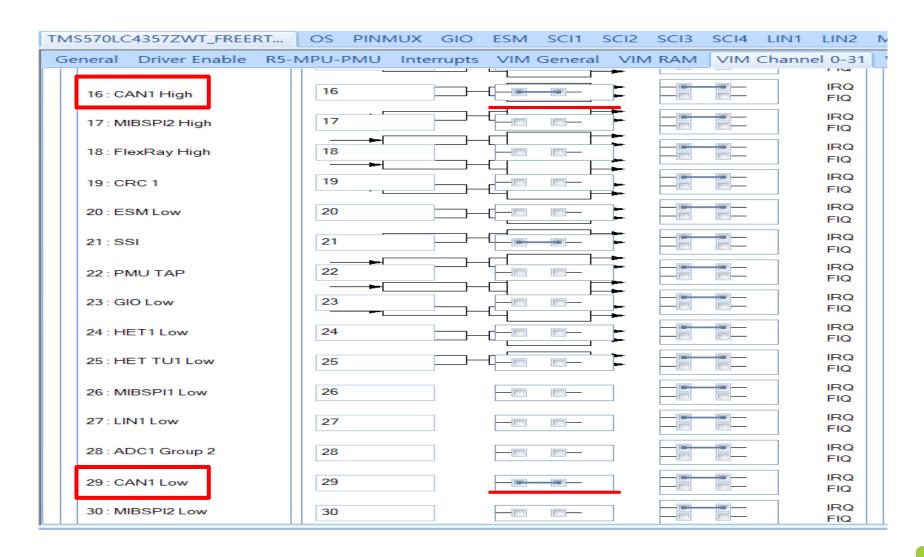
### - 시나리오 구현에 필요한 기능 설정



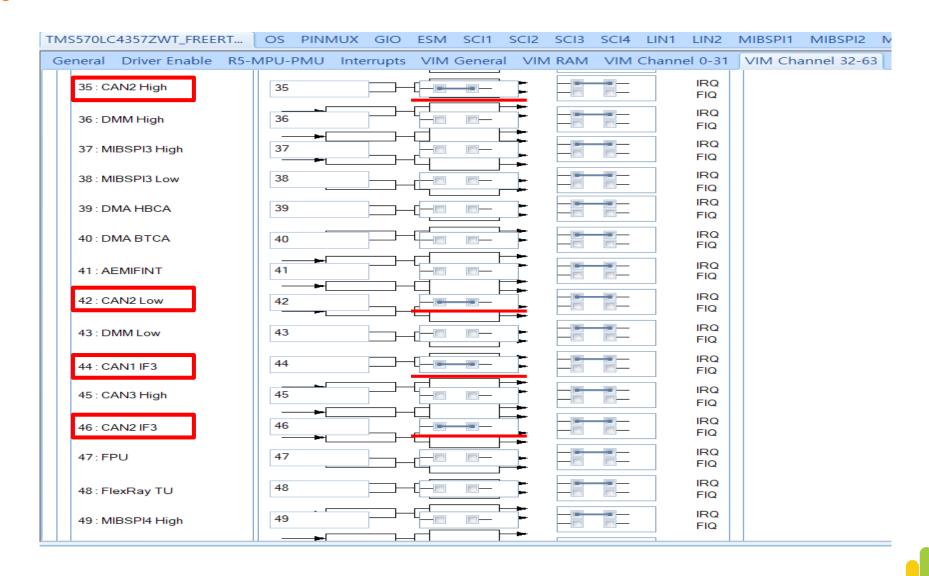
- Enable I2C2 driver \*\* Enable EMAC driver \*\* Enable DCC driver Enable EMIF driver \*\* Enable POM driver Enable CRC driver Enable CRC1 driver Enable CRC2 driver Enable EQEP driver Enable EQEP1 driver \*\* Enable EQEP2 driver \*\* Enable ETPWM driver Enable ECAP driver Enable FEE driver Enable AJSM driver
- ⊢Note :-

\*\* - Pins of these modules are muxed. Enable the corresponding pins in PINMUX Module.

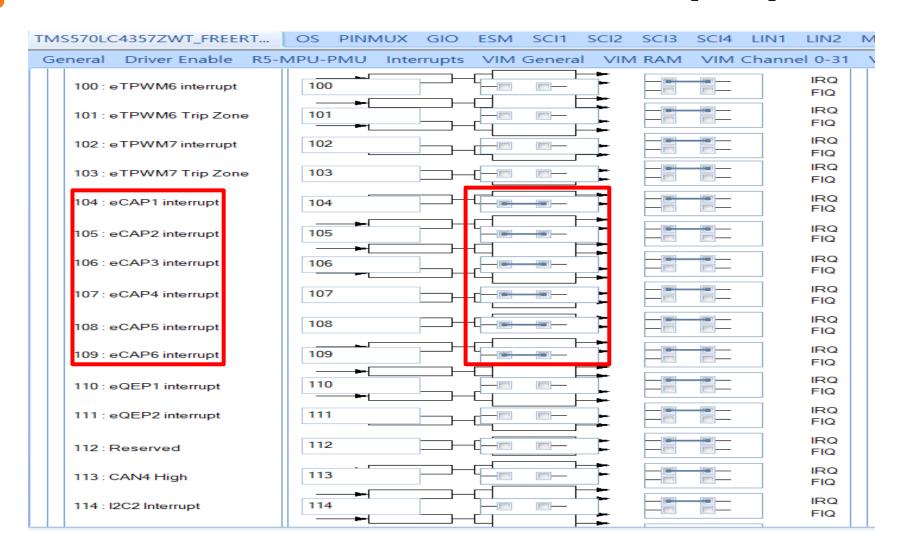
# - CAN 인터럽트를 사용하기 위한 설정(2ch)



# - CAN 인터럽트를 사용하기 위한 설정(2ch)



# - eCAP 인터럽트를 사용하기 위한 설정(6ch)



### - PWM 주기 설정에 사용하기 위한 VCLK3 값 설정

TMS570LC4357ZWT FREERT... OS PINMUX GIO ESM SCI1 SCI2 SCI3 SCI4 LIN1 LIN2 MIBSPI1 MIBSPI2 MIBSPI3 MIBSPI4 MIBSPI5 SPI1 SPI2 SPI3 SPI4 SPI5 CAN General Driver Enable R5-MPU-PMU Interrupts VIM General VIM RAM VIM Channel 0-31 VIM Channel 32-63 VIM Channel 64-95 VIM Channel 96-127 RAM Flash GCM -GCM-Clk Domains Notes GCLK Config Standard Src **GCLK** \*Clk Srcs 300.000 GCLK Max -- 330 MHz Wakup Src -HCLK Divider -HCLK Config **HCLK** HCLK Max -- 150 MHz 150.000 PLL<sub>1</sub> VCLK Max -- 110 MHz Power Down Src VCLK1 Divider VCLK1 Config VCLK1 VCLK PLL1 75.000 VCLK2 Max -- 110 MHz VCLK2 Divider VCLK2 Config VCLK2 VCLK3 Max -- 110 MHz 75.000 VCLK3 Divider VCLKA1 Max -- 110 MHz VCLK3 Config VCLK3 10.000 VCLKA2 Max -- 110 MHz VCLKA1 Src VCLKA1 Confia Clk Srcs VCLKA1 VCLKA4 Max -- 110 MHz VCLK -75.000 VCLK VCLKA2 Src RTICLK Max -- VCLK Freq VCLKA2 Config Clk Srcs \_ VCLKA2 **VCLK** 0.000 VCLK RTI1 Post Src -RTI1 Pre Src RTI1 Config RTI1 Divider RTI1CLK Clk Srcs PLL<sub>1</sub> VCLK 75.000 VCLKA4 Src VCLKA4 Divider VCLKA4 Post Src VCLKA4 Config Clk Srcs VCLKA4 DIV 75.000 VCLKA4\_DIVR VCLK **VCLK** VCLKA4 S 75.000

00.0

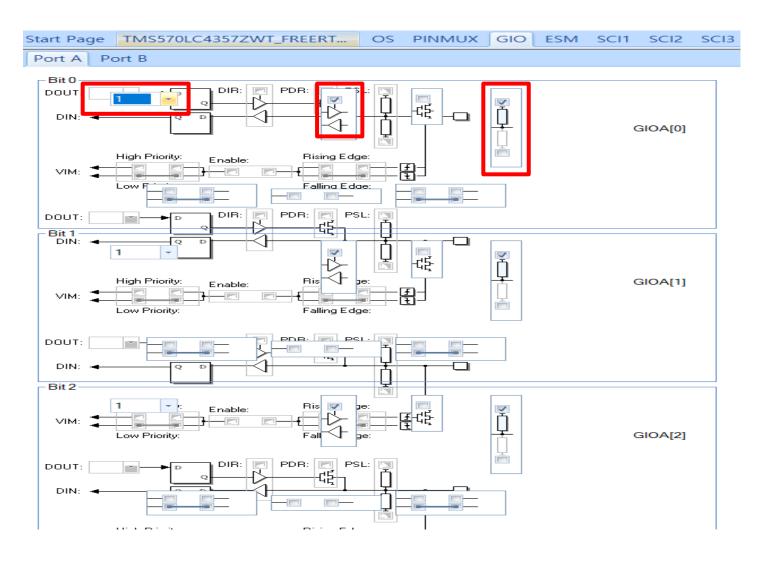
# - PINMUX 설정

B5	GIOA[5]	NONE	NONE	EXTCLKIN	NONE	eTPWM1A	<b>—</b>
G19	MIBSPI1NENA	NONE	MII_RXD[2]	N2HET1[23]	NONE	ECAP4	
H18	MIBSPI5NENA	DMM_DATA[07]	MII_RXD[3]	NONE	NONE	ECAP5	
M1 N1	GIOA[7]  N2HET1[15]	NONE  MIBSPI1NCS[4]	N2HET2[06]	NONE  N2HET2[22]	NONE NONE	eTPWM2A  ECAP1	-n n-
R2	MIBSPI1NCS[0]	MIBSPI1SOMI[1]	MII_TXD[2]	NONE	NONE	ECAP6	
U1	N2HET1[03]	MIBSPIANCS[0]	NONE	N2HET2[10]	NONE	eQEP2B	
V2	N2HET1[01]	MIBSPI4NENA	NONE	N2HET2[08]	NONE	eQEP2A	
V8	MIBSPI3SOMI	EXT_ENA	NONE	NONE	NONE	ECAP2	
W8	MIBSPI3SIMO	EXT_SEL[00]	NONE	NONE	NONE	ECAP3	

# - PWM 사용시 TBCLK 로 사용

Use GIOA_5 for disabling selected HET1 PWM outputs    Leable EMIF_CLK output   Enable Temp Sensor 1     Use Alternate ADC 'Trigger Option-A'   Ethernet Mil/   Enable Temp Sensor 2     Use Alternate ADC 'Trigger Option-B'   Ethernet Mil/   Enable Temp Sensor 3     Use Alternate ADC 'Trigger Option-B'   Ethernet Mil/   Enable Temp Sensor 3     ETPWM   EOEPERR12   FINANCIA   EOEPERR12   EOE	General		
ETPWM7 EQEPERR12 **Done in etpwmlnit Select IGIO B Port 1 for External DMA Request  Select IGIO B Port 2 for External DMA Request  Select IGIO B Port 3 for External DMA Request  Select IGIO B Port 3 for External DMA Request  Select IGIO B Port 4 for External DMA Request  Select IGIO B Port 5 for External DMA Request  Select IGIO B Port 6 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Select IGIO B Port 7 for External DMA Request  Filter eQEP18 input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter	Use GIOA_5, for disabling selected HET1 PWM outputs  Use GIOB_2, for disabling selected HET2 PWM outputs  Use Alternate ADC ' Trigger Option-A'  Use Alternate ADC ' Trigger Option-B'  ETPWM  ETPWM1  EQEPERR12  EQEPERR12  ETPWM2  EQEPERR12  EQEPERR12  ETPWM3  EQEPERR12  EQEPERR12  ETPWM4  EQEPERR12  EQEPERR12  ETPWM4  EQEPERR12  ETPWM5  EQEPERR12  ETPWM6  EQEPERR12  ETPWM7  EQEPERR12  ETPWM7  EQEPERR12  ETPWM8  EQEPERR12	Ethernet MII/ RMII select  ETPWM for ADC triqqers(Set by default).  Selecting Start of Conversion(SOC2A) of eTi Selecting Start of Conversion(SOC3A) of eTi Selecting Start of Conversion(SOC3A) of eTi Selecting Start of Conversion(SOC3A) of eTi	Select GIO A Port 1 for External DMA Request  Select GIO A Port 2 for External DMA Request  Select GIO A Port 3 for External DMA Request  Select GIO A Port 4 for External DMA Request  Select GIO A Port 5 for External DMA Request  Select GIO A Port 6 for External DMA Request  Select GIO A Port 6 for External DMA Request
Filter eQEP1A input through a 6-VCLK3-cycle counter  Filter eQEP1B input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter		71110	PWM1 Select GIO B Port 1 for External DMA Request  Select GIO B Port 2 for External DMA Request
Filter eQEP1B input through a 6-VCLK3-cycle counter  Filter eQEP1I input through a 6-VCLK3-cycle counter  Filter eQEP1I input through a 6-VCLK3-cycle counter  Filter eQEP1S input through a 6-VCLK3-cycle counter  Filter eQEP1S input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter	Control for Input Connections to eQEPx Modules.	Control for Input Connections to eCAP Modules.	Select GIO B Port 4 for External DMA Request
Filter eQEP1I input through a 6-VCLK3-cycle counter  Filter eQEP1S input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter	Filter eQEP1A input through a 6-VCLK3-cycle counter	Filter eCAP1 input through a 6-VCLK3-cycle count	ter Select GIO B Port 5 for External DMA Request
Filter eQEP1S input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter  Filter eQEP2A input through a 6-VCLK3-cycle counter	Filter eQEP1B input through a 6-VCLK3-cycle counter	Filter eCAP2 input through a 6-VCLK3-cycle count	ter Select GIO B Port 6 for External DMA Request
Filter eQEP2A input through a 6-VCLK3-cycle counter	Filter eQEP1I input through a 6-VCLK3-cycle counter	Filter eCAP3 input through a 6-VCLK3-cycle count	er Select GIO B Port 7 for External DMA Request
	Filter eQEP1S input through a 6-VCLK3-cycle counter	Filter eCAP4 input through a 6-VCLK3-cycle count	ter
Filter eQEP2B input through a 6-VCLK3-cycle counter	Filter eQEP2A input through a 6-VCLK3-cycle counter	Filter eCAP5 input through a 6-VCLK3-cycle count	ter
	Filter eQEP2B input through a 6-VCLK3-cycle counter	Filter eCAP6 input through a 6-VCLK3-cycle count	ter

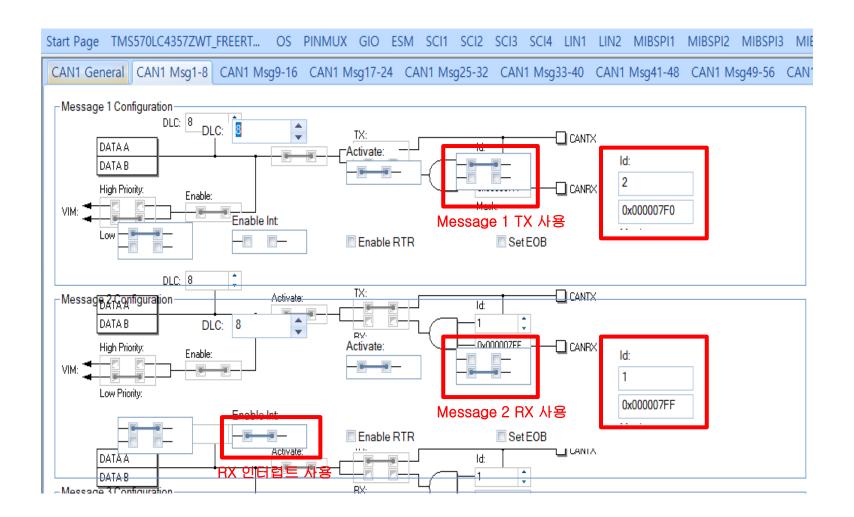
## - GIOA 4개핀 사용(출력핀으로 사용)



# - CAN 통신 설정 (DSP↔ MCU)

CAN1 Msg49-56 CAN1 Msg57-64 CAN1 Port

Start Page	TMS570LC4357Z	WT FREERT	OS F	PINMUX	GIO	ESM	SCI1 SCI2	SCI3 SCI4 I	LIN1 LIN2	MIBSPI1
	eral CAN1 Msg1					1 (Δ)	N1 Msa25-32	CAN1 Msg33	-40 CΔN1	Msa41-48
CANT OCIN	CAIVI WISG	O CAIVI IVIS	g5 10	CAIVIII	13917 2	CA	141 1413925 52	CAIVI Wisgss	THO CAIVI	Wisg+1 +0
CAN1 Tim	ing Configuration—	_								
Bit Rat	e: <mark>300</mark>	Propagatio	n Delay:	700						
SP Re	rf. 75	Calculatetd E	Bit Rate:	300.000						
Calculate	CAN1 Timing 0.000 0	→ 10.00 BRP	0 -	<b>►</b> 0 fBr	, <del>-</del>	10.000	BRPE	fCan	tQ	
VCLKA	1: 75.000	24		3.000		0		3.000	333.333	
	SYNC_SEG PROP_S	SEG PH CECH	Du cor	27						
		Nomina	ar Dik Tillik				N	Nominal Bit Time:	10	
			1				N	Nominal Bit Rate:	300.000	
				5	Sample F	oint		Sample Point	70.000	
	SYNC_SEG	PROP_SEG	PH_S	EG1	PH_SE	G2				
	1	3	3	3	3		Synchronizat	tion Jump Width:	3	
CAN1 Auto Bus On Configuration										
■ Enab	le Auto Bus On	ABO	TR: 0			tAbo	o: 0			
VCLK1: 75.000 ABO Counter tAbo Nominal 0.000										
CAN1 General Configuration										
☐ Disable Automatic Retransmission ☐ Enable Identifier Extension ☐ E							Enable Ram	ECC		



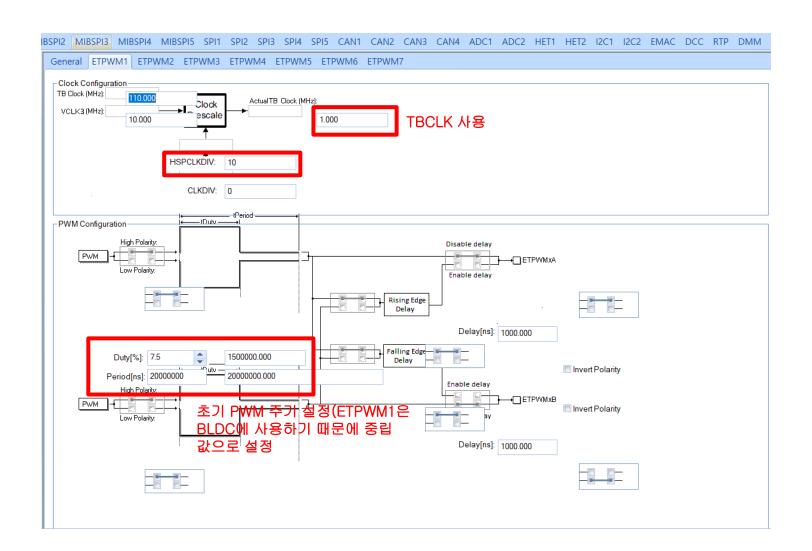
# - CAN 통신 설정 (FPGA↔ MCU)

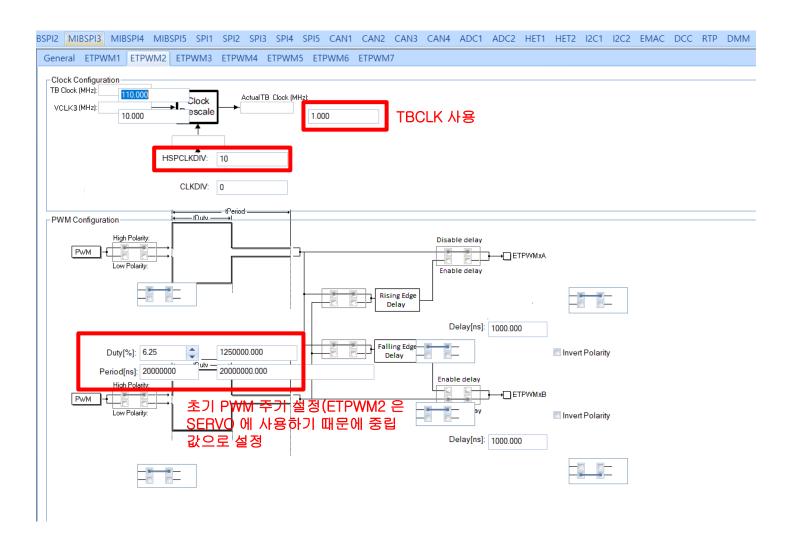
Start Page TMS570LC4357ZWT_FREERT OS PINMUX GIO ESM SCI1 SCI2 SCI3 SCI4 LIN1 LIN2 MIBSP	11 MIBSPI2 MIBSPI3 MIBSPI4 MIBSPI5 SPI1 SPI2 SPI3 SPI4 SPI5 CAN1 CAN2
CAN2 General CAN2 Msg1-8 CAN2 Msg9-16 CAN2 Msg17-24 CAN2 Msg25-32 CAN2 Msg33-40 CAN2 Msg41-	48 CAN2 Msg49-56 CAN2 Msg57-64 CAN2 Port
CAN2 Timing Configuration—	1
Bit Rate: 250 Propagation Delay: 700	
SP Ref. 75 Calculatetd Bit Rate: 250.000	
Calculated CAN2 Timing 0	- ]
VCLKA1: 75.000 24 3.000 0 333.333	
SYNC_SEG PROP_SEG PH_SEG1   DU_SEG2   Nominal Bit Time   Nominal Bit Time: 12	
Nominal Bit Rate: 250.000	
Sample Point Sample Point 66.667	
SYNC_SEG         PROP_SEG         PH_SEG1         PH_SEG2           1         3         4         4         Synchronization Jump Width: 4	
Sylvanorization camp main	
CAN2 Auto Bus On Configuration	1
Enable Auto Bus On ABOTR: 0 tAbo: 0	
VCLK1: 75.000 ABO Counter 0.000	
CAN2 General Configuration	1
☐ Disable Automatic Retransmission ☐ Enable Identifier Extension ☐ Enable Ram ECC	
체크 해제	1

Start Page TMS570LC4357ZWT\_FREERT.... OS PINMUX GIO ESM SCI1 SCI2 SCI3 SCI4 LIN1 LIN2 MIBSPI1 MIBSPI2 MIBSPI3 MIE CAN2 General CAN2 Msg1-8 CAN2 Msg9-16 CAN2 Msg17-24 CAN2 Msg25-32 CAN2 Msg33-40 CAN2 Msg41-48 CAN2 Msg49-56 CAN2 -Message 1 Configuration-DLC: 8 DLC: 8 TX: - CANTX DATAA ⊢Activate: DATA B - CANRX High Priority: Enable: Mask: 0x000007F0 Enable Int Enable RTR Set EOB DLC: 8 TX: ☐ CANTX Activate: -Message 2 Configuration -DLC: 8 DATA B - CANRX Activate: 0v000007FF High Priority: Enable: ld: Low Priority: 0x000007FF Enable Int Enable RTR Set EOB Activate: LANIA L DATAA ld: DATA B

## - PWM 설정(2ch)

BSPI2 MIBSPI3 MIBSPI4 MIBSPI5 SPI1 SPI2 SPI3 SPI4 SPI5 CAN1 CAN2 CAN3 CAN4 ADC1 General ETPWM1 ETPWM2 ETPWM3 ETPWM4 ETPWM5 ETPWM6 ETPWM7 -Enable ETPWM modules Enable ETPWM1 ▼ Enable ETPWM2 Enable ETPWM3 Enable ETPWM4 Enable ETPWM5 Enable ETPWM6 ■ Enable ETPWM7 ⊢Note :-\*\* - etpwmInit function sets the time-base counters in up-count mode. Application can configure the module in a different mode using other functions in this driver(Sample code provided in the examples folder). In that case, application need not call etpwmlnit function.





## - eCAP 설정(6ch)

BSP12 MIBSP13 MIBSP14 MIBSP15 SP11 SP12 SP13 SP14 SP15 CAN1 CAN2 CAN3 CAN4 ADC1 ADC2 HET1 HET2 12C1 12C2 EMAC DCC RTP DMM EMIF POM CRC ETPWM ECAP General ECAP1 Configuration ECAP2 Configuration ECAP3 Configuration ECAP4 Configuration ECAP5 Configuration ECAP6 Configuration -Enable ECAP modules-▼ Enable ECAP1 ▼ Enable ECAP2 ▼ Enable ECAP3 ▼ Enable ECAP4 Enable ECAP5 ▼ Enable ECAP6

	PI2 SPI3 SPI4 SPI5 CAN1 CAN2 CAN3 CANS CANS CANS CANS CANS CANS CANS CANS	
Capture 2 Polarity: RISING_EDGE  Capture 4 Polarity: RISING_EDGE  V	Capture Mode: CONTINUOUS  Stop/Wrap Capture: CAPTURE_EVENT3  Reset Counter After Capture 1  Reset Counter After Capture 2  Reset Counter After Capture 3  Reset Counter After Capture 4	
Interrupt Selection Enable CEVT1 Enable CEVT2 Enable CNTOVF Enable PRD  RISING-FALL 시점에 인터럽	■ Enable CEVT4 ■ Enable CMP  NG-RISING EDGE ■ 발생 설정	나머지 채널도 같게 설정

# - eQEP 설정

12 MIBSPI3 MIBSPI4 N	MIBSPI5 SPI1 SPI2 SPI3 SPI4 S	SPI5 CAN1 CAN2 CAN3 CAN4 A	DC1 ADC2 HET1 HET2 I2C1 I2C2 EMAC E	DCC RTP DMM EMIF POM CRC ETPWM ECAP EC
QEP1 EQEP2				
General Configuration  Position Counter Mode:	QUADRATURE_COUNT V	☐ Invert QEPxA Polarity	Compare Output Configurations  Sync Output Pin Select INDEX_PIN	Enable Sync Output
External clock rate:	RESOLUTION_1x	Invert QEPxl Polarity Invert QEPxS Polarity	ShadowLoad Mode: QPOSCNT_EQ_QPSCMP	, , , ,
Select QDIR:	CLOCKWISE	Gate Index Pin with Strobe	Sync Output Polarity: ACTIVE_HIGH	
- Position Counter Configuration	1		Interrupt Configuration—	
Counter Init Index Event	RISING_EDGE -	Max Position Count 0xFFFFFFF	Position counter error Interrupt	Position-compare ready Interrupt
Counter Init Strobe Event:	DIRECTON_DEPENDENT -	☐ Init Counter on Index Event	Quadrature phase error Interrupt     Quadrature direction change Interrupt	Position-compare match Interrupt  Strobe event latch Interrupt
Position Counter Reset On: UNITTIME_EVENT		Init Counter on Strobe Event Enable SW Inititalization	Watchdog time out Interrupt	☐ Index event latch Interrupt
Counter Latch Index Event	RISING_EDGE -	Init Position Count to: 0x00000000	Position counter underflow Interrupt	✓ Unit time out interrupt
Counter Latch Strobe Event	RISING_EDGE +		Position counter overflow Interrupt	
- Capture Configuration			-Watchdog Configuration	
Capture Timer Prescaler:	PS_8 -	☐ Init Counter on Strobe Event	Watchdog Timer Value: 0x0000	
Unit Pos Event Prescaler:	PS_1 v	Unit Init Period: 0x00000000		
Cap Timer Pos Mode:	ON_UNIT_TIMOUT_EVENT	<b>v</b>		