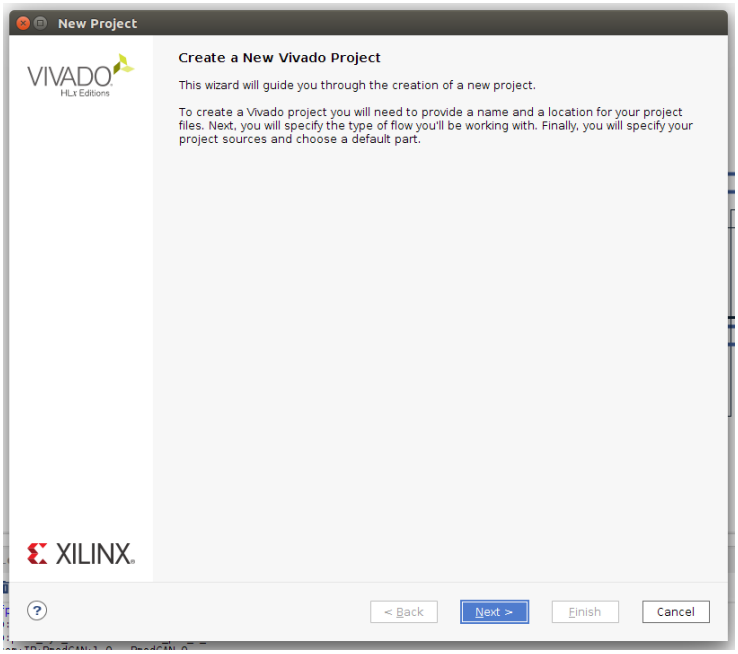
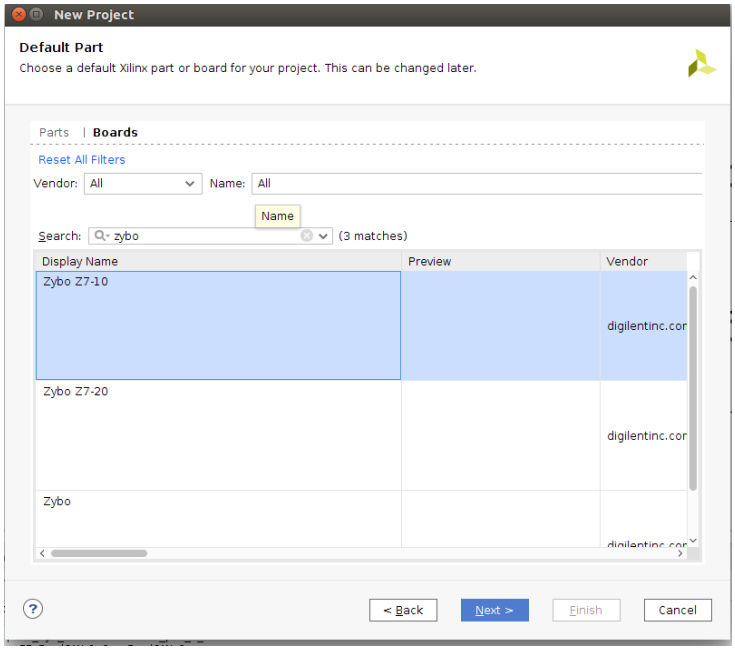
**< Pmod CAN >**

**[준비물]**
- Zybo z7 10
- pmodCAN

**[FPGA Hardware Design]**
- Digilent tutorial page 참조
https://reference.digilentinc.com/learn/programmable-logic/tutorials/pmod-ips/start

**1) zynq block design 만들기**

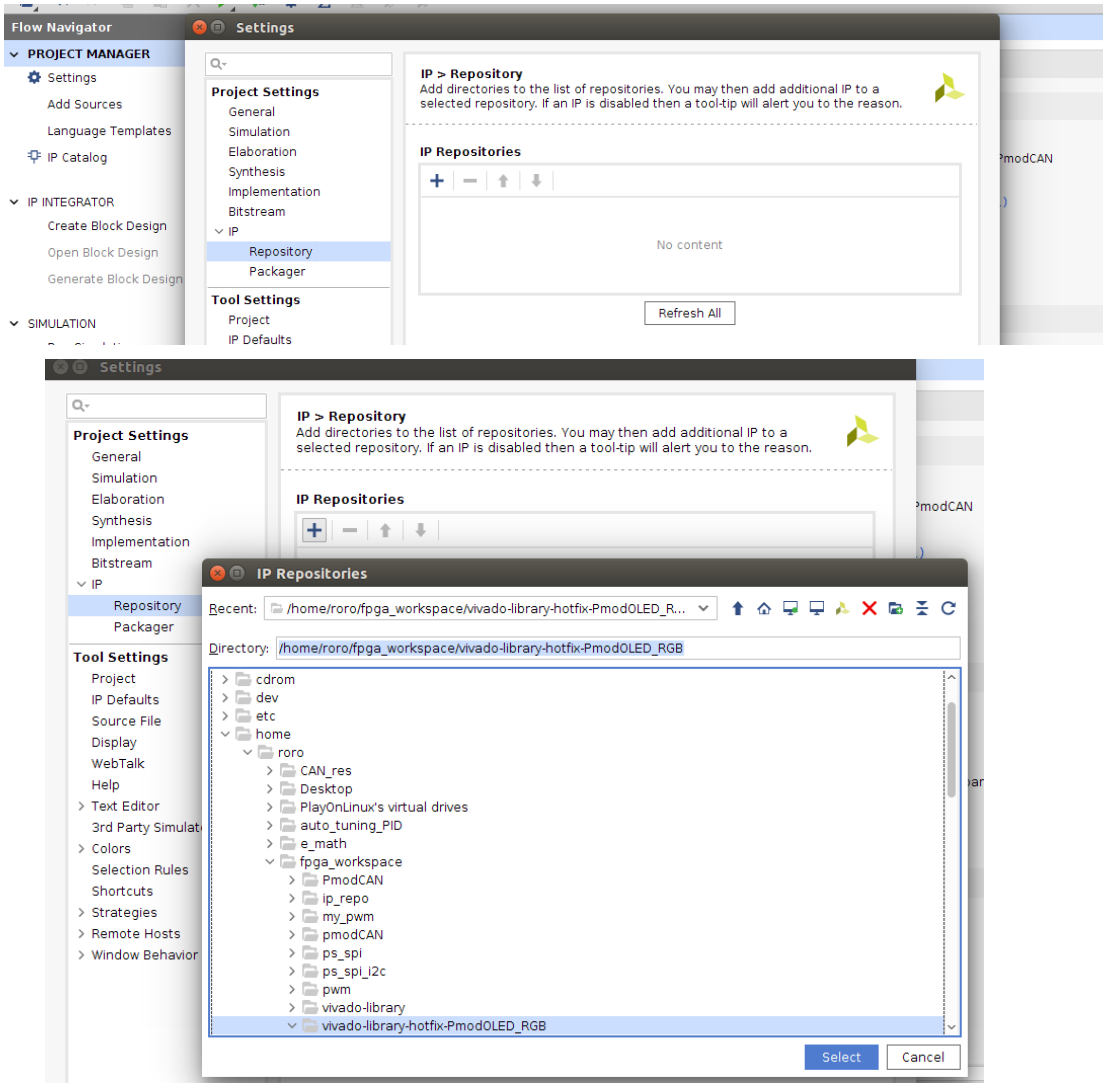


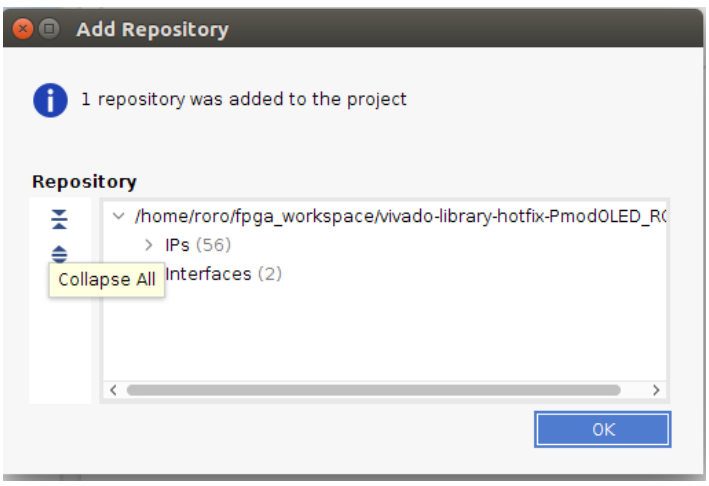
## 2) Digilent Library 추가

- Digilent/vivado-library 에서 Vivado 버전에 맞는 라이브러리 다운로드
https://github.com/Digilent/vivado-library/releases?_ga=2.237338498.301450701.1562495142-347646649.1554689188

- IP 추가하기 : Settings → IP → Repository → +

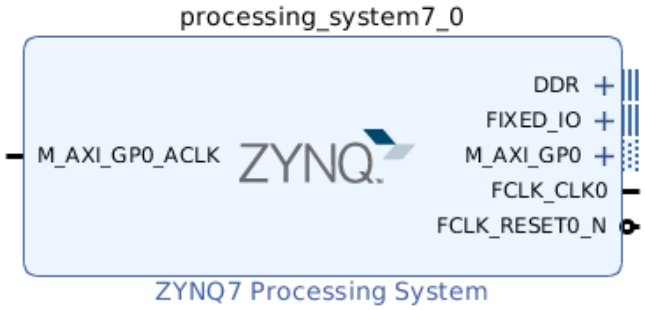



- IP와 Interfaces 모두 추가 → OK

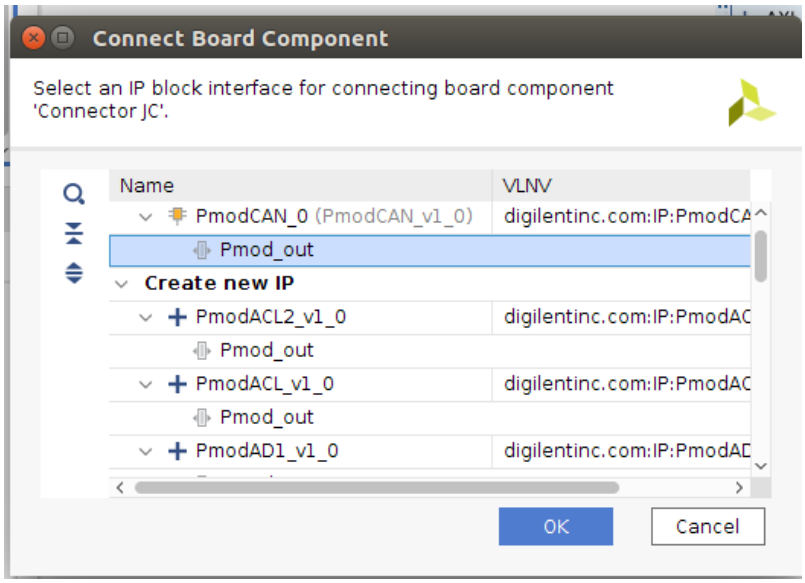


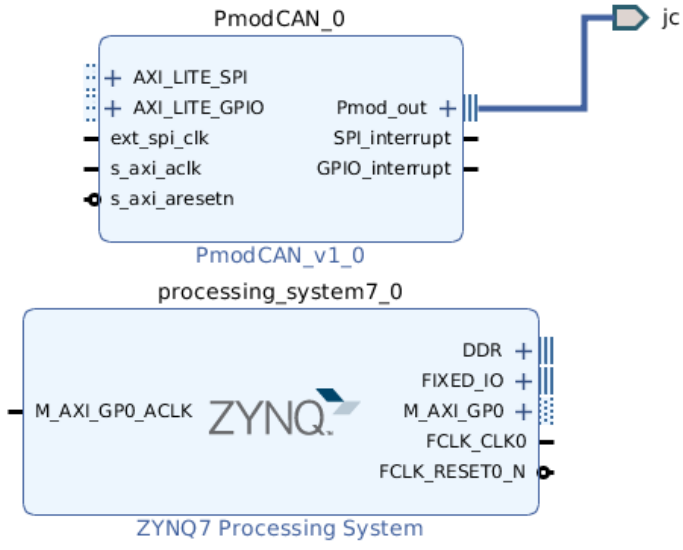
**3) Pmod CAN block 추가**

- Create Block Design → Zynq block 추가



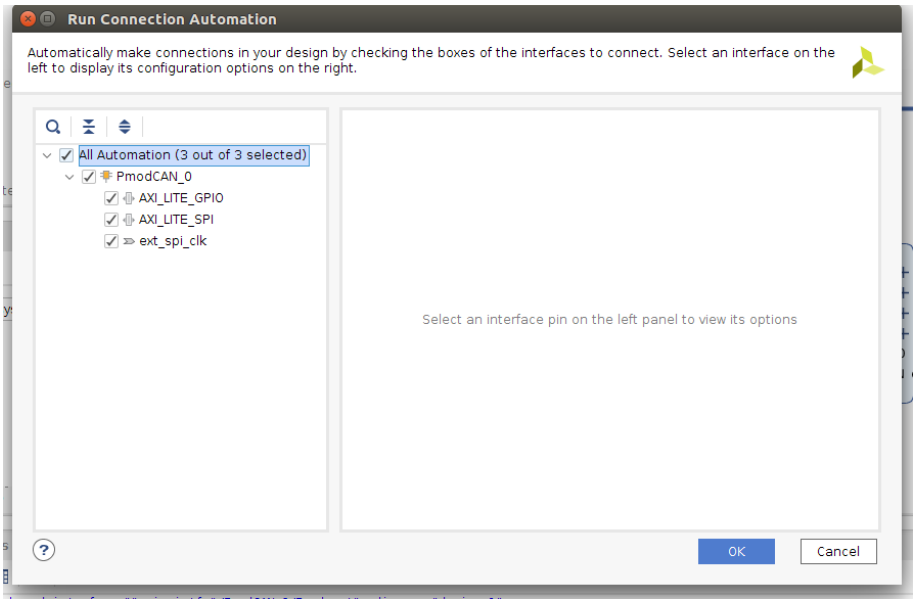

- Board → Pmod → Connector JC 우클릭 → Create Board Component → PmodCAN_0 IP 찾아서 OK

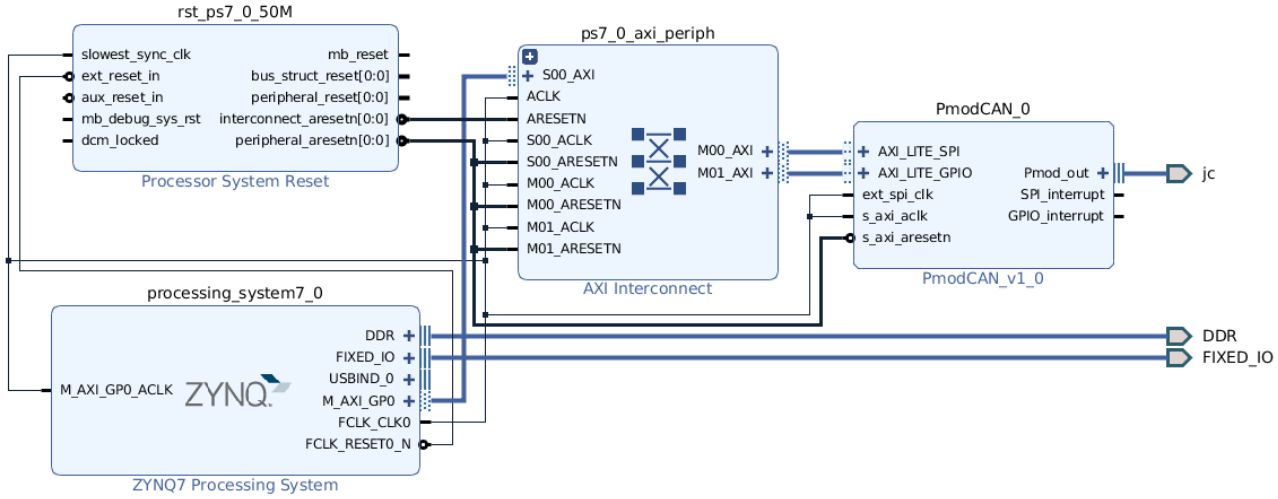


## 4) Run Connection Automation

- 모두 체크한 후 OK



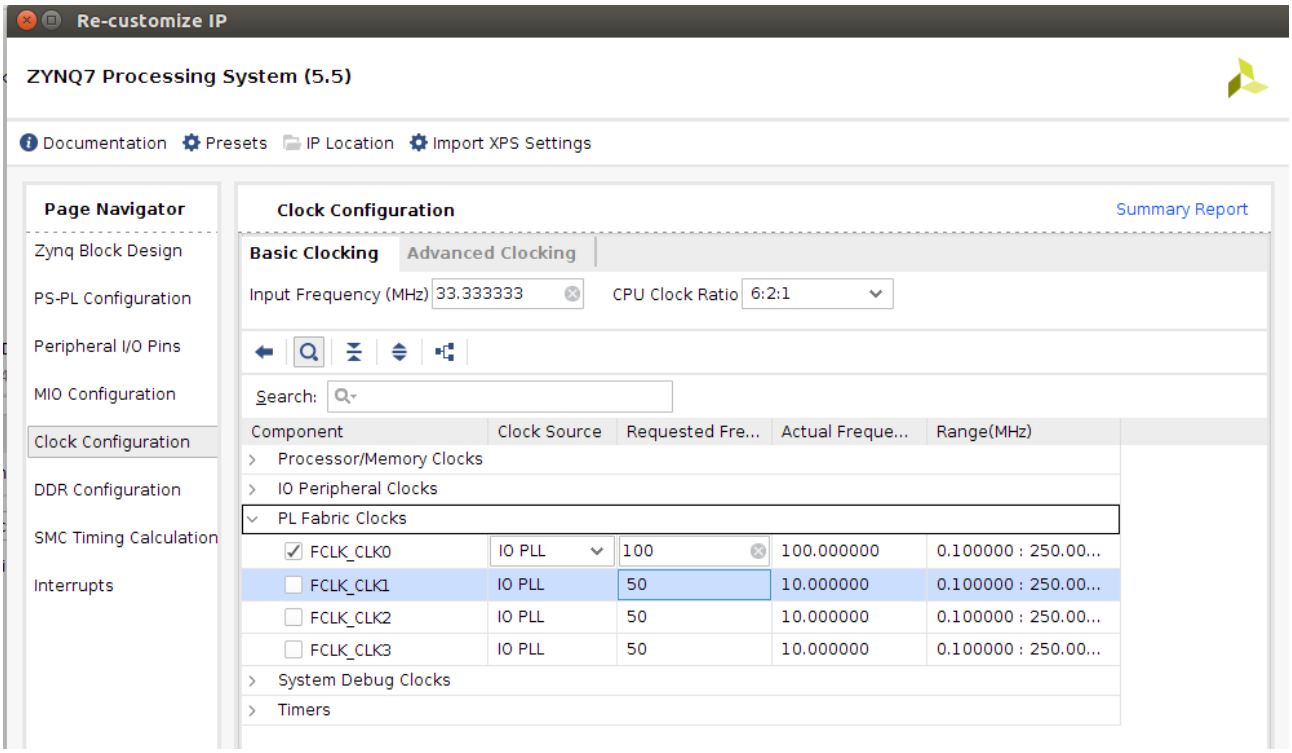
**5) Clock 설정**

- Pmod IP에 맞는 Reference clock frequency 확인 후 설정

**Pmods Supported**

| Pmod | Interface Type | Reference clock frequency (MHz) | Reference Clock signal n |
|---|---|---|---|
| BTN | GPIO | - | - |
| CAN | SPI | 100 | ext_spi_clk |
| CLS | SPI | 50 | ext_spi_clk |

- zynq block 더블 클릭 → Clock Configuration → PL Fabric Clocks
  → FCLK_CLK0 체크 후 100MHz 설정



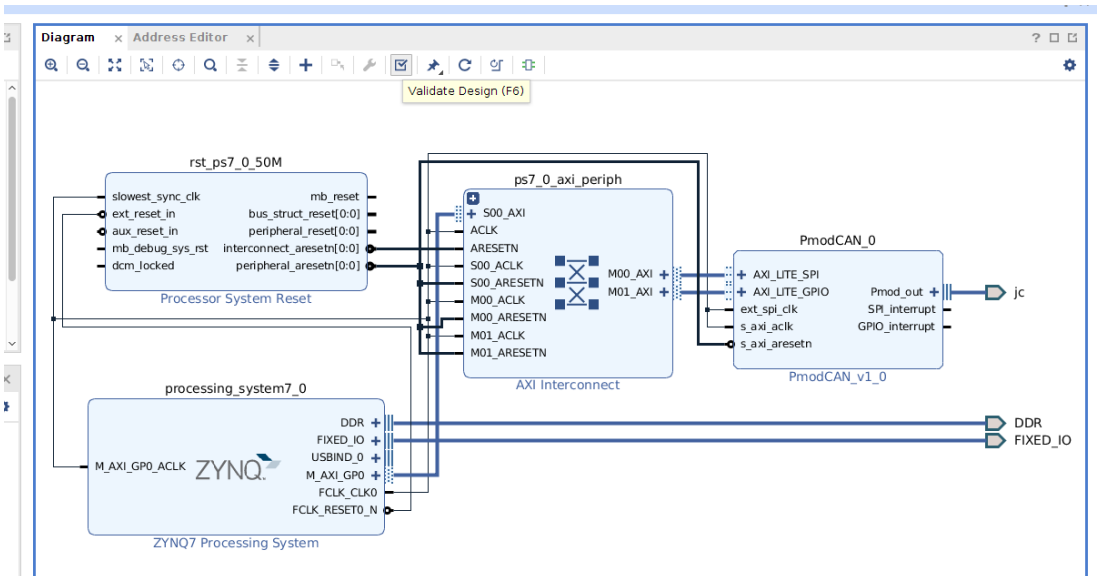

- Block Design 에서 PmodCAN_0 IP의 ext_spi_clk이
  zynq block의 FCLK_CLK0에 연결되어 있는지 확인

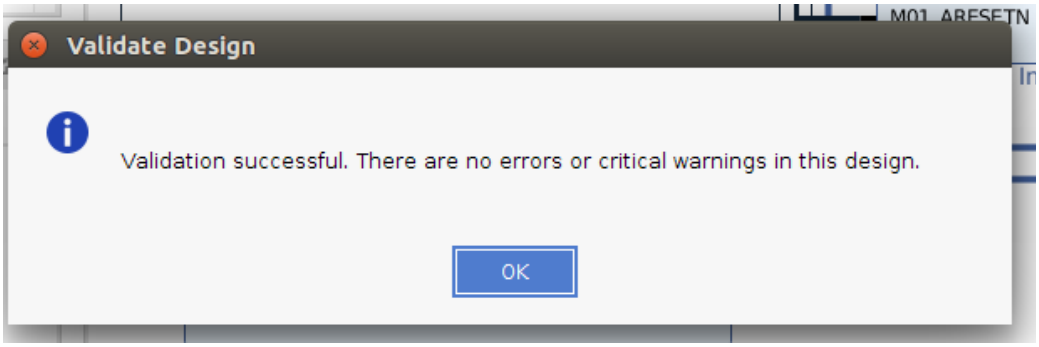
**6) 인터럽트 설정**

- PmodCAN은 인터럽트를 사용해 동작하지 않으므로 설정하지 않음

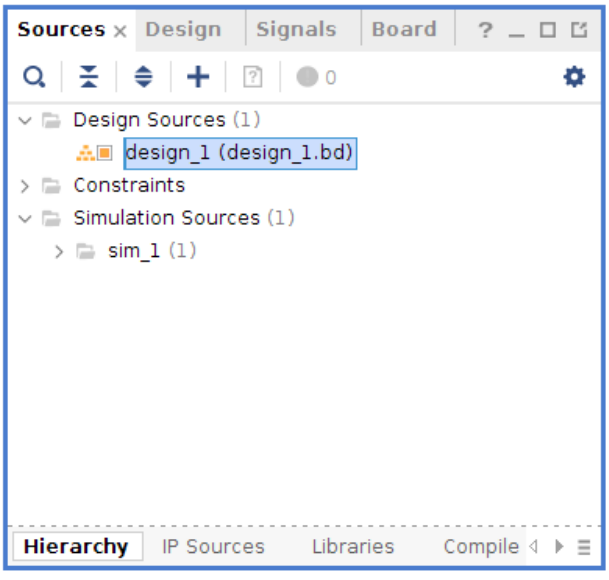
**7) Validate the Design**

- F6 또는 Validate Design 클릭

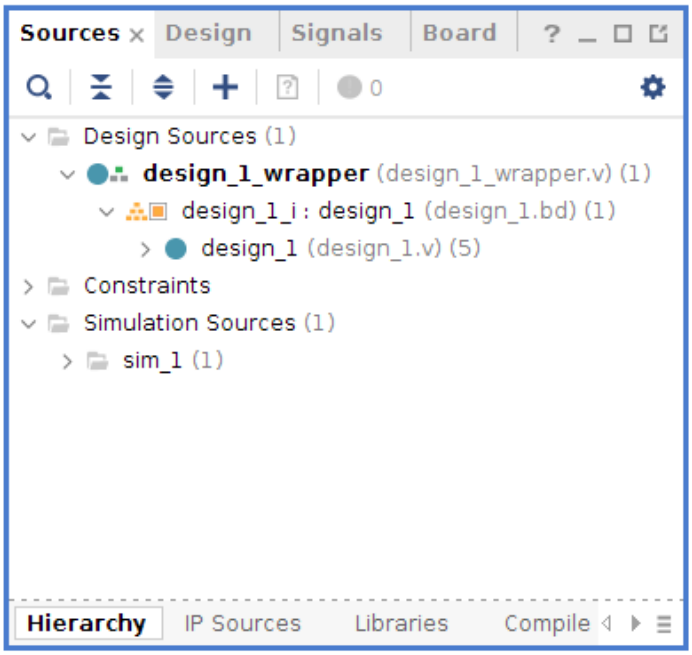



- Create HDL Wrapper : design_1 우클릭 Create HDL Wrapper 선택

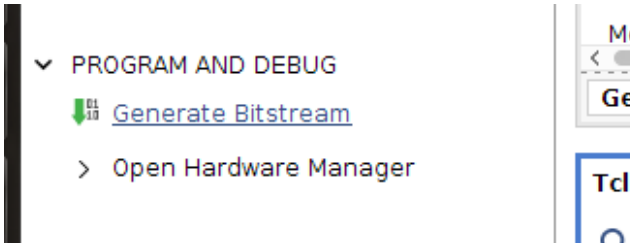


- Wrapper 생성 후

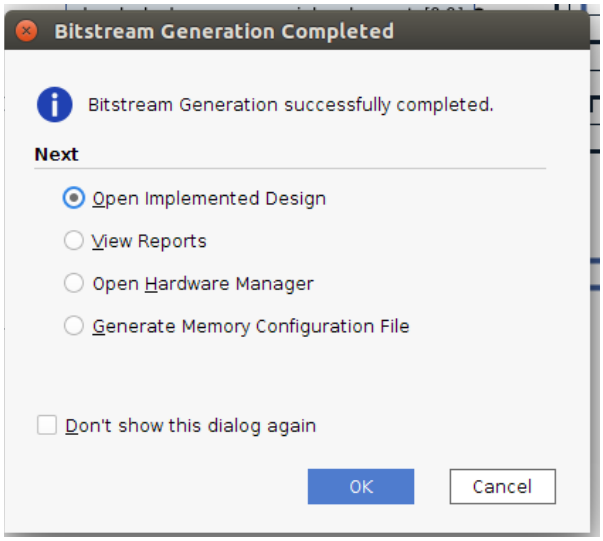



### 8) 비트 스트림 생성

- PROGRAM AND DEBUG → Generate Bitstream 클릭

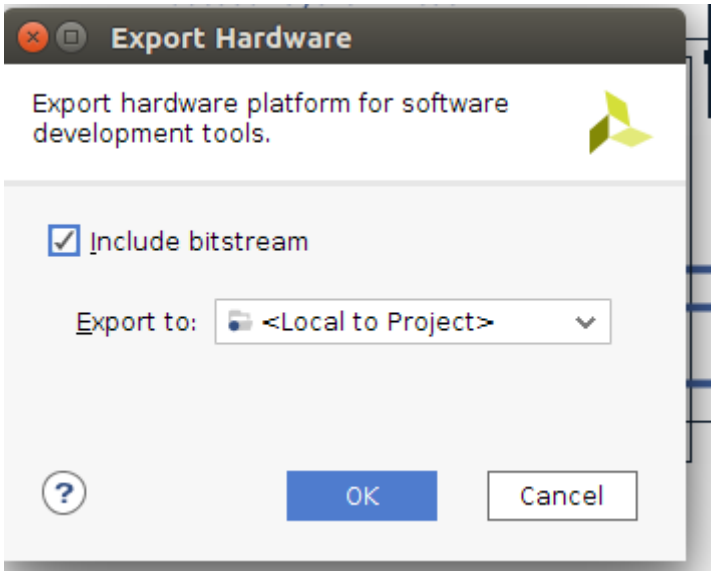



- 자동으로 Analysis, Synthesis, Implementation 과정 후 Bitstream을 생성한다.



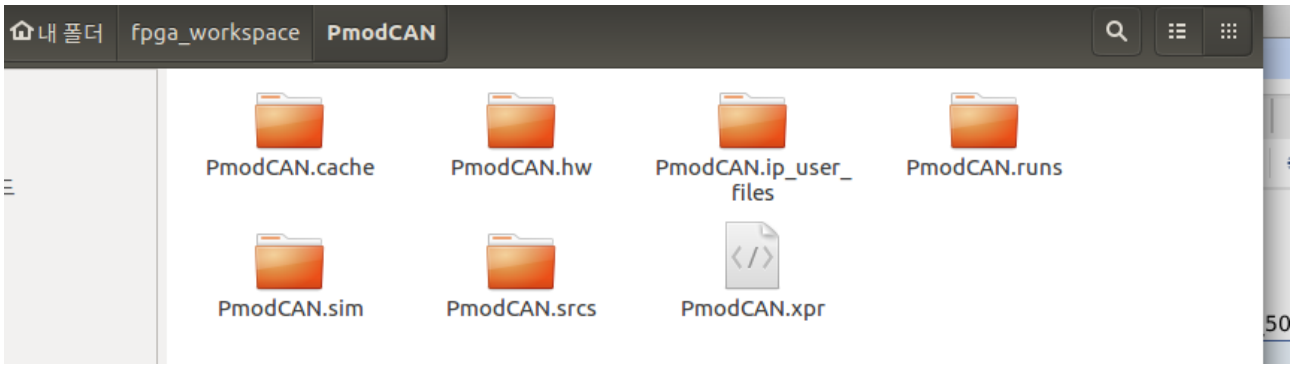
**9) Export the Hardware Design to SDK**

- File → Export → Export Hardware → include bitstream을 꼭 체크 해야 함.




- Export Hardware를 하면 프로젝트를 생성했던 폴더에 .sdk 폴더가 생성된 것을 확인 할 수 있음.

→ Export 전




→ Export 후