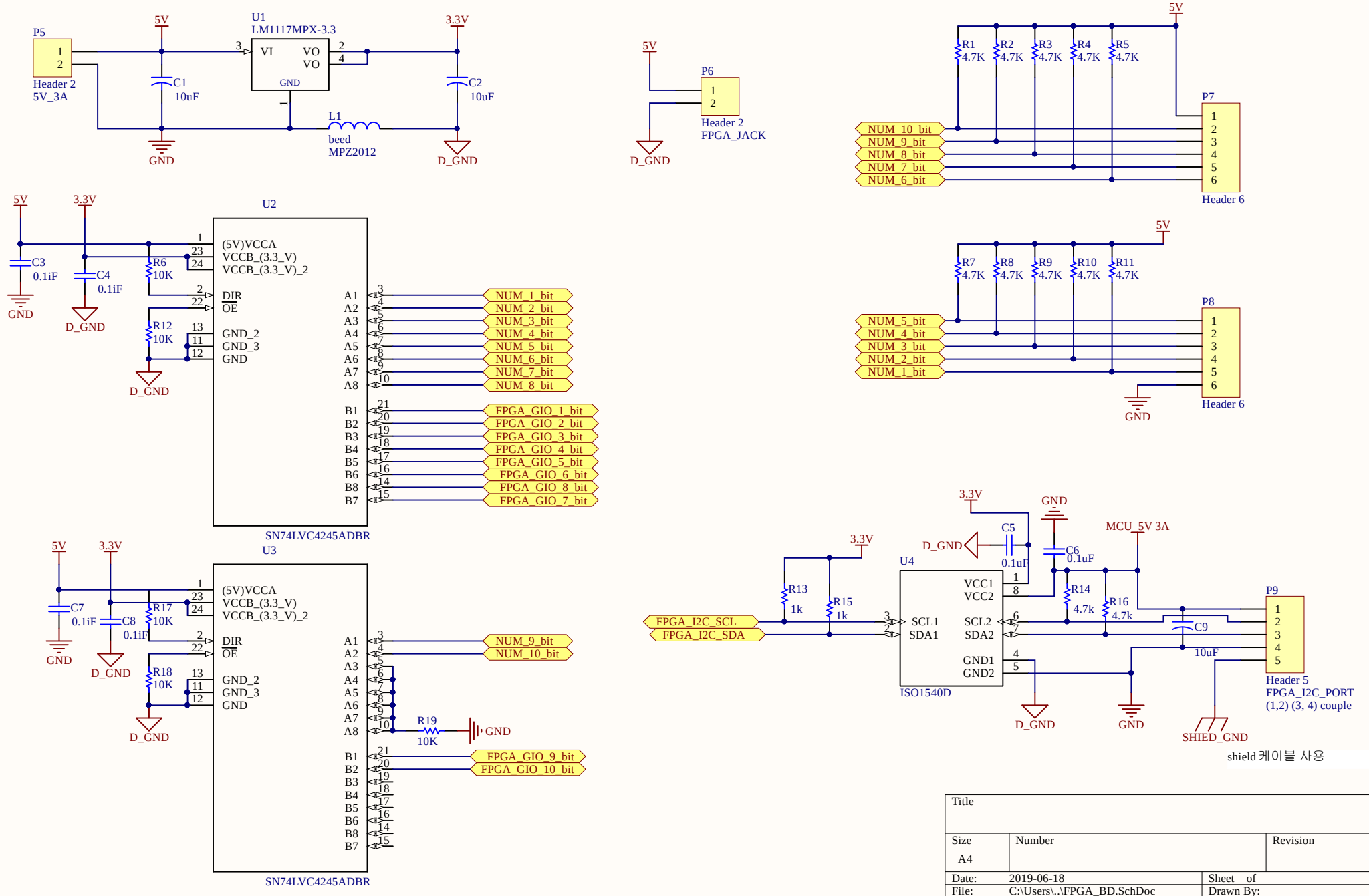
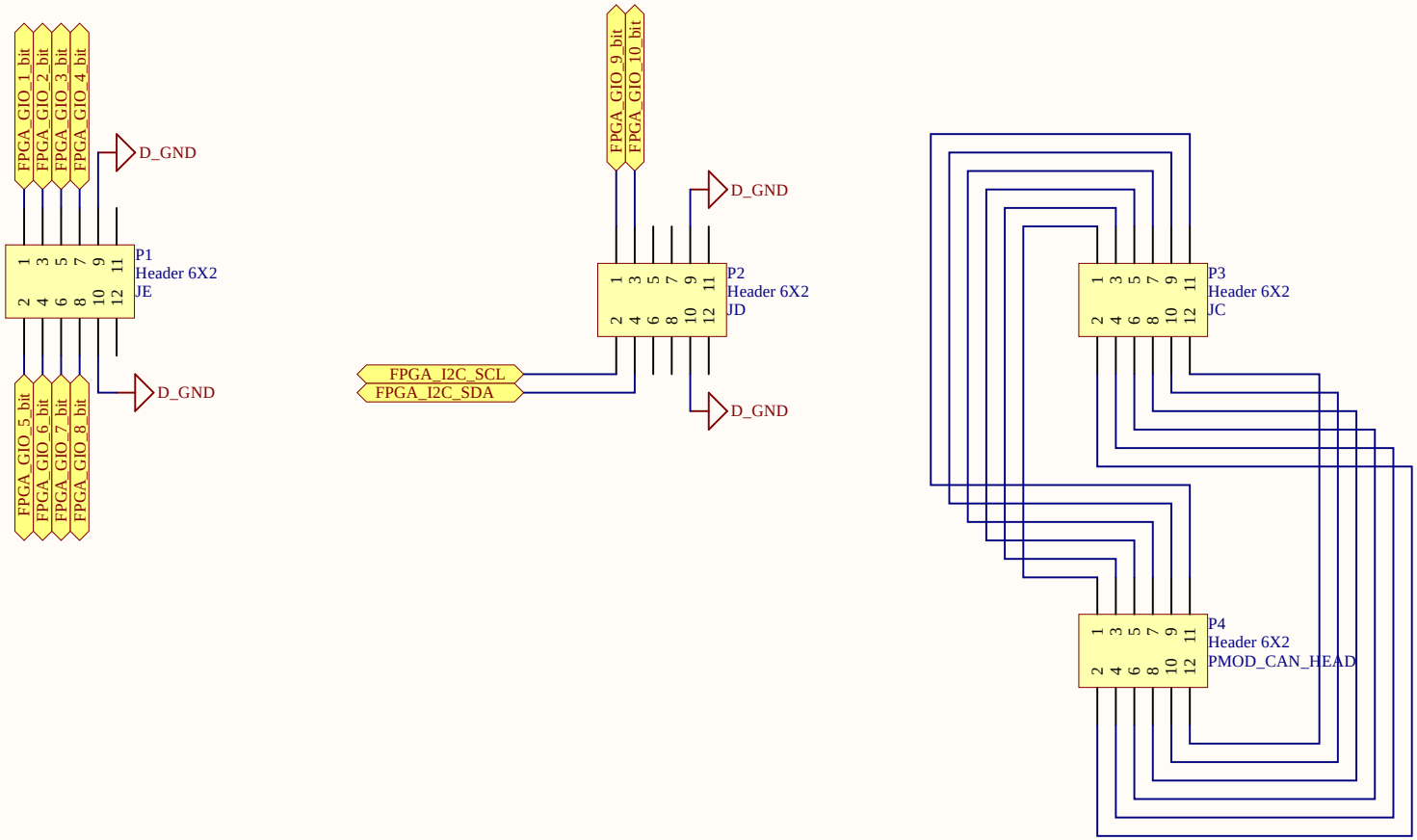

P5
Header 2
5V_3A
5V
C1
10uF
U1
LM1117MPX-3.3
VI
VO
VO
GND
3.3V
C2
10uF
L1
beed
MPZ2012
GND
D_GND
P6
Header 2
FPGA_JACK
R1 4.7K
R2 4.7K
R3 4.7K
R4 4.7K
R5 4.7K
P7
Header 6
NUM_10_bit
NUM_9_bit
NUM_8_bit
NUM_7_bit
NUM_6_bit
U2
(5V)VCCA
VCCB_(3.3_V)
VCCB_(3.3_V)_2
DIR
OE
GND_2
GND_3
GND
C3 0.1iF
C4 0.1iF
R6 10K
R12 10K
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B8 B7
NUM_1_bit
NUM_2_bit
NUM_3_bit
NUM_4_bit
NUM_5_bit
NUM_6_bit
NUM_7_bit
NUM_8_bit
FPGA_GIO_1_bit
FPGA_GIO_2_bit
FPGA_GIO_3_bit
FPGA_GIO_4_bit
FPGA_GIO_5_bit
FPGA_GIO_6_bit
FPGA_GIO_8_bit
FPGA_GIO_7_bit
SN74LVC4245ADBR
R7 4.7K
R8 4.7K
R9 4.7K
R10 4.7K
R11 4.7K
P8
Header 6
NUM_5_bit
NUM_4_bit
NUM_3_bit
NUM_2_bit
NUM_1_bit
U3
C7 0.1iF
C8 0.1iF
R17 10K
R18 10K
R19 10K
NUM_9_bit
NUM_10_bit
FPGA_GIO_9_bit
FPGA_GIO_10_bit
SN74LVC4245ADBR
U4
ISO1540D
VCC1
VCC2
SCL1
SDA1
SCL2
SDA2
GND1
GND2
C5 0.1uF
C6 0.1uF
C9 10uF
R13 1k
R15 1k
R14 4.7k
R16 4.7k
FPGA_I2C_SCL
FPGA_I2C_SDA
MCU_5V 3A
P9
Header 5
FPGA_I2C_PORT
(1,2) (3, 4) couple
SHIED_GND
shield 케이블 사용
Title
Size
A4
Number
Revision
Date: 2019-06-18
Sheet of
File: C:\Users\..\FPGA_BD.SchDoc
Drawn By:



Title		
Size: A4	Number	Revision
Date: 2019-06-18		Sheet of
File: C:\Users\..\FPGA_BD2.SchDoc		Drawn By:

Bill of Materials

<Parameter Title not found>

Source Data From: FPGA_BD.PrjPcb

Project: FPGA_BD.PrjPcb

Variant: None

Creation Date: 2019-06-18 오후 8:14:29

Print Date: 18-Jun-19 8:14:46 PM

Footprint	Comment	LibRef	Designator	Description	Quantity
CAPR5-4X5	Cap2	Cap2	C1, C2, C9	Capacitor	3
RAD-0.3	Cap	Cap	C3, C4, C5, C6, C7, C8	Capacitor	6
0402-A	beed	Inductor	L1	Inductor	1
HDR2X6	Header 6X2	Header 6X2	P1, P2, P3, P4	Header, 6-Pin, Dual row	4
HDR1X2	Header 2	Header 2	P5, P6	Header, 2-Pin	2
HDR1X6	Header 6	Header 6	P7, P8	Header, 6-Pin	2
HDR1X5	Header 5	Header 5	P9	Header, 5-Pin	1
AXIAL-0.3	Res1	Res1	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19	Resistor	19
*SOT230P700X180-4N	LM1117MPX-3.3	LM1117MPX-3.3	U1	4 pin 800mA Low-Dropout Linear Regulator 2000 per reel	1
*SOP65P780X200-24N	SN74LVC4245ADBR	SN74LVC4245ADBR	U2, U3	Octal Bus Transceiver And 3.3-V To 5-V Shifter With 3-State Outputs 24-SSOP -40 to 85	2
*SOIC127P600X175-8N	ISO1540D	ISO1540D	U4	2.5 kVrms Isolated Bidirectional Clock, Bidirectional I2C Isolators 8-SOIC -40 to 125	1
					42

Approved	Notes	