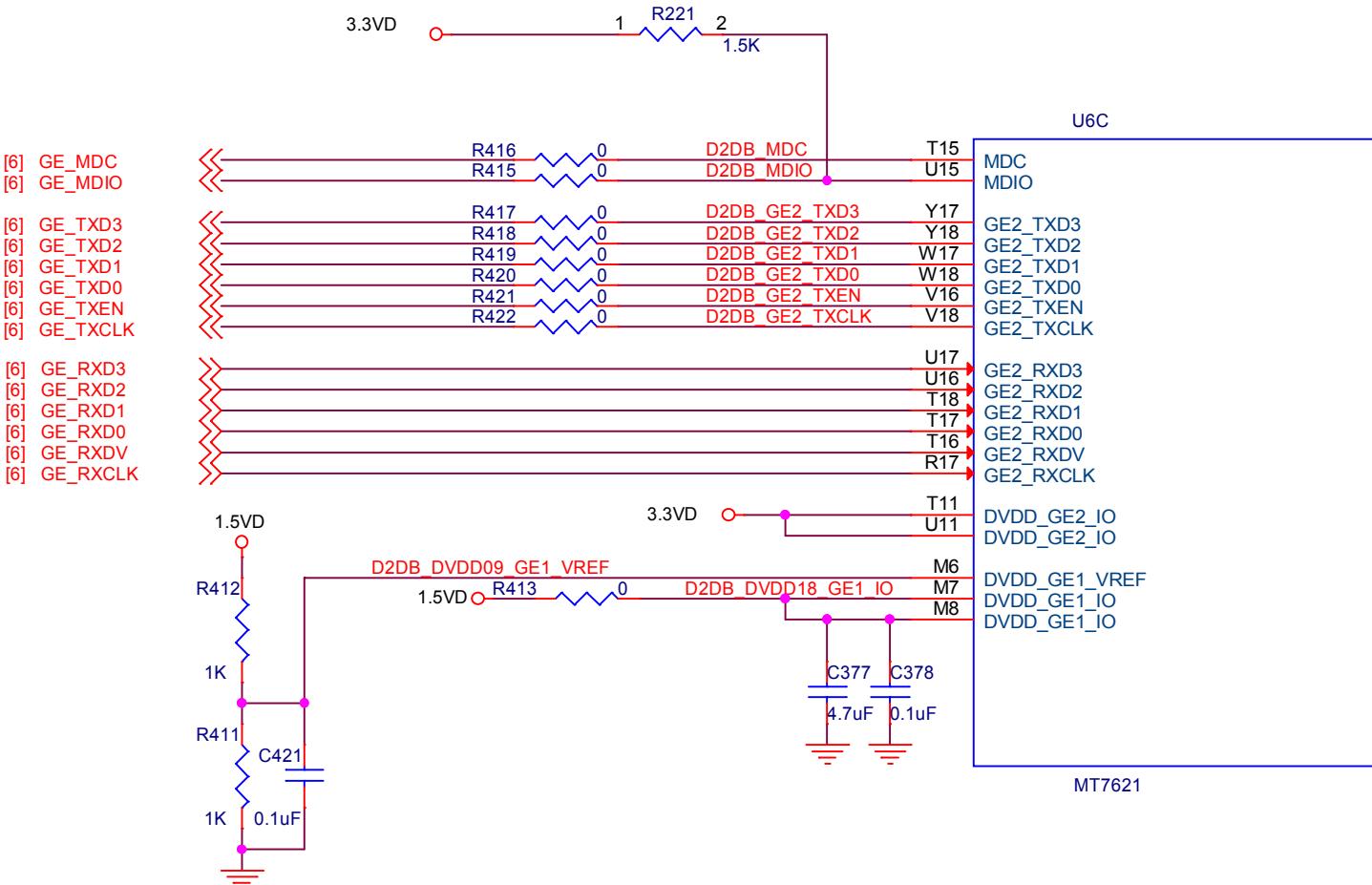


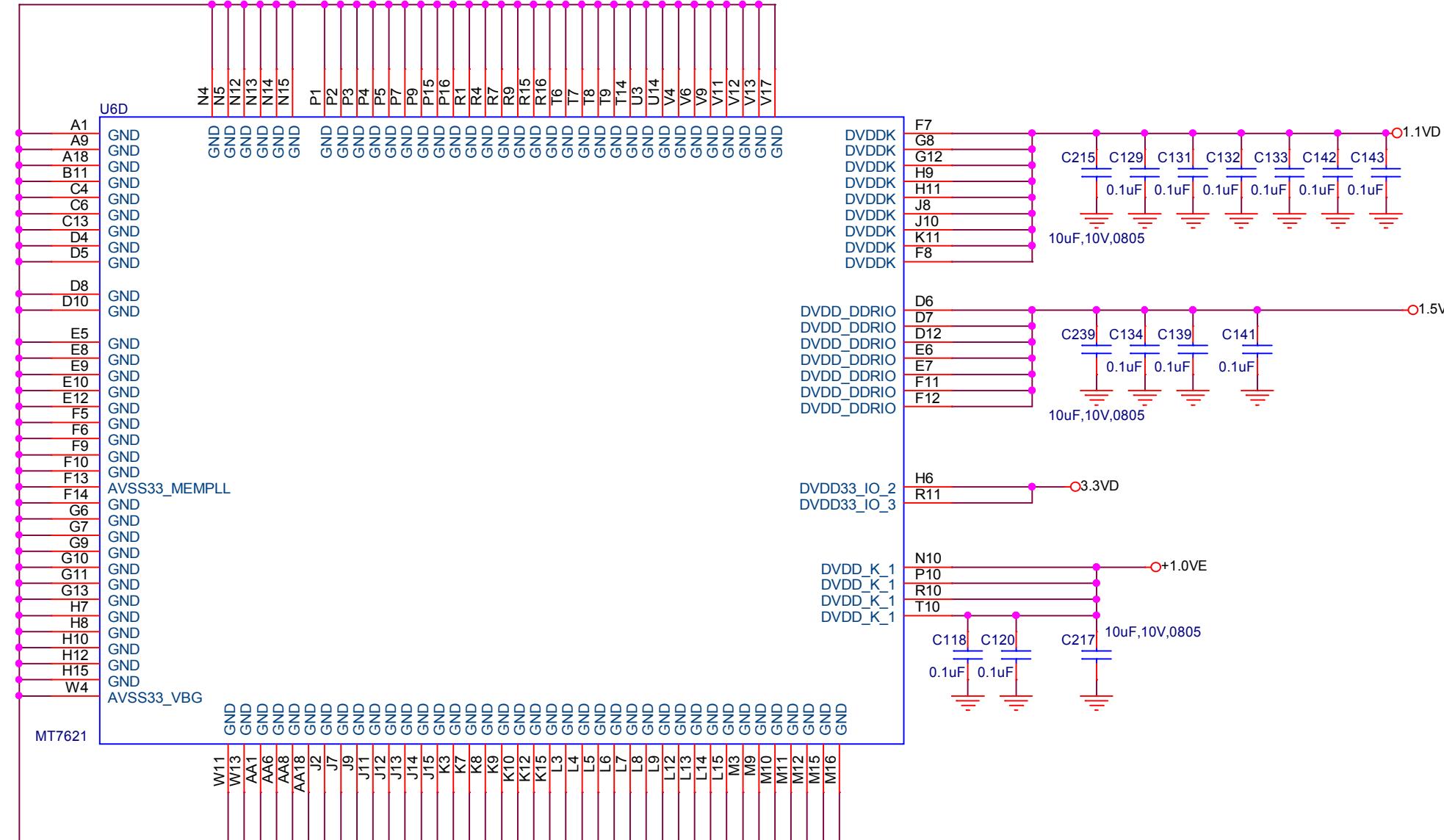
## RGMII Interface



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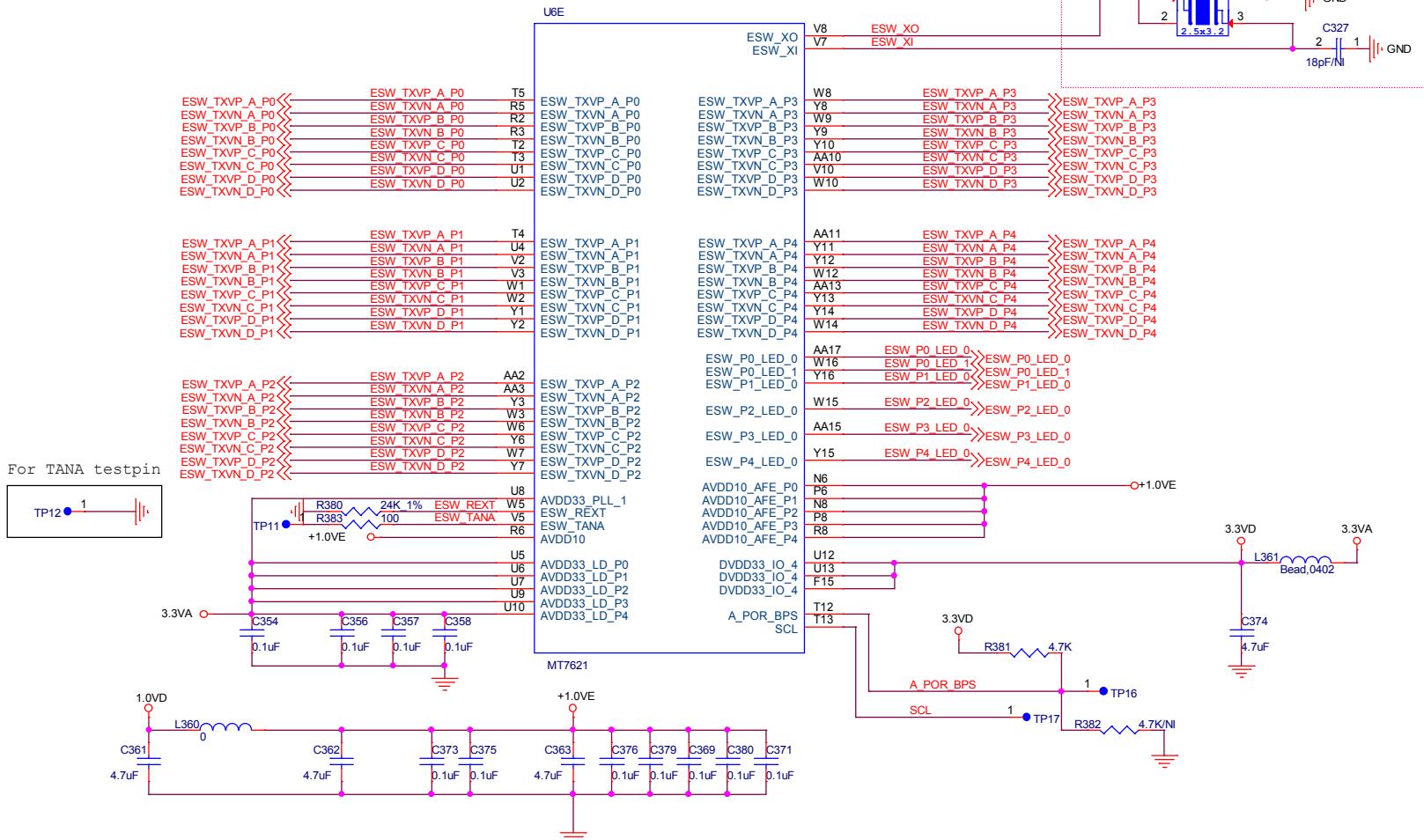
<b>MediaTek Inc.</b> <b>MEDIATEK</b>		No.1, Dusing Rd. 1, Hsinchu Science Park Hsinchu, Taiwan 300, R.O.C.		TEL:+886-3-567-0766
		Title	MT7621A	Fax:+886-3-578-7610
Size A	Document Number MT7621A	Drawn <i>Jimmy</i>	Rev V11	
Date: Tuesday, August 11, 2015	Sheet 3	of 16		

# MT7621 Power

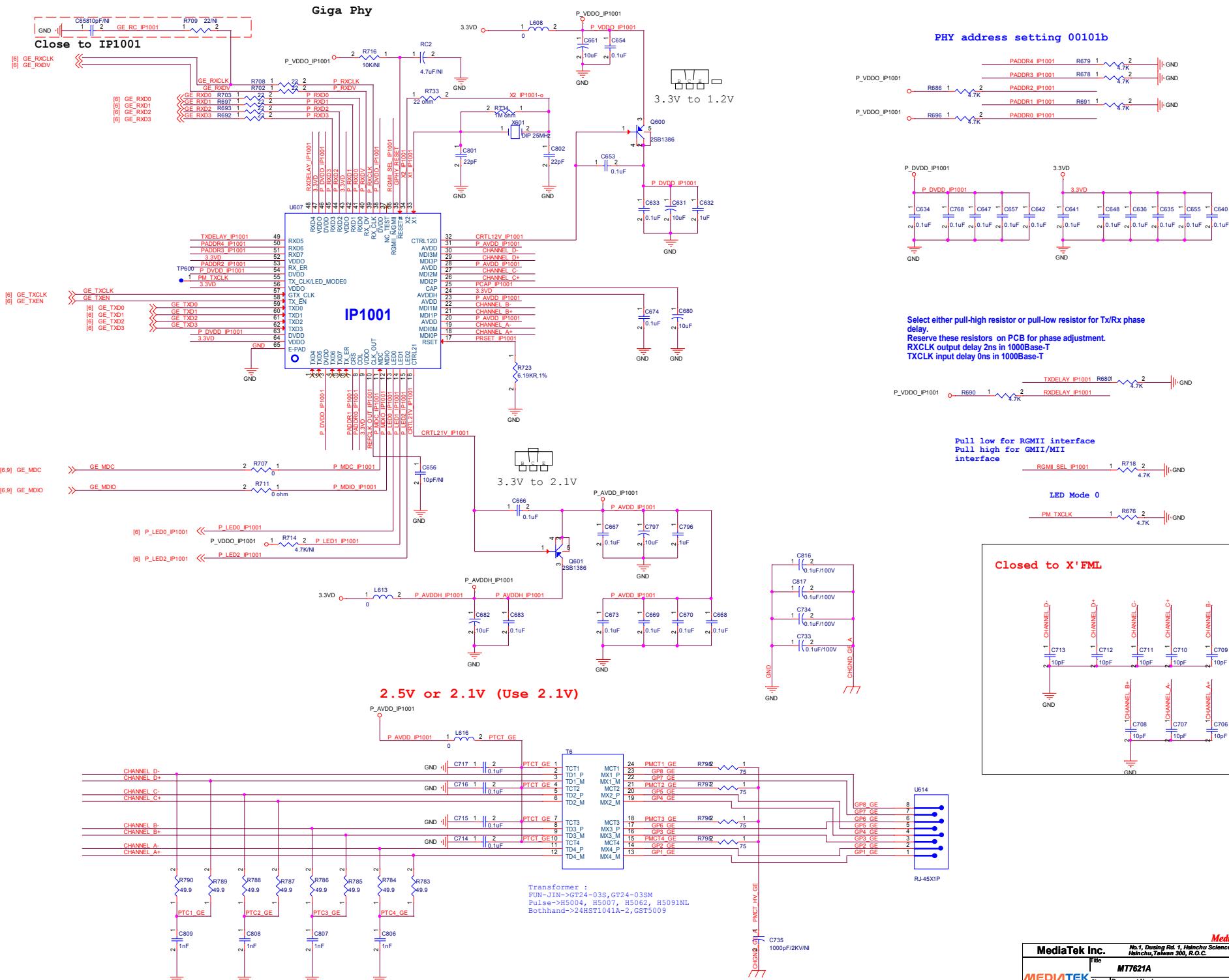


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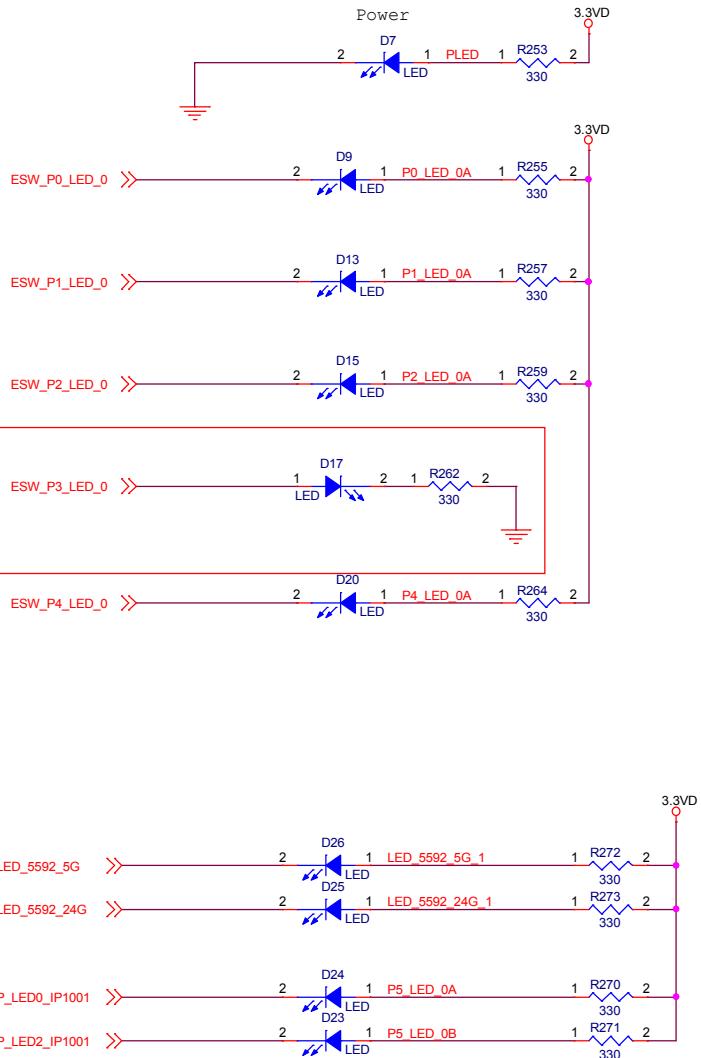
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		Hsinchu,Taiwan 300, R.O.C.		Fax:+886-3-578-7610
<b>MT7621A</b>		Title <b>MT7621A</b>		
Size A	Document Number MT7621A	Drawn <b>Jimmy</b>	Rev V11	
Date: Tuesday, August 11, 2015	Sheet 4	of 16		

**Giga SW****MediaTek Confidential****MediaTek Inc.**No.1, Dusing Rd. 1, Hsinchu Science Park  
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	Date: Tuesday, August 11, 2015	Sheet 5 of 16	1



# LED



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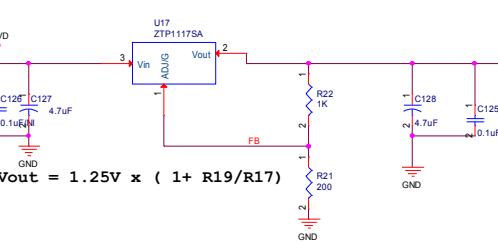
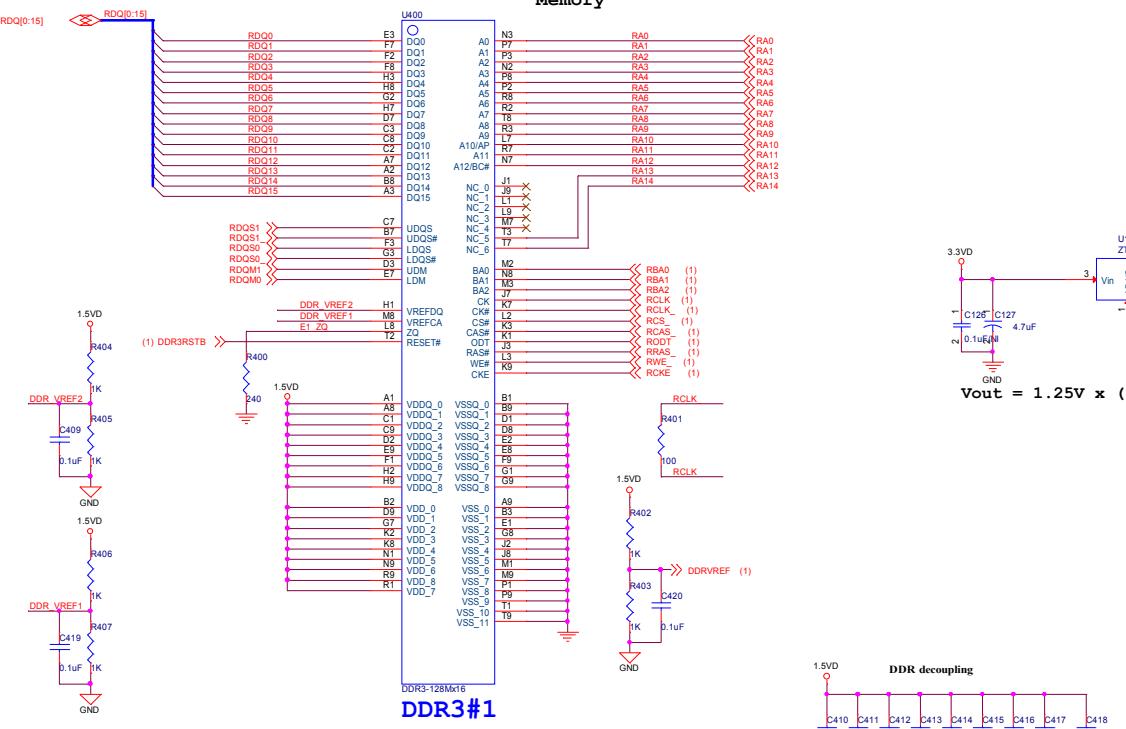
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Title MT7621A

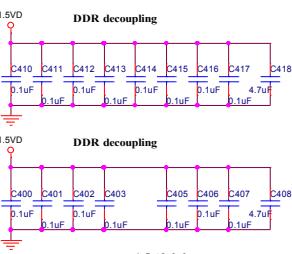
MEDIATEK

Size B Document Number MT7621A Drawn Jimmy Rev V11

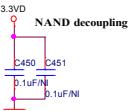
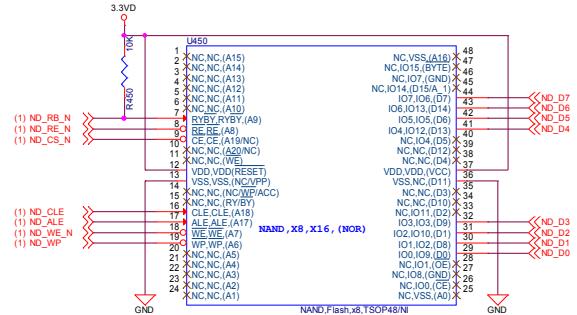
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$$V_{out} = 1.25V \times (1 + R_{19}/R_{17})$$



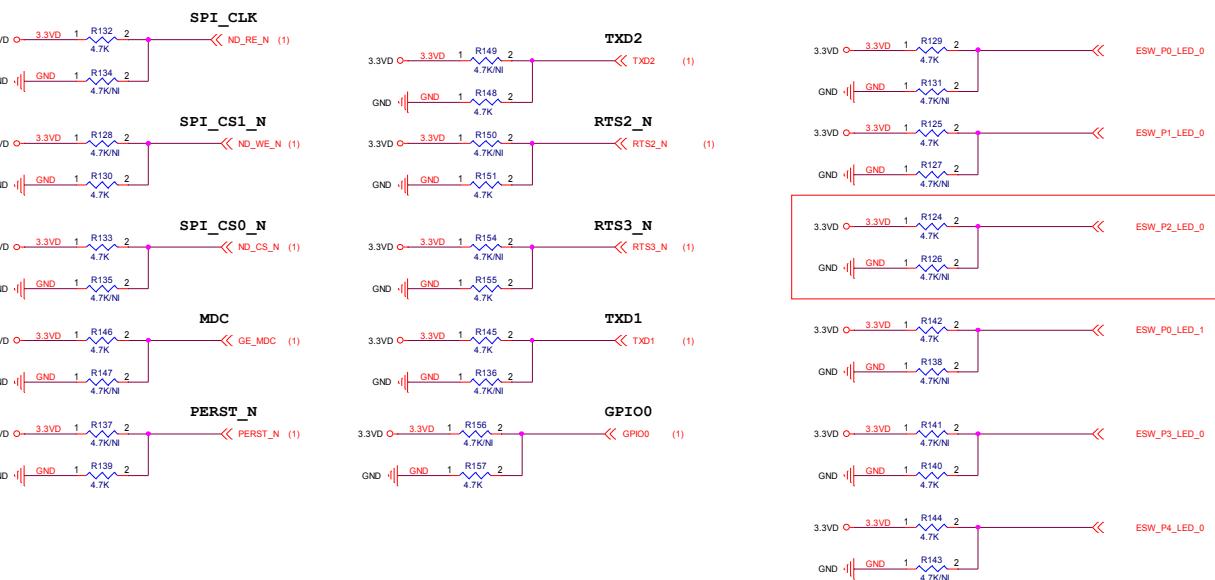
4.7uF+2+0.6u

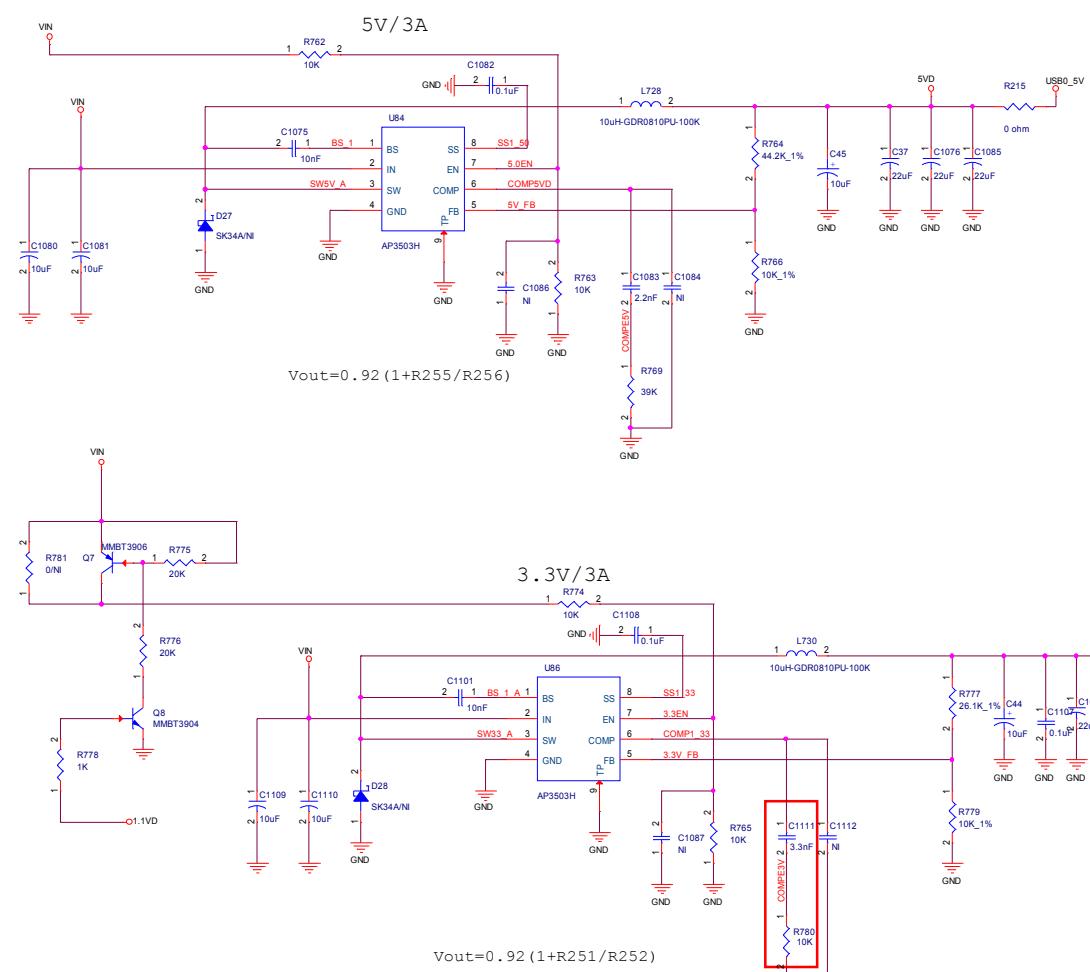


## Boot Strapping

Pin Name	Description	Value
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM <b>1: DRAM configuration from Auto Detect</b>
{SPI_CS1_N, SPI_CS0_N, MDC}	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input <b>011: 40 MHz, Self Oscillation mode</b>
PERST_N	OCP_RATIO	<b>0: 1:3</b> 1: 1:4
TXD2	DRAM_TYPE	<b>0: DDR3</b> 1: DDR2
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) <b>0010: Normal / Boot from SPI 3-byte address</b> 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMII / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test

Giga Switch Hardware Trap				
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1001: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b0: 20MHz 2'b1: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

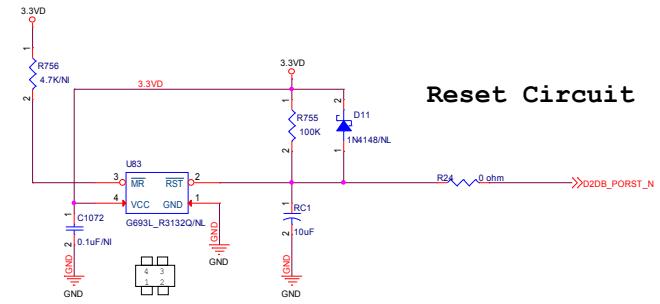




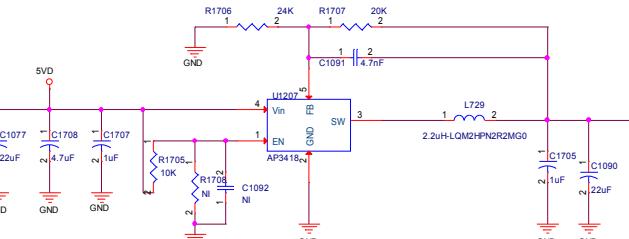
## For USB/PCIe PHY Power (1.2V)

Current = 300mA

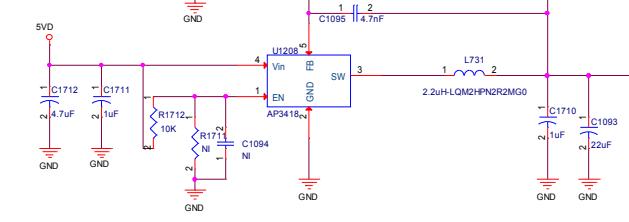
Vout = 0.8 (1 + R1/R2)



1.1V / 1.5A

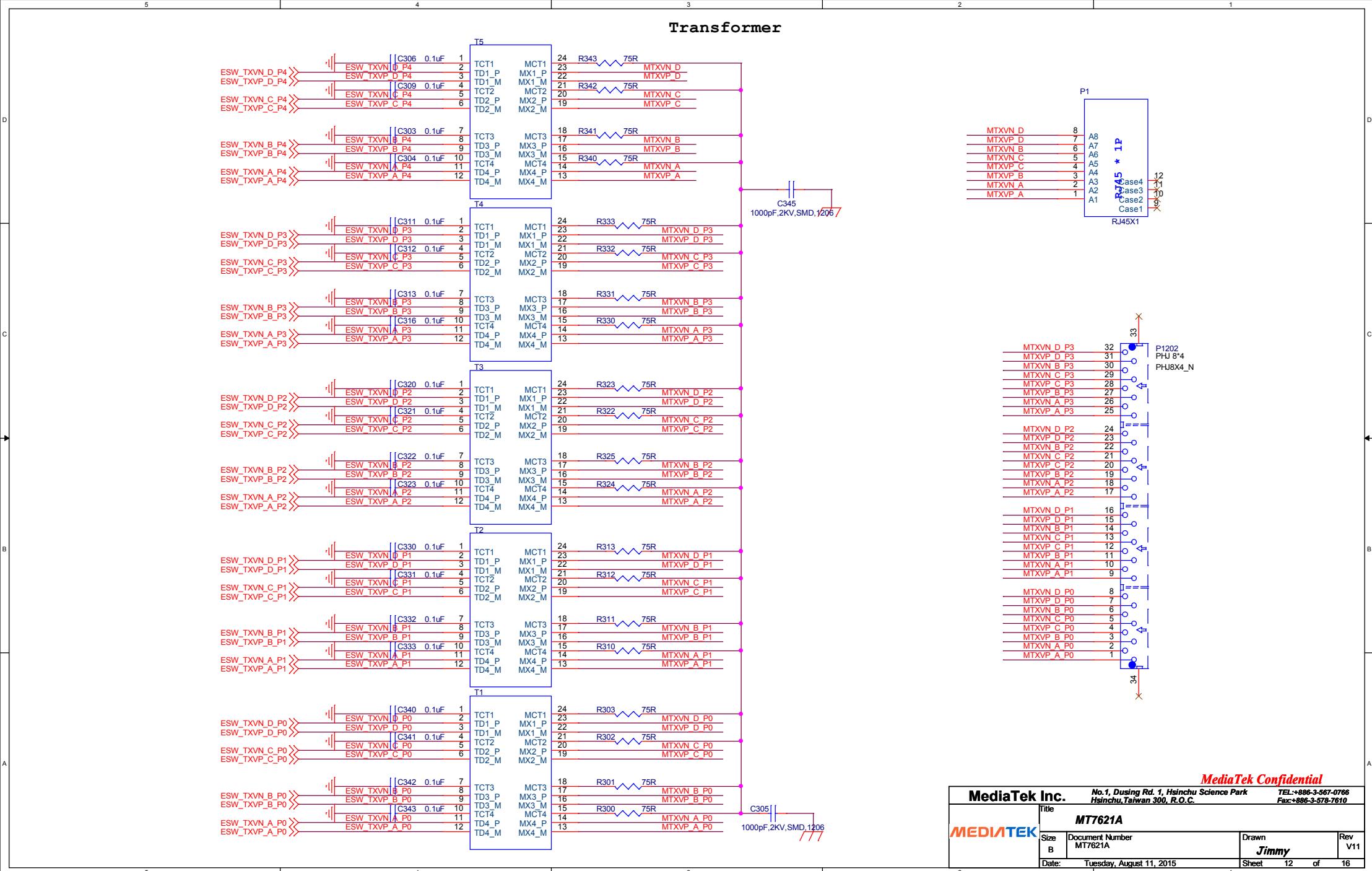


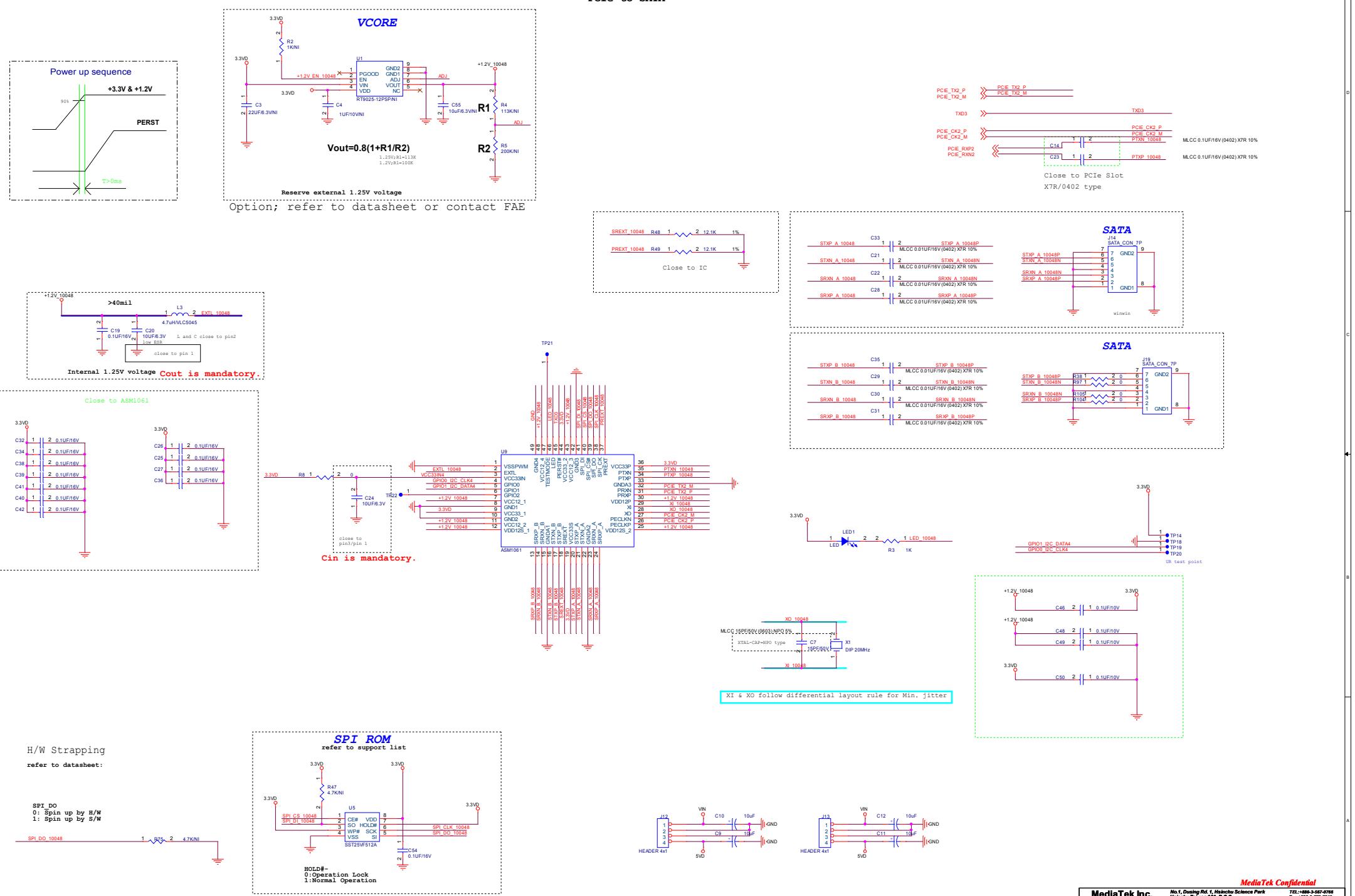
1.0V / 1.5A

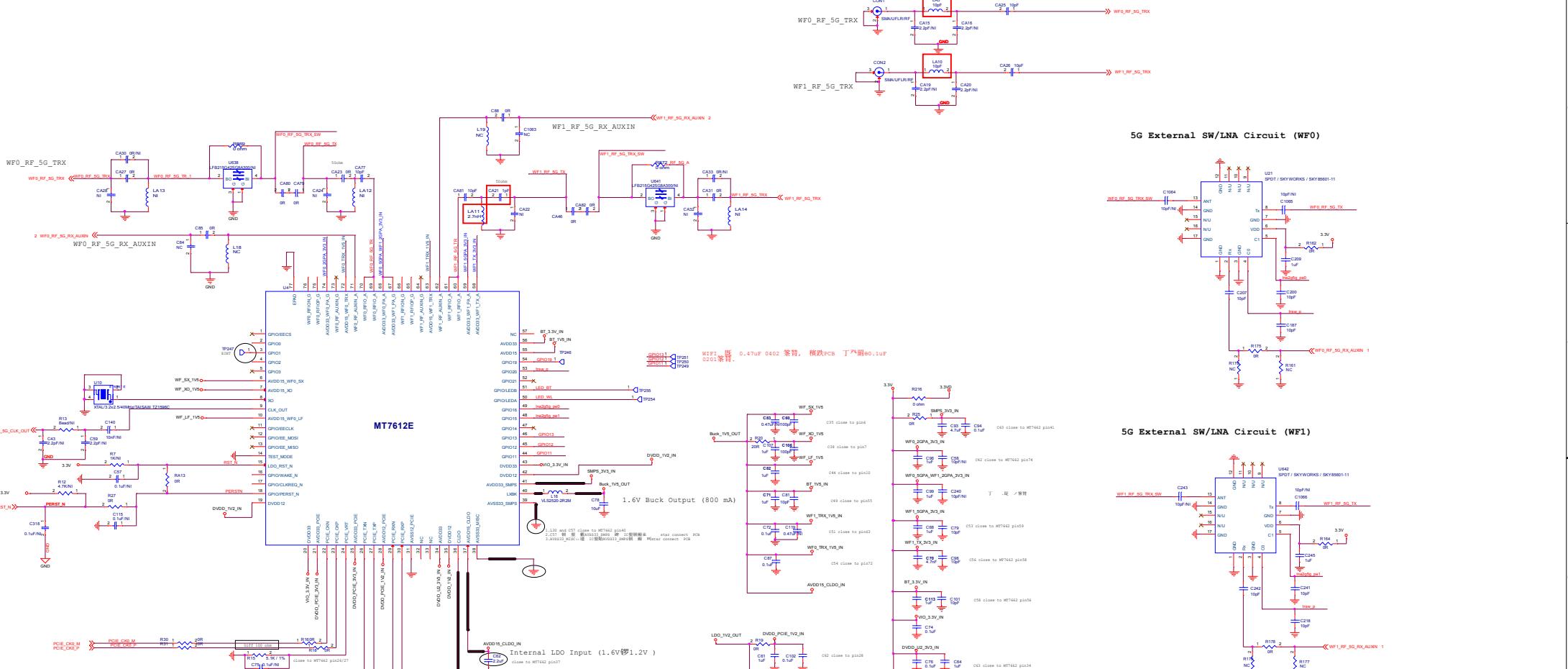


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	Document Number M7621A	Size C
	Date Tuesday, August 11, 2015	Drawn Jimmy Rev V11

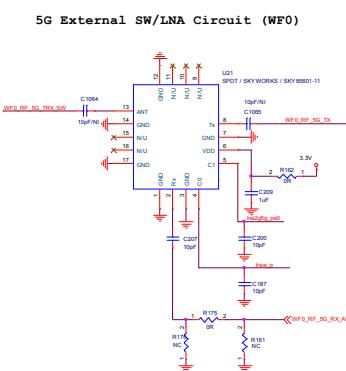
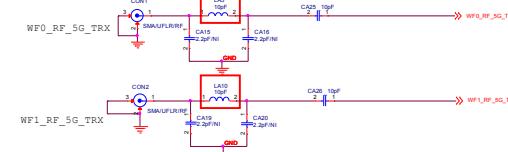




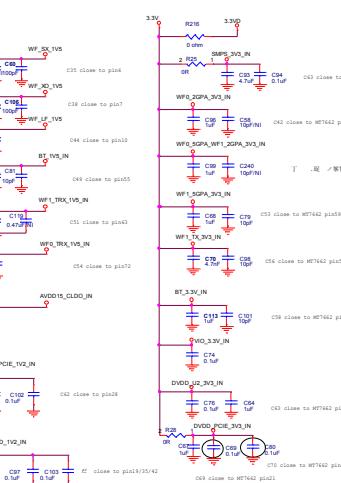


#### Boot Strapping (Internal Pull High/Low)

EE_CLK	0 : 40MHz Xtal (default) 1 : 20MHz Xtal
MOSI	0 : E-Pulse (default) 1 : EEPROM
GPIO [14:12]	Chip mode [2:0] => GPIO [14:12] 001: Boot from ROM (default)

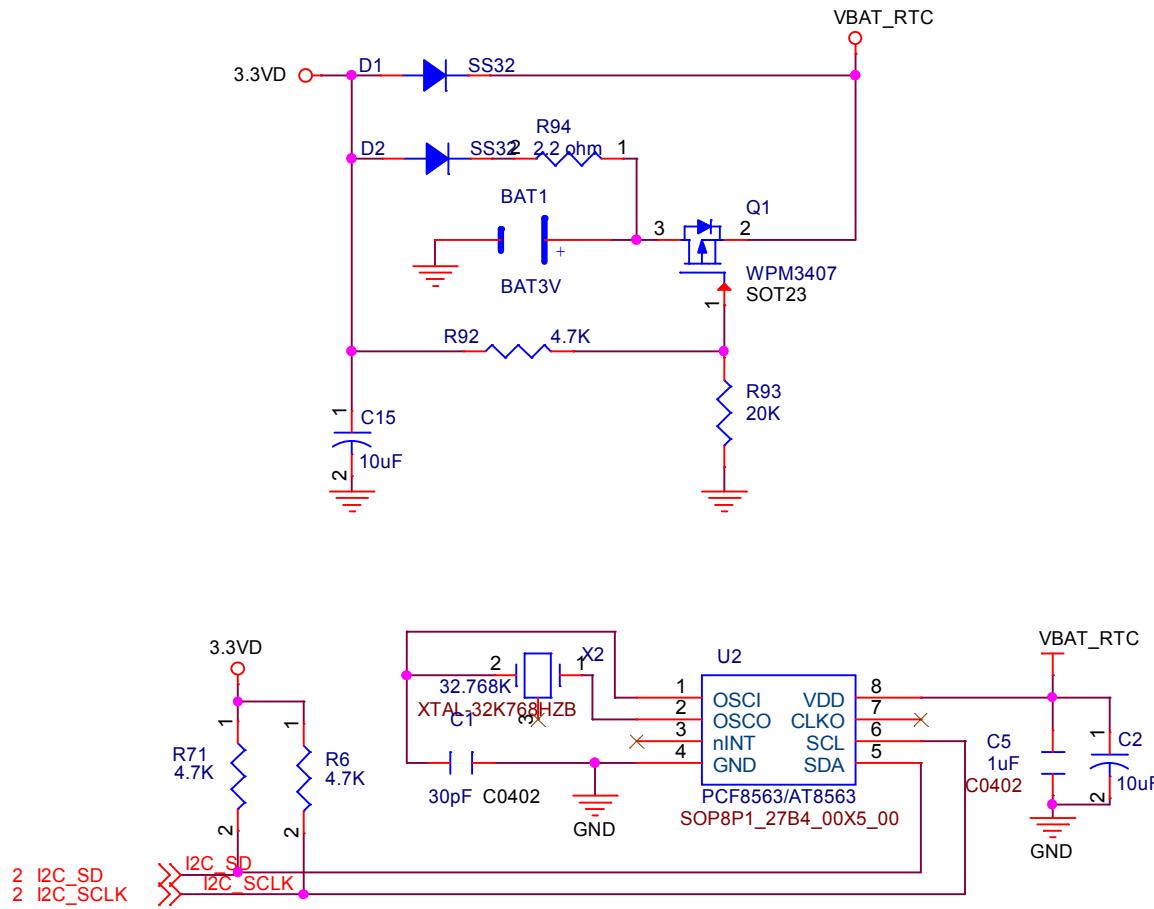


WIFI 0.47uF 0402 無極性 PCB 丁六腳 0.1uF



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Size	Document Number	Drawn	Rev
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