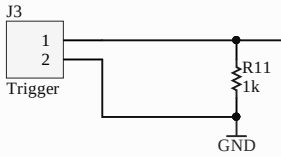
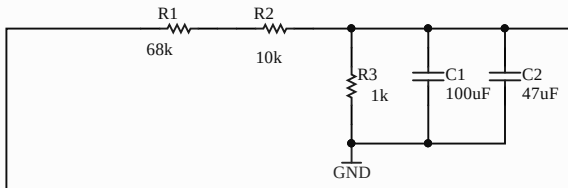
Signal enable Trigger input(TTL; high active; for pulsing up to 100kHz)

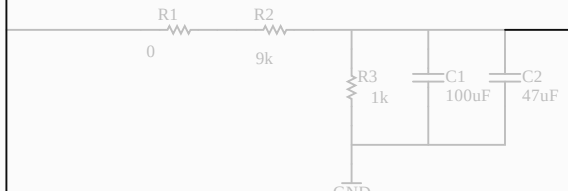


stage 2: voltage division and low passing

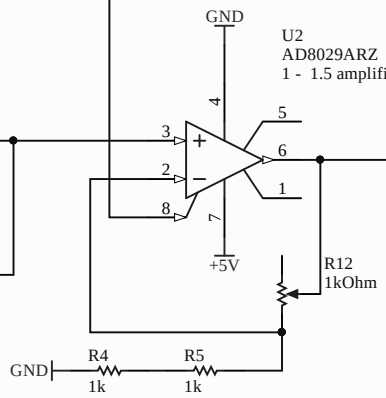
Version A (405/488nm LD): 0-3.3V PWM (>=1kHz) input; Division factor: 79 (0 - 0.042V)

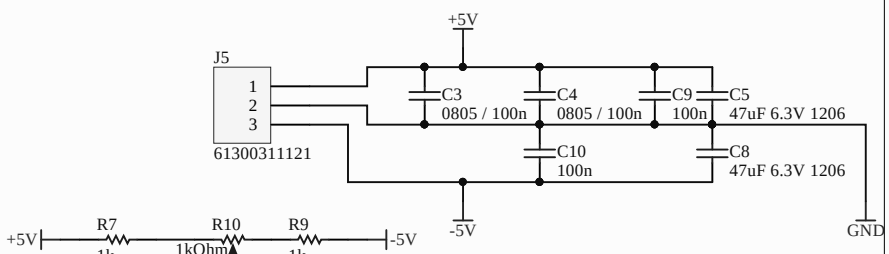


Version B (638nm LD): 0-3.3V PWM (>=1kHz) input; Division factor: 10 (0 - 0.33V)

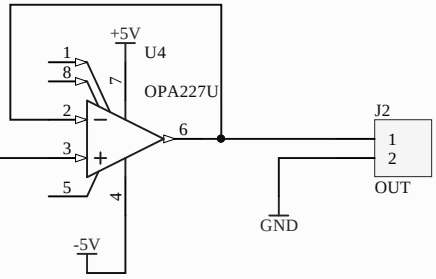


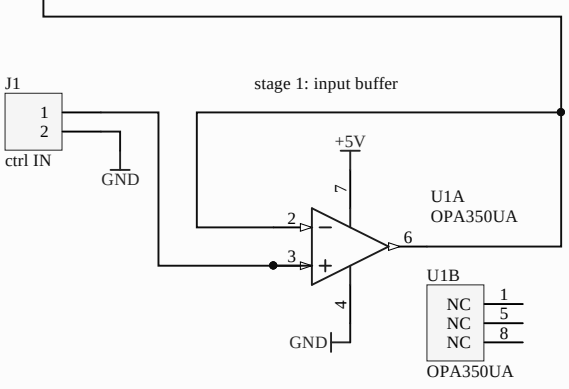
stage 3: amplification

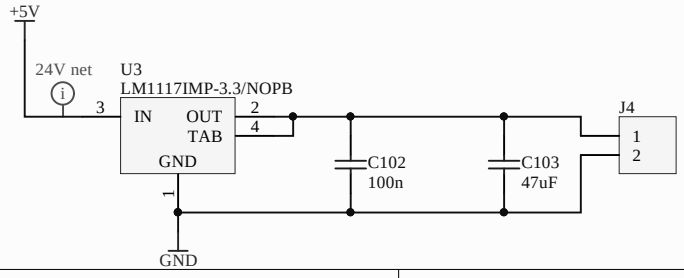




stage 4: offset correction







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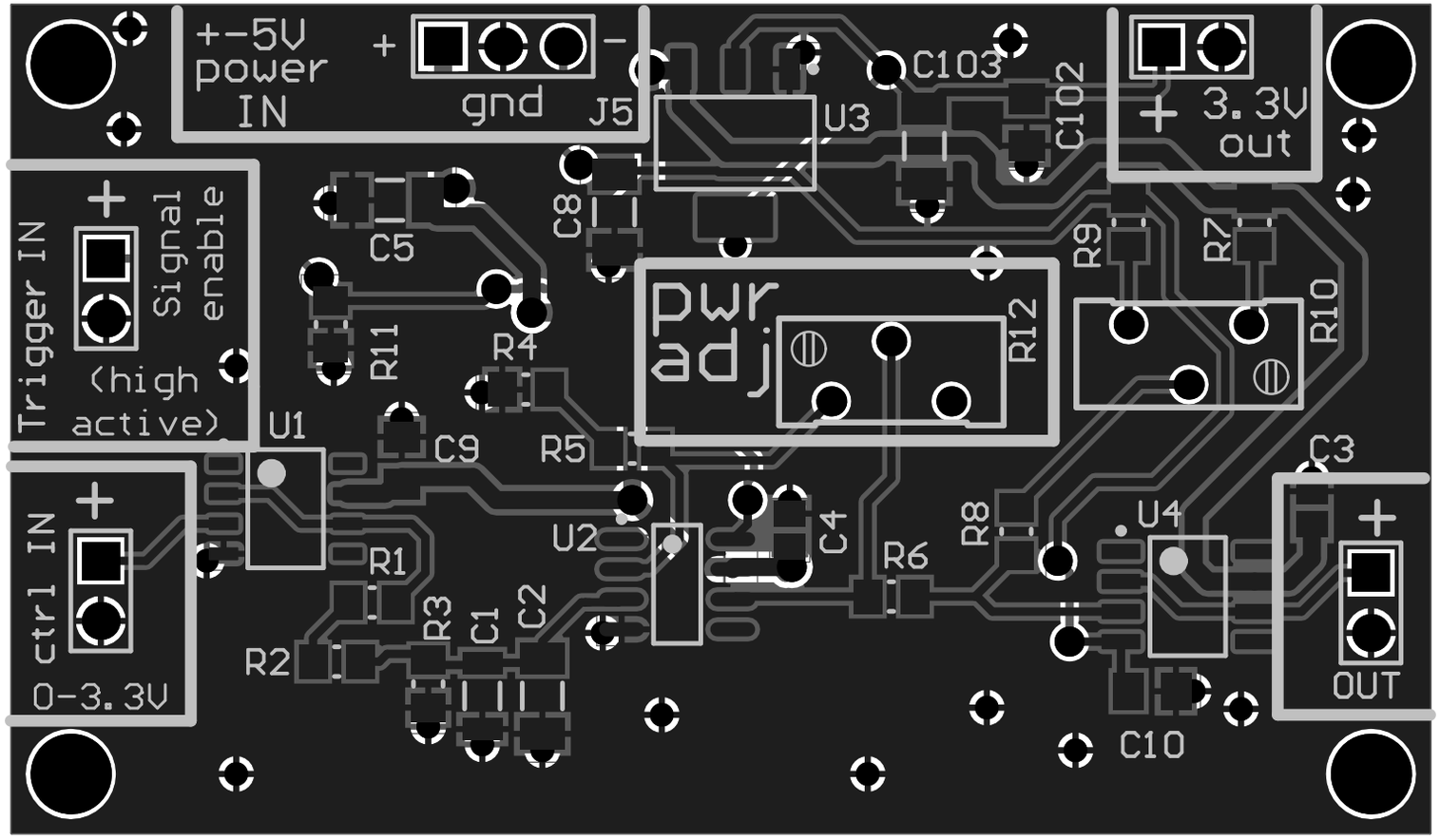
+-5V
power
IN
+
gnd
-
J5
U3
C103
C102
+
3.3V
out
Trigger IN
+
Signal
enable
(high
active)
C5
C8
R11
R4
pwr
adj
R12
R9
R7
R10
U1
C9
R5
C3
ctrl IN
+
U2
C4
R8
U4
R1
R6
R3
C1
C2
R2
OUT
C10
0-3.3V