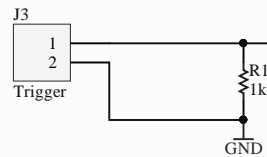
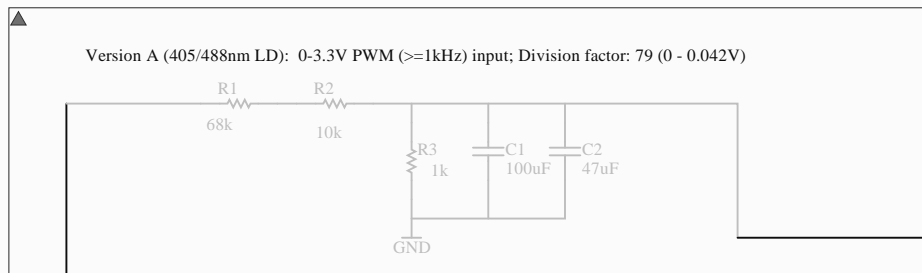


Signal enable Trigger input(TTL; high active; for pulsing up to 100kHz)

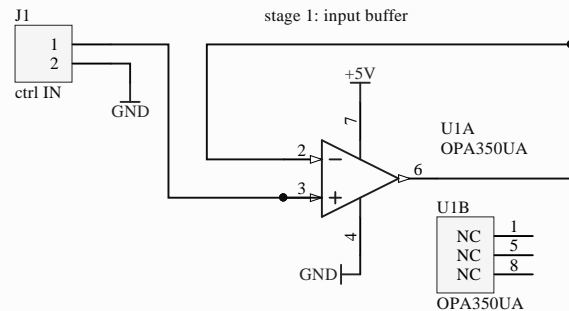
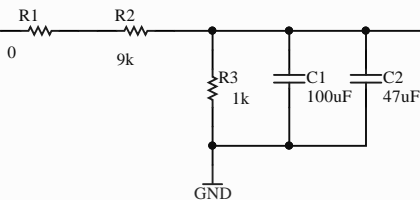


stage 2: voltage division and low passing

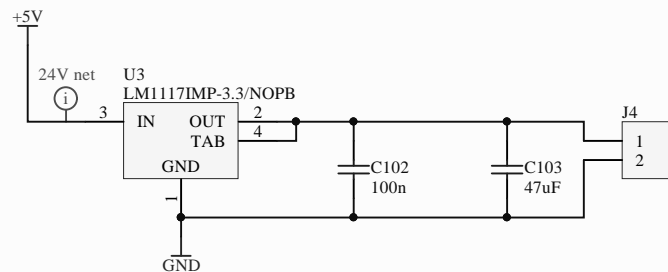


Version A (405/488nm LD): 0-3.3V PWM ( $\geq 1$ kHz) input; Division factor: 79 (0 - 0.042V)

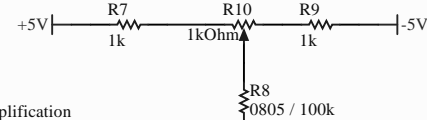
Version B (638nm LD): 0-3.3V PWM ( $\geq 1$ kHz) input; Division factor: 10 (0 - 0.33V)



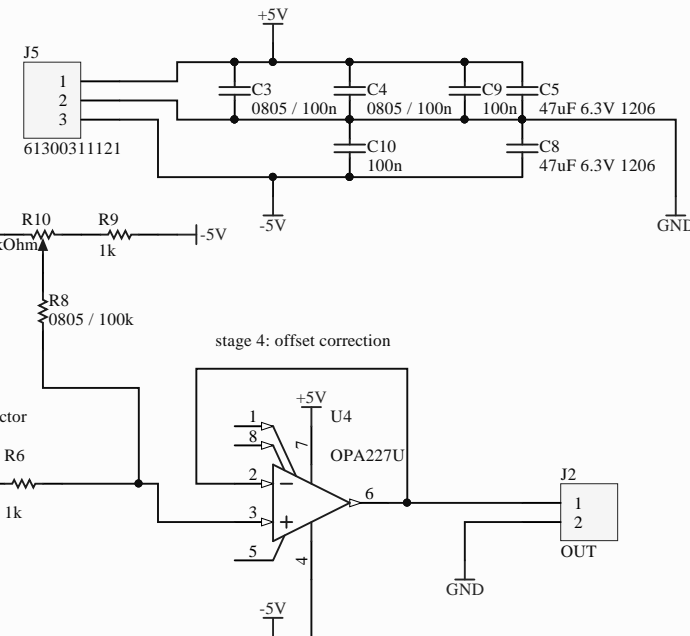
stage 1: input buffer



stage 3: amplification



stage 4: offset correction



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