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**Lime-GPSDO**

***- FPGA Gateware Description****-*

REVISION HISTORY

The following table shows the revision history of this document:

|  |  |  |
| --- | --- | --- |
| **Date** | **Version** | **Description of Revisions** |
| 03/05/2019 | 1.0 | Initial version |
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# Introduction

This document contains functional description of FPGA gateware project suited for Lime-GPSDO board.

**FPGA project** – Lime-GPSDO project can be downloaded from GitHub repository

<https://github.com/myriadrf/Lime-GPSDO_GW>.

**Required hardware** – LimeGSPDO v1.0 board.

**Development software** – project is created with Altera Quartus prime, Version 18.0.0 Build 614 04/24/2018 SJ Lite Edition with MAX 10 device support. Mentioned software edition is free and can be downloaded from [(https://www.altera.com)](https://www.altera.com). Although other Altera Quartus prime software versions supporting MAX10 family might work as well but it is recommended to use same version as project was created.

# FPGA gateware features

Gateware contains following features:

* UART-USB interface for transmitting data
* High accuracy 30.72MHz GNSS disciplined clock.
* External I2C, UART and GPIO for user defined applications.
* GNSS message parsing.

# Gateware description

This chapter describes main modules of Lime-GPSDO project.

## Main block diagram

Lime-GPSDO gateware features a NIOS II softcore processor (nios\_cpu in **Figure 1**) which provides various interfaces for communicating with on-board peripherals and other gateware modules, as well as external I2C and UART interfaces intended for user-defined use. The gateware also features a module for parsing GNSS data and performing parts of the clock tuning process (limegnss\_gpio\_top in **Figure 1).**

**Note:** EXT I2C and EXT UART logic, if required, is left to be implemented by the user.



Figure 1 Top block diagram

Table 1 Description of main instances

| **Instance** | **Description** |
| --- | --- |
| nios\_cpu | NIOS II softcore processor. Provides periphery control, tunes the VCTCXO clock based on data from limegnss\_gpio\_top. See **3.4 Softcore processor – nios\_cpu.** |
| limegnss\_gpio\_top | Parses GNSS messages, controls LEDs and provides data to the NIOS II softcore processor for VCTCXO tuning. See **3.3** **GNSS top module – limegnss\_gpio\_top** |

## Clock network

**Figure 2** shows dataflow between main modules and clocking scheme. More details can be found in **Table 2**.



Figure 2 Gateware clock network

Table 2 Clock network description

| **Clock name** | **Frequency, MHz** |  | **Description** |
| --- | --- | --- | --- |
| CLK50\_FPGA | 50 | | Clock for driving the NIOS II softcore processor |
| CLK0\_OUT | 30.72 | | VCTCXO clock, tuned by the gateware |

## GNSS top module – limegnss\_gpio\_top

Parses incoming messages from the onboard GNSS chip. Parsed data is stored in the gnsscfg submodule. Also evaluates the frequency offset of the 30.72MHz clock source and provides the data to the NIOS II softcore processor via an Avalon MM interface; controls onboard LEDs to indicate tuning status.

**Figure 3** is a block diagram for the limegnss\_gpio\_top module. Detailed descriptions of submodules can be found in **Table 3**.



Figure 3 limegnss\_gpio\_top block diagram

Table 3 Description of limegnss\_gpio\_top instances

| **Instance** | **Description** |
| --- | --- |
| UART | UART receiver and transmitter. Used to receive data from the GNSS chip. |
| gnss\_top | Parses GNSS messages. |
| vctcxo\_tamer\_top | Evaluates 30.72MHz clock’s frequency offset. |
| gnss\_led | Controls FPGA LEDs |

Table 4 limegnss\_gpio\_top module parameters

| **Parameter** | **Type** | **Default** | **Description** |
| --- | --- | --- | --- |
| UART\_BAUD\_RATE | positive | 9600 | Baud rate of UART interface. |
| VCTCXO\_CLOCK\_FREQUENCY | positive | 30720000 | VCTCXO clock frequency in Hz. |
| MM\_CLOCK\_FREQUENCY | positive | 100000000 | AvalonMM interface frequency in Hz. |

Table 5 limegnss\_gpio\_top module ports

| **Port** | **Type** | **Width** | **Description** |
| --- | --- | --- | --- |
| areset\_n | in | 1 | Active low reset. |
| tamercfg\_maddress | in | 10 | vctcxo\_tamercfg spi register start address. |
| gnsscfg\_maddress | in | 10 | gnsscfg spi register start address. |
| lreset | in | 1 | Logic reset signal. |
| mreset | in | 1 | Memory reset signal. |
| vctcxo\_clk | in | 1 | Clock from VCTCXO. |
| fpga\_led\_g | out | 1 | Green LED control signal (active high). |
| fpga\_leg\_r | out | 1 | Red LED control signal (active high). |
| en | out | 1 | VCTCXO tuning status signal. |
| fan\_ctrl\_in | in | 1 | Testing signal. |
| uart\_tx | out | 1 | Testing signal. |
| SPI | | | |
| sdin | in | 1 | SPI data in signal. |
| sclk | in | 1 | SPI clock signal. |
| sen | in | 1 | SPI enable signal (active low). |
| sdout | out | 1 | SPI data out signal. |
| GNSS | | | |
| gnss\_tx | out | 1 | GNSS chip <- FPGA UART signal (unused). |
| gnss\_rx | in | 1 | GNSS chip -> FPGA UART signal. |
| gnss\_tpulse | in | 1 | GNSS chip time pulse signal. |
| gnss\_fix | in | 1 | GNSS location fix status (unused). |
| AVALON MM | | | |
| mm\_clock | in | 1 | Avalon MM clock signal. |
| mm\_reset | in | 1 | Avalon MM reset signal. |
| mm\_rd\_req | in | 1 | Avalon MM read request. |
| mm\_wr\_req | in | 1 | Avalon MM write request. |
| mm\_addr | in | 8 | Avalon MM address bus. |
| mm\_wr\_data | in | 8 | Avalon MM write data bus. |
| mm\_rd\_data | out | 8 | Avalon MM read data bus. |
| mm\_rd\_datav | out | 1 | Avalon MM read data valid signal. |
| mm\_wait\_req | out | 1 | Avalon MM wait request signal. |
| mm\_irq | out | 1 | Avalon MM interrupt signal. |

### Registers of gnsscfg module

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Address** | **Def. value** | **Bits** | **Type** | **Name** | **Description** |
|  |  |  | **Control** | | |
| 0x0100 | 0000 | 15-1 |  | **Reserved** |  |
| 0 | R/W | **EN** | 1 - Enabled, 0 – Disabled |
|  |  |  | **Status** | | |
| 0x0101 | 0000 | 15-12 |  | **Reserved** | UTC of position fix (BCD format). HH-MM-SS1.SSS0 |
| 11-0 | R | **GPRMC\_UTC\_SSS0** |
| 0x0102 | 0000 | 15-8 | R | **GPRMC\_UTC\_MM** |
| 7-0 | R | **GPRMC\_UTC\_SS1** |
| 0x0103 | 0000 | 15-8 |  | **Reserved** |
| 7-0 | R | **GPRMC\_UTC\_HH** |
| 0x0104 | 0000 | 15-1 |  | **Reserved** |  |
| 0 | R | **GPRMC\_STATUS** | Status 1 = Data valid, 0 = Navigation receiver warning |
| 0x0105 | 0000 | 15-8 | R | **GPRMC\_LAT\_LL1** | Latitude,**LL3-LL2.LL1-LL0** |
| 7-0 | R | **GPRMC\_LAT\_LL0** |
| 0x0106 | 0000 | 15-8 | R | **GPRMC\_LAT\_LL3** |
| 7-0 | R | **GPRMC\_LAT\_LL2** |
| 0x0107 | 0000 | 15-1 |  | **Reserved** |  |
| 0 | R | **GPRMC\_LAT\_N\_S** | Latitude 0 – N, 1 – S |
| 0x0108 | 0000 | 15-8 | R | **GPRMC\_LONG\_YY1** | Longitude,**Y4-YY3-YY2.YY1-YY0** |
| 7-0 | R | **GPRMC\_LONG\_YY0** |
| 0x0109 | 0000 | 15-8 | R | **GPRMC\_LONG\_YY3** |
| 7-0 | R | **GPRMC\_LONG\_YY2** |
| 0x010A | 0000 | 15-4 |  | **Reserved** |
| 3-0 | R | **GPRMC\_LONG\_Y4** |
| 0x010B | 0000 | 15-1 |  | **Reserved** |  |
| 0 | R | **GPRMC\_LONG\_E\_W** | Longitude, 0 – E, 1 – W |
| 0x010C | 0000 | 15-8 | R | **GPRMC\_SPEED\_XX1** | Speed over ground, knots,**XX2-XX1.XX0** |
| 7-0 | R | **GPRMC\_SPEED\_XX0** |
| 0x010D | 0000 | 15-8 |  | **Reserved** |
| 7-0 | R | **GPRMC\_SPEED\_XX2** |
| 0x010E | 0000 | 15-8 | R | **GPRMC\_COURSE\_XX1** | Course Over Ground, degrees True,**X2-XX1.XX0** |
| 7-0 | R | **GPRMC\_COURSE\_XX0** |
| 0x010F | 0000 | 15-4 |  | **Reserved** |
| 3-0 | R | **GPRMC\_COURSE\_X2** |
| 0x0110 | 0000 | 15-8 | R | **GPRMC\_DATE\_MM** | Date:**DD-MM-YY** |
| 7-0 | R | **GPRMC\_DATE\_YY** |
| 0x0111 | 0000 | 15-8 |  | **Reserved** |
| 7-0 | R | **GPRMC\_DATE\_DD** |
| 0x0112 | 0000 | 15-0 |  | **Reserved** |  |
| 0x0113 | 0000 | 15-0 |  | **Reserved** |  |
| 0x0114 | 0000 | 15-12 | R | **GAGSA\_FIX** | 1 = Fix not available, 2 = 2D, 3 = 3D ; Galileo |
| 11-8 | R | **GBGSA\_FIX** | 1 = Fix not available, 2 = 2D, 3 = 3D ; BeiDu |
| 7-4 | R | **GPGSA\_FIX** | 1 = Fix not available, 2 = 2D, 3 = 3D ; GPS |
| 3-0 | R | **GLGSA\_FIX** | 1 = Fix not available, 2 = 2D, 3 = 3D ; GLONASS |

### Registers of vctcxo\_tamercfg module

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Address** | **Def. value** | **Bits** | **Type** | **Name** | **Description** |
| 0x00E0 | 0000 |  | **Control** | | |
| 15-1 |  | **Reserved** |  |
| 0 | R/W | **EN** | 1 - Enabled, 0 – Disabled |
|  |  |  | **Status** | | |
| 0x00E1 | 0000 | 15-8 |  | **Reserved** |  |
| 7-4 | R | **ACCURACY** | “0000” - tune disabled or lowest accuracy, 0001 – 1s tune , 0010 – 2s tune , 0011 – 3s tune (highest accuracy). |
| 3-0 | R | **STATE** | “0000” - Coarse Tune, “0001” - Fine tune |
| 0x00E2 | 0000 | 15-0 | R | **DAC\_TUNED\_VAL** | DAC tuned value to get frequency with best accuracy |
|  |  |  | **Tune settings** | | |
| 0x00E3 | - | 15-0 | R/W | **PPS\_1S\_ERR\_TOL\_L** | Error tolerance value in 1s period (32 bit value, L – lower 16 b, H – upper 16b). Default values are board dependant. |
| 0x00E4 | - | 15-0 | R/W | **PPS\_1S\_ERR\_TOL\_H** |
| 0x00E5 | - | 15-0 | R/W | **PPS\_10S\_ERR\_TOL\_L** | Error tolerance value in 10s period (32 bit value, L – lower 16 b, H – upper 16b). Default values are board dependant. |
| 0x00E6 | - | 15-0 | R/W | **PPS\_10S\_ERR\_TOL\_H** |
| 0x00E7 | - | 15-0 | R/W | **PPS\_100S\_ERR\_TOL\_L** | Error tolerance value in 100s period (32 bit value, L – lower 16 b, H – upper 16b). Default values are board dependant. |
| 0x00E8 | - | 15-0 | R/W | **PPS\_100S\_ERR\_TOL\_H** |
|  |  |  | **Error values** | | |
| 0x00E9 | 0000 | 15-0 | R | **PPS\_1S\_ERR\_L** | Error count in 1s period (32 bit signed value, L – lower 16 b, H – upper 16b) |
| 0x00EA | 0000 | 15-0 | R | **PPS\_1S\_ERR\_H** |
| 0x00EB | 0000 | 15-0 | R | **PPS\_10S\_ERR\_L** | Error count in 10s period (32 bit signed value, L – lower 16 b, H – upper 16b) |
| 0x00EC | 0000 | 15-0 | R | **PPS\_10S\_ERR\_H** |
| 0x00ED | 0000 | 15-0 | R | **PPS\_100S\_ERR\_L** | Error count in 100s period (32 bit signed value, L – lower 16 b, H – upper 16b) |
| 0x00EE | 0000 | 15-0 | R | **PPS\_100S\_ERR\_H** |

## Softcore processor – nios\_cpu

**Figure 4** shows the block diagram of nios\_cpu module. This module contains softcore ALTERA NIOS II CPU. The processor is programmed to read data from limegnss\_gpio\_top via an Avalon MM interface and tune the VCTCXO via the dac\_spi interface. Ports are described in Table 6.

**Note:** EXT I2C and EXT UART logic, if required, is left to be implemented by the user.



Figure 4 nios\_cpu block diagram

Table 6 nios\_cpu module ports

| **Port** | **Type** | **Width** | **Description** |
| --- | --- | --- | --- |
| clk100 | in | 1 | Free running clock. |
| reset\_n | in | 1 | Asynchronous, active low reset |
| Control data FIFO (unused) | | | |
| exfifo\_if\_d | in | 32 | External control input FIFO data |
| exfifo\_if\_rd | out | 1 | External control input FIFO read request |
| exfifo\_if\_rdempty | in | 1 | External control input FIFO read empty |
| exfifo\_of\_d | out | 32 | External control output FIFO data |
| exfifo\_of\_wr | out | 1 | External control output FIFO write request |
| exfifo\_of\_wrfull | in | 1 | External control output FIFO write full |
| exfifo\_of\_rst | out | 1 | External control output FIFO reset request, active high |
| SPI1 (dac\_spi and fpga\_spi) | | | |
| dac\_spi\_ext\_SS\_n | out | 1 | dac spi slave select, active low. Also acts as a control signal for SPI1 mux (refer to **Figure 4** nios\_cpu block diagram. |
| fpga\_spi\_ext\_SCLK | out | 1 | fpga spi clock. |
| fpga\_spi\_ext\_MOSI | out | 1 | fpga spi master output. |
| fpga\_spi\_ext\_MISO | in | 1 | fpga spi master input. |
| fpga\_spi\_ext\_SS\_n | out | 2 | fpga spi slave select, active low. |
| SPI 2 (flash\_SPI) | | | |
| flash\_spi\_MISO | In | 1 | SPI2 master input. |
| flash\_spi\_MOSI | out | 1 | SPI2 master output. |
| flash\_spi\_SCLK | out | 1 | SPI2 clock. |
| flash\_spi\_SS\_n | out | 1 | SPI2 slave select, active low. |
| I2C | | | |
| i2c\_scl | inout | 1 | I2C bus clock, connected to temperature sensor and EEPROM memory. |
| i2c\_sda | inout | 1 | I2C bus data, connected to temperature sensor and EEPROM memory. |
| UART | | | |
| uart\_rxd | in | 1 | UART RX signal, not used. |
| uart\_txd | out | 1 | Uart TX signal, connected to UART to USB interface. |
| AVALON MM | | | |
| avm\_m0\_address | out | 8 | Avalon MM address bus |
| avm\_m0\_read | out | 1 | Avalon MM read signal |
| avm\_m0\_waitrequest | in | 1 | Avalon MM waitrequest signal |
| avm\_m0\_readdata | in | 8 | Avalon MM read data bus |
| avm\_m0\_readdatavalid | in | 1 | Avalon MM read data valid bus |
| avm\_m0\_write | out | 1 | Avalon MM write signal |
| avm\_m0\_writedata | out | 8 | Avalon MM write data bus |
| avm\_m0\_clk\_clk | out | 1 | Avalon MM clock |
| avm\_m0\_reset\_reset | out | 1 | Avalon MM reset signal |
| vctcxo\_tune\_en | in | 1 | vctcxo tamer status |
| vctcxo\_irq | in | 1 | vctcxo tamer interrupt signal |
| MISC | | | |
| switch | in | 8 | Not used. |
| leds | out | 8 | Not used. |
| lms\_ctr\_gpio | out | 4 | Not used. |