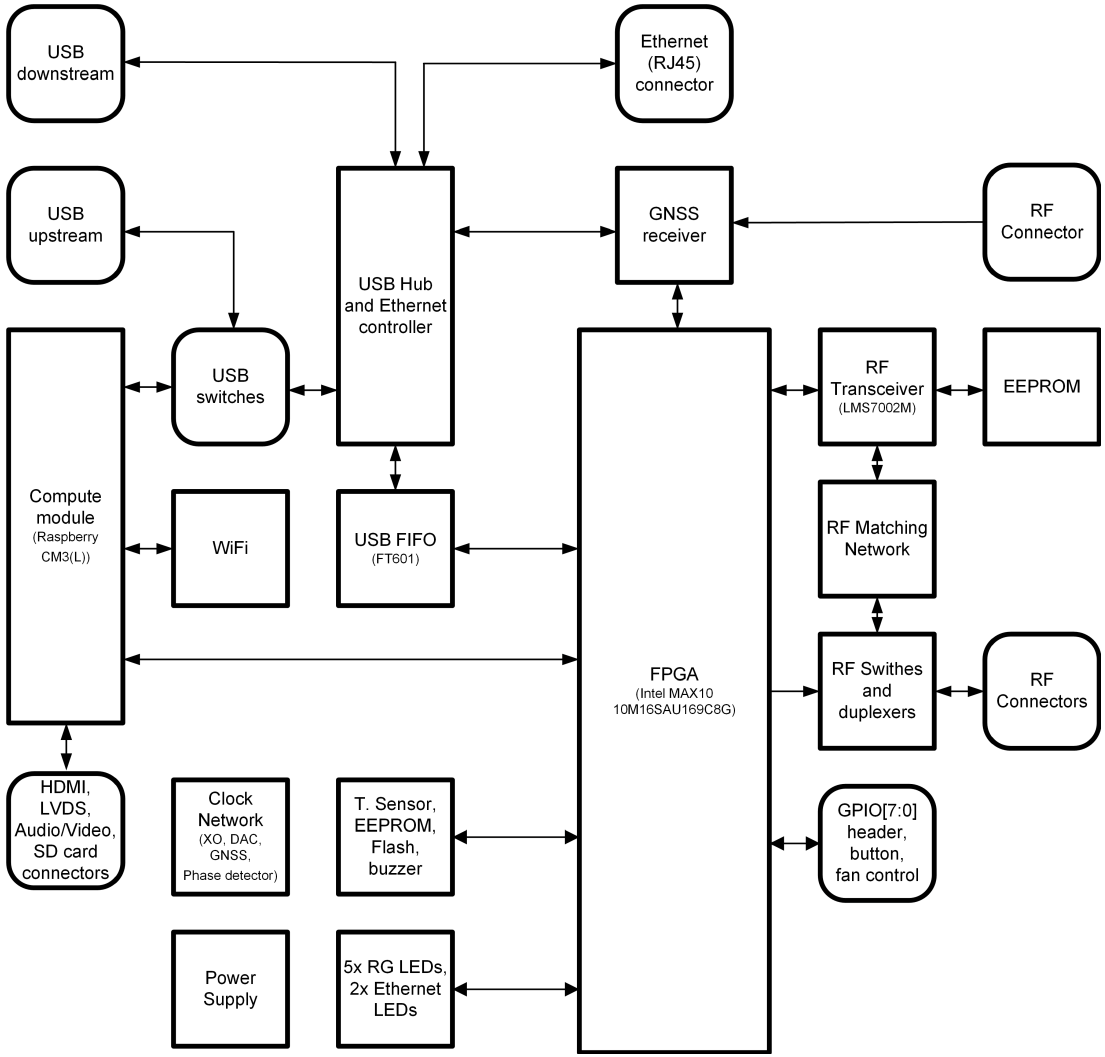
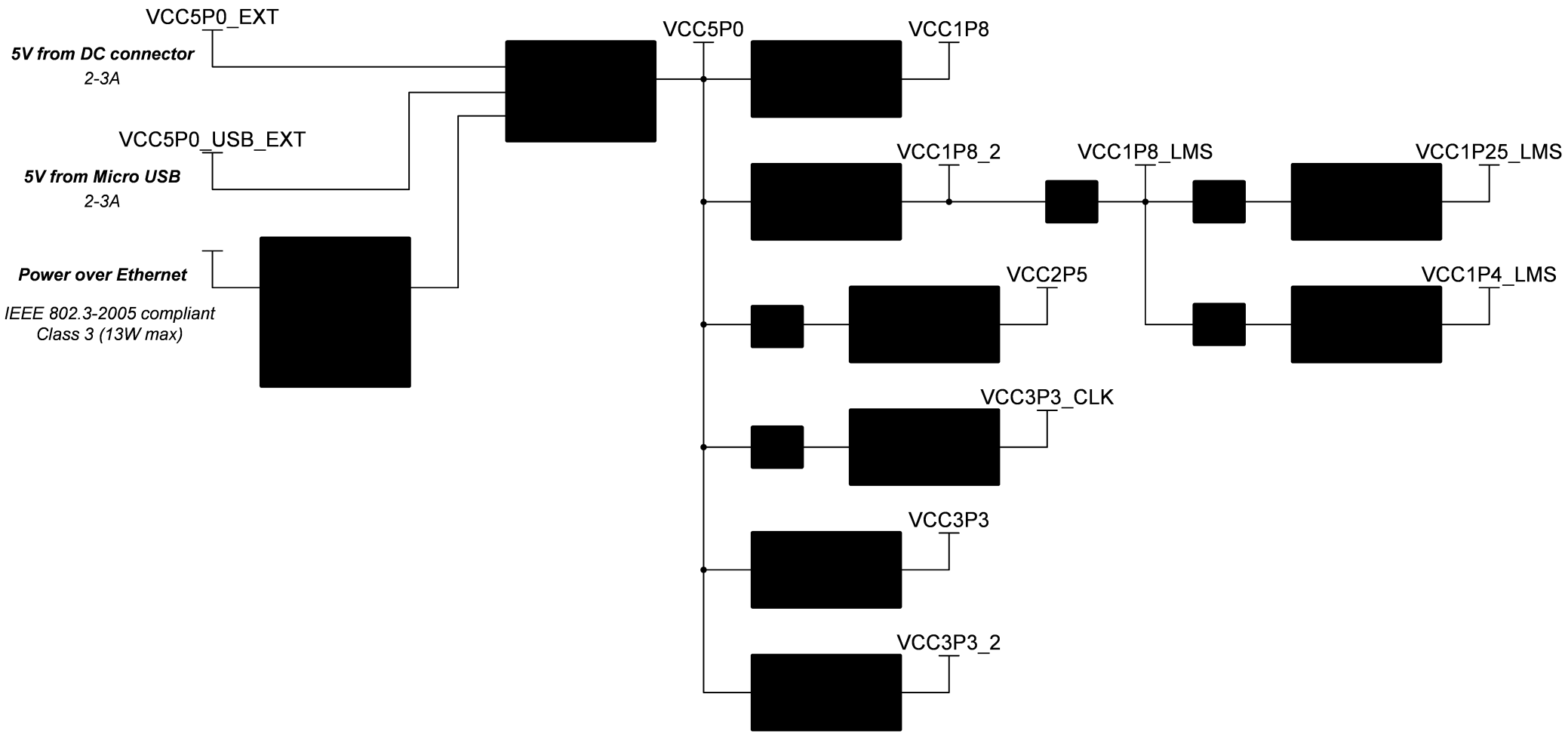
Block diagram



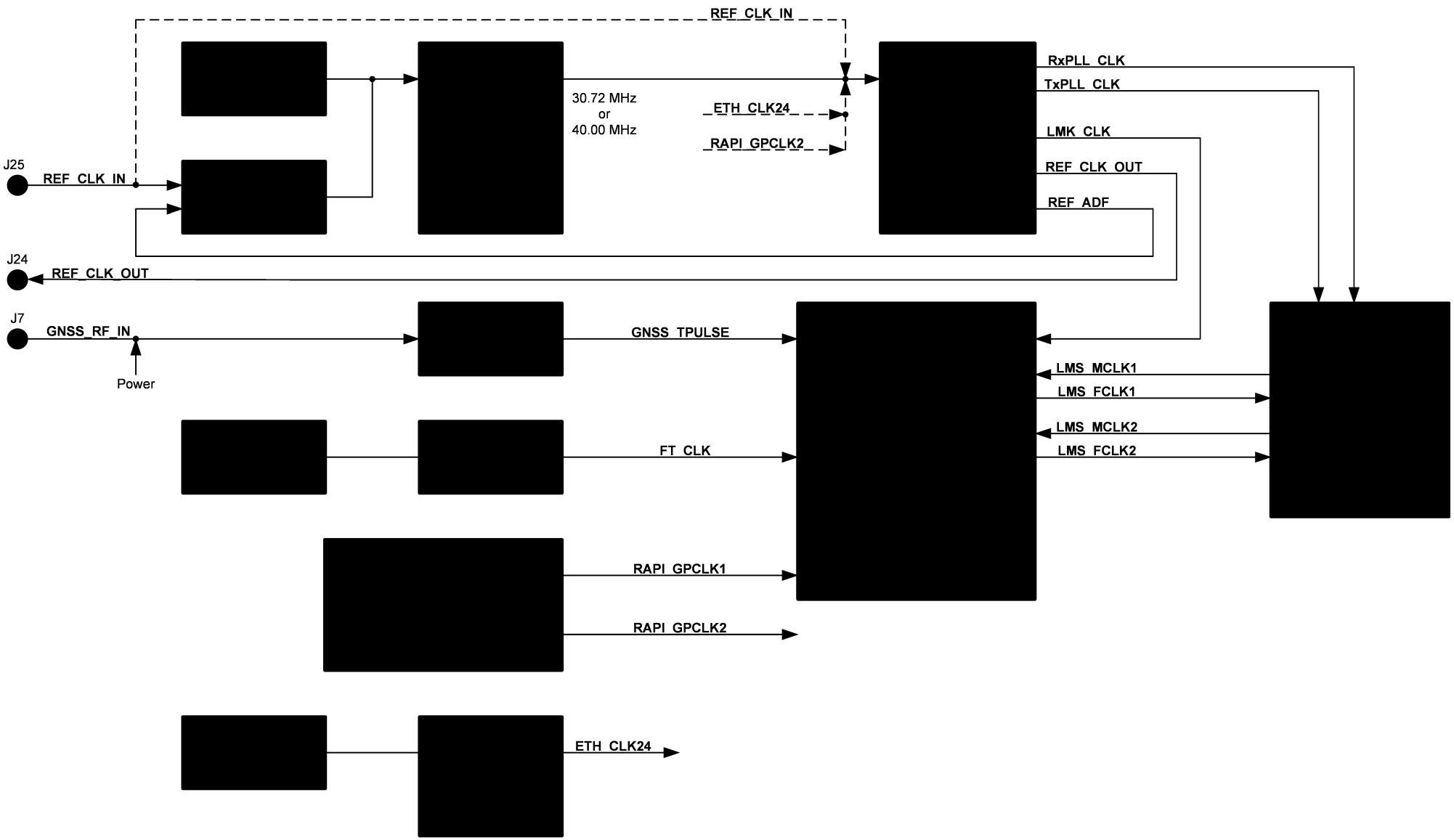
Title	Block diagram		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A4	Number: 1	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:34	Sheet1 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\01_BlockDiagram.SchDoc			

Power diagram



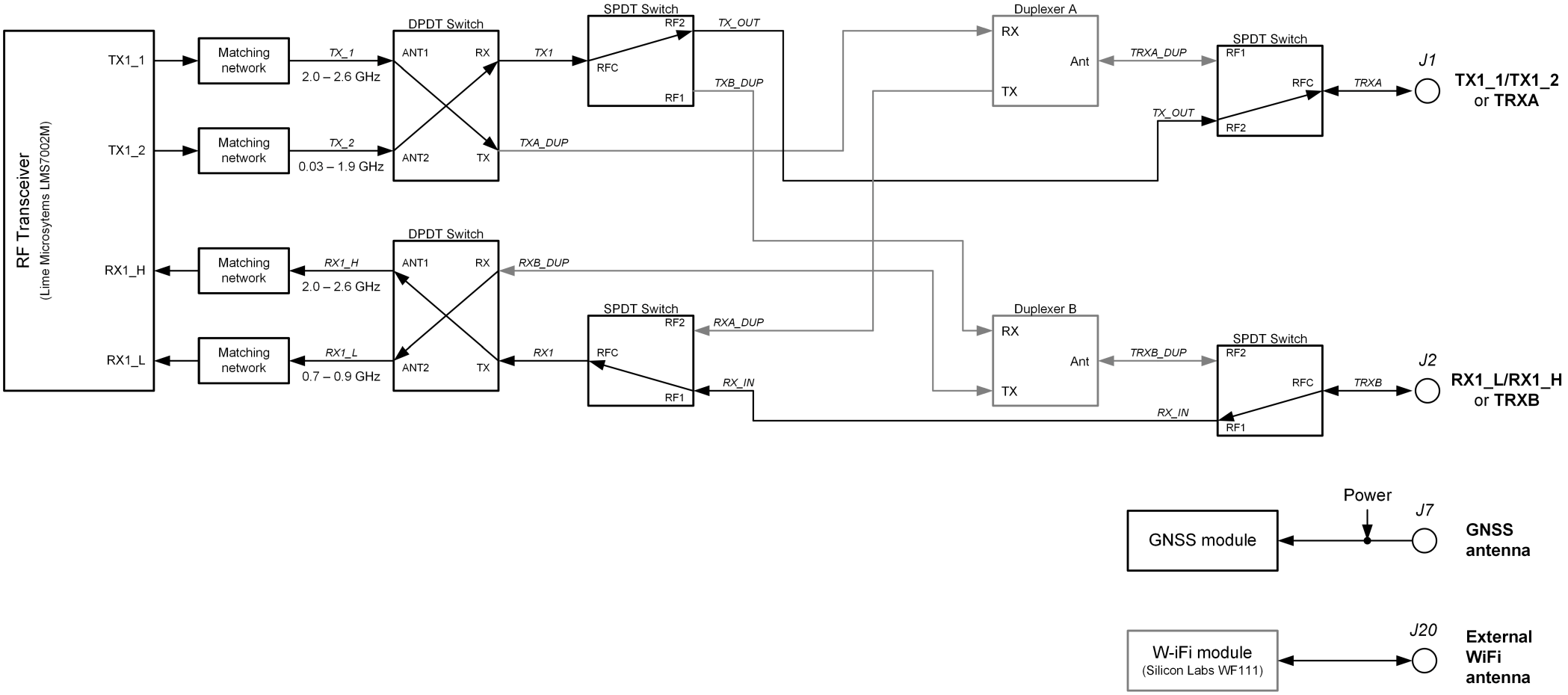
Title	Power diagram		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A4	Number:2	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:34	Sheet2 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\02_PowerDiagram.SchDoc			

Clock diagram



Title	Clock diagram		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A4	Number:3	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:35	Sheet3 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\03_ClockDiagram.SchDoc			

RF diagram

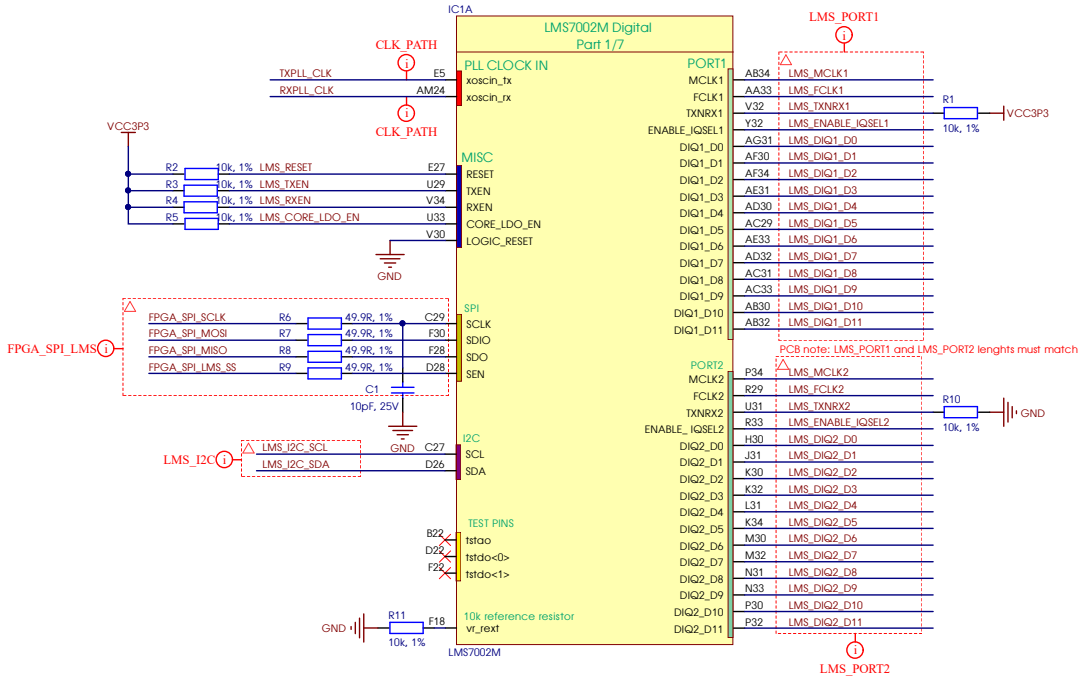


Title: RF diagram			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A4	Number: 4	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:36	Sheet 4 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\04_RFDiagram.SchDoc			

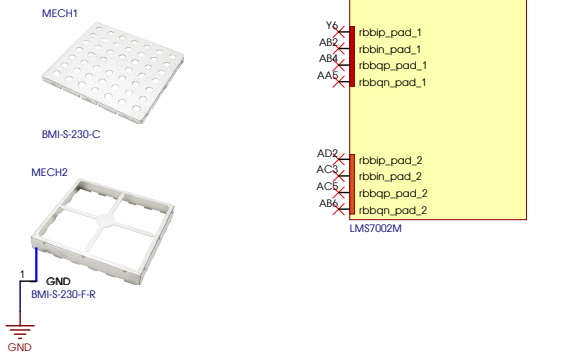
NF elements on sheet: IC2
Number of NF elements on sheet: 1

LMS7002M misc

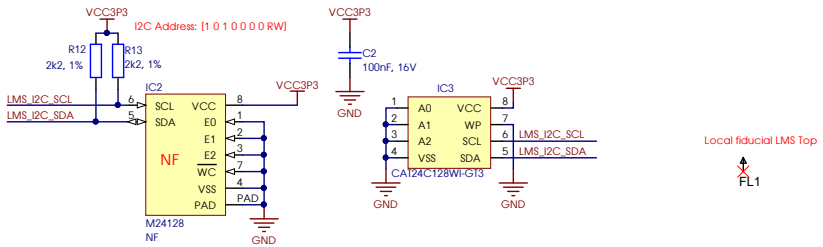
LMS7002M digital circuit



Baseband external IO



LMS EEPROM



Local fiducial LMS Top

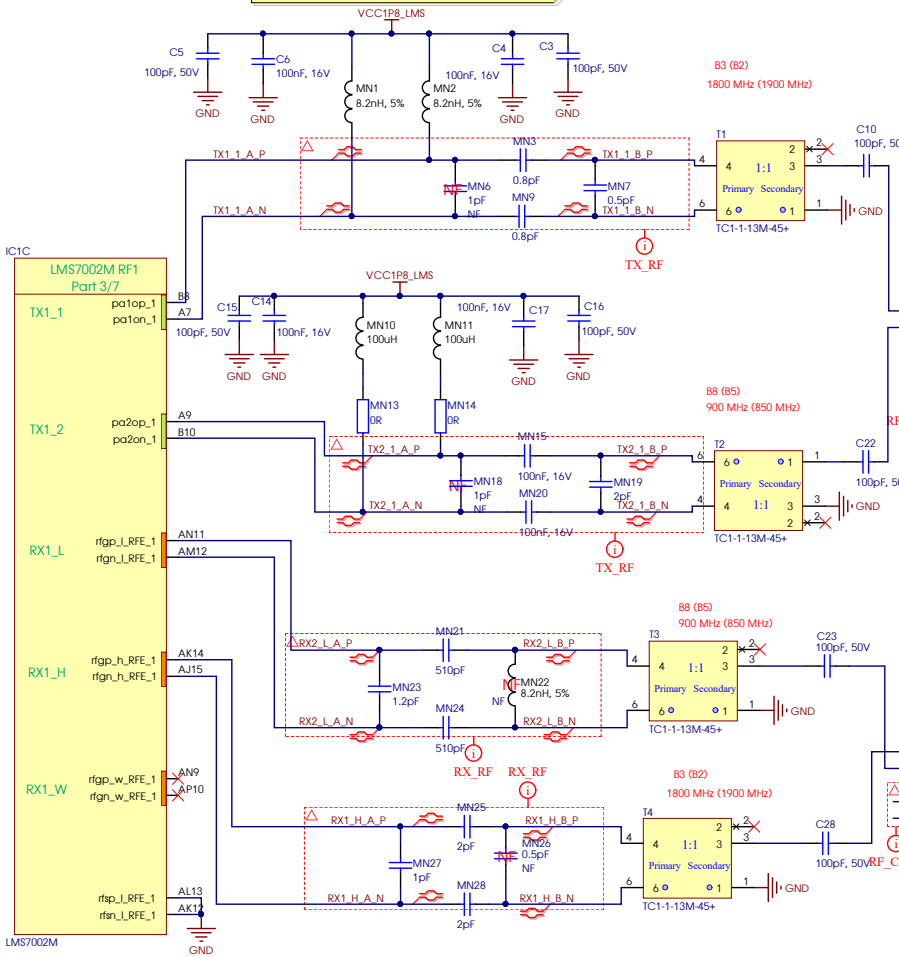
FL1

Title	LMS7002M misc		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:38	Sheet5 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\05_LMS7002M_Misc.SchDoc			

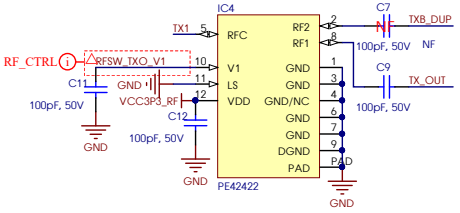
NF elements on sheet: ESD1, ESD2, MN6, MN18, MN22, MN26, C7, C19, C24, C32, MN5, MN8, IC5, C8, MN4, MN16, MN17, IC7, C18, MN12
Number of NF elements on sheet: 20

RF

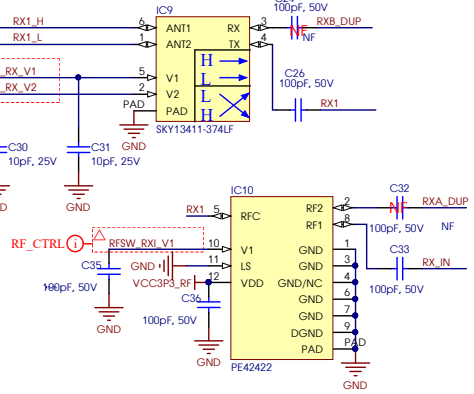
LMS RF Channel 1



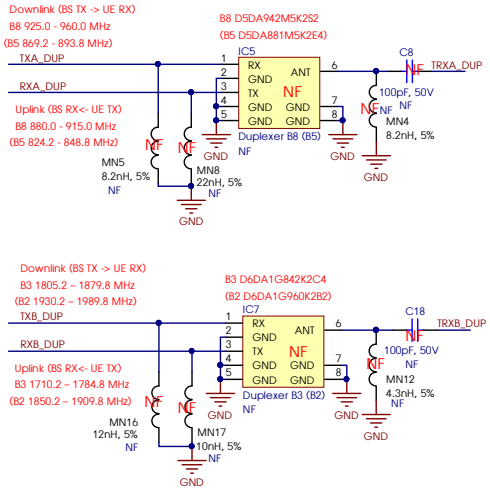
TX RF switches



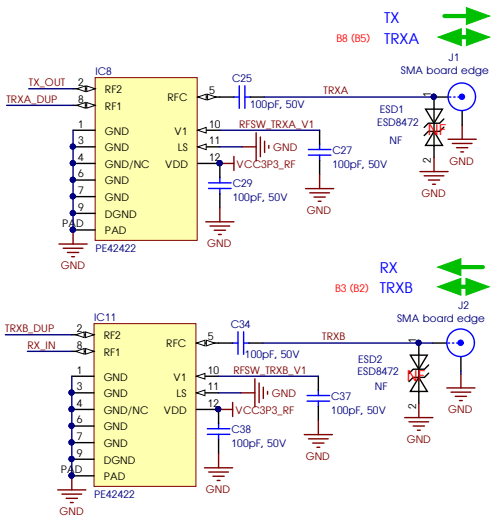
RX RF switches



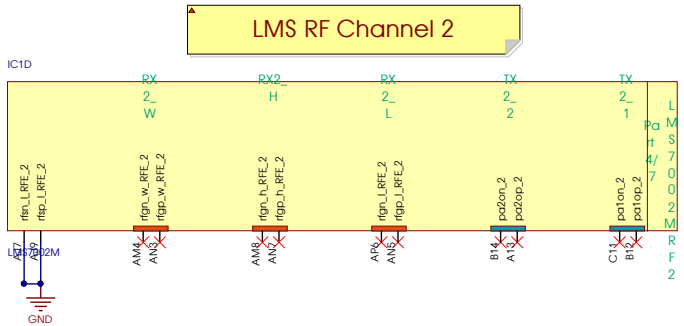
Duplexers



TRX RF switches



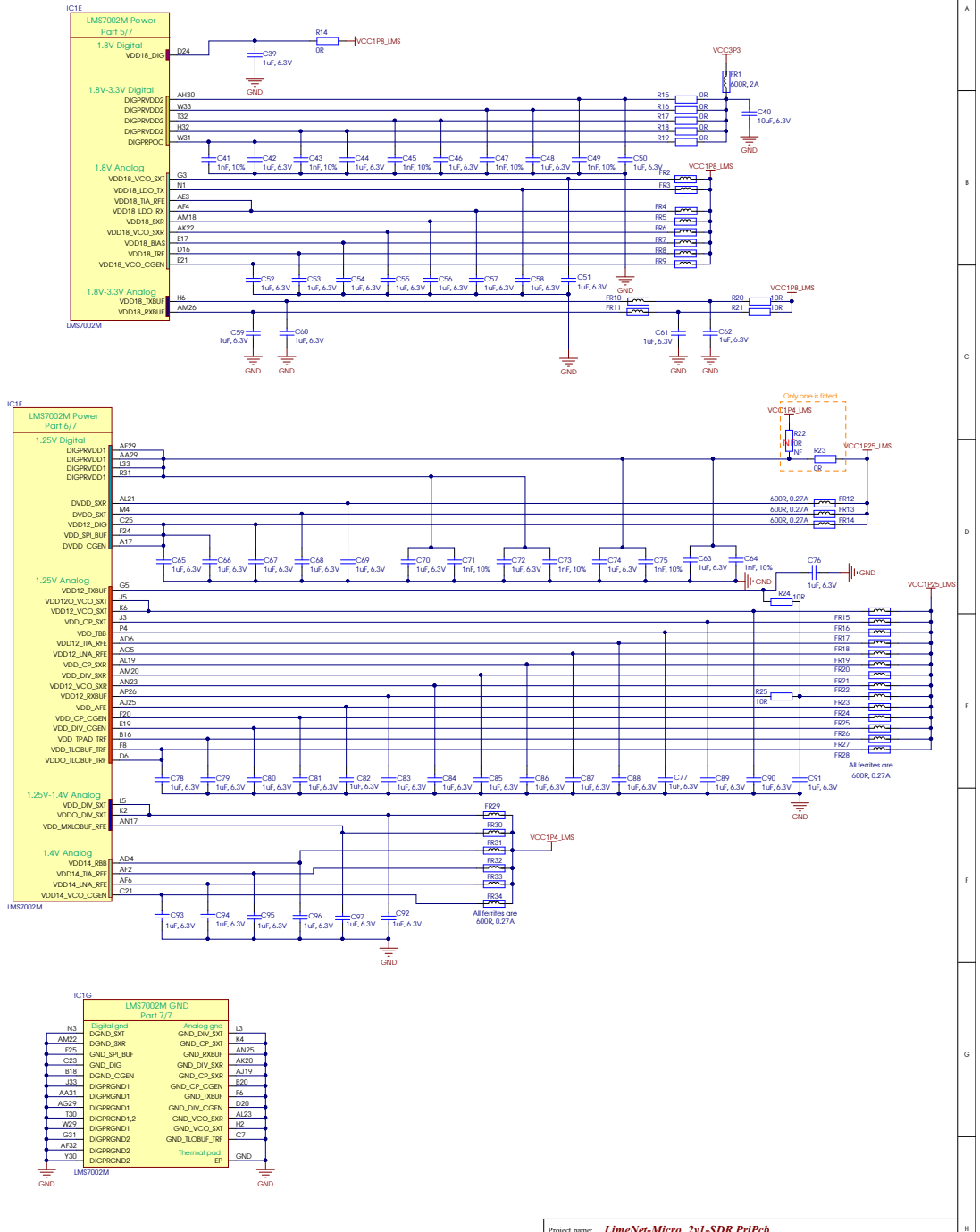
LMS RF Channel 2



Title	LMS7002M RF		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:39	Sheet6 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\06_LMS7002M_RF.SchDoc			

NF elements on sheet: 822
Number of NF elements on sheet: 1

LMS7002M power supply circuit



Project name:	*LimeNet-Micro_2v1-SDR.PrjPcb*		
Title:	***LMS7002M power supply***		*Lime Microsystems* *Surrey Tech Centre* *Guildford GU2 7YG* *Surrey* *United Kingdom*
Size: A3	Revision: v2.1		
Date: 7/6/2020	Time: 22:17:40	Sheet 7 of 15	
File: 07_LMS7002M_Power.SchDoc			

NF elements on sheet: J3, R27, R33, R34
Number of NF elements on sheet: 4

FPGA

FPGA Banks

IC12A

BANK 1A VCC1P8
BANK 1B

DIFFOUT_L1n	D1	BOM_VER2
DIFFOUT_L1p	C2	ETH_GPIO0
DIFFOUT_L3n	E3	HW_VER0
DIFFOUT_L3p	E4	HW_VER1
DIFFOUT_L5n	C1	BOM_VER1
DIFFOUT_L5p	B1	BOM_VER0
DIFFOUT_L7n	F1	BOM_VER3
DIFFOUT_L7p	E1	RAPI_EMMC_EN
DIFFOUT_L16p	H3	FPGA_BTN
JTAGEN	E5	[do not use]
TMS, DIFFOUT_L11n	G1	FPGA_JTAG_TMS
I/O	H1	ETH_GPIO2
TCK, DIFFOUT_L11p	G2	FPGA_JTAG_TCK
TDI, DIFFOUT_L12n	F5	FPGA_JTAG_TDI
TDO, DIFFOUT_L12p	F6	FPGA_JTAG_TDO
DIFFOUT_L14n	F4	HW_VER2
DIFFOUT_L14p	G4	ETH_GPIO1
DIFFOUT_L16n	H2	LM75_OS

VCC1P8 — R29 10k, 1% — GND

10M16SAU169C8G

IC12B

BANK 2 VCC3P3

CLK0n, DIFFOUT_L20n	G5	LMS_MCLK1
DIFFOUT_L21n	J1	LMS_DIQ2_D5
CLK0p, DIFFOUT_L20p	H6	LMK_CLK
DIFFOUT_L21p	J2	LMS_DIQ2_D9
CLK1n, DIFFOUT_L22n	H5	RAPI_GPCLK1
DIFFOUT_L23n	M1	LMS_DIQ2_D0
CLK1p, DIFFOUT_L22p	H4	LMS_MCLK2
DIFFOUT_L23p	M2	LMS_DIQ2_D3
DPCLK0, DIFFOUT_L24n	N2	LMS_DIQ2_D11
I/O	L1	FPGA_GPIO0
DPCLK1, DIFFOUT_L24p	N3	LMS_ENABLE_IQSEL2
I/O	L2	LMS_DIQ2_D6
PLL_L_CLKOUTn, DIFFOUT_L31n	M3	LMS_FCLK2
DIFFOUT_L32n	K1	LMS_DIQ2_D7
PLL_L_CLKOUTp, DIFFOUT_L31p	L3	LMS_FCLK1
DIFFOUT_L32p	K2	LMS_DIQ2_D2

10M16SAU169C8G

IC12C

BANK 3 VCC3P3

DIFFOUT_B1n	L5	LMS_DIQ2_D1
DIFFOUT_B2n	M4	LMS_DIQ2_D4
DIFFOUT_B1p	L4	LMS_DIQ2_D10
DIFFOUT_B2p	M5	FPGA_SPI_SCLK
DIFFOUT_B3n	K5	FPGA_SPI_MOSI
DIFFOUT_B3p	N4	LMS_DIQ2_D8
DIFFOUT_B4n	L5	FPGA_SPI_LMS_SS
DIFFOUT_B4p	N5	FPGA_SPI_MISO
DIFFOUT_B5n	N6	LMS_TXNRX1
DIFFOUT_B5p	N7	LMS_ENABLE_IQSEL1
DIFFOUT_B6n	M7	FPGA_GPIO1
DIFFOUT_B6p	N8	FPGA_GPIO2
DIFFOUT_B13n	L6	FPGA_GPIO3
DIFFOUT_B14n	M8	LMS_DIQ1_D8
DIFFOUT_B13p	K6	LMS_DIQ1_D10
DIFFOUT_B14p	M9	LMS_DIQ1_D9
DIFFOUT_B15n	J7	FPGA_GPIO5
I/O	N11	LMS_DIQ1_D2
DIFFOUT_B15p	K7	LMS_DIQ1_D11
I/O	N12	LMS_DIQ1_D0
DIFFOUT_B16n	M13	LMS_DIQ1_D5
DIFFOUT_B17n	N10	LMS_DIQ1_D7
DIFFOUT_B16p	M12	LMS_DIQ1_D1
DIFFOUT_B17p	N9	LMS_DIQ1_D4
CLK6n, DIFFOUT_B18n	M11	RAPI_SPI0_MOSI
CLK6p, DIFFOUT_B18p	L11	RAPI_SPI1_MISO
CLK7n, DIFFOUT_B20n	J8	FPGA_GPIO7
CLK7p, DIFFOUT_B20p	K8	RAPI_SPI0_MISO
DIFFOUT_B22n	M10	LMS_DIQ1_D6
DIFFOUT_B22p	L10	LMS_DIQ1_D3

10M16SAU169C8G

IC12D

BANK 5 VCC3P3

DIFFOUT_R1p, RUP	K10	FPGA_I2C_SCL
DIFFOUT_R2p	K11	FT_BE3
DIFFOUT_R1n, RDN	J10	GNSS_TPULSE
DIFFOUT_R2n	L12	GNSS_UART_RX
DIFFOUT_R11p	K12	FT_RXFN
I/O	L13	FT_D31
DIFFOUT_R11n	J12	FT_TXEN
I/O	K13	RAPI_SPI1_MOSI
DIFFOUT_R12p	J9	FT_OEN
DIFFOUT_R13p	J13	FT_D30
DIFFOUT_R12n	H10	FT_WAKEUPN
DIFFOUT_R13n	H13	FT_D29
DIFFOUT_R14p	H9	FT_BE0
DIFFOUT_R15p	G13	FT_D28
DIFFOUT_R14n	H8	FT_BE2
DIFFOUT_R15n	G12	FT_BE1

10M16SAU169C8G

IC12E

BANK 6 VCC3P3

CLK2p, DIFFOUT_R18p	G9	FT_CLK
CLK2n, DIFFOUT_R18n	G10	RAPI_SPI1_SCLK
CLK3p, DIFFOUT_R20p	E13	RAPI_SPI0_SCLK
CLK3n, DIFFOUT_R20n	E13	RAPI_SPI0_CE0
DIFFOUT_R22p	F12	FT_D27
DIFFOUT_R22n	E12	FT_WRN
DPCLK3, DIFFOUT_R30p	F9	FT_D19
I/O	D13	BUZZER
DPCLK2, DIFFOUT_R30n	E10	RAPI_GPIO12
I/O	C13	FT_D10
DIFFOUT_R31p	F8	FT_D22
DIFFOUT_R32p	B12	FT_D24
DIFFOUT_R31n	E9	FT_D20
DIFFOUT_R32n	B11	FT_D23
DIFFOUT_R33p	C12	FT_D26
DIFFOUT_R34p	B13	FT_D9
DIFFOUT_R33n	C11	FT_D25
DIFFOUT_R34n	A12	FT_D8
DIFFOUT_R35p	E10	FT_D21
DIFFOUT_R35n	D9	FT_D16
DIFFOUT_R37p	D12	FT_RDN
DIFFOUT_R37n	D11	FPGA_GPIO4

10M16SAU169C8G

IC12F

BANK 8 VCC3P3

CLK5p, DIFFOUT_T26p	C10	ADF_MUXOUT
DIFFOUT_T27p	A8	FT_D6
CLK5n, DIFFOUT_T26n	C9	WIFI_PIO5
DIFFOUT_T27n	A9	FT_D7
DIFFOUT_T28p	B10	FPGA_I2C_SDA
DIFFOUT_T29p	A10	RAPI_SPI1_CE0
DEV_CLRn, DIFFOUT_T28n	B9	SR_SCLK
DIFFOUT_T29n	A11	FPGA_GPIO6
DEV_OE, DIFFOUT_T30p	D8	GNSS_UART_TX
DIFFOUT_T30n	E8	FT_D18
VREFB8N0	B7	SR_DIN
CONFIG_SEL	D7	FPGA_CONFIG_SEL
DIFFOUT_T31p	A7	FT_D5
nCONFIG	E7	[do not use]
DIFFOUT_T31n	A6	FT_D4
DIFFOUT_T32p	B6	FT_D15
DIFFOUT_T33p	A4	FT_D2
DIFFOUT_T32n	B5	FT_D14
DIFFOUT_T33n	A3	FT_D1
DIFFOUT_T34p	E6	FT_D17
DIFFOUT_T35p	B3	FT_D12
CRC_ERROR, DIFFOUT_T34n	D6	SR_LATCH
DIFFOUT_T35n	B4	FT_D13
nSTATUS, DIFFOUT_T36p	C4	LMS_TXNRX2
I/O	A5	FT_D3
CONF_DONE, DIFFOUT_T36n	C5	FAN_CTRL
DIFFOUT_T38p	A2	FT_D0
DIFFOUT_T38n	B2	FT_D11

VCC3P3 — R38 10k, 1% — R39 10k, 1% — R40 10k, 1%

VCC3P3 — R41 10k, 1% — R42 10k, 1%

10M16SAU169C8G

FPGA JTAG

Pitch: 0.05" (1.27mm)

FPGA_CONFIG_SEL — R27 NF — VCC3P3 — R30 10k, 1% — GND

VCC1P8 — R26 10k, 1% — R28 10k, 1%

FPGA_JTAG

FPGA_JTAG_TCK	1	2
FPGA_JTAG_TDO	3	4
FPGA_JTAG_TMS	5	6
FPGA_JTAG_TDI	7	8
	9	10

J4 — FPGA JTAG — R31 1k, 1% — GND — VCC1P8 — GND

FPGA JTAG (edge)

Pitch: 0.1" (2.54mm)

J3 — FPGA JTAG (board edge)

	7	VCC5P0
	6	VCC1P8
NF	5	FPGA_JTAG_TDI
	4	FPGA_JTAG_TMS
	3	FPGA_JTAG_TDO
	2	FPGA_JTAG_TCK
NF	1	

GND

FPGA GPIO

Pitch: 0.05" (1.27mm)

FPGA_GPIO — FPGA_GPIO0, FPGA_GPIO2, FPGA_GPIO4, FPGA_GPIO6

FPGA_GPIO — FPGA_GPIO1, FPGA_GPIO3, FPGA_GPIO5, FPGA_GPIO7

J5 — FPGA GPIO — GND

VCC3P3 — R32 0R — VCC5P0 — R33 0R NF — C98 100nF, 16V — GND

HW_VER & BOM_VER

HW_VER = 3 [0 1 1]
BOM_VER = 1 [0 0 0 1] SDR

BOM_VER0 — R34 NF 0R — BOM_VER1 — R35 0R — BOM_VER2 — R36 0R — BOM_VER3 — R37 0R — GND

BOM_VER

BOM_VER = 0 [0 0 0 0] Lime (full)
BOM_VER = 1 [0 0 0 1] SDR (w/o duplexers, WiFi)
BOM_VER = 2 [0 0 1 0] GSM (duplexers, w/o PoE, audio, video)

IC12G — GND BANK

REFGND, GND ×14

E2, A1, A13, B8, C3, D5, E11, F3, G7, H12, J4, L9, M4, N1, N13

10M16SAU169C8G — GND

FPGA Power

IC12H

VCC1P8 — F2, G3 — VCCIO1A, VCCIO1B

VCC3P3 — K3, J3 — VCCIO2, VCCIO2

VCC3P3 — J11, H11 — VCCIO5, VCCIO5

VCC3P3 — G11, F11 — VCCIO6, VCCIO6 — VIO 430mA

VCC3P3 — L8, L7, L6 — VCCIO3, VCCIO3, VCCIO3

VCC3P3 — C8, C7, C6 — VCCIO8, VCCIO8, VCCIO8

VCC3P3A — K4, D10, D4, K9 — VCCA1, VCCA2, VCCA3, VCCA4

VCC3P3 — H7, G8, G6, F7 — VCC_ONE, VCC_ONE, VCC_ONE, VCC_ONE — ONE 2.3W

D3 — ADC_VREF — ANAIN1 — D2 — GND

10M16SAU169C8G

VCC3P3 — C99 10uF, 6.3V — C100 1uF, 6.3V — C101 100nF, 6.3V — C102 100nF, 6.3V — C103 100nF, 6.3V — C104 100nF, 6.3V — C105 100nF, 6.3V — GND

PCB note: Place 100nF cap close to each VCCIO2/3 pin.

VCC3P3 — FR35 220R, 0.9A — VCC3P3A — C106 10uF, 6.3V — C107 1uF, 6.3V — C108 100nF, 6.3V — C109 100nF, 6.3V — C110 100nF, 6.3V — C111 100nF, 6.3V — C112 100nF, 6.3V — GND

PCB note: Place 100nF cap close to each VCCA pin.

VCC3P3 — C113 10uF, 6.3V — C114 1uF, 6.3V — C115 100nF, 6.3V — C116 100nF, 6.3V — C117 100nF, 6.3V — C118 100nF, 6.3V — GND

PCB note: Place 100nF cap close to each VCC_ONE pin.

VCC1P8 — C119 10uF, 6.3V — C120 1uF, 6.3V — C121 100nF, 6.3V — C122 100nF, 6.3V — GND

PCB note: Place 100nF cap close to each VCCIO1 pin.

VCC3P3 — C123 10uF, 6.3V — C124 1uF, 6.3V — C125 100nF, 6.3V — C126 100nF, 6.3V — C127 100nF, 6.3V — C128 100nF, 6.3V — C129 100nF, 6.3V — C130 100nF, 6.3V — C131 100nF, 6.3V — GND

PCB note: Place 100nF cap close to each VCCIO5/6/8 pin.

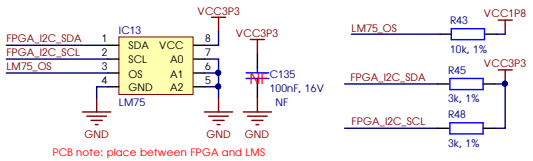
Schematic note: marked 10uF caps not crucial and can be removed to reduce BOM price

Title	FPGA		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size:	A3	Number: *.	Revision: v2.1
Date:	7/6/2020	Time: 22:17:41	Sheet 8 of 15
File:	F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\08_FPGA.SchDoc		

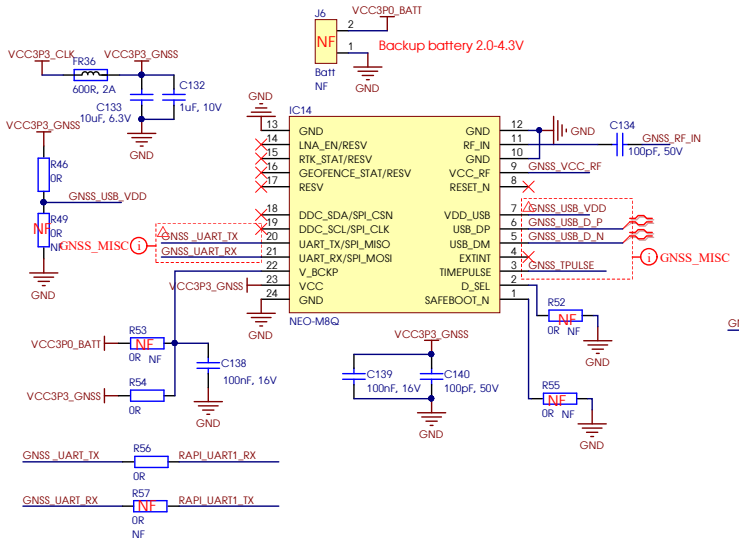
NF elements on sheet: C135, R47, R49, R52, R53, R55, R57, J6, ESD3, IC16, IC21, R59, R63, R71
Number of NF elements on sheet: 14

Misc

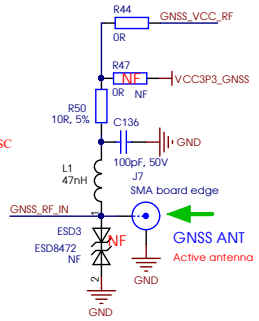
I2C Temperature sensor



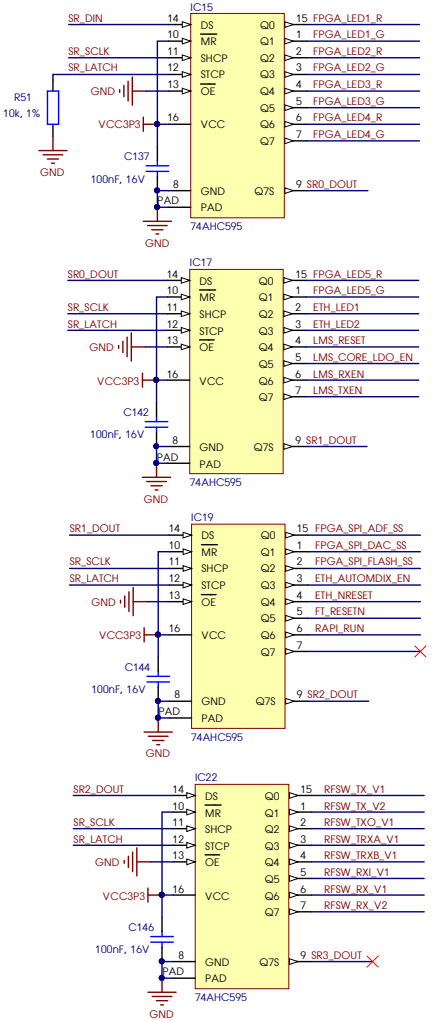
GNSS receiver



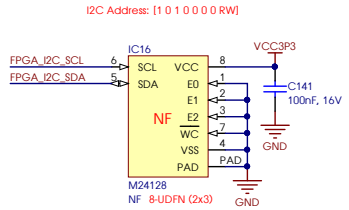
External GNSS antenna (active)

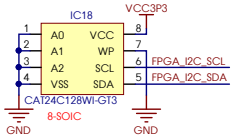


Shift registers (Outputs)

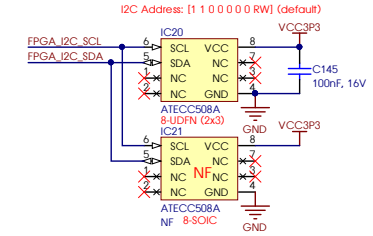


I2C EEPROM

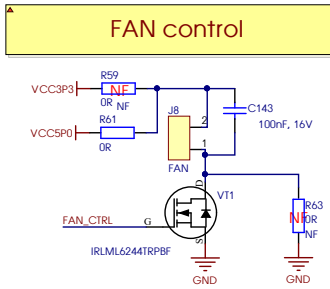




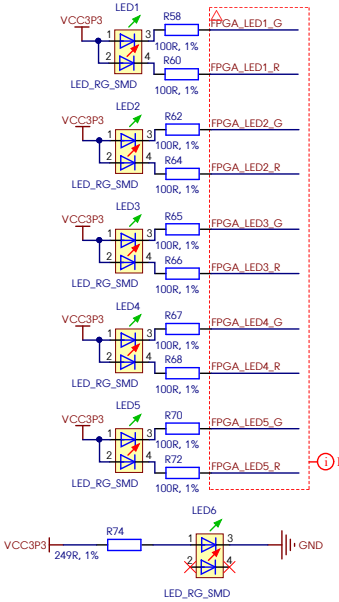
I2C secure key storage



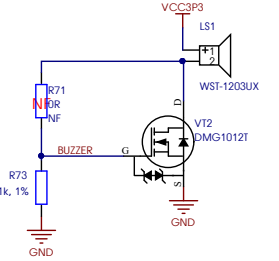
FAN control



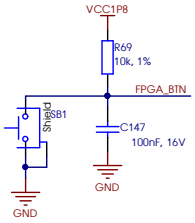
FPGA LEDs



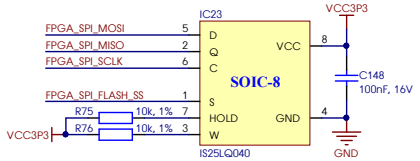
Buzzer



FPGA_BTN



SPI Flash



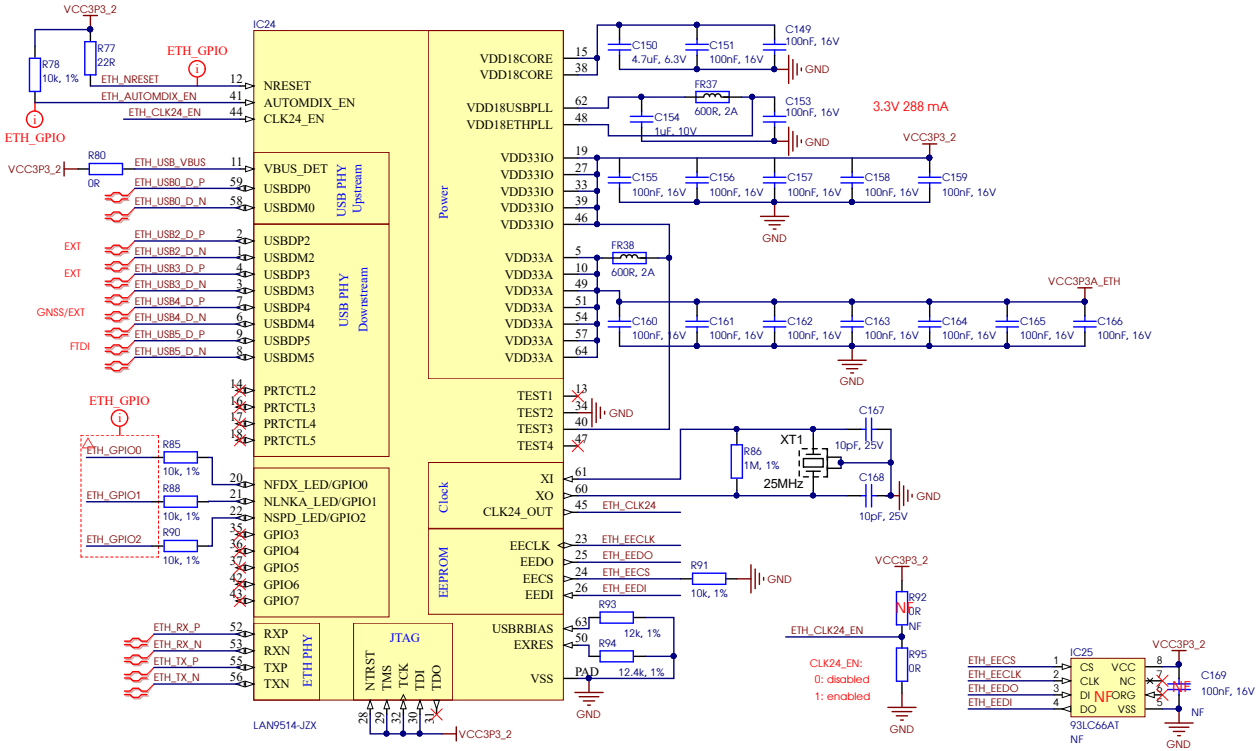
Power

Title: Misc			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *.	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:42	Sheet 9 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\09_Misc.SchDoc			

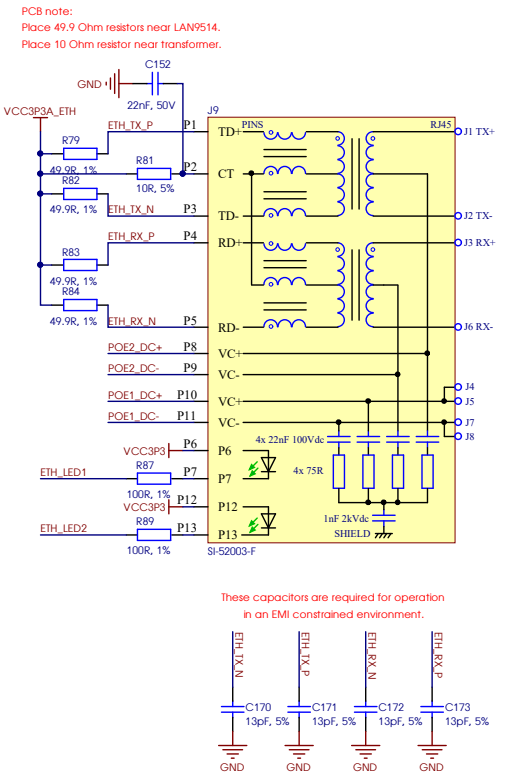
NF elements on sheet: R92, IC25, C169, J11, J12, R96, R97, R98, R101
Number of NF elements on sheet: 9

Misc

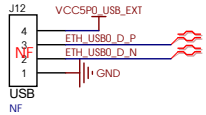
USB hub + Ethernet



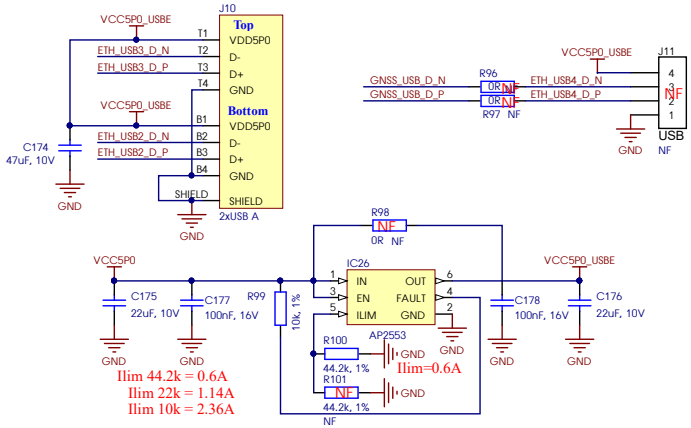
RJ45 connector



USB upstream



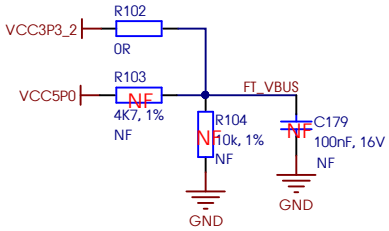
USB downstream

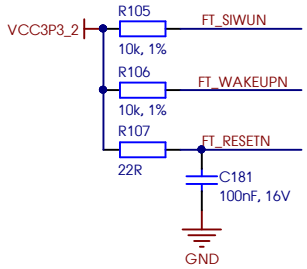


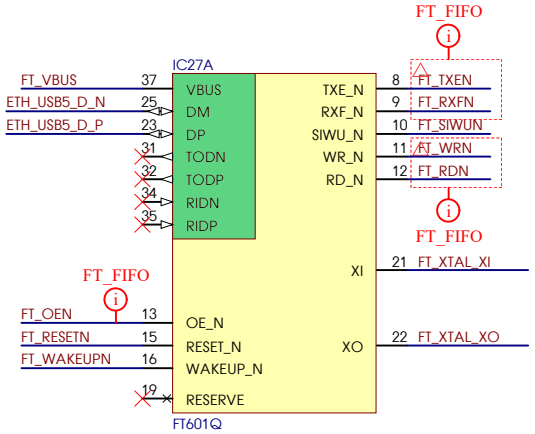
Title: USB Ethernet			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:44	Sheet 10 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\10_USB_Ethernet.SchDoc			

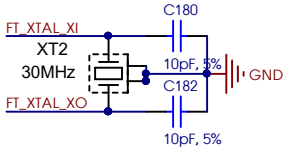
NF elements on sheet: R102, R104, C179
Number of NF elements on sheet: 3

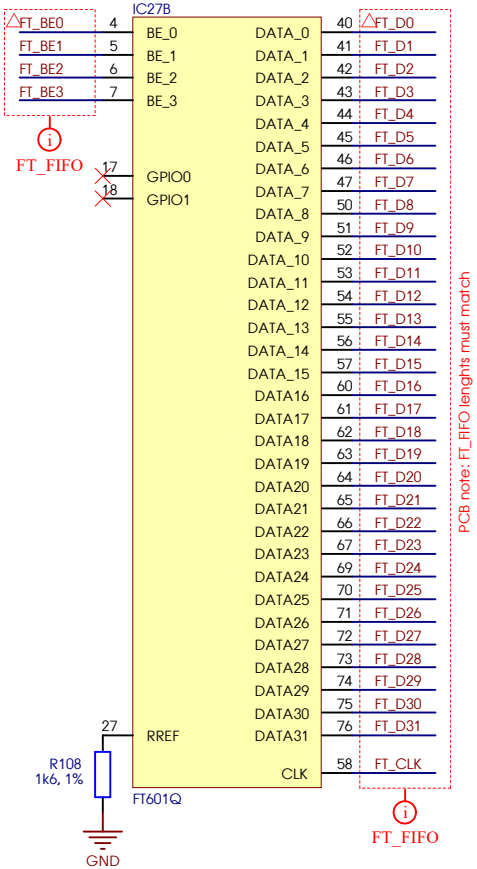
USB FIFO interface





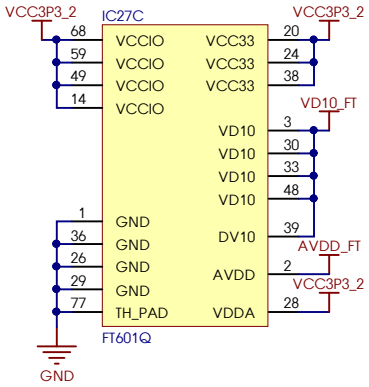


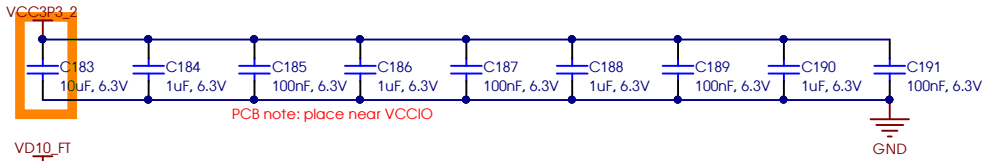


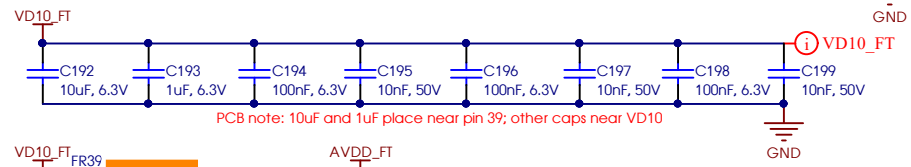


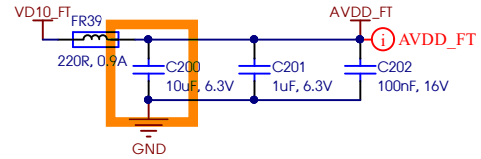
FTDI Power

3.3V 190 mA







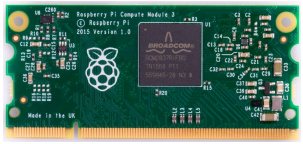


Schematic note: marked 10uF caps not crucial and can be removed to reduce BOM price

Title	USB FIFO		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A4	Number: 11	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:45	Sheet 11 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\11_USB_FIFO.SchDoc			

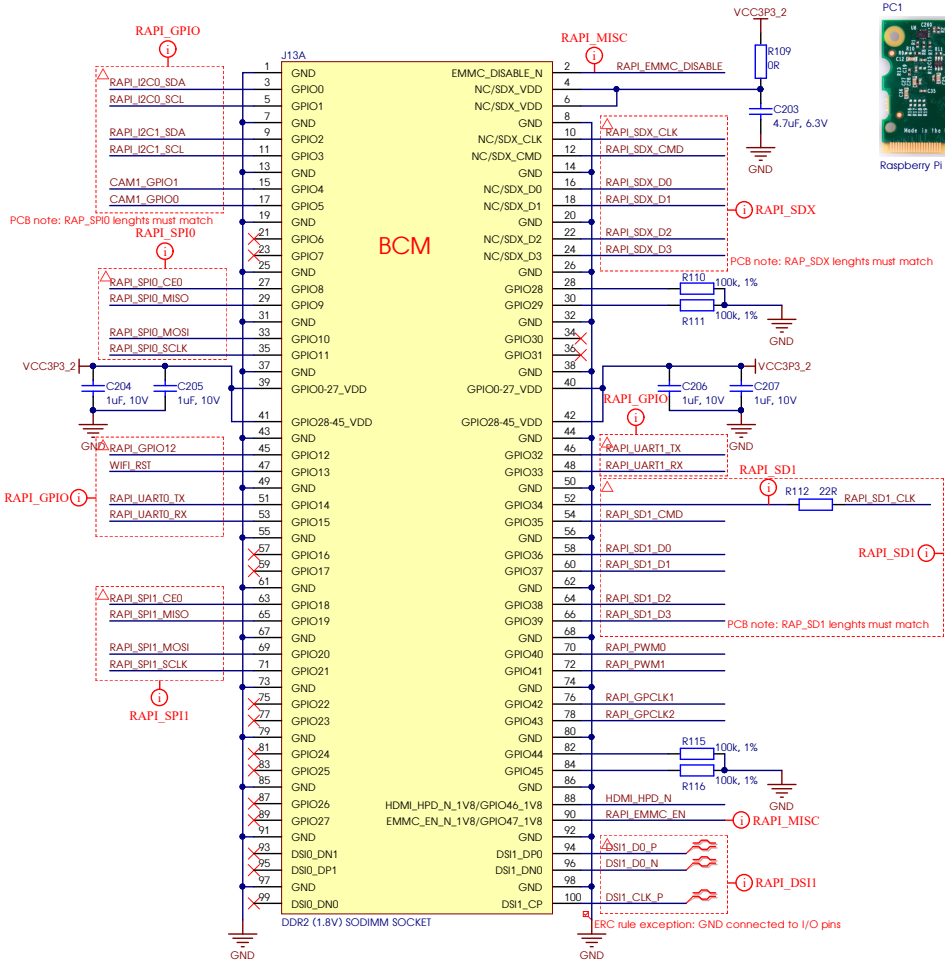
NF elements on sheet: R114, R119, R121, R122, R126, R129, R129, R132
Number of NF elements on sheet: 8

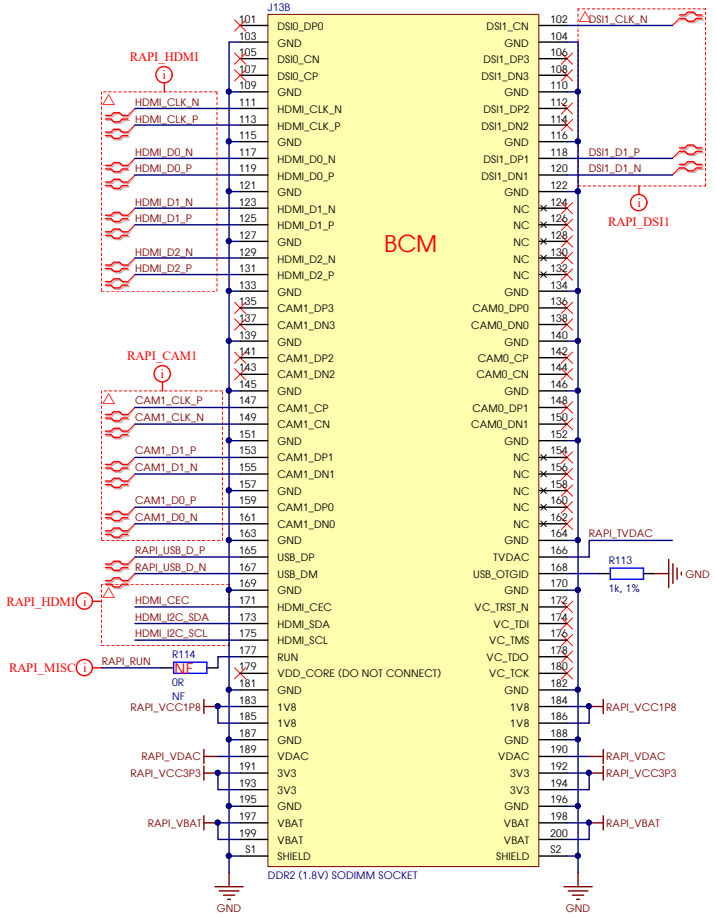
Raspberry Pi CM3(L)



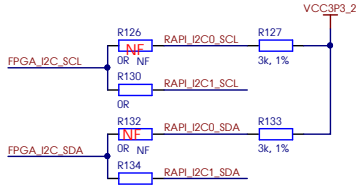
PC1

Raspberry Pi Compute Module 3+ (8GB eMMC)

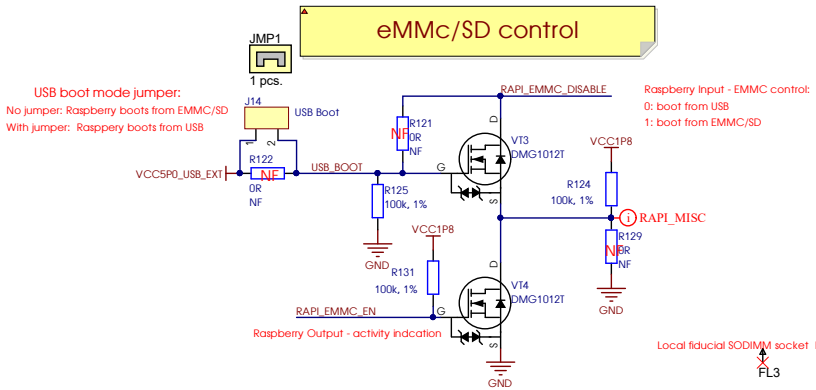


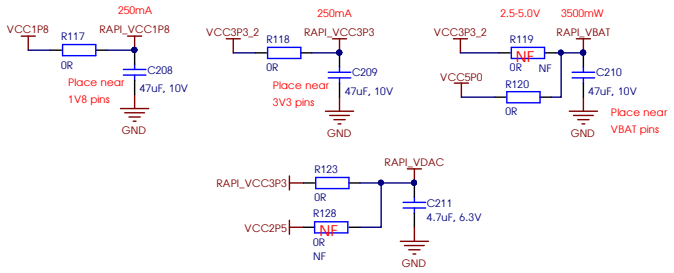


I2C bus selection



eMMc/SD control





Title	Raspberry Pi CM3(L) module		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:46	Sheet12 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\12_Raspbbery CM3.SchDoc			

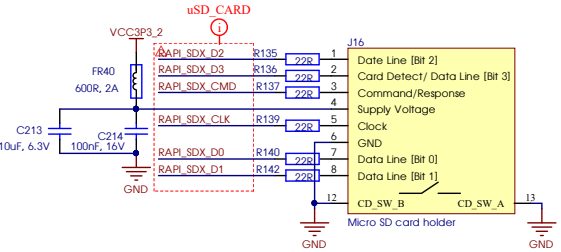
NF elements on sheet: ESD4, R158, IC30, JMP2, R143, R144, R146, R147, R148, R149, C218, J20, C220, C221, C222, C223, C224

Number of NF elements on sheet: 17

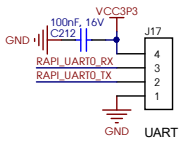
Raspberry Misc

uSD card

Only for CM3L with no on-board Flash (eMMC)



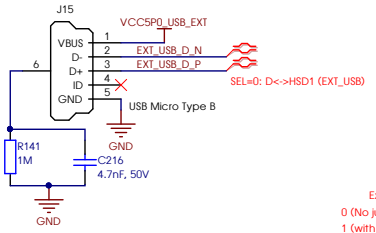
EXT_UART



Micro USB socket

USB can be used for:

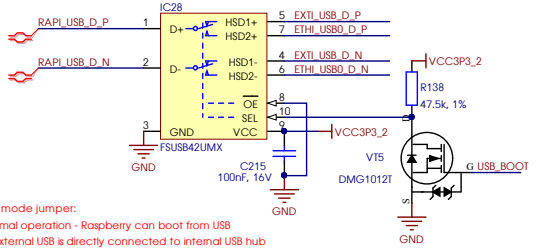
1. programming Raspberry CM3(L) eMMC/SD (J14/R122 fit, J18/R143 NF)
2. directly connecting to internal USB hub (J14/R122 NF, J18/R143 fit)



USB switches

SEL=0: D<->HSD1 (EXT_USB)

SEL=1: D<->HSD2 (ETH_USB)

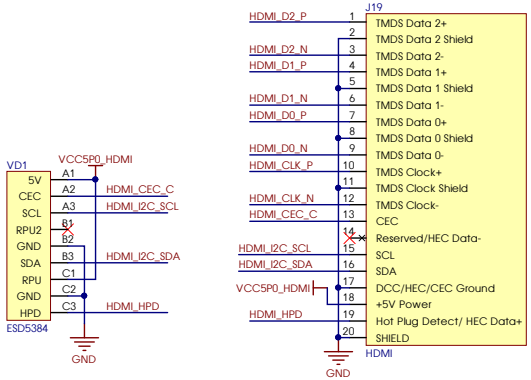


External USB mode jumper:

0 (No jumper): normal operation - Raspberry can boot from USB

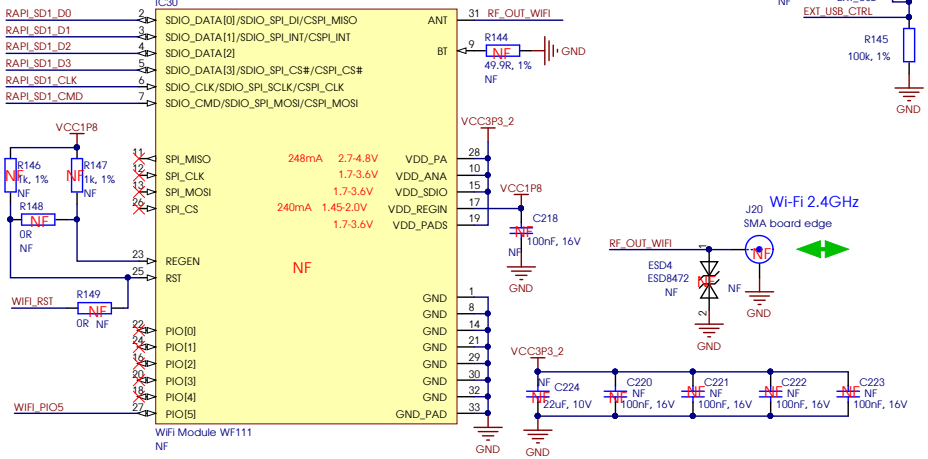
1 (with jumper): external USB is directly connected to internal USB hub

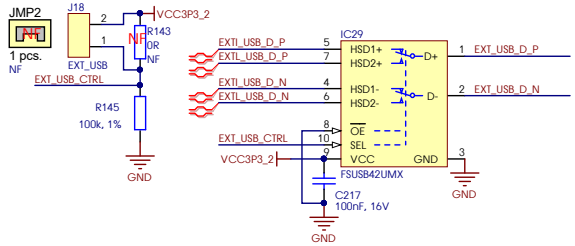
HDMI

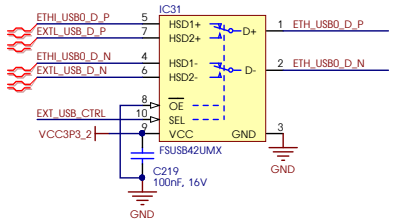


SDIO Wi-Fi

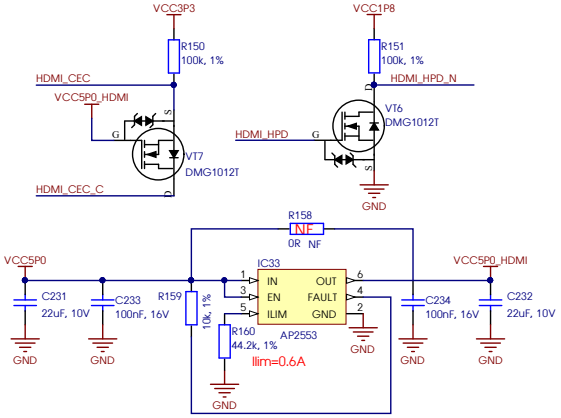
Single 2.4GHz band 802.11 b/g/n Wi-Fi



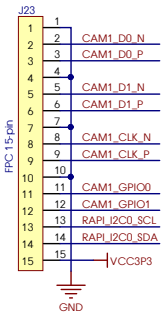




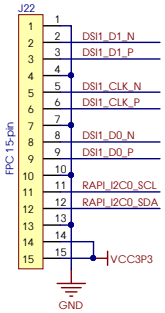
LVDS (Camera + Display)



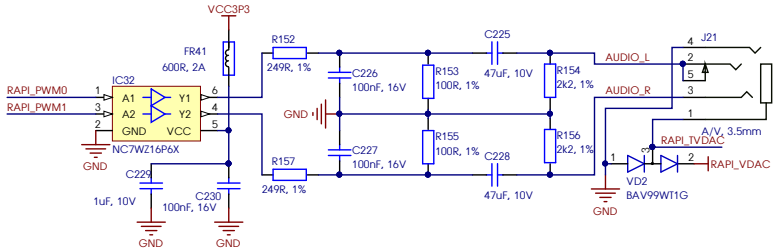
Camera



Display



Analog audio + Composite video out



Title	Raspberry Misc		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: 12.	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:47	Sheet13 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\13_Raspberry_Misc.SchDoc			

NF elements on sheet: R166, R168, R169, XO2, XO3, XO4, R170, R171, R172, R173, R174, R175, C241, C242, C255, C256, C257, C258, C259, C272, R186, IC37, R194, R195, C284
Number of NF elements on sheet: 25

Clock circuits

(VC)OCXO

VCC3P3_CLK
FR42 600R, 2A
R163 0R
C238 10uF, 16V
C237 100nF, 16V
C239 100pF, 50V
XO_VC
XO1 VCOCXO
NC/VC Output
Vcc GND
U7475LF 30.72MHz
R162 0R
Only one is fitted
CLK_PATH

(VC)TCXO

VCTCXO1
XO2
VDD OUT
TRI-ST. NF T.S.
VC GND
E6245LF 30.72 MHz
R170 0R NF
R171 0R NF
XO_VC
XO3
VDD GND NF OUT
Vc
E5280LF 30.72MHz
R172 0R NF
C256 1uF, 10V NF
C255 100nF, 16V NF
R173 0R NF
VCTCXO2
XO4
VC FILTER RF OUT
VCO
VCC
NC NC NC NC NC NC
GND
RTX5032A, 40.00MHz
R174 0R NF
R175 22R NF
C257 1uF, 10V NF
C258 100nF, 16V NF
C259 18nF, 16V NF
CLK_PATH

RAPI_GPCLK2
REF_CLK_IN
ETH_CLK24
R166 0R NF
R168 0R NF
R169 0R NF
Only one is fitted

Clock buffer

VCC3P3_LMK2
VCC3P3_LMK
+1.8V_DIG_LMK
R161 0R
IC34 LMK00105
CLKin CLKin*
OE SEL
OSCin OSCout
Vdd Vdd
Vddo Vddo
CLKout0 CLKout1
CLKout2 CLKout3 CLKout4
REF_ADF
LMK_CLK
REF_CLK_OUT
C235 100nF, 16V
C236 100nF, 16V
R165 49.9R, 1%
C240 100nF, 16V
R164 0R
R167 0R
TXPLL_CLK
RXPLL_CLK
C241 NF 47pF, 50V NF
C242 47pF, 50V NF
FR43 600R, 2A
C243 1uF, 10V
C244 100nF, 16V
C245 100pF, 50V
C246 100pF, 50V
PCB note: Place 100pF close to each Vddo pin.
FR44 600R, 2A
C248 1uF, 10V
C249 100nF, 16V
C250 100pF, 50V
C251 100pF, 50V
PCB note: Place 100pF close to each Vdd pin.
VCC1P8_2
FR45 600R, 2A
C247 1uF, 10V
C252 100nF, 16V
C253 100pF, 50V
C254 100pF, 50V

MECH3
BMI-S-230-C
MECH4
BMI-S-230-F-R

REF CLK OUT

REF_CLK_OUT
R176 0R
J24 SMA board edge

Phase detector

VCC3P3_CLK
FR46 600R, 0.27A
C260 100nF, 16V
C261 100nF, 16V
C262 100pF, 50V
C263 100pF, 50V
C264 100pF, 50V
C265 100pF, 50V
REF_ADF
R177 49.9R, 1%
R178 10R, 5%
C271 100pF, 50V
C273 100nF, 16V
C269 100pF, 50V
C270 100pF, 50V
R181 1k, 1%
IC36 ADF4002
CE Vp CP MUXOUT Rset CPGND
REFin RFinA RFinB CLK DATA LE
DVdd AVdd
R182 470R, 0.5%
R184 0R
C277 22pF, 5%
C278 22pF, 5%
C279 22pF, 5%
R190 330R, 5%
ADF_MUXOUT
R188 10k, 1%
R189 10k, 1%
C283 10pF, 25V
C274 1nF, 10%
C275 1nF, 10%
C280 220pF, 10%
R183 49.9R, 1%
REF_CLK_IN
J25 SMA board edge
R191 49.9R, 1% FPGA_SPI_SCLK
R192 49.9R, 1% FPGA_SPI_MOSI
R193 49.9R, 1% FPGA_SPI_ADF_SS

XO VC DAC (16 bit)

VCC3P3_CLK
FR47 600R, 2A
C266 1uF, 10V
C267 100nF, 16V
C268 100pF, 50V
IC35
Vdd Vout
Vref
SYNC Vfb
SCLK
DIN
GND
AD5662
TCXO_DAC_VREF
FPGA_SPI_DAC_SS_R
FPGA_SPI_SCLK_R
FPGA_SPI_MOSI_R
R179 1k, 1%
R180 0R
C272 NF 100nF, 16V NF
C276 1nF, 50V
XO_VC
VCC2P5
R185 3k, 1%
R186 1k, 1% NF
R187 10k, 1%
Vref=2.538V
C281 1uF, 10V
C282 100nF, 16V

XO DAC (8 bit)

IC37
SCLK VOUT
SDIN
SYNC NF
VDD GND
AD5601BKSZ-REEL7
Vout=2.538V
R194 NF 3k, 1%
R195 10k, 1% NF
C284 NF 100nF, 16V NF
FPGA_SPI_SCLK_R
FPGA_SPI_MOSI_R
FPGA_SPI_DAC_SS_R
FPGA_SPI_DAC_SS
FPGA_SPI_SCLK
FPGA_SPI_MOSI
R196 49.9R, 1%
R197 49.9R, 1%
R198 49.9R, 1%

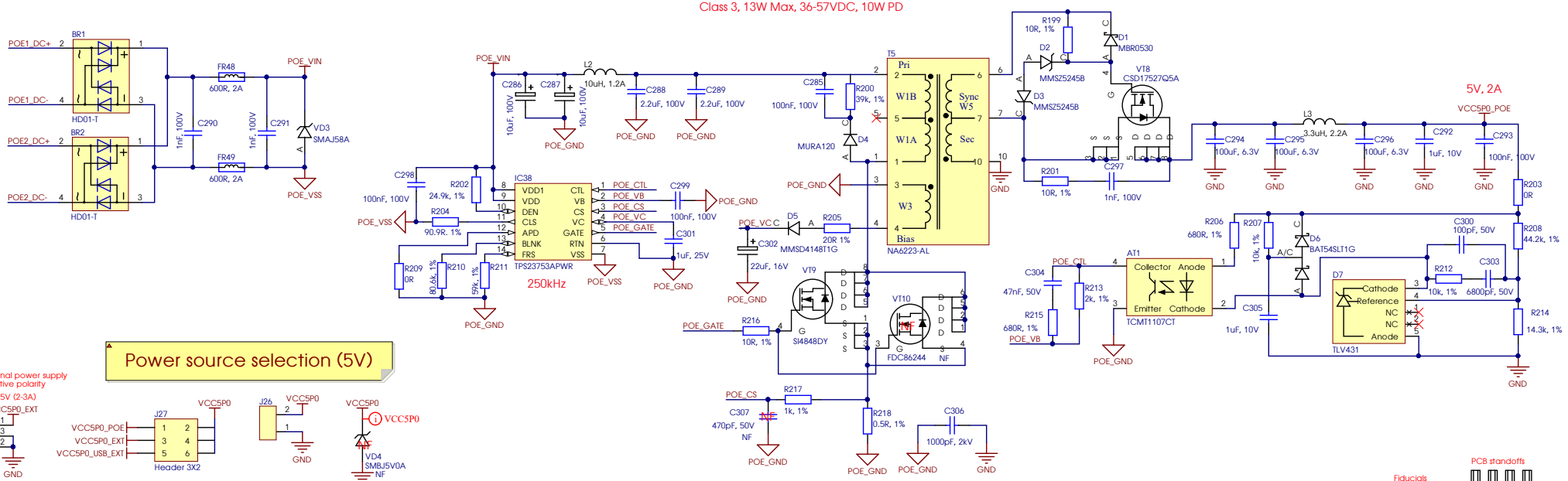
Title: Clocks			Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *.	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:49	Sheet14 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\14_Clocks.SchDoc			

NF elements on sheet: VT10, C307, VD4, FR50, C312, IC41, R219, R223, C313, R235, R239, R240, R241
Number of NF elements on sheet: 13
Total number of NF elements on all sheets: 115

Board power circuits

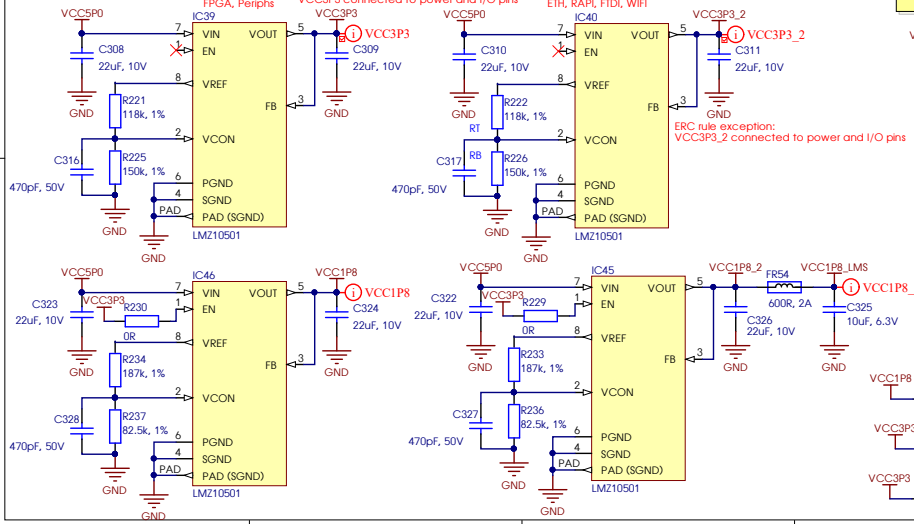
Power over Ethernet

IEEE 802.3-2005 compliant
Class 3, 13W Max, 36-57VDC, 10W PD

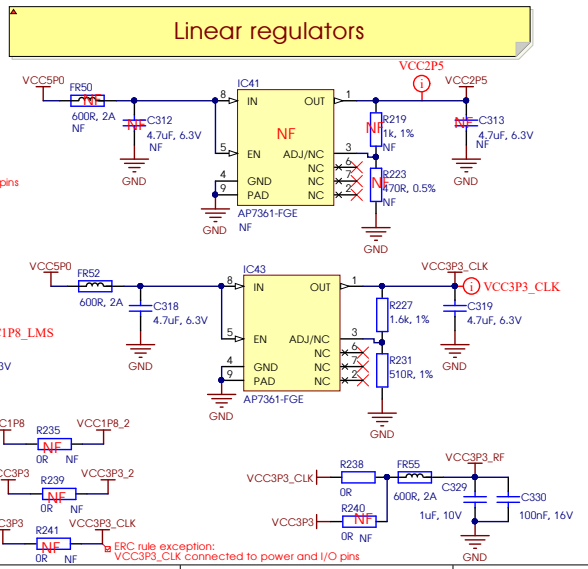


Power source selection (5V)

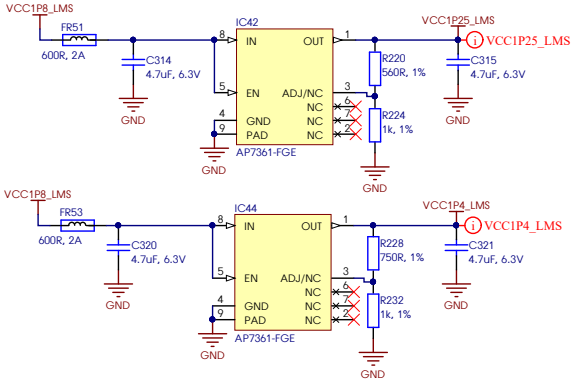
Switching regulators

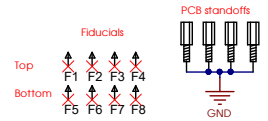


Linear regulators



Linear regulators (LMS)





Title	Board power supply		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A3	Number: *	Revision: v2.1	
Date: 7/6/2020	Time: 22:17:51	Sheet 15 of 15	
File: F:\01_PCB\RPI\github\LimeNET-Micro\hardware\2v1\Schematics\15_PowerSupply.SchDoc			