Lime microsystems

LimeSDR-PCIe v1.3

CONTROLLED IMPEDANCE

GENERAL PARAMETERS:

Top layer copper foil thickness: 17.5 um
Dielectric thickness from Top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Bottom layer copper foil thickness: 17.5 um
Dielectric thickness from L11 to Bottom = 173um (6.8 mils)
Dielectric between L11 layer and Bottom layer relative permittivity (Er): 4.2
Ground plane distance to trace on Bottom layer: 0.1mm

CALCULATIONS:

RF (Top)

50 Ohm microstrip (Top layer, no GND) characteristics:
Top layer copper foil thickness: 17.5 um
Track width = 0.325 mm (12.795 mils)
Dielectric thickness from Top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

RF (Bottom)

50 Ohm coplanar waveguide with GND (Bottom layer) characteristics:
Bottom layer copper foil thickness: 17.5 um
Track width = 0.254 mm (10 mils)
Distance to GND: 0.1 mm (3.937 mils)
Dielectric thickness from Bottom to L11 = 173um (6.8 mils)
Dielectric between Bottom layer and L11 relative permittivity (Er): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

RF (Top)

100 Ohm coupled microstrip line (Top layer) characteristics:
Top layer copper foil thickness: 17.5 um
Track width = 0.2 mm (6.8 mils)
Track spacing = 0.14 mm (5.51 mils)
Track width/spacing ratio = 1.428
Dielectric thickness from top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 100.752 Ohms (+/- 10% tolerance)

PCIe (Top)

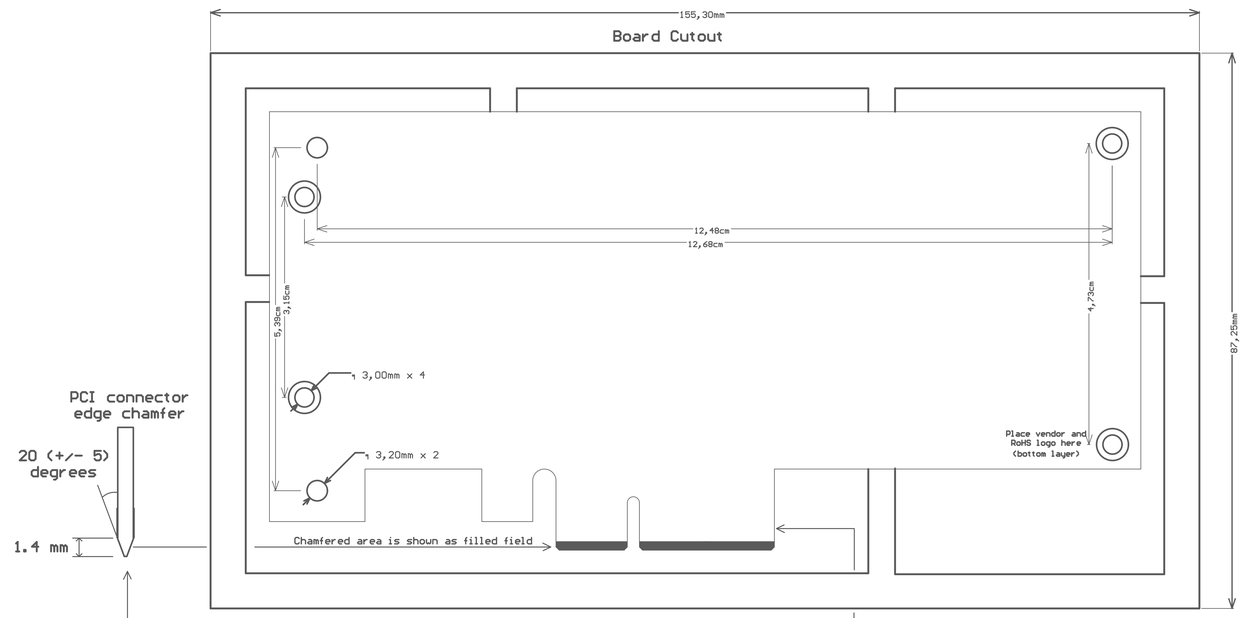
85 Ohm coupled microstrip line (Top layer, PCI traces) characteristics:
Top layer copper foil thickness: 17.5 um
Track width = 0.25 mm (9.84 mils)
Track spacing = 0.1 mm (3.93 mils)
Track width/spacing ratio = 2.5
Dielectric thickness from Top to 2nd layer = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 84.8 Ohms (+/- 10% tolerance)

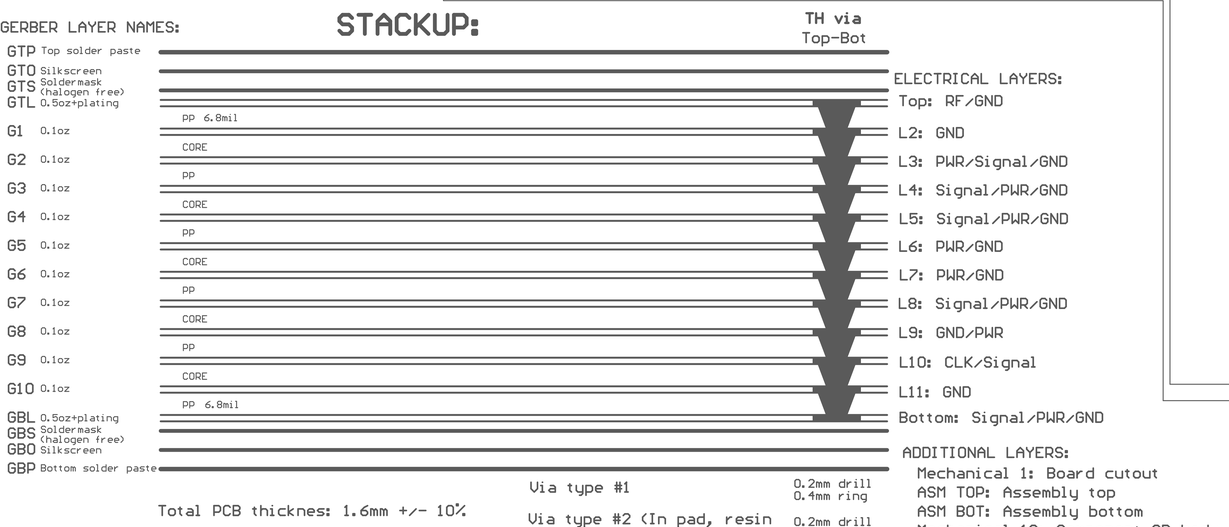
PCIe (Bottom)

85 Ohm coupled microstrip line (Bottom layer, PCI traces) characteristics:
Bottom layer copper foil thickness: 17.5 um
Track width = 0.25 mm (9.84 mils)
Track spacing = 0.1 mm (3.93 mils)
Track width/spacing ratio = 2.5
Dielectric thickness from L11 to Bottom layer = 173um (6.8 mils)
Dielectric between L11 layer and Bottom layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 85 Ohms (+/- 10% tolerance)



STACKUP:



Total PCB thickness: 1.6mm +/- 10%

Via type #1 — 0.2mm drill, 0.4mm ring

Via type #2 (In pad, resin filled with metal cap) — 0.2mm drill, 0.35mm ring

ADDITIONAL LAYERS:
Mechanical 1: Board cutout
ASM TOP: Assembly top
ASM BOT: Assembly bottom
Mechanical 13: Component 3D body

VERY IMPORTANT NOTES:

1) 0.35mm ring and 0.2mm drill via-in-pads (IC1) must be resin filled with metal cap
2) Solder mask : DARK BLUE, both sides, halogen free, glossy finish (NOT matte)
3) Silkscreen : white epoxy ink, halogen free, both sides. No silkscreen on pads.
4) DRCs must be run on Gerber files before building boards
5) Hole diameters are final manufactured diameters INCLUDING HOLE METALIZATION.
6) Minimum track spacing: 0.1 mm
   Minimum track width: 0.1 mm
7) There are plated and non-plated holes on the PCB
8) Material:
   IT-180A
   PCB vendor to silkscreen UL and RoHS compliance marks, vendor logo and date code on bottom where shown
   Copper weight: External layers 0.5 oz+plating
   Internal layers 1 oz
9) Electrical test : 100 % netlist.
10) Boards are to be individually bagged.
11) PCI EXPRESS pads (top and bottom) - 30 micro inches of gold over 50 micro inches nickel plating
12) Board edge below PCI pads must be chamfered (as shown). Edges must be free of cutting burrs
13) Assembly note: Assembly house MUST provide notes in paper with shipped board if there were any changes during assembly and the board is not assembled 100% according to BOM and P&P files. Note example:

Part	Initial BOM asm. note	Status on board	Comment
R1	FIT	NF	Not mounted due to bad footprint
IC5	FIT	NF	Not mounted due to part shortage