Lime Microsystems Limited

Surrey Technology Centre
Occam Road
The Surrey Research Park
Guildford, Surrey GU2 7YG
United Kingdom

Tel: +44 (0) 1483 685 063
e-mail: enquiries@limemicro.com

LimeSDR-PCIe

- FPGA Gateware Description-

Version: 1.0 Last modified: 12/07/2018

REVISION HISTORY

The following table shows the revision history of this document:

Date	Version	Description of Revisions
09/07/2018	1.0	Initial version

Table of Contents

1 Introduction

This document contains functional description of FPGA gateware project suited for LimeSDR-PCIe board.

FPGA project - LimeSDR-PCIe_lms7_trx project can be downloaded from GitHub repository https://github.com/myriadrf/LimeSDR-PCIe_GW.

Required hardware – LimeSDR-PCIe v1.3 board.

Development software – project is created with Altera Quartus prime, Version 15.1.2 Build 193 02/01/2016 SJ Lite Edition with Cyclone IV GX device support. Mentioned software edition is free and can be downloaded from (https://www.altera.com). Although other Altera Quartus prime software versions supporting Cyclone IV GX family might work as well but it is recommended to use same version as project was created.

2 FPGA gateware features

Gateware contains following features:

- Interface to LMS7002 LimeLight^{TM} digital IQ interface in TRXIQ double data rate mode;
- Real time data transfer between host and LMS7002 chip;
- PCIe interface for transferring data between host and FPGA;
- TX samples synchronization with RX samples time stamp;
- SPI connection between LMS7002 chip and other on-board devices;
- Reconfigurable PLL blocks for LMS7002 clocking;
- Internal SPI registers for FPGA control.

3 Gateware description

This chapter describes main modules of LimeSDR-PCIe_lms7_trx project.

3.1 Main block diagram

Cyclone IV FPGA provides FIFO interface with PCIe. There are two endpoints (F2H_C0 – FPGA to Host and H2F_C0 – Host to FPGA) implemented for control data and two endpoints for stream data (H2F_S0 – Host to FPGA and F2H_S0 – FPGA to Host). Control endpoints are connected to NIOS II softcore processor which provides SPI and I2C communication interfaces for LMS7002M chip, TCXO DAC, ADF4002 phase detector, LM75 temperature sensor, Si5351C clock generator. NIOS also provides access to internal SPI configuration registers. Stream endpoints are dedicated for receiving and sending IQ data from/to LMS7002M. **Figure 1** contains top block diagram with main modules. Description of main FPGA instances can be found in **Table 1**.

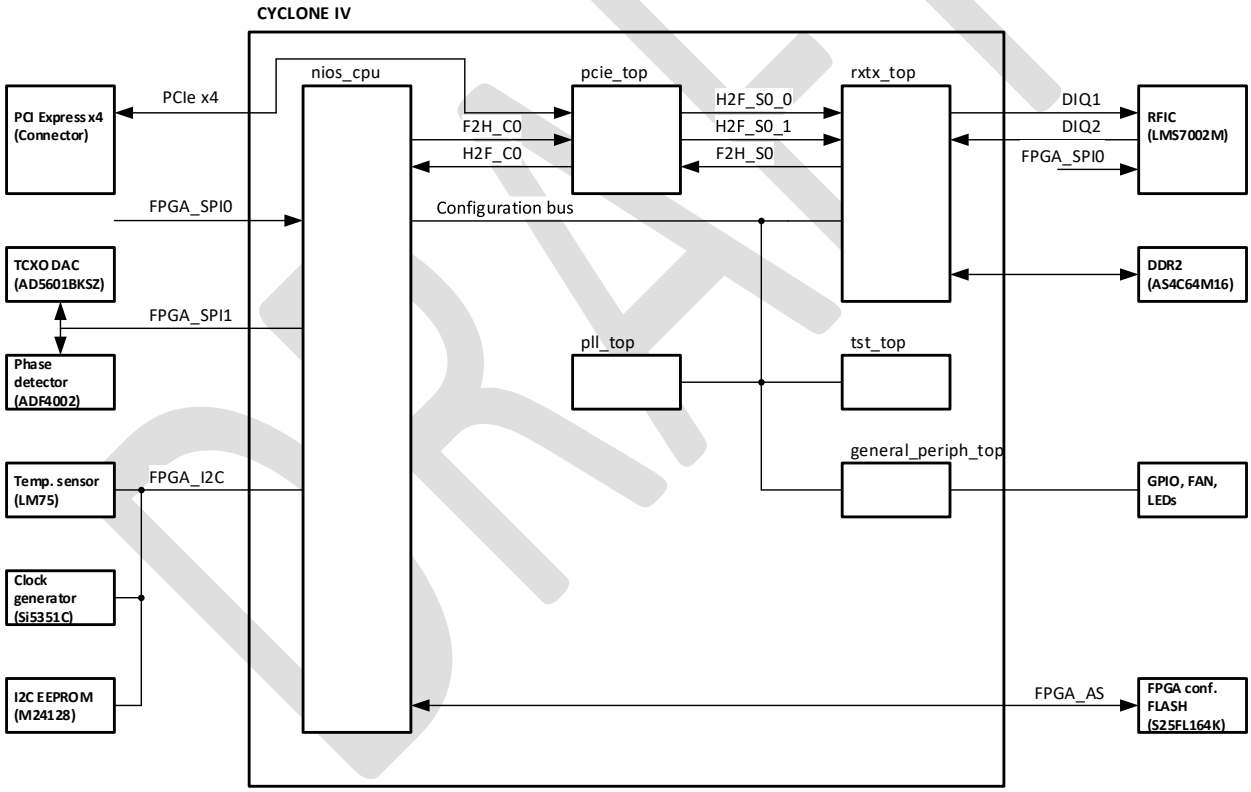

Figure 1 Top block diagram

Table 1 Description of main instances

Instance	Description
nios_cpu	NIOS II softcore processor with memory registers. Provides periphery control. See **3.3 Softcore processor – nios_cpu.**
pcie_top	Provides data transfer between external host and FPGA through PCIe interface See **3.4 PCIe interface – pcie_top.**

Instance	Description
rxtx_top	Receive and transmit logic between FPGA and external LMS7002 transceiver. See **3.5 LMS7002 Receive and transmit interface – rxtx_top.**
general_periph_top	Control module for onboard periphery such as LEDs, GPIO, FAN. See **3.6 General periphery – general_periph_top.**
pll_top	Module provides required clocks for rxtx_top module. See **3.7 PLL module – pll_top**
tst_top	Board test logic to test external DDR2 memory and external clocks. See **3.8 Board test module – tst_top.**

3.2 Clock network

Figure 2 shows dataflow between main modules and clocking scheme. More details can be found in **Table 2**.

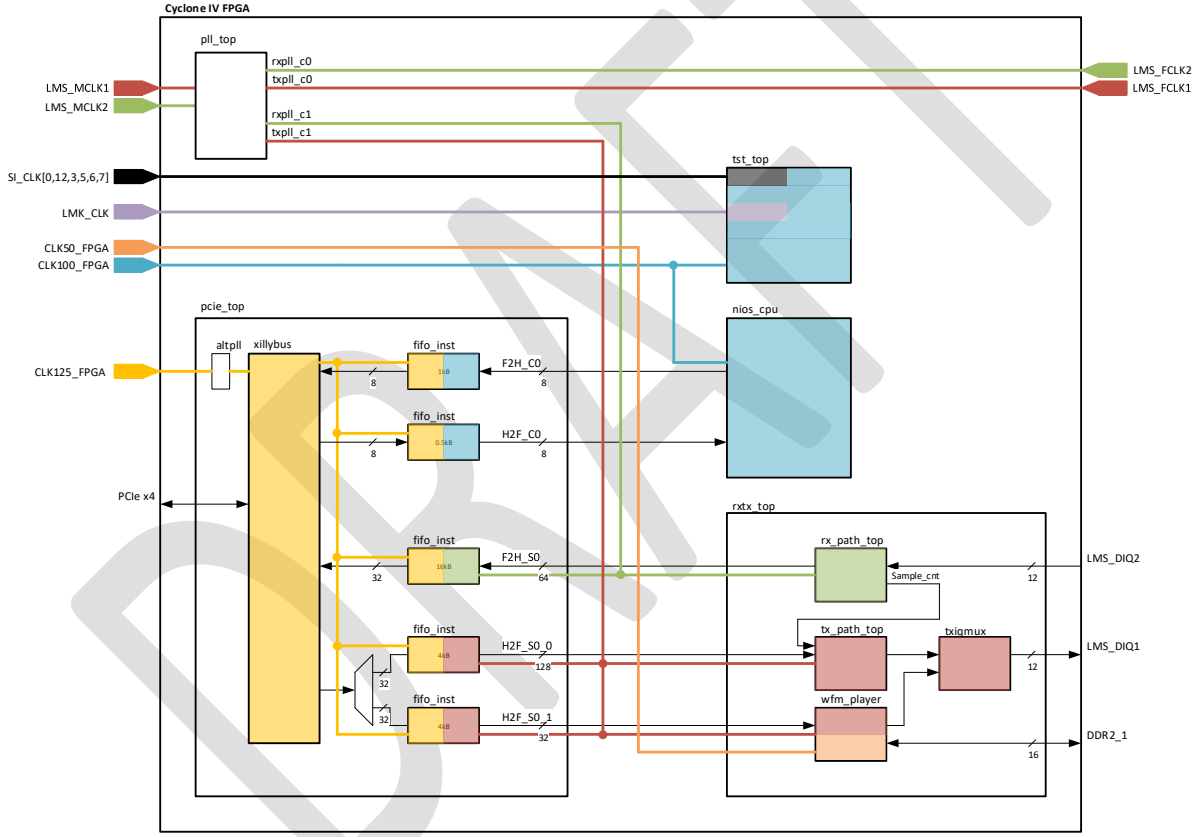

Figure 2 Gateware clock network

Table 2 Clock network description

Clock name	Frequency, MHz	Description
LMS_MCLK1	Configurable	Sample clock from LMS7002M IC. Used as a reference clock for TXPLL.
LMS_MCLK2	Configurable	Sample clock from LMS7002M IC. Used as a reference clock for RXPLL.
LMS_FCLK1	Configurable	Sample clock, LMS7002M IC latches LMS_DIQ1 bus signals using this clock.
LMS_FCLK2	Configurable	Not used

Clock name	Frequency, MHz	Description
txpll_c1	Configurable	FPGA launches LMS_DIQ1 bus signals using this clock. Used for clocking FPGA TX modules.
rxpll_c1	Configurable	FPGA latches LMS_DIQ2 bus signals using this clock. Used for clocking FPGA RX modules.
LMK_CLK	30.72	Reference clock from LMK00105 clock buffer.
CLK50_FPGA	50	External oscillator, used for DDR2_1 memory controller.
CLK100_FPGA	100	External oscillator, used for NIOS CPU.
CLK125_FPGA	125	External oscillator, used for PCIe controller.
SI_CLK0	27	Connected only to tst_top module
SI_CLK1	27	
SI_CLK2	27	
SI_CLK3	27	
SI_CLK5	27	
SI_CLK6	27	
SI_CLK7	27	

3.3 Softcore processor – nios_cpu

Figure 3 shows block diagram of nios_cpu module. This module contains softcore ALTERA NIOS II CPU and user accessible configuration registers for other modules. More detailed description can be found in **Table 3**. Module generic parameters are explained in **Table 4** and ports are described in **Table 5**.

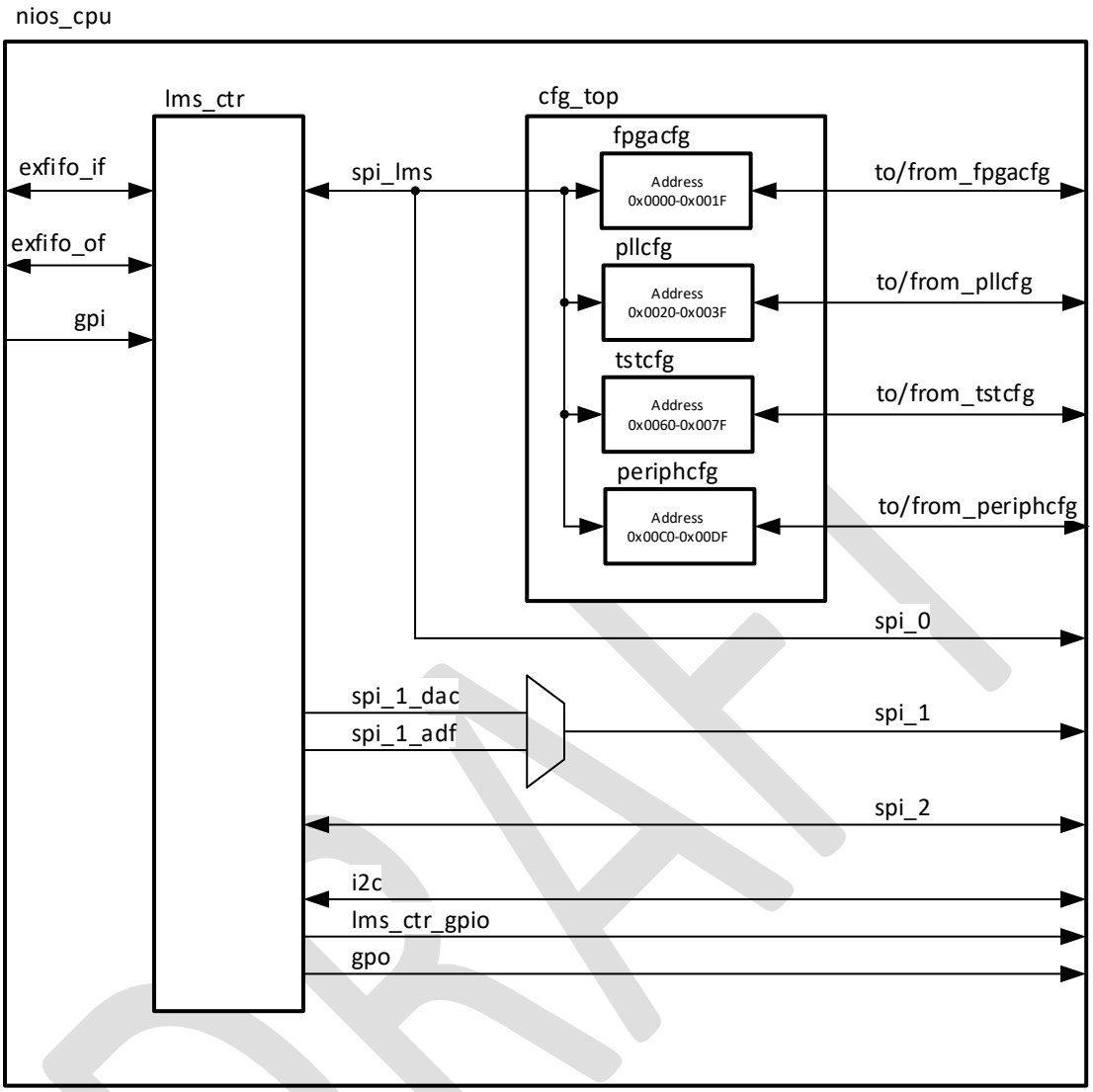

Figure 3 nios_cpu block diagram

Table 3 Description of nios_cpu instances

Instance	Description
lms_ctr	NIOS II softcore processor instance. Processor constantly monitors input FIFO buffer connected to *exfifo_if* ports and reads one packet containing 64 bytes. See **LMS64C control protocol** document for protocol description and command list. NIOS CPU executes received command and writes 64 bytes response packet to FIFO buffer connected to *exfifo_of* ports.
cfg_top	Wrapper module for SPI configuration registers.
fpgacfg	General configuration 32x16b addressable registers. Address range 0x0000 - 0x001F. See **Table 6** for register description.
pllcfg	PLL configuration registers. Address range 0x0020 - 0x003F. See **Table 7** for register description.
tstcfg	Test module configuration registers. Address range 0x0060 - 0x007F. see **Table 8** for register description.

Instance	Description
periphcfg	Peripheral configuration registers. Address range 0x0020 - 0x003F. See **Table 9** for register description.

Table 4 nios_cpu module parameters

Parameter	Type	Default	Description
Start address of SPI registers			
FPGACFG_START_ADDR	integer	0	Start address of SPI register modules. Has to be multiple of 32
PLLCFG_START_ADDR	integer	32	
TSTCFG_START_ADDR	integer	64	
PERIPHCFG_START_ADDR	integer	192	

Table 5 nios_cpu module ports

Port	Type	Width	Description
clk	in	1	Free running clock. 100MHz
reset_n	in	1	Asynchronous, active low reset
Control data FIFO			
exfifo_if_d	in	32	External control input FIFO data
exfifo_if_rd	out	1	External control input FIFO read request
exfifo_if_rdempty	in	1	External control input FIFO read empty
exfifo_of_d	out	32	External control output FIFO data
exfifo_of_wr	out	1	External control output FIFO write request
exfifo_of_wrfull	in	1	External control output FIFO write full
exfifo_of_rst	out	1	External control output FIFO reset request, active high
SPI 0			
spi_0_MISO	in	1	SPI 0 master input
spi_0_MOSI	out	1	SPI 0 master output
spi_0_SCLK	out	1	SPI 0 clock
spi_0_SS_n	out	5	SPI 0 slave select. spi_0_SS_n[0] - connected to LMS7002, spi_0_SS_n[1] - to internal SPI modules
SPI 1			
spi_1_MISO	in	1	SPI 1 master input
spi_1_MOSI	out	1	SPI 1 master output
spi_1_SCLK	out	1	SPI 1 clock
spi_1_SS_n	out	2	SPI 1 slave select. spi_1_SS_n[0] - connected to onboard TCXO DAC, spi_1_SS_n[1] - to phase detector ADF4002
SPI 2			
spi_2_MISO	in	1	SPI 2 master input
spi_2_MOSI	out	1	SPI 2 master output
spi_2_SCLK	out	1	SPI 2 clock

Port	Type	Width	Description
spi_2_SS_n	out	1	spi_2_SS_n - connected to external FPGA configuration flash
I2C			
i2c_scl	inout	1	I2C bus clock, connected to temperature sensor and EEPROM memory.
i2c_sda	inout	1	I2C bus data, connected to temperature sensor and EEPROM memory.
Genral purpose I/O			
gpi	in	8	Not used
gpo	out	8	gpo[0] - indicates NIOS activity. 0 - Idle, 1 - Busy. gpo[7-1] - not used
LMS7002 control			
lms_ctr_gpio	out	4	lms_ctr_gpio[0] - LMS7002 reset. lms_ctr_gpio{3-1] - not used
Configuration registers			
from_fpgacfg	out	512	Input/output ports from/to SPI configuration registers
to_fpgacfg	in	512	
from_pllcfg	out	512	
to_pllcfg	in	512	
from_tstcfg	out	512	
to_tstcfg	in	512	
to_tstcfg_from_rxtx	in	512	
to_periphcfg	in	512	
from_periphcfg	out	512	

3.3.1 Registers of fpgacfg module

Table 6 Register description of fpgacfg module

Address	Def. value	Bits	Name	Description
0x0000		**Board identification number**		
		15-0	**Board ID**	LimeSDR-PCIe (**Default 000F**)
0x0001		**Gateware version control**		
		15-0	**GW_VER**	Gatewate version number
0x0002		**Gateware revision control**		
		15-0	**GW_REV**	Gateware revision number
0x0003		**Board version control**		
		15-7	Reserved	
		6-4	**BOM_VER**	Bill of material version
		3-0	**HW_VER**	Hardware version.
0x0004	0000	15-0	Reserved	
0x0005	0000	**Clock source selection for TX and RX interfaces**		
		15-2	Reserved	
		1	**DRCT_CLK_EN**	RX clk: 0 - PLL source **(Default)** 1 - Direct clock source
		0		TX clk:

Address	Def. value	Bits	Name	Description
				0 - PLL source **(Default)** 1 - Direct clock source
0x0006	0000	15-0	Reserved	
0x0007	0303	**RX TX MIMO Channel control**		
		15-10	Reserved	
		9	**CH_EN**	TX ch. 1: 0 - Disabled 1 - Enabled **(Default)**
		8		TX ch. 0: 0 - Disabled 1 - Enabled **(Default)**
		7-2	Reserved	
		1	**CH_EN**	RX ch. 1: 0 - Disabled 1 - Enabled **(Default)**
		0		RX ch. 0: 0 - Disabled 1 - Enabled **(Default)**
0x0008	0102	**DIQ interface control**		
		15-11	Reserved	
		10	**DLB_EN**	Not used
		9	**SYNCH_DIS**	Packets synchronization using timestamps: 0 - Enabled 1 - Disabled **(Default)**
		8	**MIMO_INT_EN**	MIMO mode: 0 - Disabled 1 - Enabled **(Default)**
		7	**TRIQ_PULSE**	TRXIQ_pulse mode: 0 - OFF **(Default)** 1 - ON
		6	**DDR_EN**	DIQ interface mode: 0 - SDR 1 - DDR **(Default)**
		5	**MODE**	Limelight port mode: 0 - TRXIQ **(Default)** 1 - JESD207 (Currently not implemented)
		4-2	Reserved	
		1-0	**SMPL_WIDTH**	Interface sample width selection: "10" - 12bit **(Default)** "01" - Do not use "00" - 16bit
0x0009	0003	**Packet control**		
		15-2	Reserved	
		1	**TXPCT_LOSS_CLR**	TX packets dropping flag clear: 0 - Normal operation **(Default)** 1 - Rising edge clears flag
		0	**SMPL_NR_CLR**	Reset timestamp: 0 - Normal operation **(Default)** 1 - Timestamp is cleared
0x000A	0000	**RX and TX module control**		
		15-10	Reserved	
		9	**TX_PTRN_EN**	Test pattern on TX: 0 - Disabled **(Default)** 1 - Enabled
		8	**RX_PTRN_EN**	Test pattern on RX: 0 - Disabled **(Default)** 1 - Enabled
		7-2	Reserved	
		1	**TX_EN**	TX chain: 0 - Disabled **(Default)** 1 - Enabled

Address	Def. value	Bits	Name	Description
		0	**RX_EN**	RX chain: 0 - Disabled **(Default)** 1 - Enabled
0x000B	0000	15-0	Reserved	
0x000C	0003	**WFM player control 1**		
		15-2	Reserved	
		1	**WFM_CH_EN**	WFM ch.1: 0 - Disabled 1 - Enabled **(Default)**
		0		WFM ch.0: 0 - Disabled 1 - Enabled **(Default)**
0x000D	0001	**WFM player control 2**		
		15-3	Reserved	
		2	**WFM_LOAD**	WFM player file load: 0 to 1 transition starts WFM file loading 0 - WFM file loading disabled **(Default)**
		1	**WFM_PLAY**	WFM player loaded file play enable: 0 - Disabled 1 - Enabled **(Default)**
		0	Reserved	
0x000E	0002	**WFM player control 3**		
		15-2	Reserved	
		1-0	**WFM_SMPL_WIDTH**	WFM player sample width control: "10" - 12bit, **(Default)** "01" - Do not use "00" - 16bit
0x000F	0000	15-0	Reserved	
0x0010	0000	15-0	Reserved	
0x0011	0000	15-0	Reserved	
0x0012	FFFF	**Controlled SPI enable**		
		15-8	Reserved	Not used
		7	**SPI_SS7**	
		6	**SPI_SS6**	
		5	**SPI_SS5**	
		4	**SPI_SS4**	
		3	**SPI_SS3**	
		2	**SPI_SS2**	
		1	**SPI_SS1**	
		0	**SPI_SS0**	
0x0013	6F6F	**LMS7002 MISC pin control**		
		15	Reserved	
		14	**LMS2_RXEN**	Not used
		13	**LMS2_TXEN**	
		12	**LMS2_TXNRX2**	
		11	**LMS2_TXNRX1**	
		10	**LMS2_CORE_LDO_EN**	
		9	**LMS2_RESET**	
		8	**LMS2_SS**	
		7	Reserved	
		6	**LMS1_RXEN**	RX hard enable: 0 - Disabled 1 - Enabled **(Default)**
		5	**LMS1_TXEN**	TX hard enable: 0 - Disabled 1 - Enabled **(Default)**
		4	**LMS1_TXNRX2**	Port 2 mode selection: 0 - TXIQ **(Default)** 1 - RXIQ
		3	**LMS1_TXNRX1**	Port 1 mode selection: 0 - TXIQ

Address	Def. value	Bits	Name	Description
				1 - RXIQ (**Default)**
		2	**LMS1_CORE_LDO_EN**	Internal LDO control: 0 - Disabled **(Default)** 1 - Enabled
		1	**LMS1_RESET**	Hardware reset: 0 - Reset activated 1 - Reset inactive **(Default)**
		0	**LMS1_SS**	Not used
0x0014	0000	15-0	Reserved for lms3_4	
0x0015	0000	15-0	Reserved for lms5-6	
0x0016	0000	15-0	Reserved for lms7-8	
0x0017	0000	**GPIO for external periphery**		
		15-14	Reserved	
		13	**GPIO13**	Not used
		12	**GPIO12**	
		11	**GPIO11**	
		10	**GPIO10**	
		9	**GPIO9**	
		8	**GPIO8**	
		7	**GPIO7**	
		6	**GPIO6**	Ch. B shunt: 0 - Disabled 1 - Enabled **(Default)**
		5	**GPIO5**	Ch. B attenuator 0 - Disabled **(Default)** 1 - Enabled
		4	**GPIO4**	RF loopback ch. B: 0 - Disabled **(Default)** 1 - Enabled
		3	**GPIO3**	Reserved
		2	**GPIO2**	Ch. A shunt: 0 - Disabled 1 - Enabled **(Default)**
		1	**GPIO1**	Ch. A attenuator: 0 - Disabled **(Default)** 1 - Enabled
		0	**GPIO0**	RF loopback ch. A: 0 - Disabled **(Default)** 1 - Enabled
0x0018	0001	15-1	Reserved	
		0	**DEV_CTRL0**	Not used
0x0019		15-0	Reserved	
0x001A	0000	**Onboard led control**		
		15	Reserved	
		14	Reserved	
		13	Reserved	
		12	Reserved	
		11	Reserved	
		10	Reserved	
		9	Reserved	
		8	Reserved	
		7	Reserved	
		6	**FPGA_LED2_G**	Green LED2 control, do not turn on while red LED2 is on: 0 - OFF **(Default)** 1 - ON
		5	**FPGA_LED2_R**	Red LED2 control, do not turn on while green LED2 is on: 0 - OFF **(Default)** 1 - ON
		4	**FPGA_LED2_OVRD**	LED2 control override: 0 - OFF **(Default)** 1 - ON

Address	Def. value	Bits	Name	Description
		3	Reserved	
		2	**FPGA_LED1_G**	Green LED1 control, do not turn on while red LED1 is on: 0 - OFF **(Default)** 1 - ON
		1	**FPGA_LED1_R**	Red LED1 control, do not turn on while green LED1 is on: 0 - OFF **(Default)** 1 - ON
		0	**FPGA_LED1_OVRD**	LED1 control override: 0 - OFF **(Default)** 1 - ON
0x001B	0000	15-8	Reserved	
		7	Reserved	
		6	Reserved	
		5	Reserved	
		4	Reserved	
		3	Reserved	
		2	Reserved	
		1	Reserved	
		0	Reserved	
0x001C	0000	15-3	Reserved	Onboard led control
		2	**FX3_LED_G**	Green FX3 control, do not turn on while red FX3 is on: 0 - OFF **(Default)** 1 - ON
		1	**FX3_LED_R**	Red FX3 control, do not turn on while green FX3 is on: 0 - OFF **(Default)** 1 - ON
		0	**FX3_LED_OVRD**	FX3 control override: 0 - OFF **(Default)** 1 - ON
0x001D	0000	15-0	Reserved	
0x001E	0000	15-0	Reserved	
0x001F	0000	15-0	Reserved	

3.3.2 Registers of pllcfg module

Table 7 Register description of pllcfg module

Address	Def. value	Bits	Name	Description
0x0020	0000	15-0	Reserved	
0x0021	0001	**PLL configuration status**		
		15-4	Reserved	
		3	**AUTO_PHCFG_ERR**	Auto phase configuration error status: 0 – no error 1 – Error
		2	**AUTO_PHCFG_DONE**	Auto phase configuration status: 0 – Not done 1 – Done
		1	**BUSY**	PLL reconfiguration busy status: 0 – Idle 1 – Busy
		0	**DONE**	PLL configuration status: 0 – Not done 1 – Done
0x0022	0000	**PLL lock status**		
		15-2	Reserved	
		1	**PLL_LOCK**	RX PLL: 0 – No lock 1 – Locked

Address	Def. value	Bits	Name	Description
		0		TX PLL: 0 – No lock 1 – Locked
0x0023	0000	**PLL control**		
		15	Reserved	
		14	**PHCFG_MODE**	PLL phase configuration mode: 0 - Manual 1 - AUTO
		13	**PHCFG_UpDn**	Phase shift direction: 0 - Down 1 - Up
		12-8	**CNT_IND**	Counter index for phase shift: 0000 - All output counters 0001 - M counter 0010 - C0 counter 0011 - C1 counter
		7-3	**PLL_IND**	PLL index for reconfiguration: 0000 - TX PLL 0001 - RX PLL Do not use other index values
		2	**PLLRST_START**	Reset bit for PLL: 0 - Reset inactive 0 to 1 transition triggers reset for PLL with selected index
		1	**PHCFG_START**	Phase shift start: 0 - Phase shift process inactive 0 to 1 - transition triggers phase shift process for PLL with selected indexes
		0	**PLLCFG_START**	PLL reconfiguration start: 0 - Phase shift process inactive 0 to 1 - transition triggers phase shift process for PLL with selected indexes
0x0024	0000	**PLL reconfiguration settings**		
		15-0	**CNT_PHASE**	Counter phase value
0x0025	01F0	15	Reserved	
		14-11	**PLLCFG_BS**	Bandwidth setting (Not used)
		10-8	**CHP_CURR**	PLL charge Pump Current (1)
		7	**PLLCFG_VCODIV**	PLL VCO division value 0 = 2 1 = 1
		6-2	**PLLCFG_LF_RES**	PLL Loop filter resistance (1)
		1-0	**PLLCFG_LF_CAP**	PLL Loop filter capacitance (1)
0x0026	0001	15-4	Reserved	Counter bypass and odd division control bits (1)
		3	**M_ODDDIV**	
		2	**M_BYP**	
		1	**N_ODDDIV**	
		0	**N_BYP**	
0x0027	555A	15	**C7_ODDDIV**	
		14	**C7_BYP**	
		13	**C6_ODDDIV**	
		12	**C6_BYP**	
		11	**C5_ODDDIV**	
		10	**C5_BYP**	
		9	**C4_ODDDIV**	
		8	**C4_BYP**	
		7	**C3_ODDDIV**	
		6	**C3_BYP**	
		5	**C2_ODDDIV**	
		4	**C2_BYP**	
		3	**C1_ODDDIV**	
		2	**C1_BYP**	
		1	**C0_ODDDIV**	

Address	Def. value	Bits	Name	Description
		0	**C0_BYP**	
0x0028	5555	15	**C15_ODDDIV**	
		14	**C15_BYP**	
		13	**C14_ODDDIV**	
		12	**C14_BYP**	
		11	**C13_ODDDIV**	
		10	**C13_BYP**	
		9	**C12_ODDDIV**	
		8	**C12_BYP**	
		7	**C11_ODDDIV**	
		6	**C11_BYP**	
		5	**C10_ODDDIV**	
		4	**C10_BYP**	
		3	**C9_ODDDIV**	
		2	**C9_BYP**	
		1	**C8_ODDDIV**	
		0	**C8_BYP**	
0x0029		15-0	Reserved	
0x002A	0000	15-8	**N_HCNT[15:8]**	N counter values (1)
		7-0	**N_LCNT[7:0]**	
0x002B	0000	15-8	**M_HCNT[15:8]**	M counter values (1)
		7-0	**M_LCNT[7:0]**	
0x002C	0000	15-0	**M_FRAC[15:0]**	M fractional counter values (Only for fractional PLL) (1)
0x002D	0000	15-0	**M_FRAC[31:16]**	
0x002E	0000	15-8	**C0_HCNT[15:8]**	C0 counter values (1)
		7-0	**C0_LCNT[7:0]**	
0x002F	0000	15-8	**C1_HCNT[15:8]**	C1 counter values (1)
		7-0	**C1_LCNT[7:0]**	
0x0030	0000	15-8	**C2_HCNT[15:8]**	C2counter values (1)
		7-0	**C2_LCNT[7:0]**	
0x0031	0000	15-8	**C3_HCNT[15:8]**	C3 counter values (1)
		7-0	**C3_LCNT[7:0]**	
0x0032	0000	15-8	**C4_HCNT[15:8]**	C4 counter values (1)
		7-0	**C4_LCNT[7:0]**	
0x0033	0000	15-8	**C5_HCNT[15:8]**	C5 counter values (1)
		7-0	**C5_LCNT[7:0]**	
0x0034	0000	15-8	**C6_HCNT[15:8]**	C6 counter values (1)
		7-0	**C6_LCNT[7:0]**	
0x0035	0000	15-8	**C7_HCNT[15:8]**	C7 counter values (1)
		7-0	**C7_LCNT[7:0]**	
0x0036	0000	15-8	**C8_HCNT[15:8]**	C8 counter values (1)
		7-0	**C8_LCNT[7:0]**	
0x0037	0000	15-8	**C9_HCNT[15:8]**	C9 counter values (1)
		7-0	**C9_LCNT[7:0]**	
0x0038		15-0	Reserved	Reserved for C10-C15 counter values
0x0039		15-0	Reserved	
0x003A		15-0	Reserved	
0x003B		15-0	Reserved	
0x003C		15-0	Reserved	
0x003D		15-0	Reserved	
0x003E	0FFF	**Auto phase shift options**		
			AUTO_PHCFG_SMPLS	Samples to compare in auto phase shift mode
0x003F	0002		**AUTO_PHCFG_STEP**	Step size for auto phase

Note 1: For detailed description see “Cyclone IV Device Handbook”, Chapter 5. Clock Networks and PLLs in Cyclone IV Devices.

3.3.3 Registers of tstcfg module

Table 8 Register description of tstcfg module

Address	Def. value	Bits	Type	Name	Description
0x0060	00F0	**SPI signature**			
		15-8		Reserved	
		7-4	R	**SPI_SIGN_REZULT**	Inverted bits from SPI_SIGN register
		3-0	R/W	**SPI_SIGN**	SPI module test register.
		Test enable			
0x0061	0000	15-6		Reserved	
		5	R/W	**DDR2_2_TST_EN**	DDR2_2 memory test: 0 - Disabled **(Default)** 1 - Enabled
		4	R/W	**DDR2_1_TST_EN**	DDR2_2 memory test: 0 - Disabled **(Default)** 1 - Enabled
		3	R/W	**ADF_TST_EN**	Phase detector test: 0 - Disabled **(Default)** 1 - Enabled
		2	R/W	**VCTCXO_TST_EN**	VCTCXO test: 0 - Disabled **(Default)** 1 - Enabled
		1	R/W	**Si5351C_TST_EN**	Si5351C clock test: 0 - Disabled **(Default)** 1 - Enabled
		0	R/W	**FX3_PCLK_TST_EN**	FX3 PCLK clock test: 0 - Disabled **(Default)** 1 - Enabled
0x0062				Reserved	
0x0063	0000	**Error insertion**			
		15-6		Reserved	
		5	R/W	**DDR2_2_TST_FRC_ERR**	DDR2_2 insert error to memory test: 0 - Disabled **(Default)** 1 - Enabled
		4	R/W	**DDR2_1_TST_FRC_ERR**	DDR2_1 insert error to memory test: 0 - Disabled **(Default)** 1 - Enabled
		3	R/W	**ADF_TST_FRC_ERR**	Insert error to phase detector test: 0 - Disabled **(Default)** 1 - Enabled
		2	R/W	**VCTCXO_TST_FRC_ERR**	Insert error to VCTCXO test: 0 - Disabled **(Default)** 1 - Enabled
		1	R/W	**Si5351C_TST_FRC_ERR**	Insert error to Si5351C clock test: 0 - Disabled **(Default)** 1 - Enabled
		0	R/W	**FX3_PCLK_TST_FRC_ERR**	Insert error to FX3 PCLK clock test: 0 - Disabled **(Default)** 1 - Enabled
0x0064				Reserved	
0x0065	0000	**Test status**			
		15-6		Reserved	
		5	R	**DDR2_2_TST_CMPLT**	DDR2_2 test status: 0 - Not completed 1 - Completed
		4	R	**DDR2_1_TST_CMPLT**	DDR2_1test status: 0 - Not completed 1 - Completed
		3	R	**ADF_TST_CMPLT**	Phase detector test status: 0 - Not completed 1 - Completed
		2	R	**VCTCXO_TST_CMPLT**	VCTCXO test status: 0 - Not completed 1 - Completed

Address	Def. value	Bits	Type	Name	Description
		1	R	**Si5351C_TST_CMPLT**	Si5351C clock test status: 0 - Not completed 1 - Completed
		0	R	**FX3_PCLK_TST_CMPLT**	FX3 PCLK clock test status: 0 - Not completed 1 - Completed
0x0066				Reserved	
		Test results			
0x0067	0000	15-6		Reserved	
		5	R	**DDR2_2_TST_REZ**	DDR2_2 test result: 0 - Fail 1 - Pass
		4	R	**DDR2_1_TST_REZ**	DDR2_1 test result: 0 - Fail 1 - Pass
		3	R	**ADF_TST_REZ**	Not used
		2	R	**VCTCXO_TST_REZ**	Not used
		1	R	**Si5351C_TST_REZ**	Not used
		0	R	**FX3_PCLK_TST_REZ**	Not used
		Clock test counter values			
0x0068				Reserved	
0x0069			R	**FX3_CLK_CNT**	FX3 PCLK clock counter value
0x006A			R	**Si5351C_CLK0_CNT**	Si5351C CLK0 counter value
0x006B			R	**Si5351C_CLK1_CNT**	Si5351C CLK1 counter value
0x006C			R	**Si5351C_CLK2_CNT**	Si5351C CLK2 counter value
0x006D			R	**Si5351C_CLK3_CNT**	Si5351C CLK3 counter value
0x006E				Reserved	
0x006F			R	**Si5351C_CLK5_CNT**	Si5351C CLK5 counter value
0x0070			R	**Si5351C_CLK6_CNT**	Si5351C CLK6 counter value
0x0071			R	**Si5351C_CLK7_CNT**	Si5351C CLK7 counter value
0x0072			R	**LMK_CLK_CNT_L**	LMK clock counter value
0x0073			R	**LMK_CLK_CNT_H**	
0x0074			R	**ADF_CNT**	ADF transition count value
0x0075				Reserved	
		DDR2_1 detailed test results 1			
0x0076		15-3		Reserved	
		2	R	**DDR2_1_TST_FAIL**	DDR2_1 test result: 0 - Test not completed 1 - Fail
		1	R	**DDR2_1_TST_PASS**	DDR2_1 test result: 0 - Test not completed 1 - Pass
		0	R	**DDR2_1_TST_CMPLT**	DDR2_1 test result: 0 - Test not completed 1 - Test complete
0x0077		**DDR2_1 detailed test results 2**			
		15-0	R	**DDR2_1_PNF_PER_BIT_L**	DDR2_1 data [15:0] bus pas not fail per bit: 0 - Fail 1 - Pass
0x0078		**DDR2_1 detailed test results 3**			
		15-0	R	**DDR2_1_PNF_PER_BIT_H**	DDR2_1 data [31:16] bus pas not fail per bit: 0 - Fail 1 - Pass
0x0079		15-0		Reserved	
0x007A		**DDR2_2 detailed test results 1**			
		15-3		Reserved	
		2	R	**DDR2_2_TST_FAIL**	DDR2_2 test result: 0 - Test not completed 1 - Fail
		1	R	**DDR2_2_TST_PASS**	DDR2_2 test result:

Address	Def. value	Bits	Type	Name	Description
					0 - Test not completed 1 - Pass
		0	R	**DDR2_2_TST_CMPLT**	DDR2_2 test result: 0 - Test not completed 1 - Test complete
0x007B		**DDR2_2 detailed test results 2**			
		15-0	R	**DDR2_2_PNF_PER_BIT_L**	DDR2_2 data [15:0] bus pas not fail per bit: 0 - Fail 1 - Pass
0x007C		**DDR2_2 detailed test results 3**			
		15-0	R	**DDR2_2_PNF_PER_BIT_H**	DDR2_2 data [31:16] bus pas not fail per bit: 0 - Fail 1 - Pass
0x007D	AAAA	**TX test pattern 1**			
		15-0	R/W	**TX_TST_I**	TX test pattern I sample value
0x007E	5555	**TX test pattern 2**			
		15-0	R/W	**TX_TST_Q**	TX test pattern Q sample value
0x007F		15-0		Reserved	

3.3.4 Registers of periphcfg module

Table 9 Register description of periphcfg module

Address	Def. value	Bits	Type	Name	Description
0x00C0	FFFF	**Board GPIO control 1**			
		15-8		Reserved	
		7-0	**R/W**	**BOARD_GPIO_OVRD**	GPIO control override (each bit controls corresponding GPIO): 0 - Dedicated function 1 - Overridden by user **(Default)**
0x00C1		15-0		Reserved for GPIO	
0x00C2	0000	**Board GPIO control 2**			
		15-8		Reserved	
		7-0	**R**	**BOARD_GPIO_RD**	GPIO read value (each from corresponding GPIO): 0 - Low level 1 - High level
0x00C3		15-0		Reserved for GPIO	
0x00C4	0000	**Board GPIO control 3**			
		15-8		Reserved	
		7-0	**R/W**	**BOARD_GPIO_DIR**	Onboard GPIO direction (each bit controls corresponding GPIO): 0 - Input **(Default)** 1 - Output
0x00C5		15-0		Reserved for GPIO	
0x00C6	0000	**Board GPIO control 4**			
		15-8		Reserved	
		7-0	**R/W**	**BOARD_GPIO_VAL**	GPIO output value (each bit controls corresponding GPIO): 0 - Low level 1 - High level
0x00C7		15-0		Reserved for GPIO	
0x00C8	0000	15-0		**PERIPH_INPUT_RD_0**	Not used
0x00C9	0000	15-0		**PERIPH_INPUT_RD_1**	Not used
0x00CA		15-0		Reserved	
0x00CB		15-0		Reserved	
0x00CC	0000	**Board peripheral control 1**			
		15-1		**PERIPH_OUTPUT_OVRD_0**	Not used
		0	**R/W**		Fan control override:

					0 - Dedicated function **(Default)** 1 - User controlled
0x00CD	0000	**Board peripheral control 1**			
		15-1		**PERIPH_OUTPUT_VAL_0**	Not used
		0	**R/W**		Fan control pin: 0 - OFF **(Default)** 1- ON
0x00CE	0000	15-0		**PERIPH_OUTPUT_OVRD_1**	Not used
0x00CF	0000	15-0		**PERIPH_OUTPUT_VAL_1**	Not used
0x00D0		15-0		Reserved	
0x00D1		15-0		Reserved	
0x00D2		15-0		Reserved	
0x00D3		15-0		Reserved	
0x00D4		15-0		Reserved	
0x00D5		15-0		Reserved	
0x00D6		15-0		Reserved	
0x00D7		15-0		Reserved	
0x00D8		15-0		Reserved	
0x00D9		15-0		Reserved	
0x00DA		15-0		Reserved	
0x00DB		15-0		Reserved	
0x00DC		15-0		Reserved	
0x00DD		15-0		Reserved	
0x00DE		15-0		Reserved	
0x00DF		15-0		Reserved	

3.4 PCIe interface – pcie_top

Provides data transfer between external host and FPGA trough PCIe interface.

All data exchange between pcie_top module and other FPGA logic is done through FIFO buffers. Module xillybus constantly monitors all FIFO buffers. For example, internal logic writes IQ stream packets containing 4kB data to FIFO buffer through F2H_S0 ports. Once xillybus module detects

that F2H_S0 FIFO buffer is not empty and external host is ready, all data is read from FIFO buffer and written to host controller trough PCIe interface.

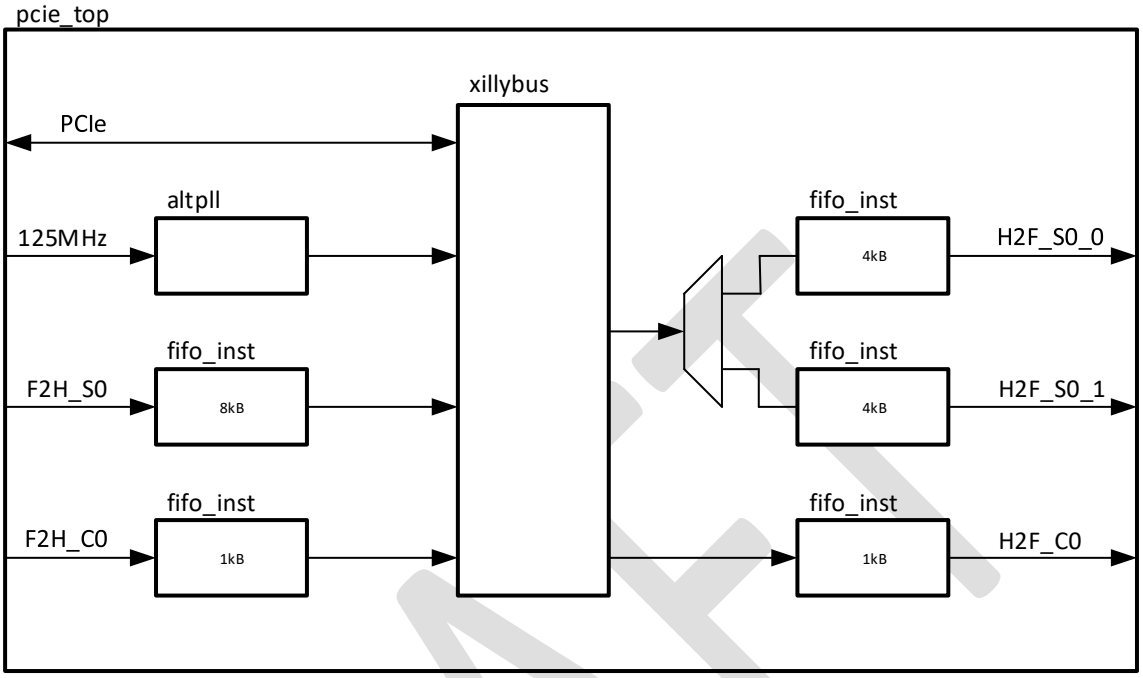

Figure 4 pcie_top block diagram

Table 10 Description of pcie_top instances

Instance	Description
xillybus	Provides data transfer between PCIe interface and internal FIFO buffers.
altpll	PLL instance, provides clocking for PCIe core
fifo_inst (F2H_S0)	Stream endpoint FIFO buffer of 8kB size.
fifo_inst (F2H_S0_0)	Stream endpoint FIFO buffer of 4kB size.
fifo_inst (F2H_S0_1)	Stream endpoint FIFO buffer of 4kB size.
fifo_inst (F2H_C0)	Control endpoint FIFO buffer of 1kB size.
fifo_inst (H2F_C0)	Control endpoint FIFO buffer of 1kB size.

Table 11 pcie_top module parameters

Parameter	Type	Default	Description
General parameters			
dev_family	string	Cyclone IV GX	Device family name
g_S0_DATA_WIDTH	integer	32	Stream interface data width
g_C0_DATA_WIDTH	integer	8	Control interface data width
Stream (PC->FPGA)			
g_H2F_S0_0_RDUSEDW_WIDTH	integer	9	Host to FPGA stream FIFO read used words size (2^{9-1}= 256 words)
g_H2F_S0_0_RWIDTH	integer	128	Host to FPGA stream FIFO read word size
g_H2F_S0_1_RDUSEDW_WIDTH	integer	11	Host to FPGA stream FIFO read used words size (2^{11-1}= 1024 words)
g_H2F_S0_1_RWIDTH	integer	32	Host to FPGA stream FIFO read word size

Parameter	Type	Default	Description
Stream (FPGA->PC)			
g_F2H_S0_WRUSEDW_WIDTH	integer	11	FPGA to host stream FIFO write used words size (2^{11-1}= 1028 words)
g_F2H_S0_WWIDTH	integer	64	FPGA to host stream FIFO write word size
Control (PC->FPGA)			
g_H2F_C0_RDUSEDW_WIDTH	integer	11	Host to FPGA control FIFO read used words size (2^{11-1}= 1024 words)
g_H2F_C0_RWIDTH	integer	8	Host to FPGA control FIFO read word size
Control (FPGA->PC)			
g_F2H_C0_WRUSEDW_WIDTH	integer	11	FPGA to host control FIFO write used words size (2^{11-1}= 1024 words)
g_F2H_C0_WWIDTH	integer	8	FPGA to host control FIFO write word size

Table 12 pcie_top module ports

Port	Type	Width	Description
inclk_125	in	1	Clock 125 MHz
reset_n	in	1	Reset active low
PCIe interface			
pcie_perstn	in	1	Link reactivation
pcie_refclk	in	1	Reference clock
pcie_rx	in	4	PCIe Receive ports
pcie_tx	out	4	PCIe Transmit ports
pcie_bus_clk	out	1	PCIe bus user interface clock
EP01 buffer select			
H2F_S0_0_sel	in	1	0 - H2F_S0_0, 1 - H2F_S0_1
Stream endpoint FIFO 0 (Host->FPGA)			
H2F_S0_0_rdclk	in	1	Read clock
H2F_S0_0_aclrn	in	1	Asynchronous clear, active low
H2F_S0_0_rd	in	1	Read request
H2F_S0_0_rdata	out	g_H2F_S0_0_RWIDTH	Read data
H2F_S0_0_rempty	out	1	Read empty
H2F_S0_0_rdusedw	out	g_H2F_S0_0_RDUSEDW_WIDTH	Red used words
Stream endpoint FIFO 1 (Host->FPGA)			
H2F_S0_1_rdclk	in	1	Read clock
H2F_S0_1_aclrn	in	1	Asynchronous clear, active low
H2F_S0_1_rd	in	1	Read request
H2F_S0_1_rdata	out	g_H2F_S0_1_RWIDTH	Read data
H2F_S0_1_rempty	out	1	Read empty
H2F_S0_1_rdusedw	out	g_H2F_S0_1_RDUSEDW_WIDTH	Red used words
Stream endpoint FIFO (FPGA->Host)			
F2H_S0_wclk	in	1	Write clock
F2H_S0_aclrn	in	1	Asynchronous clear, active low

Port	Type	Width	Description
F2H_S0_wr	in	1	Write request
F2H_S0_wdata	in	g_F2H_S0_WWIDTH	Write data
F2H_S0_wfull	out	1	Write full
F2H_S0_wrusedw	out	g_F2H_S0_WRUSEDW_WIDTH	Write used words
Control endpoint FIFO (Host->FPGA)			
H2F_C0_rdclk	in	1	Read clock
H2F_C0_aclrn	in	1	Asynchronous clear, active low
H2F_C0_rd	in	1	Read request
H2F_C0_rdata	out	g_H2F_C0_RWIDTH	Read data
H2F_C0_rempty	out	1	Read empty
Control endpoint FIFO (FPGA->Host)			
F2H_C0_wclk	in	1	Write clock
F2H_C0_aclrn	in	1	Asynchronous clear, active low
F2H_C0_wr	in	1	Write request
F2H_C0_wdata	in	g_F2H_C0_WWIDTH	Write data
F2H_C0_wfull	out	1	Write full
Status			
user_read_32_open	out	1	Indicates when stream endpoint S0 is ready.

3.5 LMS7002 Receive and transmit interface – rxtx_top

Main function of rxtx_top module is for receive and transmit IQ samples from/to LMS7002 chip and provide IQ sample synchronization. See **Figure 5** for block diagram and **Table 13** for instance description.

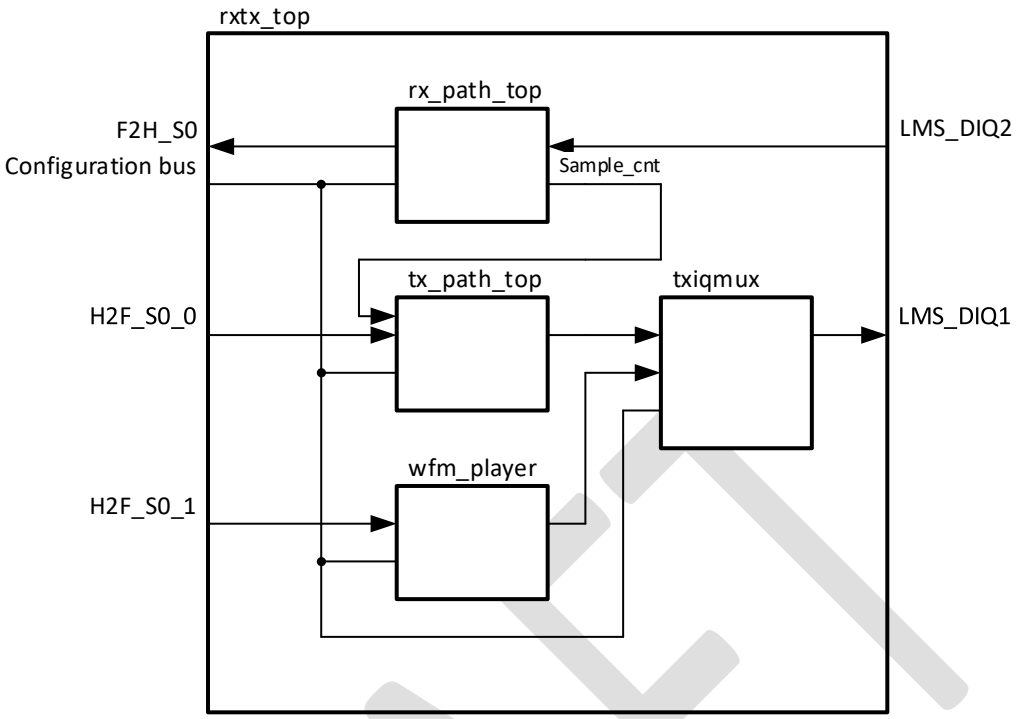

Figure 5 rxtx_top block diagram

Table 13 Description of rxtx_top instances

Instance	Description
tx_path_top	Transmit logic. See **3.5.2 Transmit interface – tx_path_top**.
wfm_player	Waveform player for LMS_DIQ1 interface
txiqmux	Mux for tx_path_top and wfm_player modules
rx_path_top	Receive logic. See **3.5.1 Receive interface – rx_path_top**.

Table 14 rxtx_top parameters description

Parameter	Type	Default	Description
DEV_FAMILY	string	Cyclone IV GX	Device family
TX parameters			
TX_IQ_WIDTH	integer	12	TX IQ sample width
TX_N_BUFF	integer	2	TX number of buffers, 2,4 valid values
TX_IN_PCT_SIZE	integer	4096	TX packet size in bytes
TX_IN_PCT_HDR_SIZE	integer	16	TX packet header size in bytes
TX_IN_PCT_DATA_W	integer	128	TX packet read data width
TX_IN_PCT_RDUSEDW_W	integer	11	TX packet read used words width
TX_OUT_PCT_DATA_W	integer	64	TX output packet data width
RX parameters			
RX_IQ_WIDTH	integer	12	RX IQ sample width
RX_INVERT_INPUT_CLOCKS	string	ON	Clock invert option on LMS_DIQ2 interface
RX_SMPL_BUFF_RDUSEDW_W	integer	11	RX sample buffer read used words width. Words=2^{11-1}
RX_PCT_BUFF_WRUSEDW_W	integer	11	RX packet buffer read used words width. Words=2^{11-1}

Parameter	Type	Default	Description
WFM			
WFM_IN_PCT_DATA_W	integer	32	WFM in packet read data width
WFM_IN_PCT_RDUSEDW_W	integer	11	WFM in packet read used words width. Words= 2^{11-1}
DDR2 controller parameters			
WFM_CNTRL_RATE	integer	1	1 - full rate, 2 - half rate
WFM_CNTRL_BUS_SIZE	integer	16	DDR2 memory data width
WFM_ADDR_SIZE	integer	25	DDR2 memory address width
WFM_LCL_BUS_SIZE	integer	64	DDR2 controller local data bus size
WFM_LCL_BURST_LENGTH	integer	2	DDR2 controller local burst length
WFM player parameters			
WFM_WFM_INFIFO_SIZE	integer	11	WFM in FIFO buffer write used words width. Words= 2^{11-1}
WFM_DATA_WIDTH	integer	32	WFM data width
WFM_IQ_WIDTH	integer	12	WFM IQ sample width

Table 15 rxtx_top port description

Port	Type	Width	Description
Configuration memory ports			
from_fpgacfg	in	t_FROM_FPGACFG;	Configuration registers bus
to_tstcfg_from_rxtx	out	t_TO_TSTCFG_FROM_RXTX;	
from_tstcfg	in	t_FROM_TSTCFG;	
TX path			
tx_clk	in	1	TX interface clock
tx_clk_reset_n	in	1	TX interface reset, active low
tx_pct_loss_flg	out	1	TX packet loss flag, 0 - No packet loss, 1 - Packet losst.
tx_txant_en	out	1	TX transmit flag. 0 - No transmission, 1 - TX is transmitting samles
TX interface data			
tx_DIQ	out	TX_IQ_WIDTH	TX samples
tx_fsync	out	1	TX sync signal
TX FIFO read ports			
tx_in_pct_reset_n_req	out	1	TX packet buffer reset request, active low
tx_in_pct_rdreq	out	1	TX packet buffer read request
tx_in_pct_data	in	TX_IN_PCT_DATA_W	TX packet buffer read data
tx_in_pct_rdempty	in	1	TX packet buffer read empty
tx_in_pct_rdusedw	in	TX_IN_PCT_RDUSEDW_W	TX packet buffer read used words
WFM Player			
wfm_pll_ref_clk	in	1	Reference clock for DDR2 controller

Port	Type	Width	Description
wfm_pll_ref_clk_reset_n	in	1	Reset for DDR2 controller, active low.
wfm_phy_clk	out	1	DDR2 controller local interface clock output
WFM FIFO read ports			
wfm_in_pct_reset_n_req	out	1	WFM packet buffer reset request, active low
wfm_in_pct_rdreq	out	1	WFM packet buffer read request
wfm_in_pct_data	in	WFM_IN_PCT_DATA_W	WFM packet buffer read data
wfm_in_pct_rdempty	in	1	WFM packet buffer read empty
wfm_in_pct_rdusedw	in	WFM_IN_PCT_RDUSEDW_W	WFM packet buffer read used words
DDR2 external memory signals			
wfm_mem_odt	out	1	External memory interface
wfm_mem_cs_n	out	1	
wfm_mem_cke	out	1	
wfm_mem_addr	out	13	
wfm_mem_ba	out	3	
wfm_mem_ras_n	out	1	
wfm_mem_cas_n	out	1	
wfm_mem_we_n	out	1	
wfm_mem_dm	out	2	
wfm_mem_clk	inout	1	
wfm_mem_clk_n	inout	1	
wfm_mem_dq	inout	16	
wfm_mem_dqs	inout	2	
RX path			
rx_clk	in	1	RX interface clock
rx_clk_reset_n	in	1	RX interface reset, active low
Rx interface data			
rx_DIQ	in	RX_IQ_WIDTH	RX IQ samples
rx_fsync	in	1	RX IQ sync signal
Packet fifo ports			
rx_pct_fifo_aclrn_req	out	1	RX packet buffer reset request, active low
rx_pct_fifo_wusedw	in	RX_PCT_BUFF_WRUSEDW_W	RX packet buffer write used words
rx_pct_fifo_wrreq	out	1	RX packet buffer write request
rx_pct_fifo_wdata	out	64	RX packet buffer write data
Sample compare			

Port	Type	Width	Description
rx_smpl_cmp_start	in	1	RX interface sample compare. 0 - disabled, 1-enabled
rx_smpl_cmp_length	in	16	RX interface number of samples to compare.
rx_smpl_cmp_done	out	1	RX outterface sample compare done. 0 - not done, 1-done
rx_smpl_cmp_err	out	1	RX outterface sample compare status. 0 - no error, 1 - error

3.5.1 Receive interface – rx_path_top

Once rx_path_top **Figure 6** is enabled diq2fifo and data2packets modules starts continuously packing IQ samples into 4kB packets. For packet structure see Stream protocol document.

Packets are written to 16kB F2H_S0 FIFO buffer to maintain continuous data flow in short periods when PCIe host cannot accept data. If PCIe host halts data transfer for longer time period and two packets are buffered into 8kB buffer, FIFO full condition arises and other packets are dropped. When host starts to receive data after FIFO full condition, host should expect to receive those two buffered packets.

Module rx_path_top provides two 64bit sample counters. One is for TX logic – tx_path_top. TX logic uses this counter to synchronize transmitted LMS_DQ1 samples with received LMS_DIQ2 samples. Other is used for LMS_DI2 samples packing into 4kB packets.

When rx_path_top is enabled diq2fifo module starts to collect IQ samples from LMS_DIQ2 bus, collected samples are written to FIFO buffer and each write enables smpl_cnt:inst4 module to increase its counter value. This means that counter value increases in same continuous rate as IQ sample rate.

Module smpl_cnt:inst3 is used for LMS_DIQ2 samples packing into 4kB packets. Module data2packets reads IQ samples in bursts from FIFO buffer, each read enables smpl_cnt:inst3 module to increase its counter value. One read burst fills one 4kB packet and there are some idle cycles between bursts.

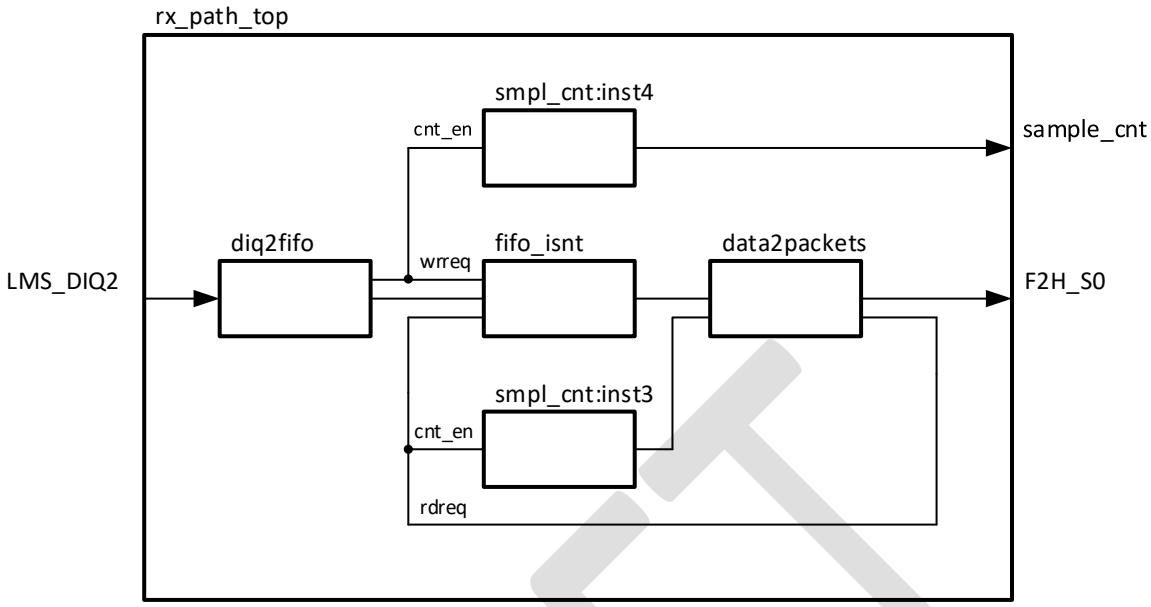

Figure 6 rx_path_top block diagram

Table 16 rx_path_top inctance description

Instance	Description
diq2fifo	Captures IQ samples and writes to FIFO buffer.
fifo_inst	FIFO buffer for storing samples.
data2packets	Module for packing IQ samples to 4kB packets.
smpl_cnt:inst3	Sample counter for tx_path_top.
smpl_cnt:inst4	Sample counter for data2packets module.

3.5.2 Transmit interface – tx_path_top

Transmit module tx_path_top reads IQ samples from H2F_S0_0 FIFO buffer packed in 4kB packets. Packet header (see Stream protocol document) contains sample number (or so-called time stamp) at which packet should be transmitted.

By using sample numbers from rx_path_top and received sample numbers in packet header transmitted IQ samples can be synchronized with received IQ samples.
Module p2d_wr_fsm separates packet header and payload. Packet payload is written into one of two 4kB FIFO buffers located in packets2data module and packet header is stored in p2d_rd module. This module can work in two modes:

- **Synchronization enabled** - module compares received sample number from packet header and sample number from rx_path_top. When sample number from received packet is equal to sample number of rx_path_top module (this means that it is time to send TX packet), read process begins and IQ samples are transmitted to LMS_DIQ1 interface. When sample number from received packet is greater than sample number of rx_path_top module (this means that received packet should be sent after some time) p2d_rd waits until those sample number will be equal. When sample number from received packet is less than sample number of rx_path_top module (this means that packet arrived too late) corresponding FIFO buffer is cleared.

- **Synchronization disabled** – module does not compare sample numbers and every received packet is transmitted to LMS_DIQ1 interface.

Block diagram can be found in **Figure 7** and instance description in **Table 17**.

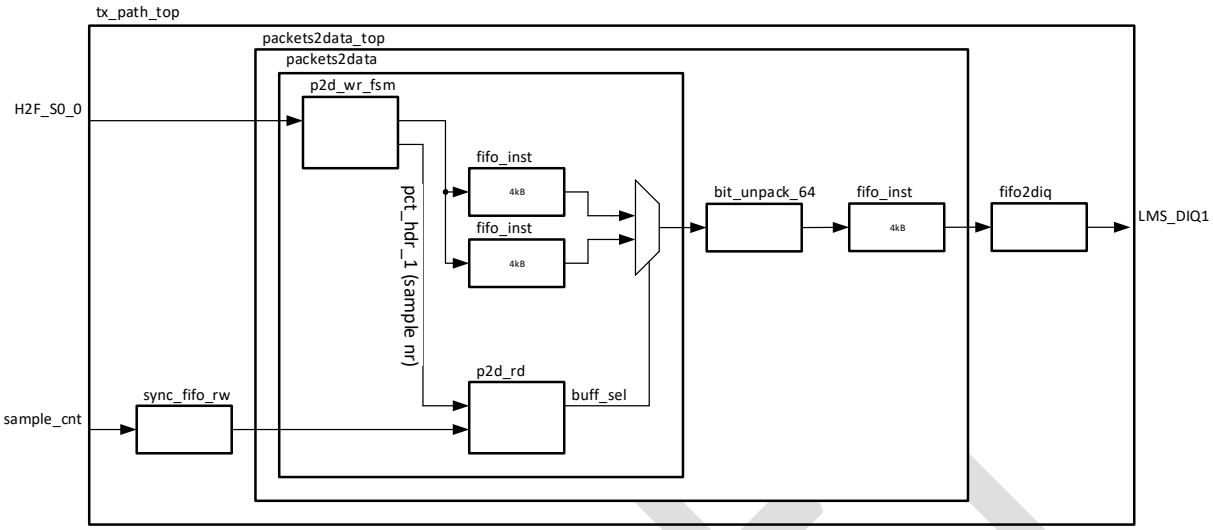

Figure 7 tx_path_top block diagram

Table 17 tx_path_top instance description

Instance	Description
packets2data_top	Wrapper file
packets2data	Wrapper file
p2d_wr_fsm	Module reads packets from EP01_0 buffer and places to one of the 4kB FIFO buffers in increasing order and stores corresponding sample number from packet header.
p2d_rd	Module checks one of the FIFO buffers if it is filled with samples in increasing order. When buffer is ready depending on received sample number from packet header and sample number from rx_path_top module buffer can be cleared or IQ sample reading begins.
fifo_inst	FIFO buffer
fifo2diq	Module reads samples from FIFO buffer and writes to LMS_DIQ1 interface.
sync_fifo_rw	Dual clock FIFO buffer for clock domain crossing.
bit_unpack_64	Depending on mode selection samples are unpacked (see Stream protocol document).

3.5.3 Waveform player – wfm_player_top

Waveform player – wfm_player_top can be used to load waveform from H2F_S0_0 endpoint to external DDR2 memory and played back to LMS_DIQ1 interface. Samples can be loaded using 4kB packets (see Stream protocol document). External memory can store 128MB of data. Block diagram can be found in **Figure 8**.

When loading waveform for LMS_DIQ1 channels (MIMO mode) waveforms should be same length.

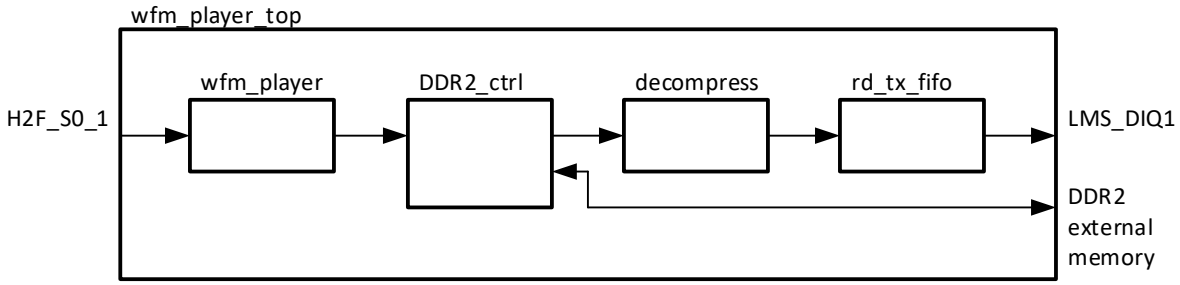

Figure 8 wfm_player_top block diagram

Table 18 wfm_player_top instance description

Instance	Description
wfm_player	Waveform player instance, reads IQ packets from H2F_S0_1 FIFO buffer and writes to DDR2_ctrl module.
DDR2_ctrl	External DDR2 memory controller.
decompress	Decompress IQ samples.
rd_tx_fifo	Reads decompressed samples and writes to LMS_DIQ1 interface.

3.6 General periphery – general_periph_top

General periphery - general_periph_top module is responsible for controlling on board periphery such as LED, GPIO and Fan, default functions can be found in **Table 19**. Also default function can be overridden by internal registers see chapter **3.3 Softcore processor – nios_cpu**.

Table 19 Default functions of LEDS, GPIO and fan

Schematic name	Board label	Type	Description
FPGA_LED1	FPGA_LED1	Clock status	Blinking indicates presence of TCXO clock. Colour indicates status of FPGA PLLs that are used for LMS digital interface clocking: Green – both PLLs are locked; Red/Green – at least one PLL is not locked.
FPGA_LED2	FPGA_LED2	TCXO control mode	No light – TCXO is controlled from DAC Red – TCXO is controlled from phase detector and is not locked to external reference clock Green – TCXO is controlled from phase detector and is locked to external reference clock
FPGA_LED3	FPGA_LED3	RXPLL status	Indicates RXPLL lock status. 0 – no lock, 1 - locked
FPGA_LED4	FPGA_LED4	TXPLL status	Indicates TXPLL lock status. 0 – no lock, 1 - locked
FPGA_LED5	FPGA_LED5		-
FPGA_LED6	FPGA_LED6	-	-
FPGA_GPIO0	FPGA_GPIO		Indicates when TX is transmitting IQ samples. 0 – not transmitting, 1 – transmitting.
FPGA_GPIO1			Indicates RXPLL lock status. 0 – no lock, 1 - locked
FPGA_GPIO2			Indicates TXPLL lock status. 0 – no lock, 1 - locked
FPGA_GPIO3			Indicates TX packet loss, 0 – no loss, 1 – packet lost.

Schematic name	Board label	Type	Description
FPGA_GPIO4-15			-
FAN_CTRL	FAN		Fan control pin. Connected to LM75_OS temperature sensor pin.

Block diagram can be found in **Figure 9**, instances are described in **Table 20**. See **Table 21** and **Table 22** for module parameters and port description.

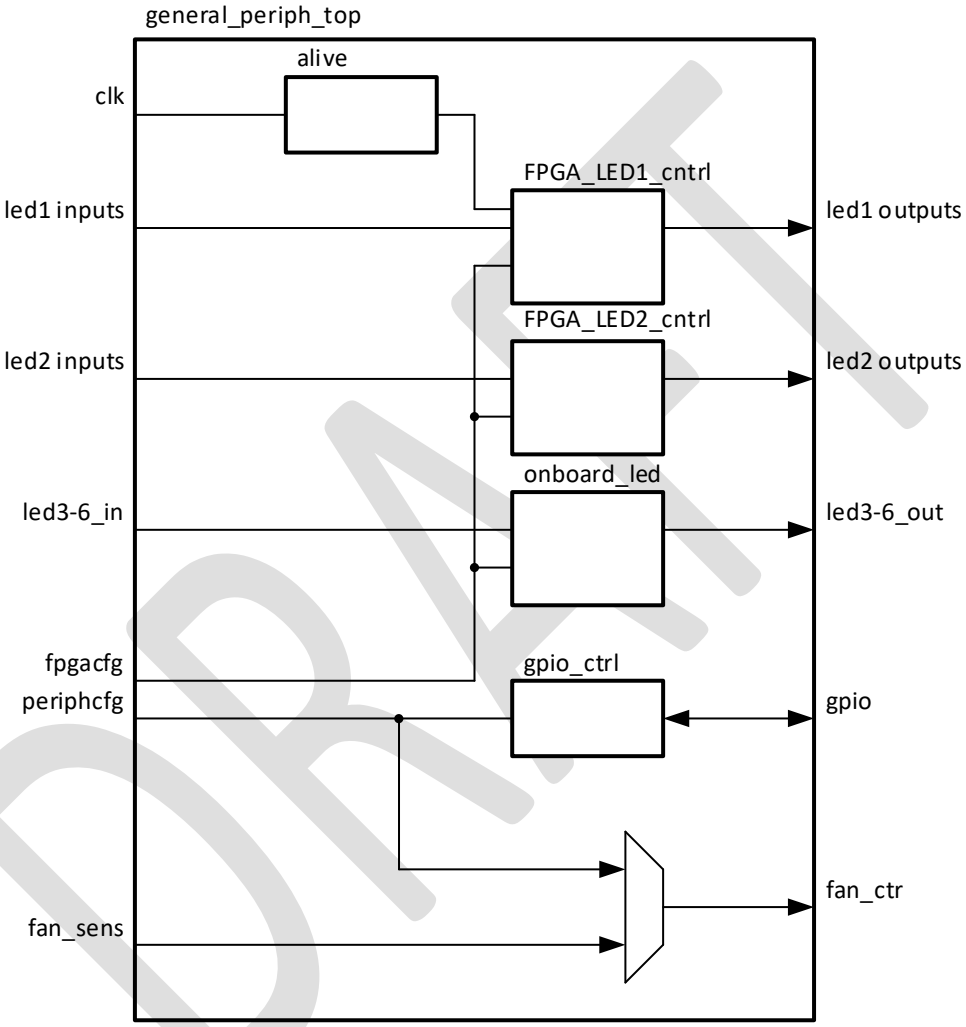

Figure 9 Module general_periph_top block diagram

Table 20 Module instance description

Instance	Description
alive	Basic counter to implement blinking on led1.
FPGA_LED1_cntrl	Led1 control module, for showing clock status
FPGA_LED2_cntrl	Led2 control module, for showing TCXO control mode
onboard_led	Led3-6 control module.
gpio_ctrl	GPIO control instance

Table 21 Module general_periph_top parameters

Parameter	Type	Default	Description
DEV_FAMILY	string	CYCLONE IV GX	FPGA device family name
N_GPIO	integer	16	Number of GPIO used

Table 22 Module general_periph_top input and output port description

Port	Type	Width	Description
clk	in	1	Free running clock
reset_n	in	1	Asynchronous, active low reset
Configuration bus			
from_fpgacfg	in	-	Input/output ports from/to SPI configuration registers
to_periphcfg	out	-	
from_periphcfg	in	-	
LED1(Clock and PLL lock status)			
led1_pll1_locked	in	1	Lock status from PLL1
led1_pll2_locked	in	1	Lock status from PLL2
led1_ctrl	in	3	led1_ctrl[0]–manual LED control enable;led1_ctrl[1]–red LED enable in manual mode;led1_ctrl[2]–green LED enable in manual mode;
led1_g	out	1	Output to dual color LED1 pin
led1_r	out	1	Output to dual color LED1 pin
LED2(TCXO control status)			
led2_clk	in	1	Clock from SPI master connected to DAC and ADF
led2_adf_muxout	in	1	Multiplexer output from ADF4002
led2_dac_ss	in	1	DAC slave select
led2_adf_ss	in	1	ADF slave select
led2_ctrl	in	3	led2_ctrl[0]–manual LED control enable;led2_ctrl[1]–red LED enable in manual mode;led2_ctrl[2]–green LED enable in manual mode;
led2_g	out	1	Output to dual color LED2 pin
led2_r	out	1	Output to dual color LED2 pin
LED3-6			
led3_in	in	1	Input for controlling FPGA_LED3
led4_in	in	1	Input for controlling FPGA_LED4
led5_in	in	1	Input for controlling FPGA_LED5
led6_in	in	1	Input for controlling FPGA_LED6
led3_out	out	1	Output to FPGA_LED3 pin
led4_out	out	1	Output to FPGA_LED4 pin
led5_out	out	1	Output to FPGA_LED5 pin
led6_out	out	1	Output to FPGA_LED6 pin
GPIO			
gpio_dir	in	N_GPIO	GPIO direction control, 0 – input, 1 – output
gpio_out_val	in	N_GPIO	GPIO output value when direction is set to output

Port	Type	Width	Description
gpio_rd_val	out	N_GPIO	GPIO input value vhen direction is set to input
gpio	inout	N_GPIO	Connect to GPIO pins
Fan control			
fan_sens_in	in	1	From temperature sensor
fan_ctrl_out	out	1	To Fan control output

3.7 PLL module – pll_top

PLL module – pll_top (**Figure 10)** provides required clock sources for LM7002 RX and TX digital interfaces. Inside this module there are two dynamically reconfigurable PLL instances **Figure 11**. Clock frequency and phase relationship can be changed while FPGA is in user mode. Instance description can be found in **Table 23**.

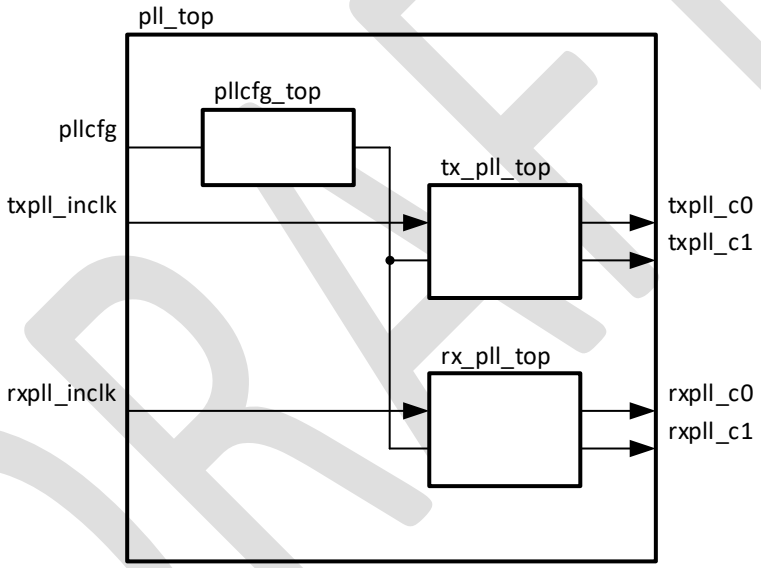

Figure 10 PLL module – pll_top

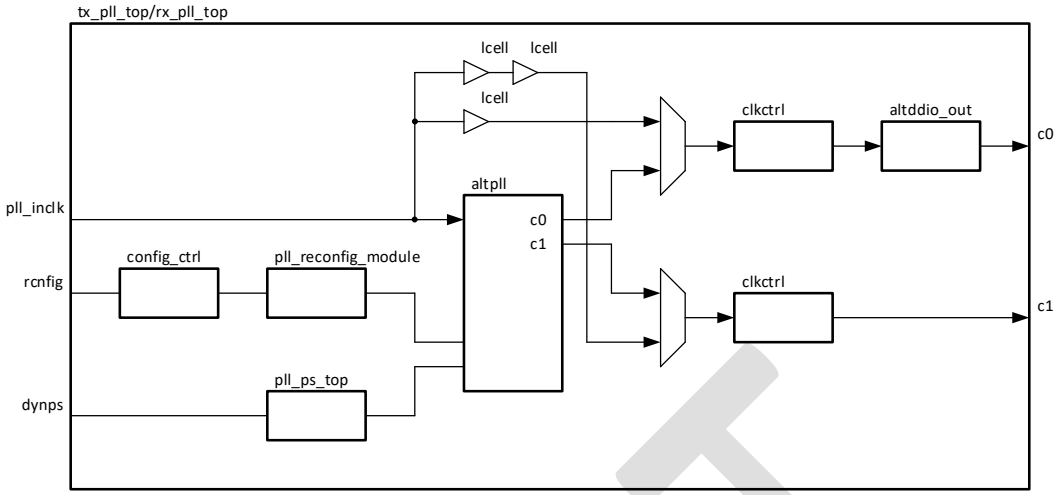

Figure 11 tx_pll_top/rx_pll_top modules

Table 23. pll_top module instance description

Instance	Description
pllcfg_top	PLL configuration control module
tx_pll_top	PLL dedicated for TX interface
rx_pll_top	PLL dedicated for RX interface

Table 24. pll_top module parameters

Parameter	Type	Default	Description
N_PLL	integer	2	
TX PLL parameters			
TXPLL_BANDWIDTH_TYPE	string	"AUTO"	PLL bandwidth setting
TXPLL_CLK0_DIVIDE_BY	natural	1	PLL c0 output division factor
TXPLL_CLK0_DUTY_CYCLE	natural	50	PLL c0 output duty cycle
TXPLL_CLK0_MULTIPLY_BY	natural	1	PLL c0 multiplication factor
TXPLL_CLK0_PHASE_SHIFT	string	"0"	PLL c0 phase shift setting in degrees
TXPLL_CLK1_DIVIDE_BY	natural	1	PLL c1 output division factor
TXPLL_CLK1_DUTY_CYCLE	natural	50	PLL c1 output duty cycle
TXPLL_CLK1_MULTIPLY_BY	natural	1	PLL c1 multiplication factor
TXPLL_CLK1_PHASE_SHIFT	string	"0"	PLL c0 phase shift setting in degrees
TXPLL_COMPENSATE_CLOCK	string	"CLK1"	Specifies for which PLL output delay compensation is done
TXPLL_INCLK0_INPUT_FREQUENCY	natural	6250	TX PLL input frequency period in ps
TXPLL_INTENDED_DEVICE_FAMILY	string	"Cyclone IV E"	FPGA device family
TXPLL_OPERATION_MODE	string	"SOURCE_ SYNCHRONOUS"	PLL compensation mode setting
TXPLL_SCAN_CHAIN_MIF_FILE	string	"ip/txpll/pll.mif"	PLL memory initialization file location
TXPLL_DRCT_C0_NDLY	integer	1	Number of logic cells in c0 TX PLL output when PLL is bypassed

Parameter	Type	Default	Description
TXPLL_DRCT_C1_NDLY	integer	2	Number of logic cells in TX PLL c1 output when PLL is bypassed
RX PLL parameters			
RXPLL_BANDWIDTH_TYPE	string	"AUTO"	PLL bandwidth setting
RXPLL_CLK0_DIVIDE_BY	natural	1	PLL c0 output division factor
RXPLL_CLK0_DUTY_CYCLE	natural	50	PLL c0 output duty cycle
RXPLL_CLK0_MULTIPLY_BY	natural	1	PLL c0 multiplication factor
RXPLL_CLK0_PHASE_SHIFT	string	"0"	PLL c0 phase shift setting in degrees
RXPLL_CLK1_DIVIDE_BY	natural	1	PLL c1 output division factor
RXPLL_CLK1_DUTY_CYCLE	natural	50	PLL c1 output duty cycle
RXPLL_CLK1_MULTIPLY_BY	natural	1	PLL c1 multiplication factor
RXPLL_CLK1_PHASE_SHIFT	string	"0"	PLL c0 phase shift setting in degrees
RXPLL_COMPENSATE_CLOCK	string	"CLK1"	Specifies for which PLL output delay compensation is done
RXPLL_INCLK0_INPUT_FREQUENCY	natural	6250	RX PLL input frequency period in ps
RXPLL_INTENDED_DEVICE_FAMILY	string	"Cyclone IV E"	FPGA device family
RXPLL_OPERATION_MODE	string	"SOURCE_ SYNCHRONOUS"	PLL compensation mode setting
RXPLL_SCAN_CHAIN_MIF_FILE	string	"ip/pll/pll.mif"	PLL memory initialization file location
RXPLL_DRCT_C0_NDLY	integer	1	Number of logic cells in RX PLL c0 output when PLL is bypassed
RXPLL_DRCT_C1_NDLY	integer	2	Number of logic cells in RX PLL c1 output when PLL is bypassed

Table 25 pll_top port description

Port	Type	Width	Description
TX PLL ports			
txpll_inclk	in	1	PLL input clock from LMS_MCLK1 pin
txpll_reconfig_clk	in	1	Free running clock, used for PLL reconfiguration.
txpll_logic_reset_n	in	1	PLL logic active low reset.
txpll_c0	out	1	TX PLL c0 output clock
txpll_c1	out	1	TX PLL c1 output clock (phase shifted version of c0)
txpll_locked	out	1	TX PLL lock status. Outputs high level vhen PLL is locked
txpll_smpl_cmp_en	out	1	Sample compare enable. Used in auto phase searching mode.
txpll_smpl_cmp_done	in	1	Sample compare done indication. Used in auto phase searching mode.
txpll_smpl_cmp_error	in	1	Sample compare error status. Used in auto phase searching mode.

Port	Type	Width	Description
txpll_smpl_cmp_cnt	out	16	Number of samples to be checked. Used in auto phase searching mode
RX PLL ports			
rxpll_inclk	in	1	PLL input clock from LMS_MCLK2 pin
rxpll_reconfig_clk	in	1	Free running clock, used for PLL reconfiguration.
rxpll_logic_reset_n	in	1	PLL logic active low reset.
rxpll_c0	out	1	RX PLL c0 output clock
rxpll_c1	out	1	RX PLL c1 output clock (phase shifted version of c0)
rxpll_locked	out	1	RX PLL lock status. Outputs high level vhen PLL is locked
rxpll_smpl_cmp_en	out	1	Sample compare enable. Used in auto phase searching mode.
rxpll_smpl_cmp_done	in	1	Sample compare done indication. Used in auto phase searching mode.
rxpll_smpl_cmp_error	in	1	Sample compare error status. Used in auto phase searching mode.
rxpll_smpl_cmp_cnt	out	16	Number of samples to be checked. Used in auto phase searching mode
pllcfg ports			
pllcfg_in	in	1	Configuration register bus
pllcfg_out	out	1	

3.8 Board test module – tst_top

Board test module – tst_top **Figure 12** is used to test clock inputs and DDR2 memory. Separate tests can be enabled and results can be read from internal registers see **3.3.3 Registers of tstcfg module**. Module port description can be found in **Table 26**.

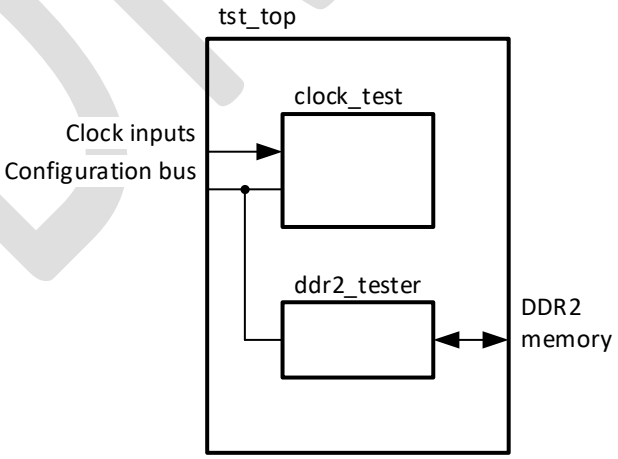

Figure 12 tst_top block diagram

Table 26 tst_top module port description

Port	Type	Width	Description
FX3_clk	in	1	100MHz reference clock
reset_n	in	1	Reset, active low
Clock inputs			
Si5351C_clk_0	in	1	Clock inputs form clock generator Si5351C
Si5351C_clk_1	in	1	
Si5351C_clk_2	in	1	
Si5351C_clk_3	in	1	
Si5351C_clk_5	in	1	
Si5351C_clk_6	in	1	
Si5351C_clk_7	in	1	
LMK_CLK	in	1	Clock buffer
ADF_MUXOUT	in	1	Phase detector mux output
DDR2 external memory signals			
mem_pllref_clk	in	1	External memory interface
mem_odt	out	1	
mem_cs_n	out	1	
mem_cke	out	1	
mem_addr	out	13	
mem_ba	out	3	
mem_ras_n	out	1	
mem_cas_n	out	1	
mem_we_n	out	1	
mem_dm	out	2	
mem_clk	inout	1	
mem_clk_n	inout	1	
mem_dq	inout	16	
mem_dqs	inout	2	
To configuration memory			
to_tstcfg	out	t_TO_TSTCFG	Configuration bus
from_tstcfg	in	t_FROM_TSTCFG	

4 Examples

In this chapter various examples can be found on how to use gateware.

4.1 Accessing FPGA registers

Internal FPGA registers can be accessed using PCIe host via pipe-like device files. For Linux host they are named /dev/xillybus_read_8 and /dev/xillybus_write_8. For windows host they are named \\.\xillybus_read_8 and \\.\xillybus_write_8. See http://xillybus.com/doc for documentation. See **LMS64C_protocol** document for protocol structure and description of commands used in examples. See chapter **3.3 Softcore processor – nios_cpu** for internal FPGA register description.

Read – 64byte packet containing request command "CMD_BRDSPI16_RD" has to be sent from host to FPGA and 64 bytes response packet has to be read from FPGA to host. Read example reads 0x0000 address Board_ID register value, which is 0x000F for LimeSDR-PCIe board.

Request – host writes 64B to /dev/xillybus_write_8 or \\.\xillybus_write_8:

Address	
0000	56 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00
0010	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Response –host reads 64B from /dev/xillybus_read_8 or \\.\xillybus_read_8:

Address	
0000	56 01 01 00 00 00 00 00 00 00 0E 00 00 00 00
0010	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Write – 64byte packet containing request command "CMD_BRDSPI16_WR" has to be sent from host to FPGA and 64 bytes response packet has to be read from FPGA to host. Write example writes 0x1234 value to 0x00DF address. This register is currently reserved and has no dedicated function.

Request – host writes 64B to /dev/xillybus_write_8 or \\.\xillybus_write_8:

Address	
0000	55 00 01 00 00 00 00 00 00 DF 12 34 00 00 00 00
0010	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Response – host reads 64B from /dev/xillybus_read_8 or \\.\xillybus_read_8:

Address	
0000	55 01 01 00 00 00 00 00 00 00 00 00 00 00 00 00
0010	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

0030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

4.2 Accessing LMS7002M registers

Configuration memory which is inside LMS7002M can be accessed using PCIe host via pipe-like device files. For Linux host they are named /dev/xillybus_read_8 and /dev/xillybus_write_8. For windows host they are named \\.\xillybus_read_8 and \\.\xillybus_write_8. See http://xillybus.com/doc for documentation. See **LMS64C_protocol** document for protocol structure and description of commands used in examples. Registers map of LMS7002M can be found in LMS7002M – Multi-Band, Multi-Standard MIMO, Programming and Calibration Guide.

Read – 64byte packet containing request command "CMD_LMS7002_RD" has to be sent from host to FPGA and 64 bytes response packet has to be read from FPGA to host. Read example reads 0x0020 address register value, which is 0xFFFF by default.

Request – host writes 64B to /dev/xillybus_write_8 or \\.\xillybus_write_8:

Address
0000 22 00 01 00 00 00 00 00 00 20 00 00 00 00 00 00
0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Response – host reads 64B from /dev/xillybus_read_8 or \\.\xillybus_read_8:

Address
0000 22 01 01 00 00 00 00 00 00 FF FF 00 00 00 00
0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Write – 64byte packet containing request command "CMD_LMS7002_WR" has to be sent from host to FPGA and 64 bytes response packet has to be read from FPGA to host. Write example writes 0xE4E4 value to 0x0024 address.

Request – host writes 64B to /dev/xillybus_write_8 or \\.\xillybus_write_8: :

Address
0000 21 00 01 00 00 00 00 00 00 24 E4 E4 00 00 00 00
0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Response – host reads 64B from /dev/xillybus_read_8 or \\.\xillybus_read_8:

Address
0000 21 01 01 00 00 00 00 00 00 00 00 00 00 00 00 00
0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

4.3 Periphery control

LED control - modify FPGA register as showed in **Table 27** to turn on and change colour of FPGA_LED2.

Table 27 FPGA_LED2 control example

N	CMD	Address (HEX)	Value (HEX)	Description
1	WR	001A	0010	Override FPGA_LED2 control
2	WR	001A	0030	Turn on FPGA_LED2_R (red is on, green - off)
3	WR	001A	0050	Turn on FPGA_LED2_G (green is on, red - off)

4.4 Configuring FPGA PLL module

To configure PLLs of pll_top module LMS7002M chip has to be already configured and valid clock sources provided to LMS_MCLK1 (connected to txpll_top module) and LMS_MCLK2 (connected to rxpll_top module) pins. For LMS7002M chip configuration see chapter 4.2 Accessing LMS7002M registers.

Configuration of pll_top module can be done by accessing FPGA registers see chapter **4.1 Accessing FPGA registers**. For register description see chapter **3.3 Softcore processor – nios_cpu**.

PLL output frequency F_{out} can be calculated using following equation:

$$F_{ref} = \frac{F_{in}}{N} \quad (1); \qquad F_{VCO} = F_{ref} * M \quad (2); \qquad F_{out} = \frac{F_{VCO}}{C} \quad (3);$$

where F_{ref} - PLL reference frequency, F_{VCO} – VCO frequency, F_{OUT} – Output frequency. See Cyclone IV datasheet for allowed frequency ranges.

4.4.1 RX PLL module - rxpll_top configuration (auto phase shift mode)

This example assumes that LMS7002M chip is already configured, outputs 20MHz clock on LMS_MCLK2 pin and LMS_DIQ2 interface outputs constant IQ values (I=0xAAA, Q=0x555). See **Table 28** for configuration sequence.

Table 28 rxpll_top configuration sequence in auto phase shift mode

N	CMD	Address (HEX)	Value (HEX)	Description
1	WR	0005	0000	Turn off direct clocking
2	WR	0025	01F0	Set PLL parameters
		0023	0008	Set PLL index to 1 and rest bits to zero

N	CMD	Address (HEX)	Value (HEX)	Description
3	WR	0023	0008	Set PLL index to 1 and rest bits to zero
		0026	000A	N, M division bypass and odd division values. N, M division is not bypassed, odd division values enabled
		002A	0201	N, count value = 0x02 + 0x01 = 0x03 (3 DEC)
		002B	6261	M count value = 0x62 + 0x61 = 0xC3 (195 DEC)
		002E	2120	C0 count value = 0x21 + 0x20 = 0x41 (65 DEC)
		002F	2120	C1 count value = 0x21 + 0x20 = 0x41 (65 DEC)
		0027	555a	Counter C0-C7 bypass and odd division control bits. C0 and C1 not bypassed, others bypassed. C0 and C1 odd division values enabled, others not enabled.
		0028	5555	Counter C7-C15 bypass and odd division control bits. All counters are bypassed.
		0023	0009	Trigger reconfiguration for PLL index 1.
4	WR	0023	6308	Release PLL reconfiguration bit, set PLL index - 1, cnt index - 3, phase shift - up, phase shift mode - auto
		0024	0207	Phase shift value = 0x0207 (519 DEC), represents 360 degrees (range in which auto phase shift is executed)
		0023	630a	Trigger auto phase shift for PLL index 1, cnt index 3, phase shift - up, phase shift mode - auto
5	RD	0021	-	Read PLL configuration status register and wait for configuration done (0x0005)
6	WR	0023	6308	Release PLL phase shift bit, set PLL index - 1, cnt index - 3, phase shift - up, phase shift mode - auto

4.4.2 TX PLL module - txpll_top configuration (auto phase shift mode)

This example assumes that LMS7002M chip is already configured, outputs 20MHz clock on LMS_MCLK1-2 pins, LimeLight digital loopback is enabled and FPGA rxpll_top module is already configured. See **Table 29** for configuration sequence.

Table 29 txpll_top configuration sequence in auto phase shift mode

N	CMD	Address (HEX)	Value (HEX)	Description
1	WR	000A	0200	Enable TX test pattern
2	WR	0005	0000	Turn off direct clocking
3	WR	0025	01F0	Set PLL parameters
		0023	0000	Set PLL index to 0 and rest bits to zero
4	WR	0023	0000	Set PLL index to 0 and rest bits to zero
		0026	000A	N, M division bypass and odd division values. N, M division is not bypassed, odd division values enabled
		0002A	0201	N, count value = 0x02 + 0x01 = 0x03 (3 DEC)
		002B	6261	M count value = 0x62 + 0x61 = 0xC3 (195 DEC)
		002E	2120	C0 count value = 0x21 + 0x20 = 0x41 (65 DEC)
		002F	2120	C1 count value = 0x21 + 0x20 = 0x41 (65 DEC)
		0027	555a	Counter C0-C7 bypass and odd division control bits. C0 and C1 not bypassed, others bypassed. C0 and C1 odd division values enabled, others not enabled.
		0028	5555	Counter C7-C15 bypass and odd division control bits. All counters are bypassed.
		0023	0001	Trigger reconfiguration for PLL index 0.
5	WR	0023	6300	Release PLL reconfiguration bit, set PLL index - 0, cnt index - 3, phase shift - up, phase shift mode - auto
		0024	0207	Phase shift value = 0x0207 (519 DEC), represents 360 degrees (range in which auto phase shift is executed)
		0023	6302	Trigger auto phase shift for PLL index 0, cnt index 3, phase shift - up, phase shift mode - auto
6	RD	0021	-	Read PLL configuration status register and wait for configuration done (0x0005)
7	WR	0023	6300	Release PLL phase shift bit, set PLL index - 0, cnt index - 3, phase shift - up, phase shift mode - auto

4.5 Controlling TX and RX data stream

Data stream can be enabled when LMS7002M chip and FPGA PLL modules are configured. See chapters **4.2 Accessing LMS7002M registers** and **4.4 Configuring FPGA PLL module.**

To enable TX and RX data stream – follow FPGA register write sequence described in **Table 30**.

Table 30 enabling TX and RX data stream

N	CMD	Address (HEX)	Value (HEX)	Description
1	WR	000A	0000	Stop data stream
2	WR	0009	0000	Clear packet loss and reset timestamp bits.
3	WR	0009	0003	Clear packet loss flag and reset timestamp.
4	WR	0009	0000	Clear packet loss and reset timestamp bits.
5				Reset xillybus_write_32 and xillybus_read_32 streams
6	WR	0008	102	Set sample width -12, mode - TRXIQ, DDR - enabled, TRXIQ_PULSE mode - disabled, packet synchronization - enabled
7	WR	0007	0001	Set active channels - 1
8	WR	000A	0001	Start stream

To disable TX and RX data stream – follow FPGA register write sequence described in **Table 31.**

Table 31 disabling TX and RX data stream

N	CMD	Address (HEX)	Value (HEX)	Description
1	WR	000A	0000	Stop data stream

4.6 Using WFM player

WFM player requires that LMS7002M has to be configured. See **Table 32** for data loading sequence.

Table 32 WFM data loading

N	CMD	Address (HEX)	Value (HEX)	Description
1	WR	000C	0003	Enable both channels
2	WR	000E	0002	Set sample width to 16bit mode
4	WR	000D	0006	Enable WFM loading
5				Load WFM data to xillybus_write_32
6	WR	000D	0002	Disable WFM loading, start playing file