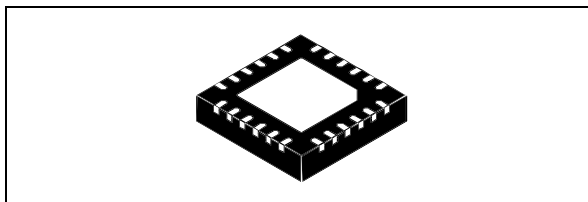


USB Type-C™ controller with TX/RX line driver and BMC

Datasheet - production data



Features

- Type-C attach and cable orientation detection
- Power role support: source/sink/DRP
- Configurable start-up profiles
- Integrated power switch for V_{CONN} supply:
 - programmable current limit up to 600 mA
 - overcurrent, overvoltage, and thermal protection
 - under-voltage lockout
- I²C interface and interrupt
- Integrated V_{BUS} voltage monitoring
- Integrated V_{BUS} and V_{CONN} discharge path
- Integrated BMC transceiver
- V_{BUS} switch gate driver
- Low power standby mode
- Dead battery mode support
- High voltage protection (including CC pins)
- Accessory mode support
- Dual power supply (V_{SYS} and/or V_{DD}):
 - V_{SYS} = [3.0 V; 5.5 V]
 - V_{DD} = [4.1 V; 22 V]

- Fully compatible with:
 - USB Type-C™ rev 1.2
 - USB PD rev 2.0

Applications

- Smart plugs, wall adapters, and chargers
- Power hubs and docking stations
- Smartphones and tablets
- Gaming and PNDs
- Displays
- Cameras, camcorders, and MP3 players
- Any Type-C source or sink device

Description

The STUSB1602 is a generic IC designed in a 20 V technology. It addresses USB Type-C™ port management both on the host and/or device side, and is suited for a broad range of applications.

The STUSB1602 can handle all functions from Type-C attach detection, plug orientation detection, host to device connection, V_{CONN} support, and V_{BUS} configuration.

It also provides a USB PD TX/RX line driver and BMC (biphase mark coding) transceiver which allows USB PD negotiation and alternative mode through an external MCU.

Additionally, the STUSB1602 provides support for dead battery operation.

Table 1. Device summary table

| Order code | Description | Package | Marking | Temperature range |
|--------------|---|-----------------|---------|---------------------|
| STUSB1602QTR | USB Type-C™ controller with TX/RX line driver and BMC | QFN24 EP 4x4 mm | 1602 | -40 °C up to 105 °C |

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1 Functional description

The STUSB1602 is a USB Type-C controller IC. It is designed to interface with the Type-C receptacle both on host and/or device sides. It is used to establish and manage the source-to-sink connection between two USB Type-C host and device ports.

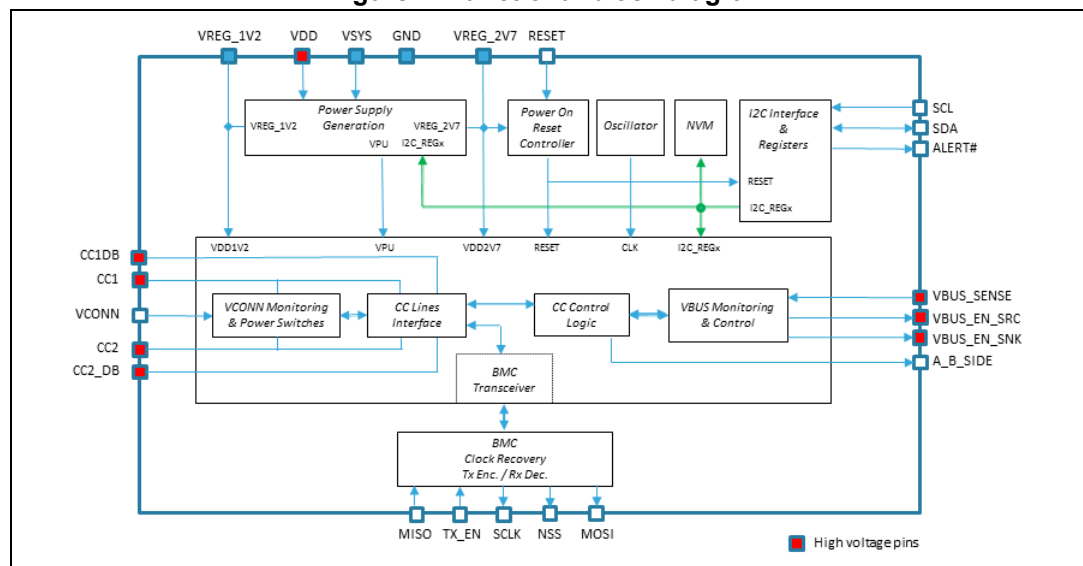
The major role of the STUSB1602 is to:

1. Detect the connection between two USB Type-C ports (attach detection)
2. Establish a valid source-to-sink connection
3. Determine the attached device mode: source, sink or accessory
4. Resolve cable orientation and twist connections to establish USB data routing (mux control).
5. Configure and monitor the V_{BUS} power path
6. Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode.
7. Configure V_{CONN} when required
8. Support USB PD negotiation

The STUSB1602 also provides:

1. Low power standby mode
2. Dead battery mode
3. I²C interface and interrupt
4. Start-up configuration customization: static through NVM and/or dynamic through I²C
5. High voltage protection
6. Accessory mode detection

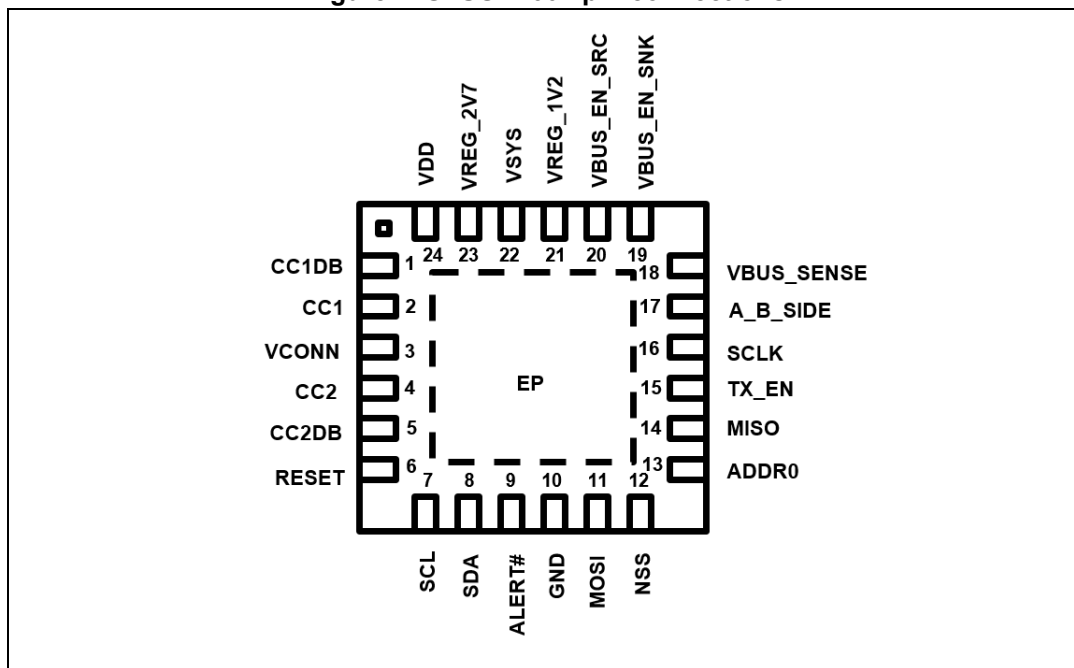
Figure 1. Functional block diagram



2 Inputs/outputs

2.1 Pinout

Figure 2. STUSB1602 pin connections



2.2 Pin list

Table 2. Pin function list

| Pin | Name | Type | Description | Typical Connection |
|-----|--------|--------|---|--|
| 1 | CC1DB | HV AIO | Dead battery enable on CC1 pin | CC1 pin if used or ground |
| 2 | CC1 | HV AIO | Type-C configuration channel 1 | Type-C receptacle A5 |
| 3 | VCONN | PWR | Power input for active plug | 5 V power source |
| 4 | CC2 | HV AIO | Type-C configuration channel 2 | Type-C receptacle B5 |
| 5 | CC2DB | HV AIO | Dead battery enable on CC2 pin | CC2 pin if used or ground |
| 6 | RESET | DI | Reset input (active high) | — |
| 7 | SCL | DI | I ² C clock input | To I ² C master, ext. pull-up |
| 8 | SDA | DI/OD | I ² C data input/output, active low open drain | To I ² C master, ext. pull-up |
| 9 | ALERT# | OD | I ² C interrupt, active low open drain | To I ² C master, ext. pull-up |
| 10 | GND | GND | Ground | Ground |

Table 2. Pin function list

| | | | | |
|----|-------------|--------|--|---|
| 11 | MOSI | DO | Master out slave in: serial data from STUSB1602 to MCU, BMC decoded from connected CC line | To MCU, ext. pull-up referenced to MCU Vio |
| 12 | NSS | OD | Chip select, open drain active low to control MCU SPI/MSP interface | To MCU, ext. pull-up referenced to MCU Vio |
| 13 | ADDR0 | DI | I ² C device address setting (see Section 5: I²C interface) | Static |
| 14 | MISO | DI | Master in slave out: serial data from MCU to STUSB1602 encoded in BMC to drive the CC line | From MCU, ext. pull-up referenced to MCU Vio |
| 15 | TX_EN | DI | TX enable, open drain active high to drive CC line from the embedded BMC interface | From MCU, needs to be maintained low by MCU or pulled down when receiving standby |
| 16 | SCLK | DO | Serial clock to clock data transfer between MCU and STUSB1602. Open drain output pin, needs external pull-up referenced to MCU Vio | To MCU, ext. pull-up referenced to MCU Vio |
| 17 | A_B_SIDE | OD | Cable orientation, active low open drain | USB super speed mux select, ext. pull-up |
| 18 | VBUS_SENSE | HV AI | V _{BUS} voltage monitoring and discharge path | From V _{BUS} |
| 19 | VBUS_EN_SNK | HV AIO | V _{BUS} sink power path enable, active low open drain | To switch or power system, ext. pull-up |
| 20 | VBUS_EN_SRC | HV AIO | V _{BUS} source power path enable, active low open drain | To switch or power system, ext. pull-up |
| 21 | VREG_1V2 | PWR | 1.2 V internal regulator output | 1 µF typ. decoupling capacitor |
| 22 | VSYS | PWR | Power supply from system | From power system, connect to ground if not used |
| 23 | VREG_2V7 | PWR | 2.7 V internal regulator output | 1 µF typ. decoupling capacitor |
| 24 | VDD | HV PWR | Main power supply from USB power line | From V _{BUS} |
| — | EP | GND | Exposed pad is connected to ground | To ground |

Table 3. Pin function descriptions

| Type | Description |
|------|-------------------|
| D | Digital |
| A | Analog |
| O | Output pad |
| I | Input pad |
| IO | Bidirectional pad |
| OD | Open drain output |
| PD | Pull-down |
| PU | Pull-up |
| HV | High voltage |
| PWR | Power supply |
| GND | Ground |

2.3 Pin description

2.3.1 CC1/CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination, and system configuration management across the USB Type-C cable.

2.3.2 CC1DB/CC2DB

CC1DB and CC2DB are used for dead battery mode when the STUSB1602 is configured in sink power role or dual power role. This mode is enabled by connecting CC1DB and CC2DB respectively to CC1 and CC2. Thanks to this connection, the pull down terminations on the CC pins are present by default even if the device is not supplied (see [Section 3.6: Dead battery mode](#)).

Warning: CC1DB and CC2DB must be connected to ground when the STUSB1602 is configured in source power role or when dead battery mode is not supported.

2.3.3 VCONN

This power input is connected to a power source that can be a 5 V power supply or a lithium battery. It is used to provide power to the local plug. It is internally connected to power switches that are protected against short circuit and overvoltage. This does not require any protection on the input side. When a valid source-to-sink connection is determined and the V_{CONN} power switches are enabled, V_{CONN} is provided by the source to the unused CC pin (see [Section 3.4: V_{CONN} supply](#)).

2.3.4 RESET

Active high reset

2.3.5 I²C interface pins

Table 4. I²C interface pin list

| Name | Description |
|--------|--|
| SCL | I ² C clock, need external pull-up |
| SDA | I ² C data, need external pull-up |
| ALERT# | I ² C interrupt, need external pull-up |
| ADDR0 | I ² C device address bit (see Section 5: I²C interface) |

2.3.6 GND

Ground

2.3.7 MOSI

Master out slave in: data from the connected CC line are decoded using the BMC and then transmitted via the STUSB1602 to the MCU. Data are valid on the **falling** edge of the SCLK line and must be sampled by the MCU on this edge.

2.3.8 NSS

The chip select signal is driven by the STUSB1602 and is connected to the MCU. It activates the SPI/MSP interface transfer. The NSS signal drives the MCU so that:

- When TX_EN is asserted (TX mode), the STUSB1602 transmits data from the MCU over the CC line. Note, the MCU must provide data to be encoded on the MISO line which must be in synchrony with the SCLK.
- When TX_EN is not asserted (RX mode, default), the CC line is activity detected, data are received, and the BMC is decoded by the STUSB1602. Decoded data are sent on the MOSI line in synchrony with the SCLK

2.3.9 MISO

Master in slave out: data from the MCU are encoded using the BMC and then transmitted via the STUSB1602 to the connected CC line driver. Data are sampled by the STUSB1602 on the **rising** edge of the SCLK line and must be stable on this edge.

2.3.10 TX_EN

TX_EN is a control signal from the MCU to the STUSB1602. It enables the BMC control logic that transfers data from the MCU serial interface, encodes it in BMC format, and drives the connected CC line.

Note: TX mode overrides RX mode.

2.3.11 SCLK

The serial clock signal from the STUSB1602 drives the SPI/MSP interface of the MCU and the clock data on the MISO and MOSI pins.

2.3.12 A_B_SIDE

This output pin provides cable orientation. It is used to establish USB SuperSpeed signal routing. The cable orientation is also provided by an internal I²C register. This signal is not required in the case of USB 2.0 support.

Table 5. USB data mux select

| Value | CC pin position |
|-------|--------------------------------|
| HiZ | CC1 pin is attached to CC line |
| 0 | CC2 pin is attached to CC line |

2.3.13 VBUS_SENSE

This input pin is used to sense V_{BUS} presence, monitor V_{BUS} voltage, and discharge the V_{BUS} on the USB Type-C receptacle side.

2.3.14 VBUS_EN_SNK

In sink power role, this pin allows the incoming V_{BUS} power to be enabled when the connection to a source is established and V_{BUS} is in a valid operating range. The open drain output allows a PMOS transistor to be directly driven. The logic value of the pin is also advertised in a dedicated I²C register bit.

2.3.15 VBUS_EN_SRC

In source power role, this pin allows the outgoing V_{BUS} power to be enabled when the connection to a sink is established and V_{BUS} is in a valid operating range. The open drain output allows a PMOS transistor to be directly driven. The logic value of the pin is also advertised in a dedicated I²C register bit.

2.3.16 VREG1V2

This pin is used for external decoupling of the 1.2 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min, 10 µF max).

2.3.17 VSYS

This is the low power supply of the system, if there is any. It can be connected directly to a single cell Lithium battery or to the system power supply delivering 3.3 V or 5 V. It is recommended to connect this pin to ground when it is not used.

2.3.18 VREG2V7

This pin is used for external decoupling of the 2.7 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min, 10 µF max).

2.3.19 VDD

This is the power supply from the USB power line for applications powered by V_{BUS} .

In source power role, this pin can be used to sense the voltage level of the main power supply providing the V_{BUS} . It allows UVLO and OVLO thresholds to be considered independently on the VDD pin as additional conditions to enable the V_{BUS} power path through the VBUS_EN_SRC pin (see [Section 3.3.3: \$V_{BUS}\$ power path assertion](#)). When the UVLO threshold detection is enabled, the VDD pin must be connected to the main power supply to establish the connection and to assert the V_{BUS} power path.

3 Features description

3.1 CC interface

The STUSB1602 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks: the CC line interface block and the CC control logic block.

The CC line interface block is used to:

- Configure termination mode on the CC pins relative to the power mode supported i.e. pull-up for source power role and pull-down for sink power role.
- Monitor the CC pin voltage values relative to the attachment detection thresholds
- Configure V_{CONN} on the unconnected CC pin when required
- Protect the CC pins against overvoltage

The CC control logic block is used to:

- Execute the Type-C FSM relative to the Type-C power mode supported
- Determine the electrical state for each CC pin relative to the detected thresholds
- Evaluate the conditions relative to the CC pin states and the V_{BUS} voltage value to transition from one state to another in the Type-C FSM.
- Detect and establish a valid source-to-sink connection
- Determine the attached device mode: source, sink or accessory
- Determine cable orientation to allow external routing of the USB data
- Manage V_{BUS} power capability: USB default, Type-C medium or Type-C high current mode.
- Handle hardware faults

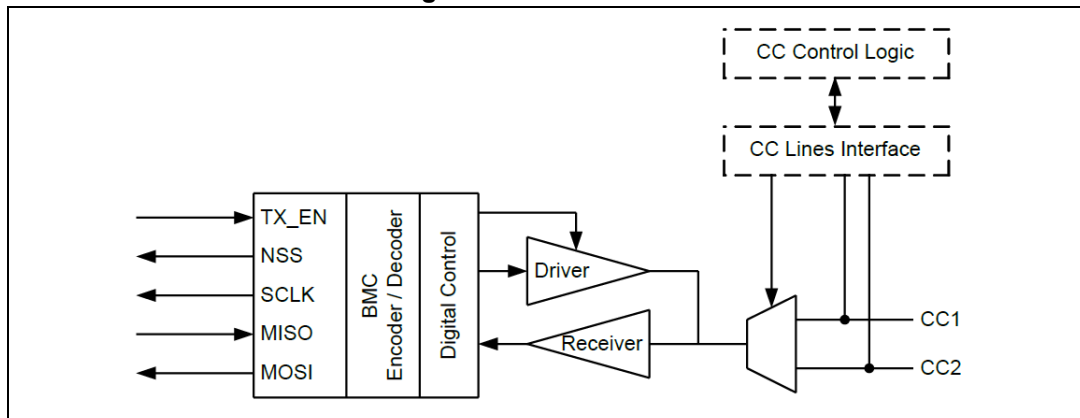
The CC control logic block implements the Type-C FSMs corresponding to the following Type-C power modes:

- Source power role with accessory support
- Sink power role with accessory support
- Sink power role without accessory support
- Dual power role with accessory support
- Dual power role with accessory and Try.SRC support
- Dual power role with accessory and Try.SNK support

The default Type-C power mode is selected through NVM programming (see [Section 6: Start-up configuration](#)) and can be changed by software during operation through the I²C interface.

3.2 BMC interface

Figure 3. BMC interface



3.2.1 BMC interface behavior

When a connection is established on the STUSB1602 (any attached state), the CC line used for connection is also internally connected to BMC block which allows communication on this line.

The CC line is primary managed by CC control logic. BMC communication on the CC line must not interact with this control logic, as driving times of the line are short and are related to denounce times of the CC logic.

The BMC block handles BMC encoding and decoding. It also handles CC line activity detection, discharging the external MCU of such operations.

The default state of the BMC block is to listen to the line (RX mode). TX mode is enabled only by assertion of the TX_EN signal via the external MCU.

3.2.2 TX mode

When the TX_EN signal is asserted via the MCU, the BMC block goes to the TX state:

- The NSS signal is driven low, indicating to the SPI/MSP slave interface of the MCU that data are being transmitted on the CC line. The MCU provides the data.
- The STUSB1602 drives the NSS signal low, indicating to the SPI/MSP slave interface of the MCU that data are requested on the MISO line.
- The STUSB1602 clocks the SCLK signal
- The MCU presents data to be transmitted on the MISO line and data are sampled on the rising edge of SCLK (data must be stable on this edge).
- Sampled data (from the MISO line) are encoded by the BMC, and the resulting values drive the CC line according to USB PD standard.

When all data are transmitted, the MCU drives the TX_EN pin low, which signals the end of transmission. The STUSB1602 ends transmission with a corresponding trailing edge termination. It then goes back into to default state and releases the CC line from the BMC driver to the pull-up/pull-down CC line interfaces.

3.2.3 RX mode

RX mode is the default state of the BMC interface.

In this mode, the receiver listens to the connected CC line. It does not interface with the CC line interfaces or the CC control logic.

When all data are detected and received on the CC line, according to the activity described in the USB Power Delivery Standard, the BMC interface:

- Drives the NSS signal low
- Outputs the clock on the SCLK signal which is recovered from the BMC signal
- Outputs recovered data (from the BMC signal) on the MOSI line to the connected MCU. Data are valid on the SCLK falling edge and are sampled on this edge by the SPI/MSP interface of the MCU.

When no more data are detected on the CC line, the NSS goes back to “high” which is its default state. This indicates to the MCU that no more activity is present on the bus.

3.3 V_{BUS} power path control

3.3.1 V_{BUS} monitoring

The V_{BUS} monitoring block supervises (from the VBUS_SENSE pin) the V_{BUS} voltage on the USB Type-C receptacle side.

It is used to check that the V_{BUS} is within a valid voltage range:

- To establish a valid source-to-sink connection according to USB Type-C standard specifications.
- To safely enable the V_{BUS} power path through the VBUS_EN_SRC pin or VBUS_EN_SNK pin depending on the power role.

It allows detection of unexpected V_{BUS} voltage conditions such as under-voltage or overvoltage relative to the valid V_{BUS} voltage range. When such conditions occur, the STUSB1602 reacts as follows:

- At attachment, it prevents the source-to-sink connection and the V_{BUS} power path assertion.
- After attachment, it deactivates the source-to-sink connection and disables the V_{BUS} power path. In source power role, the device goes into error recovery state. In Sink power role, the device goes into unattached state.

The V_{BUS} voltage value is adjusted automatically at attachment (vSafe5V) and via the MCU at each PDO transition. Monitoring is then disabled during T_PDO_transition (i.e. the default value of 300 ms is changed through NVM programming). Additionally, if a transition occurs to a lower voltage, the discharge path is activated during this time.

The valid V_{BUS} voltage range is defined from the V_{BUS} nominal voltage by a high threshold voltage and a low threshold voltage whose nominal values are respectively V_{BUS}+5% and V_{BUS}-5%. The nominal threshold limits can be shifted by a fraction of V_{BUS} from +1% to +15% for the high threshold voltage and from -1% to -15% for the low threshold voltage. This means the threshold limits can vary from V_{BUS}+5% to V_{BUS}+20% for the high limit and from V_{BUS}-5% to V_{BUS}-20% for the low limit.

The threshold limits are preset by default in the NVM with different shift coefficients depending on whether the device operates in source power role or in sink power role (see [Section 8.3: Electrical and timing characteristics](#)). The threshold limits can be changed independently through NVM programming (see [Section 6: Start-up configuration](#)) and also by software during attachment through the I²C interface.

3.3.2 V_{BUS} discharge

The monitoring block also handles the internal V_{BUS} discharge path connected to the VBUS_SENSE pin. The discharge path is activated at detachment, or when the device goes into the error recovery state whatever the power role (see [Section 3.8: Hardware fault management](#)).

The V_{BUS} discharge path is enabled by default in the NVM and can be disabled through NVM programming only (see [Section 6: Start-up configuration](#)). The discharge time duration is also preset by default in the NVM (see [Section 8.3: Electrical and timing characteristics](#)). The discharge time duration can be changed through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I²C interface.

3.3.3 V_{BUS} power path assertion

The STUSB1602 can control the assertion of the V_{BUS} power path on the USB Type-C port, directly or indirectly, through the VBUS_EN_SRC and VBUS_EN_SNK pins according to the system power role.

The tables below summarize the configurations and the conditions that determine the electrical value of the VBUS_EN_SRC and VBUS_EN_SNK pins during system operation.

Table 6. Conditions for V_{BUS} power path assertion in source power role

| Pin | Electrical value | Operation conditions | | | Comment |
|-------------|------------------|--|--|---|---|
| | | Type-C attached state | VDD pin monitoring | VBUS_SENSE pin monitoring | |
| VBUS_EN_SRC | 0 | Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC | VDD > UVLO if VDD_UVLO enabled and/or VDD < OVLO if VDD_OVLO enabled | V _{BUS} is within valid voltage range if VBUS_VALID_RANGE enabled or V _{BUS} > UVLO if VBUS_VALID_RANGE disabled | The signal is asserted only if all the valid operation conditions are met |
| | HiZ | Any other state | VDD < UVLO if VDD_UVLO enabled and/or VDD > OVLO if VDD_OVLO enabled | V _{BUS} is out of valid voltage range if VBUS_VALID_RANGE enabled or V _{BUS} < UVLO if VBUS_VALID_RANGE disabled | The signal is de-asserted when at least one non valid operation condition is met |

As specified in the USB Type-C standard specification, the attached state “Attached.SRC” is reached only if the voltage on the V_{BUS} receptacle side is at vSafe0V condition when a connection is detected.

Table 7. Conditions for V_{BUS} power path assertion in sink power role

| Pin | Electrical value | Operation conditions | | | Comment |
|-------------|------------------|--|--------------------|--|--|
| | | Type-C attached state | VDD pin monitoring | VBUS_SENSE pin monitoring | |
| VBUS_EN_SNK | 0 | Attached.SNK or Debug Accessory.SNK | Not applicable | VBUS is within valid voltage range if VBUS_VALID_RANGE enabled or VBUS > UVLO if VBUS_VALID_RANGE disabled | The signal is asserted only if all the valid operation conditions are met |
| | HiZ | Any other state | Not applicable | VBUS is out of valid voltage range if VBUS_VALID_RANGE enabled or VBUS < UVLO if VBUS_VALID_RANGE disabled | The signal is de-asserted when at least one non valid operation condition is met |

“Type-C attached state” refers to the Type-C FSM states as defined in the USB Type-C standard specification and as described in the I²C register CC_OPERATION_STATUS.

“VDD pin monitoring” is valid only in source power role. Activation of the UVLO and OVLO threshold detections can be done through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I²C interface. When the UVLO and/or OVLO threshold detection is activated, the VBUS_EN_SRC pin is asserted only if the device is attached and the valid threshold conditions on VDD are met. Once the VBUS_EN_SRC pin is asserted, the V_{BUS} monitoring is done on VBUS_SENSE pin instead of the VDD pin.

“VBUS_SENSE pin monitoring” relies, by default, on a valid V_{BUS} voltage range. The voltage range condition can be disabled to consider UVLO threshold detection instead. The monitoring condition of the V_{BUS} voltage can be changed through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I²C interface. The VBUS_EN_SRC pin is maintained asserted as long as the device is attached and a valid voltage condition on the V_{BUS} is met.

3.4 V_{CONN} supply

3.4.1 V_{CONN} input voltage

V_{CONN} is a regulated supply used to power circuits in the plug of the USB3.1 full-featured cables and other accessories. The V_{CONN} nominal operating voltage is 5.0 V \pm 5 %.

3.4.2 V_{CONN} application conditions

The V_{CONN} pin of the STUSB1602 is connected to each CC pin (CC1 and CC2) across independent power switches.

The STUSB1602 applies V_{CONN} only to the CC pin not connected to the CC wire when all below conditions are met:

- The device is configured in source power role or dual power role
- V_{CONN} power switches are enabled
- A valid connection to a sink is achieved
- Ra presence is detected on the unwired CC pin
- A valid power source is applied on the V_{CONN} pin with respect to a predefined UVLO threshold.

The STUSB1602 does not provide V_{CONN} when it is operating in sink power role.

3.4.3 V_{CONN} monitoring

The V_{CONN} monitoring block detects whether the V_{CONN} power supply is available on the V_{CONN} pin. It is used to check that the V_{CONN} voltage is above a predefined undervoltage lockout (UVLO) threshold to allow enabling of the V_{CONN} power switches.

The default value of the UVLO threshold is 4.65 V typical for powered cables operating at 5 V. This value can be changed by software to 2.65 V typical to support V_{CONN} -powered accessories that operate down to 2.7 V.

3.4.4 V_{CONN} discharge

The behavior of Type-C FSMs is extended with an internal V_{CONN} discharge path capability on the CC pins in source power mode only. The discharge path is activated during 250 ms from sink detachment detection. This feature is disabled by default. It can be activated through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I²C interface.

3.4.5 V_{CONN} control and status

The supplying conditions of V_{CONN} across the STUSB1602 are managed through the I²C interface. Different I²C registers and bits are used specifically for this purpose.

3.4.6 V_{CONN} power switches

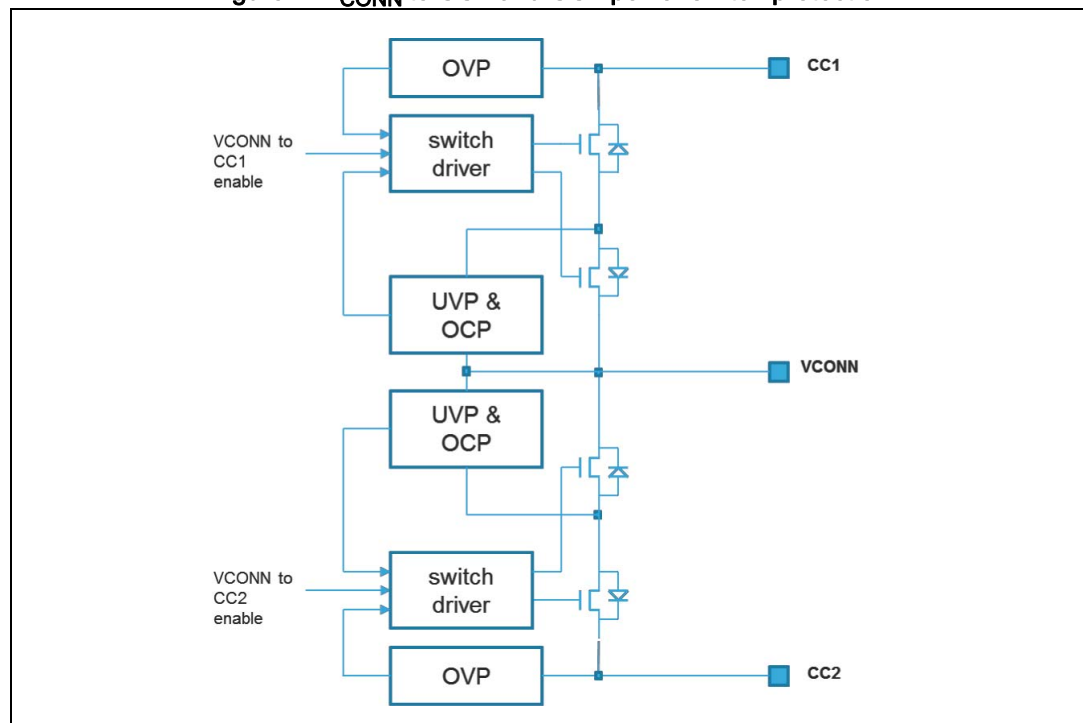
Features

The STUSB1602 integrates two current limited high-side power switches with protection that tolerates high voltage up to 22 V on the CC pins.

Each V_{CONN} power switch presents the following features:

- Soft-start to limit inrush current
- Constant current mode overcurrent protection
- Adjustable current limit
- Thermal protection
- Undervoltage and overvoltage protection
- Reverse current and reverse voltage protection

Figure 4. V_{CONN} to CC1 and CC2 power switch protection



Current limit programming

The current limit can be set within the range 100 mA to 600 mA by a step of 50 mA. The default current limit is programmed through NVM programming (see [Section 6: Start-up configuration](#)) and can be changed by software through the I²C interface. At power-on or after a reset, the current limit takes the default value preset in the NVM.

Fault management

The table below summarizes the different fault conditions that could occur during operation of the switch and the associated responses. An I²C alert is generated when a fault condition happens.

Table 8. Fault management conditions

| Fault types | Fault conditions | Expected actions |
|-----------------|--|--|
| Short circuit | CC output pin shorted to ground via very low resistive path causing rapid current surge | Power switch limits the current and reduces the output voltage. I ² C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits. |
| Overcurrent | CC output pin connected to a load that sinks current above programmed limit | Power switch limits the current and reduces the output voltage. I ² C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits. |
| Overheating | Junction temperature exceeding 145 °C due to any reason | Power switch is disabled immediately until the temperature falls below 145 °C minus hysteresis of 15 °C. I ² C alert is asserted immediately thanks to THERMAL_FAULT bit. STUSB1602 goes into transient error recovery state. |
| Undervoltage | V _{CONN} input voltage drops below UVLO threshold minus hysteresis | Power switch is disabled immediately until the input voltage rises above the UVLO threshold. I ² C alert is asserted immediately thanks to VCONN_PRESENCE bit. |
| Overvoltage | CC output pin voltage exceeds maximum operating limit of 6.0 V | Power switch is opened immediately until the voltage falls below the voltage limit. I ² C alert is asserted immediately thanks to VCONN_SW_OVP_FAULT bits. |
| Reverse current | CC output pin voltage exceeds V _{CONN} input voltage when the power switch is turned-off | The reverse biased body diode of the back-to-back MOS switches is naturally disabled preventing current to flow from the CC output pin to the input. |
| Reverse voltage | CC output pin voltage exceeds V _{CONN} input voltage of more than 0.35 V for 5 V when the power switch is turned-on | Power switch is opened immediately until the voltage difference falls below the voltage limit. I ² C alert is asserted immediately thanks to VCONN_SW_RVP_FAULT bits. |

3.5 Low power standby mode

The STUSB1602 proposes a standby mode to reduce the device power consumption when no device is connected to the USB Type-C port. It is disabled by default and can be activated through NVM programming (see [Section 6: Start-up configuration](#)).

When activated, the STUSB1602 enters standby mode at power up, after a reset, or after a disconnection. In this mode, the CC interface and the voltages monitoring blocks are turned off. Only a monitoring circuitry is maintained active on the CC pins to detect a connection. When the connection is detected, all the internal circuits are turned on to allow normal operation.

Standby mode does not operate when the device is configured in sink power role with accessory support (see [Section 6: Start-up configuration](#)).

3.6 Dead battery mode

Dead battery mode allows systems powered by a battery to be supplied by the V_{BUS} when the battery is discharged and to start the battery charging process. This mode is also used in systems that are powered through the V_{BUS} only.

Dead battery mode is only supported in sink power role and dual power role configurations. It operates only if the CC1DB and CC2DB pins are connected respectively to the CC1 and CC2 pins. Thanks to these connections, the STUSB1602 presents a pull down termination on its CC pins and advertises itself as a sink even if the device is not supplied.

When a source system connects to a USB Type-C port with the STUSB1602 configured in dead battery mode, it can detect the pull down termination, establish the source-to-sink connection, and provide the V_{BUS} . The STUSB1602 is then supplied thanks to the VDD pin connected to the V_{BUS} on the USB Type-C receptacle side. The STUSB1602 can finalize the source-to-sink connection and enable the power path on the V_{BUS} thanks to the $VBUS_EN_SNK$ pin which allows the system to be powered.

3.7 High voltage protection

The STUSB1602 can be safely used in systems or connected to systems that handle high voltage on the V_{BUS} power path. The device integrates an internal circuitry on the CC pins that tolerates high voltages and ensures protection up to 22 V in case of unexpected short circuits with the V_{BUS} or in the case of a connection to a device supplying high voltage on the V_{BUS} .

3.8 Hardware fault management

The STUSB1602 handles hardware fault conditions related to the device itself and to the V_{BUS} power path during system operation.

When such conditions occur, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM. When entering in this state, the device de-asserts the V_{BUS} power path by disabling the $VBUS_EN_SRC$ pin and it removes the terminations from the CC pins during several tens of milliseconds. Then, it transitions to the unattached source state.

The STUSB1602 goes into error recovery state when at least one condition listed below is met:

- If an overtemperature is detected, the “THERMAL_FAULT” flag is asserted
- If an internal pull-up voltage on the CC pins is below the UVLO threshold, the “VPU_VALID” flag is asserted.
- If an overvoltage is detected on the CC pins, the “VPU_OVP_FAULT” flag is asserted
- If the V_{BUS} voltage is out of the valid voltage range during attachment, the “VBUS_VALID” flag is asserted.
- If an undervoltage is detected on the VDD pin during attachment when UVLO detection is enabled, the “VDD_UVLO_DISABLE” flag is asserted.
- If an overvoltage is detected on the VDD pin during attachment when OVLO detection is enabled, the “VDD_OVLO_DISABLE” flag is asserted.

The I²C register bits mentioned above in quotes give either the state of the hardware fault when it occurs or the setting condition to detect the hardware fault.

3.9 Accessory mode detection

The STUSB1602 supports the detection of audio accessory mode and debug accessory mode as defined in the USB Type-C standard specification with the following Type-C power modes (see [Section 6: Start-up configuration](#)):

- Source power role with accessory support
- Sink power role with accessory support
- Dual power role with accessory support
- Dual power role with accessory and Try.SRC support
- Dual power role with accessory and Try.SNK support.

3.9.1 Audio accessory mode detection

The STUSB1602 detects an audio accessory device when both the CC1 and CC2 pins are pulled down to ground by an Ra resistor from the connected device. The audio accessory detection is advertised through the CC_ATTACHED_MODE bits of the I²C register CC_CONNECTION_STATUS.

3.9.2 Debug accessory mode detection

The STUSB1602 detects a connection to a debug and test system (DTS) when it operates either in sink power role or in source power role. The debug accessory detection is advertised by the DEBUG1 and DEBUG2 pins as well as through the CC_ATTACHED_MODE bits of the I²C register CC_CONNECTION_STATUS.

- In sink power role, a debug accessory device is detected when both the CC1 and CC2 pins are pulled up by an Rp resistor from the connected device. The voltage levels on the CC1 and CC2 pins give the orientation and current capability as described in the table below. The DEBUG1 pin is asserted to advertise the DTS detection and the A_B_SIDE pin indicates the orientation of the connection. The current capability of the DTS is given through the SINK_POWER_STATE bits of the I²C register CC_OPERATION_STATUS.

Table 9. Orientation and current capability detection in sink power role

| # | CC1 pin (CC2 pin) | CC2 pin (CC1 pin) | Charging current configuration | A_B_SIDE pin CC1/CC2 (CC2/CC1) | Current capability state SINK_POWER_STATE bit values |
|---|----------------------|----------------------|--------------------------------------|--------------------------------------|---|
| 1 | Rp 3A | Rp 1.5A | Default | HiZ (0) | PowerDefault.SNK (source supplies default USB current) |
| 2 | Rp 1.5A | Rp default | 1.5 A | HiZ (0) | Power1.5.SNK (source supplies 1.5 A USB Type-C current) |
| 3 | Rp 3A | Rp default | 3.0 A | HiZ (0) | Power3.0.SNK (source supplies 3.0 A USB Type-C current) |
| 4 | Rp def/1.5A/3A | Rp def/1.5A/3A | Default | HiZ (HiZ) | PowerDefault.SNK (source supplies default USB current) |

- In source power role, a debug accessory device is detected when both the CC1 and CC2 pins are pulled down to ground by an Rd resistor from the connected device. The orientation detection is performed in two steps as described in the table below. The DEBUG2 pin is asserted to advertise the DTS detection and the A_B_SIDE pin indicates the orientation of the connection. The orientation detection is advertised through the TYPEC_FSM_STATE bits of the I²C register CC_OPERATION_STATUS.

Table 10. Orientation detection in source power role

| # | CC1 pin (CC2 pin) | CC2 pin (CC1 pin) | Detection process | A_B_SIDE pin CC1/CC2 (CC2/CC1) | Orientation detection state TYPEC_FSM_STATE bits value |
|---|----------------------|----------------------|--|--------------------------------------|---|
| 1 | Rd | Rd | 1 st step: debug accessory mode detected | HiZ (HiZ) | UnorientedDebugAccessory.SRC |
| 2 | Rd | ≤ Ra | 2 nd step: orientation detected (DTS presents a resistance to GND with a value ≤ Ra on its CC2 pin) | HiZ (0) | OrientedDebugAccessory.SRC |

4 Managing USB PD transactions

Due to specific HW/SW partitioning, the STUSB1602 requires specific alignment between the lower protocol stack (managed by the STUSB1602) and the higher protocol stack (managed by the external MCU). Therefore, dedicated read and write I²C accesses are needed to perform the following actions:

- Acknowledge a HW reset request
- Request a HW reset
- Perform a V_{CONN} SWAP
- Perform a data role SWAP
- Acknowledge a power role SWAP request
- Request a power role SWAP

5 I²C interface

5.1 Read and write operations

The I²C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I²C Bus® (version 2.1). The I²C is a slave serial interface based on two signals:

- SCL - Serial clock line: input clock used to shift data
- SDA - Serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Two 7-bit device addresses are available for the STUSB1602 thanks to external programming of DevADDR0 through ADDR0 pin setting, i.e. 0x28 or 0x29. This allows two STUSB1602 devices to be connected on the same I²C bus.

Table 11. Device address format

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------|----------|----------|----------|----------|----------|----------|------|
| DevADDR6 | DevADDR5 | DevADDR4 | DevADDR3 | DevADDR2 | DevADDR1 | DevADDR0 | R/W |
| 0 | 1 | 0 | 1 | 0 | 0 | ADDR0 | 0/1 |

Table 12. Register address format

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RegADDR7 | RegADDR6 | RegADDR5 | RegADDR4 | RegADDR3 | RegADDR2 | RegADDR1 | RegADDR0 |

Table 13. Register data format

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |

Figure 5. Read operation

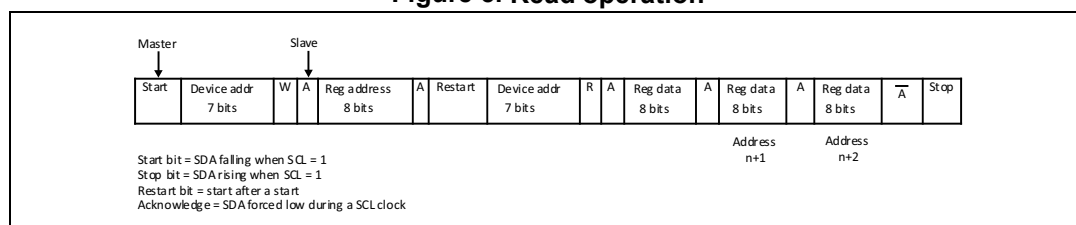
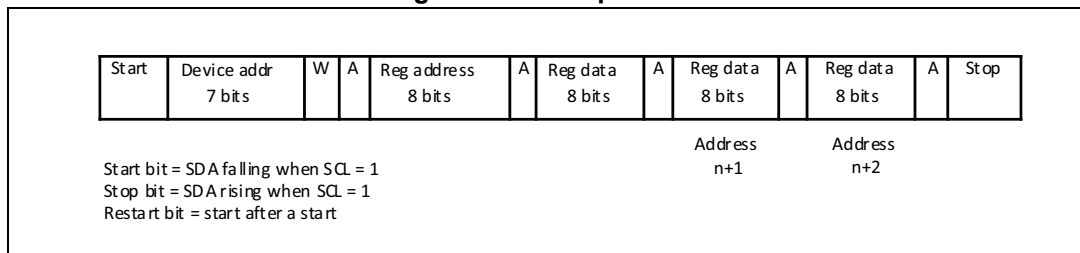


Figure 6. Write operation



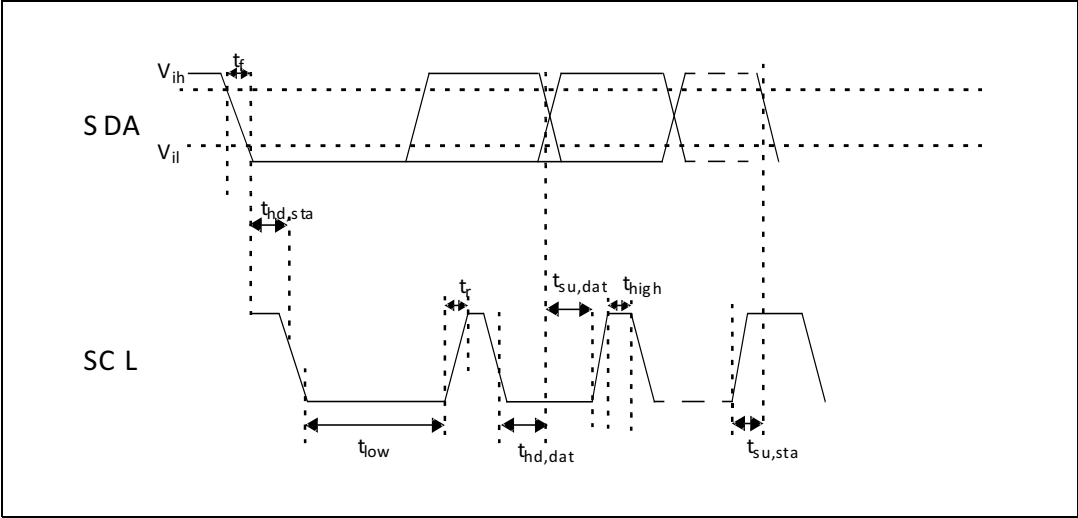
5.2 Timing specifications

The device uses a standard slave I²C channel at speed up to 400 kHz.

Table 14. I²C timing parameters - V_{DD} = 5 V

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------|--|-------------------------|------|------|------|
| F _{scl} | SCL clock frequency | 0 | — | 400 | kHz |
| t _{hd,sta} | Hold time (repeated) START condition | 0.6 | | — | μs |
| t _{low} | LOW period of the SCL clock | 1.3 | | — | |
| t _{high} | HIGH period of the SCL clock | 0.6 | | — | |
| t _{su,dat} | Setup time for repeated START condition | 0.6 | | — | |
| t _{hd,dat} | Data hold time | 0.04 | | 0.9 | |
| t _{su,dat} | Data setup time | 100 | | — | ns |
| t _r | Rise time of both SDA and SCL signals | 20 + 0.1 C _b | | 300 | |
| t _f | Fall time of both SDA and SCL signals | 20 + 0.1 C _b | | 300 | μs |
| t _{su,sto} | Setup time for STOP condition | 0.6 | | — | |
| t _{buf} | Bus free time between a STOP and START condition | 1.3 | | — | |
| C _b | Capacitive load for each bus line | — | | 400 | pF |

Figure 7. I²C timing diagram



5.3 I²C register map

Table 15. Register access legend

| Access code | Expanded name | Description |
|-------------|----------------|--|
| RO | Read only | Register can be read only |
| R/W | Read/write | Register can be read or written |
| RC | Read and clear | Register can be read and is cleared after it is read |

Table 16. STUSB1602 register map overview

| Address | Register name | Access | Description |
|------------|--|--------|---|
| 00h to 0Ah | Reserved | RO | Do not use |
| 0Bh | ALERT_STATUS | RC | Alerts register linked to transition registers |
| 0Ch | ALERT_STATUS_MASK | R/W | Allows the interrupt mask on the ALERT_STATUS register to be changed |
| 0Dh | CC_DETECTION_STATUS_TRANS | RC | Alerts about transition in CC_DETECTION_STATUS register |
| 0Eh | CC_DETECTION_STATUS | RO | CC detection status |
| 0Fh | TYPE_C_HANDSHAKE and MONITORING_STATUS_TRANS | RC | Allows Type-C FSM to be synchronized with software. Alerts about transition in MONITORING_STATUS register |
| 10h | MONITORING_STATUS | RO | Gives status on V_{BUS} and V_{CONN} voltage monitoring |
| 11h | CC_CONNECTION_STATUS | RO | CC connection status |

Table 16. STUSB1602 register map overview (continued)

| Address | Register name | Access | Description |
|------------------|----------------------------|--------|---|
| 12h | HW_FAULT_STATUS_TRANS | RC | Alerts about transition in HW_FAULT_STATUS register |
| 13h | HW_FAULT_STATUS | RO | Gives status on hardware faults |
| 14h to 17h | Reserved | RO | Do not use |
| 18h | CC_CAPABILITY_CTRL | R/W | Allows the CC capabilities to be changed |
| 19h to 1Dh | Reserved | RO | Do not use |
| 1Eh | CC_VCONN_SWITCH_CTRL | R/W | Allows the current limit of V _{CONN} power switches to be changed |
| 1Fh | TYPE_C_CTRL | R/W | Allows software to be synchronized with Type-C FSM |
| 20h | VCONN_MONITORING_CTRL | R/W | Allows the monitoring conditions of V _{CONN} voltage to be changed |
| 21h | VBUS_SELECT | R/W | Allows the DAC value related to the targeted VBUS voltage to be changed |
| 22h | VBUS_RANGE_MONITORING_CTRL | R/W | Allows the voltage range for V _{BUS} monitoring to be changed |
| 23h | RESET_CTRL | R/W | Controls the device reset by software |
| 24h | CC_POWERED_ACCESSORY_CTRL | R/W | Controls powered accessory detection |
| 25h | VBUS_DISCHARGE_TIME_CTRL | R/W | Allows the V _{BUS} discharge time to be changed |
| 26h | VBUS_DISCHARGE_CTRL | R/W | Controls the V _{BUS} discharge path |
| 27h | VBUS_ENABLE_STATUS | RO | Gives status on V _{BUS} power path activation |
| 28h | CC_POWER_MODE_CTRL | R/W | Allows the CC power mode to be changed |
| 29h to 2Dh | Reserved | RO | Do not use |
| 2Eh | VBUS_MONITORING_CTRL | R/W | Allows the monitoring conditions of V _{BUS} voltage to be changed |
| 2Fh | Reserved | RO | Do not use |

6 Start-up configuration

6.1 User-defined parameters

The STUSB1602 has a set of user-defined parameters that can be customized by NVM re-programming and/or by software through the I²C interface. This feature allows the customer to change the preset configuration of the USB Type-C interface and to define a new configuration to meet specific customer requirements addressing various applications, use cases, or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that is used at power-up or after a reset. The default value is copied at power-up, or after a reset, from the embedded NVM into dedicated I²C register bits. The NVM re-programming is possible only once with a customer password.

When a default value is changed during functioning by software, the new setting remains in effect as long as the STUSB1602 is operating or when it is changed again. But after power-off and power-up, or after a reset, the STUSB1602 takes back the default values defined in the NVM.

6.2 Default start-up configuration

The table below lists the user-defined parameters and indicates the default start-up configuration of the STUSB1602.

Three types of user-defined parameters are specified in the table with respect to the “Customization type” column:

- SW: indicates parameters that can be customized only by software through the I²C interface during system operation.
- NVM: indicates parameters that can be customized only by NVM re-programming
- NVM/SW: indicates parameters that can be customized by NVM re-programming and/or by software through the I²C interface during system operation.

Table 17. STUSB1602 user-defined parameters and default setting

| Customization type | Parameter | Default value and description | I ² C register address |
|--------------------|------------------------------|---|-----------------------------------|
| NVM/SW | CC_CONNECTION_STATUS_AL_MASK | 1b: interrupt masked | 0Ch |
| NVM/SW | MONITORING_STATUS_AL_MASK | 1b: interrupt masked | 0Ch |
| NVM/SW | HW_FAULT_STATUS_AL_MASK | 1b: interrupt masked | 0Ch |
| NVM | STANDBY_POWER_MODE_DISABLE | 1b: disables standby power mode | n. a. |
| NVM/SW | CC_CURRENT_ADVERTISED | 00b: default USB current, 500 mA or 900 mA | 18h |
| NVM/SW | CC_VCONN_DISCHARGE_EN | 0b: V _{CONN} discharge disabled on CC pin | 18h |
| NVM/SW | CC_VCONN_SUPPLY_EN | 1b: V _{CONN} supply capability enabled on CC pin | 18h |
| NVM/SW | CC_VCONN_SWITCH_ILIM | 0000b: 350 mA | 1Eh |

Table 17. STUSB1602 user-defined parameters and default setting (continued)

| Customization type | Parameter | Default value and description | I ² C register address |
|--------------------|--------------------------------|---|-----------------------------------|
| SW | VCONN_MONITORING_EN | 1b: enables UVLO threshold detection on VCONN pin | 20h |
| SW | VCONN_UVLO_THRESHOLD | 0b: high UVLO threshold of 4.65 V | 20h |
| NVM/SW | SHIFT_HIGH_VBUS_LIMIT_SOURCE | 0111b: in source power role, shifts nominal high voltage limit by 7 % of V _{BUS} | 22h |
| NVM/SW | SHIFT_LOW_VBUS_LIMIT_SOURCE | 0101b: in source power role, shifts nominal low voltage limit by -5 % of V _{BUS} | 22h |
| NVM/SW | SHIFT_HIGH_VBUS_LIMIT_SINK | 0111b: in sink power role, shifts nominal high voltage limit by 7 % of V _{BUS} | 22h |
| NVM/SW | SHIFT_LOW_VBUS_LIMIT_SINK | 1111b: in sink power role, shifts nominal low voltage limit by -15 % of V _{BUS} | 22h |
| SW | SW_RESET_EN | 0b: device reset is performed from hardware RESET pin | 23h |
| NVM/SW | VBUS_DISCHARGE_TIME_TO_0V | 1010b: 840 ms discharge time | 25h |
| NVM/SW | VBUS_DISCHARGE_TIME_TRANSITION | 1010b: 200 ms discharge time | 25h |
| NVM | VBUS_DISCHARGE_DISABLE | 0b: enables V _{BUS} discharge path | n. a. |
| NVM/SW | CC_POWER_MODE | 011b: dual power role with accessory support | 28h |
| NVM/SW | VDD_OVLO_DISABLE | 0b: enables OVLO threshold detection on VDD pin | 2Eh |
| NVM/SW | VBUS_VALID_RANGE_DISABLE | 0b: enables valid V _{BUS} voltage range detection | 2Eh |
| NVM/SW | VBUS_VSAFE0V_THRESHOLD | 00b: V _{BUS} vSafe0V threshold = 0.6 V | 2Eh |
| NVM/SW | VDD_UVLO_DISABLE | 1b: disables UVLO threshold detection on VDD pin | 2Eh |

7 Application

The sections below are not part of the ST product specification. They are intended to give a generic application overview to be used by the customer as a starting point for further implementation and customization. ST does not warrant compliancy with customer specifications. Full system implementation and validation are under the customer's responsibility.

7.1 General information

7.1.1 Power supplies

The STUSB1602 can be supplied in three different ways depending on the targeted application:

- Through the VDD pin only for applications powered by V_{BUS} that operate either in source power role or in sink power role with dead battery mode support.
- Through the VSYS pin only for AC powered applications with a system power supply delivering 3.3 V or 5 V.
- Through the VDD and VSYS pins either for applications powered by a battery with dead battery mode support or for applications powered by V_{BUS} with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V. Otherwise VDD is selected.

7.1.2 Connection to MCU or application processor

The I²C interface is used to provide extensive functionality during system operation. For instance:

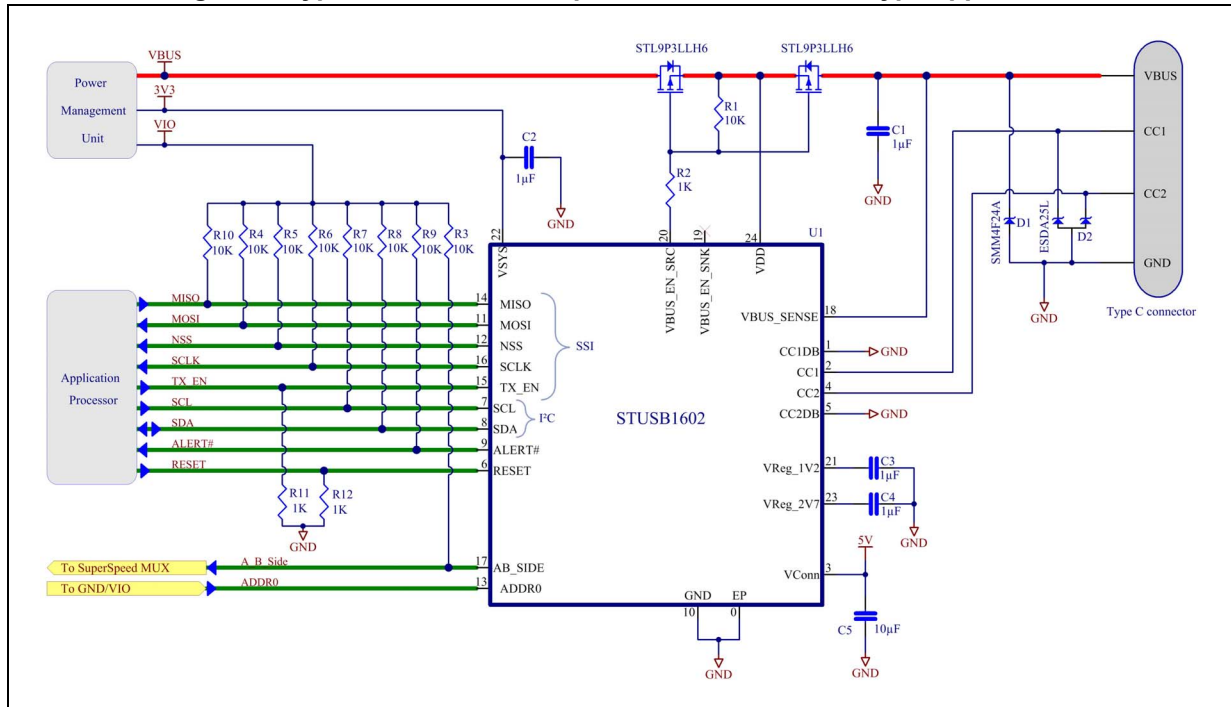
1. Define the port configuration during system boot (in case the NVM parameters are not customized during manufacturing).
2. Change the default configuration at any time during operation
3. Re-configure the port power mode (i.e. source, sink or dual role)
4. Adjust the port power capability in source power role according to contextual power availability and/or the power partitioning with other ports.
5. Save system power by shutting down the DC-DC converter according to the attachment detection state.
6. Provide a diagnostic of the Type-C connection and the VBUS power path in real time

7.2 USB Type-C typical applications

7.2.1 Source type application

Application schematic

Figure 8. Typical STUSB1602 implementation in source type application



Default start-up configuration

Table 18. Default setting for a source type application

| I ² C register address | I ² C register field name | I ² C register reset value/description | Customization type |
|-----------------------------------|--------------------------------------|---|--------------------|
| 0Eh | START_UP_POWER_MODE | 0b: device starts in normal mode | NVM/SW |
| 18h | CC_CURRENT_ADVERTISED | 00b: default USB current (500 mA or 900 mA) | NVM/SW |
| 18h | CC_VCONN_DISCHARGE_EN | 0b: VCONN discharge disabled on CC pin | NVM/SW |
| 18h | CC_VCONN_SUPPLY_EN | 1b: VCONN supply capability enabled on CC pin | NVM/SW |
| 1Eh | CC_VCONN_SWITCH_ILIM | 0000b: 350 mA | NVM/SW |
| 1Fh | POWER_MODE | 0000b: source power role with accessory support ⁽¹⁾ | NVM/SW |
| 20h | VCONN_MONITORING_EN | 1b: enables UVLO threshold detection on VCONN pin | SW |
| 20h | VCONN_UVLO_THRESHOLD | 0b: high UVLO threshold of 4.65 V | SW |
| 21h | VBUS_SELECT | 0032b: 5V DAC value related to targeted VBUS | SW |
| 22h | VBUS_VSHIFT_HIGH | 1010b: 5 % plus the high threshold value | NVM/FSM/SW |
| 22h | VBUS_VSHIFT_LOW | 1010b: 5 % minus the low threshold value | NVM/FSM/SW |
| 24h | PWR_ACC_DETECT_EN | Not applicable | NVM/SW |
| 25h | VBUS_DISCHARGE_TIME_TO_0V | 1010b: 840 ms discharge time | NVM/SW |
| 25h | VBUS_DISCHARGE_TIME_TRANSITION | 1010b: 200 ms discharge time | NVM/SW |
| 26h | VBUS_DISCHARGE_EN | 1b: enables the VBUS discharge path | NVM/SW |
| 2Eh | VDD_OVLO_DISABLE | 0b: enables OVLO threshold detection on VDD pin | SW |
| 2Eh | VBUS_RANGE_DISABLE | 0b: enables V _{BUS} voltage range detection | SW |
| 2Eh | VBUS_VSAFE0V_THRESHOLD | 00b: V _{BUS} vSafe0V threshold = 0.6 V | SW |
| 2Eh | VDD_UVLO_DISABLE | 1b: disables UVLO threshold detection on VDD pin | SW |

1. Italic text indicates this parameter is customized by NVM re-programming

V_{BUS} power path assertion**Table 19. Conditions for V_{BUS} power path assertion in source power role**

| Pin | Electrical value | Operation conditions | | | Comment |
|-------------|------------------|--|-----------------------------------|--|---|
| | | Type-C attached state | VDD pin monitoring | VBUS_SENSE pin monitoring | |
| VBUS_EN_SRC | 0 | Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC | VDD < OVLO if VDD pin is supplied | V _{BUS} within valid voltage range | The signal is asserted only if all the valid operation conditions are met |
| | HiZ | Any other state | VDD > OVLO if VDD pin is supplied | V _{BUS} is out of valid voltage range | The signal is de-asserted when at least one non valid operation condition is met. |

Device state according to application state

Table 20. Source power role with accessory support

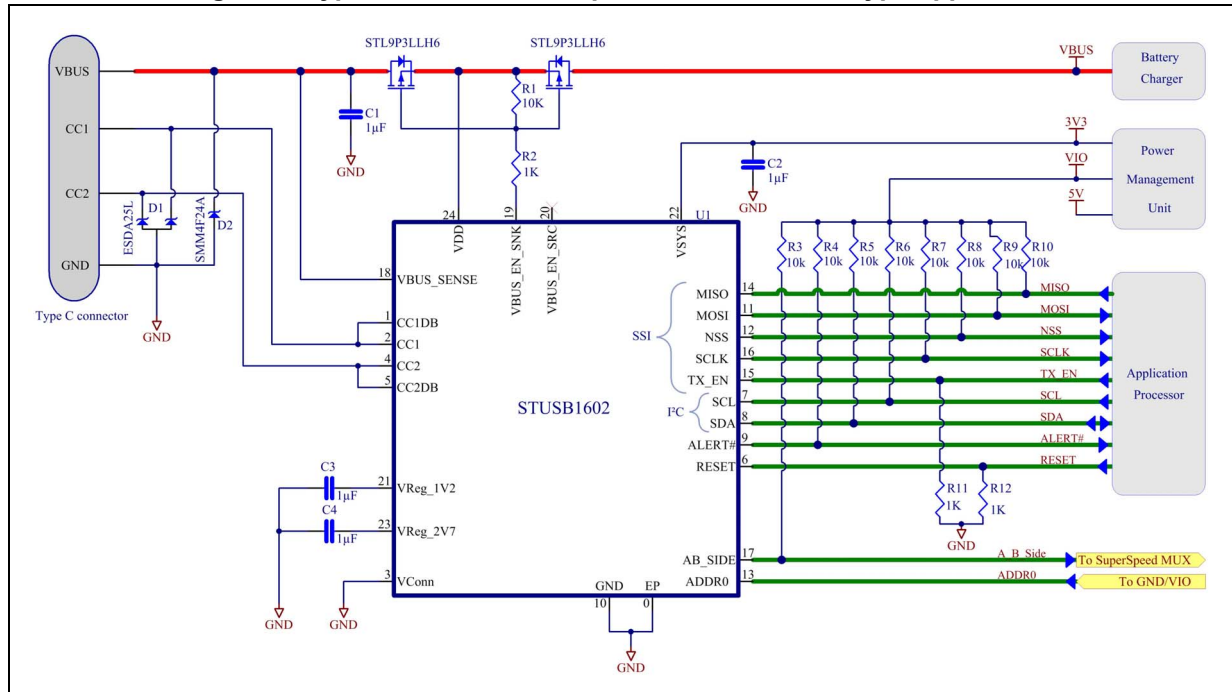
| Connection state | CC1 pin | CC2 pin | Type-C device state CC_OPERATION_STATUS register @11h | A_B_SIDE pin | VCONN supply | VBUS_EN_SRC pin | CC_CONNECTION_STATUS register @0Eh |
|--|---------|---------|--|--------------|--------------|-----------------|------------------------------------|
| Nothing attached | Open | Open | Unattached.SRC | HiZ | OFF | HiZ | 00h |
| Sink attached | Rd | Open | Attached.SRC | HiZ | OFF | 0 | 2Dh |
| | Open | Rd | | 0 | OFF | 0 | 2Dh |
| Powered cable without sink attached | Open | Ra | Unattached.SRC | HiZ | OFF | HiZ | 00h |
| | Ra | Open | | HiZ | OFF | HiZ | 00h |
| Powered cable with sink attached or VCONN-powered accessory attached | Rd | Ra | Attached.SRC | HiZ | CC2 | 0 | 2Fh |
| | Ra | Rd | | 0 | CC1 | 0 | 2Fh |
| Debug accessory mode attached source role | Rp | Rp | Unattached.SRC | HiZ | OFF | HiZ | 00h |
| Debug accessory mode attached sink role | Rd | Rd | UnorientedDebug Accessory.SRC | HiZ | OFF | 0 | 6Dh |
| Debug accessory mode attached sink role | Rd | ≤ Ra | OrientedDebug Accessory.SRC | HiZ | OFF | 0 | 6Dh |
| | ≤ Ra | Rd | | 0 | OFF | 0 | 6Dh |
| Audio adapter accessory mode attached | Ra | Ra | Audio accessory | HiZ | OFF | HiZ | 81h |

The value of the CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device. The CC_CONNECTION_STATUS register can report other values than the one presented in [Table 20](#). In this table, it reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

7.2.2 Sink type application

Application schematic

Figure 9. Typical STUSB1602 implementation in sink type application



Default start-up configuration

Table 21. Default setting for a sink type application

| I ² C register address | I ² C register field name | I ² C register reset value/description | Customization type |
|-----------------------------------|--------------------------------------|--|--------------------|
| 0Eh | START_UP_POWER_MODE | 0b: device starts in normal mode | NVM/SW |
| 18h | CC_CURRENT_ADVERTISED | Not applicable | NVM/SW |
| 18h | CC_VCONN_DISCHARGE_EN | Not applicable | NVM/SW |
| 18h | CC_VCONN_SUPPLY_EN | Not applicable | NVM/SW |
| 1Eh | CC_VCONN_SWITCH_ILIM | Not applicable | NVM/SW |
| 1Fh | POWER_MODE | 001b: sink power role with accessory support ⁽¹⁾ | NVM/SW |
| 20h | VCONN_MONITORING_EN | Not applicable | SW |
| 20h | VCONN_UVLO_THRESHOLD | Not applicable | SW |
| 21h | VBUS_SELECT | 0032b: 5V DAC value related to targeted VBUS | FSM/SW |
| 22h | VBUS_VSHIFT_HIGH | 1010b: 5 % plus the high threshold value | NVM/FSM/SW |
| 22h | VBUS_VSHIFT_LOW | 1010b: 5 % minus the low threshold value | NVM/FSM/SW |
| 24h | PWR_ACC_DETECT_EN | 1b: enables the powered accessory detection | NVM/SW |
| 25h | VBUS_DISCHARGE_TIME_TO_0V | 1010b: 840 ms discharge time | NVM/SW |
| 25h | VBUS_DISCHARGE_TIME_TRANSITION | 1010b: 200 ms discharge time | NVM/SW |
| 26h | VBUS_DISCHARGE_EN | 1b: enables the VBUS discharge path | NVM/SW |
| 2Eh | VDD_OVLO_DISABLE | Not applicable | SW |
| 2Eh | VBUS_RANGE_DISABLE | 0b: enables V _{BUS} voltage range detection | SW |
| 2Eh | VBUS_VSAFE0V_THRESHOLD | Not applicable | SW |
| 2Eh | VDD_UVLO_DISABLE | Not applicable | SW |

1. Italic text indicates this parameter is customized by NVM re-programming

V_{BUS} power path assertion**Table 22. Conditions for V_{BUS} power path assertion in sink power role**

| Pin | Electrical value | Operation conditions | | | Comment |
|-------------|------------------|--|--------------------|--|---|
| | | Type-C attached state | VDD pin monitoring | VBUS_SENSE pin monitoring | |
| VBUS_EN_SNK | 0 | Attached.SNK or Debug Accessory.SNK | Not applicable | V _{BUS} is within valid voltage range | The signal is asserted only if all the valid operation conditions are met |
| | HiZ | Any other state | Not applicable | V _{BUS} is out of valid voltage range | The signal is de-asserted when at least one non valid operation condition is met. |

Device state according to application state

Table 23. Sink power role with accessory support

| Connection state | CC1 pin | CC2 pin | Type-C device state CC_OPERATION_STATUS register @11h | A_B_SIDE pin | VCONN supply | VBUS_EN_SNK pin | CC_CONNECTION_STATUS register @0Eh |
|---|------------------|------------------|--|--------------|--------------|-----------------|------------------------------------|
| Nothing attached | Open | Open | (Toggling) Unattached.SNK Unattached.Accessory | HiZ | OFF | HiZ | 00h |
| Source attached | Rp | Open or Ra | Attached.SNK | HiZ | OFF | 0 | 41h |
| | Open or Ra | Rp | | 0 | OFF | 0 | 41h |
| Powered cable without source attached | Open | Ra | (Toggling) Unattached.SNK Unattached.Accessory | HiZ | OFF | HiZ | 00h |
| | Ra | Open | | HiZ | OFF | HiZ | 00h |
| Debug accessory mode attached sink role | Rd | Rd | (Toggling) Unattached.SNK Unattached.Accessory | HiZ | OFF | HiZ | 00h |
| Debug accessory mode attached source role | Rp Def/ 1.5A/ 3A | Rp Def/ 1.5A/ 3A | Debug Accessory.SNK (Default USB) | HiZ | OFF | 0 | 61h |
| Debug accessory mode attached source role | Rp 3A | Rp 1.5A | Debug Accessory.SNK (Default USB) | HiZ | OFF | 0 | 61h |
| | Rp 1.5A | Rp 3A | | 0 | OFF | 0 | 61h |
| Debug accessory mode attached source role | Rp 1.5A | Rp def. | Debug Accessory.SNK (1.5 A) | HiZ | OFF | 0 | 61h |
| | Rp def. | Rp 1.5A | | 0 | OFF | 0 | 61h |
| Debug accessory mode attached source role | Rp 3A | Rp def. | Debug Accessory.SNK (3.0 A) | HiZ | OFF | 0 | 61h |
| | Rp def. | Rp 3A | | 0 | OFF | 0 | 61h |
| Audio adapter accessory mode attached | Ra | Ra | Audio accessory | HiZ | OFF | HiZ | 81h |

Table 23. Sink power role with accessory support (continued)

| Connection state | CC1 pin | CC2 pin | Type-C device state CC_OPERATION_STATUS register @11h | A_B_SIDE pin | VCONN supply | VBUS_EN_SNK pin | CC_CONNECTION_STATUS register @0Eh |
|----------------------------------|---------|---------|--|--------------|--------------|-----------------|------------------------------------|
| VCONN-powered accessory attached | Rd | Ra | (Toggling) Unattached.SNK Unattached.Accessory | HiZ | OFF | HiZ | 00h |
| | Ra | Rd | | HiZ | OFF | HiZ | 00h |

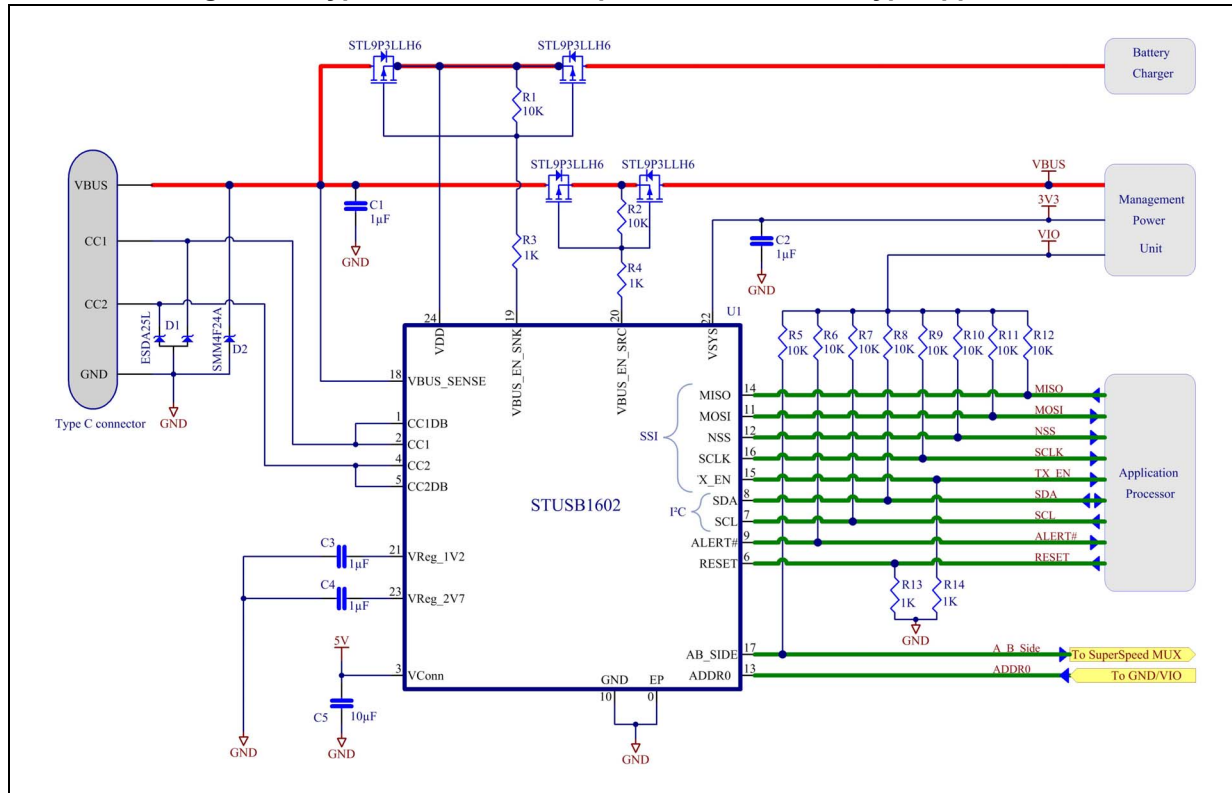
The value of the CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device.

The CC_CONNECTION_STATUS register can report other values than the one presented in [Table 23](#). In this table, it reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

7.2.3 Dual role type application

Application schematic

Figure 10. Typical STUSB1602 implementation in dual type application



Note: Schematic configuration is in dead battery mode

Default start-up configuration

Table 24. Default setting for a dual type application

| I ² C register address | I ² C register field name | I ² C register reset value/description | Customization type |
|-----------------------------------|--------------------------------------|--|--------------------|
| 0Eh | START_UP_POWER_MODE | 0b: device starts in normal mode | NVM/SW |
| 18h | CC_CURRENT_ADVERTISED | 00b: default USB current (500 mA or 900 mA) | NVM/SW |
| 18h | CC_VCONN_DISCHARGE_EN | 0b: VCONN discharge disabled on CC pin | NVM/SW |
| 18h | CC_VCONN_SUPPLY_EN | 1b: VCONN supply capability enabled on CC pin | NVM/SW |
| 1Eh | CC_VCONN_SWITCH_ILIM | 0000b: 350 mA | NVM/SW |
| 1Fh | POWER_MODE | 011b: dual power role with accessory support ⁽¹⁾ | NVM/SW |
| 20h | VCONN_MONITORING_EN | 1b: enables UVLO threshold detection on VCONN pin | SW |
| 20h | VCONN_UVLO_THRESHOLD | 0b: high UVLO threshold of 4.65 V | SW |
| 21h | VBUS_SELECT | 0032b: 5V DAC value related to targeted VBUS | SW |
| 22h | VBUS_VSHIFT_HIGH | 1010b: 5 % plus the high threshold value | NVM/FSM/SW |
| 22h | VBUS_VSHIFT_LOW | 1010b: 5 % minus the low threshold value | NVM/FSM/SW |
| 24h | PWR_ACC_DETECT_EN | Not applicable | NVM/SW |
| 25h | VBUS_DISCHARGE_TIME_TO_0V | 1010b: 840 ms discharge time | NVM/SW |
| 25h | VBUS_DISCHARGE_TIME_TRANSITION | 1010b: 200 ms discharge time | NVM/SW |
| 26h | VBUS_DISCHARGE_EN | 1b: enables the VBUS discharge path | NVM/SW |
| 2Eh | VDD_OVLO_DISABLE | 0b: enables OVLO threshold detection on VDD pin | SW |
| 2Eh | VBUS_RANGE_DISABLE | 0b: enables V _{BUS} voltage range detection | SW |
| 2Eh | VBUS_VSAFE0V_THRESHOLD | 00b: V _{BUS} vSafe0V threshold = 0.6 V | SW |
| 2Eh | VDD_UVLO_DISABLE | 1b: disables UVLO threshold detection on VDD pin | SW |

1. Italic text indicates this parameter is customized by NVM re-programming

V_{BUS} power path assertion**Table 25. Conditions for V_{BUS} power path assertion in source power role**

| Pin | Electrical value | Operation conditions | | | Comment |
|-------------|------------------|--|---|---|---|
| | | Type-C attached state | VDD pin monitoring | VBUS_SENSE pin monitoring | |
| VBUS_EN_SRC | 0 | Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC | VDD < OVLO if VDD pin is supplied | V _{BUS} is within valid voltage range | The signal is asserted only if all the valid operation conditions are met |
| | HiZ | Any other state | VDD > OVLO if VDD pin is supplied | V _{BUS} is out of valid voltage range | The signal is de-asserted when at least one non valid operation condition is met. |

Table 26. Conditions for V_{BUS} power path assertion in sink power role

| Pin | Electrical value | Operation conditions | | | Comment |
|-------------|------------------|--|--------------------|---|---|
| | | Type-C attached state | VDD pin monitoring | VBUS_SENSE pin monitoring | |
| VBUS_EN_SNK | 0 | Attached.SNK or Debug Accessory.SNK | Not applicable | V _{BUS} is within valid voltage range | The signal is asserted only if all the valid operation conditions are met |
| | HiZ | Any other state | Not applicable | V _{BUS} is out of valid voltage range | The signal is de-asserted when at least one non valid operation condition is met. |

Device state according to application state

Table 27. Dual power role with accessory support

| Connection state | CC1 pin | CC2 pin | Type-C device state CC_OPERATION_STATUS register @11h | A_B_SIDE pin | VCONN supply | VBUS_EN_SRC pin | VBUS_EN_SNK pin | CC_CONNECTION_STATUS register @0Eh |
|--|------------------|------------------|--|--------------|--------------|-----------------|-----------------|------------------------------------|
| Nothing attached | Open | Open | (Toggling) Unattached.SRC Unattached.SNK | HiZ | OFF | HiZ | HiZ | 00h |
| Sink attached | Rd | Open | Attached.SRC | HiZ | OFF | 0 | HiZ | 2Dh |
| | Open | Rd | | 0 | OFF | 0 | HiZ | 2Dh |
| Powered cable without sink or source attached | Open | Ra | (Toggling) Unattached.SRC Unattached.SNK | HiZ | OFF | HiZ | HiZ | 00h |
| | Ra | Open | | HiZ | OFF | HiZ | HiZ | 00h |
| Powered cable with sink attached or VCONN-powered accessory attached | Rd | Ra | Attached.SRC | HiZ | CC2 | 0 | HiZ | 2Fh |
| | Ra | Rd | | 0 | CC1 | 0 | HiZ | 2Fh |
| Debug accessory mode attached sink role | Rd | Rd | UnorientedDebug Accessory.SRC | HiZ | OFF | 0 | HiZ | 6Dh |
| Debug accessory mode attached sink role | Rd | ≤ Ra | OrientedDebug Accessory.SRC | HiZ | OFF | 0 | HiZ | 6Dh |
| | ≤ Ra | Rd | | 0 | OFF | 0 | HiZ | 6Dh |
| Audio adapter accessory mode attached | Ra | Ra | Audio accessory | HiZ | OFF | HiZ | HiZ | 81h |
| Source attached | Rp | Open or Ra | Attached.SNK | HiZ | OFF | HiZ | 0 | 41h |
| | Open or Ra | Rp | | 0 | OFF | HiZ | 0 | 41h |
| Debug accessory mode attached source role | Rp def/ 1.5A/ 3A | Rp def/ 1.5A/ 3A | Debug Accessory.SNK (Default USB) | HiZ | OFF | HiZ | 0 | 61h |

Table 27. Dual power role with accessory support (continued)

| Connection state | CC1 pin | CC2 pin | Type-C device state CC_OPERATION_STATUS register @11h | A_B_SIDE pin | VCONN supply | VBUS_EN_SRC pin | VBUS_EN_SNK pin | CC_CONNECTION_STATUS register @0Eh |
|---|---------|---------|--|--------------|--------------|-----------------|-----------------|------------------------------------|
| Debug accessory mode attached source role | Rp 3A | Rp 1.5A | Debug Accessory.SNK (Default USB) | HiZ | OFF | HiZ | 0 | 61h |
| | Rp 1.5A | Rp 3A | | 0 | OFF | HiZ | 0 | 61h |
| Debug accessory mode attached source role | Rp 1.5A | Rp def. | Debug Accessory.SNK (1.5 A) | HiZ | OFF | HiZ | 0 | 61h |
| | Rp def. | Rp 1.5A | | 0 | OFF | HiZ | 0 | 61h |
| Debug accessory mode attached source role | Rp 3A | Rp def. | Debug Accessory.SNK (3.0 A) | HiZ | OFF | HiZ | 0 | 61h |
| | Rp def. | Rp 3A | | 0 | OFF | HiZ | 0 | 61h |

The value of the CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device.

The CC_CONNECTION_STATUS register can report other values than the one presented in [Table 27](#). In this table, it reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

8 Electrical characteristics

8.1 Absolute maximum ratings

All voltages are referenced to GND.

Table 28. Absolute maximum ratings

| Symbol | Parameter | Value. | Unit |
|--|--|------------|------|
| V_{DD} | Supply voltage | 28 | V |
| V_{SYS} | Supply voltage on VSYS pin | 6 | |
| V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB} | High voltage on CC pins | 22 | |
| $V_{VBUS_EN_SRC}$ $V_{VBUS_EN_SNK}$ V_{VBUS_SENSE} | High voltage on VBUS pins | 28 | |
| V_{SCL}, V_{SDA} $V_{ALERT\#}$ V_{RESET} $V_{A_B_SIDE}$ | Operating voltage on I/O pins | -0.3 to 6 | |
| V_{CONN} | V_{CONN} voltage | 6 | °C |
| T_{STG} | Storage temperature | -55 to 150 | |
| T_J | Maximum junction temperature | 145 | |
| ESD | Electrostatic discharge CDM: contact discharge model - IEC61000-4-2 | 4 | kV |

8.2 Operating conditions

Table 29. Operating conditions

| Symbol | Parameter | Value | Unit |
|--|---|-------------|------|
| V_{DD} | Supply voltage | 4.1 to 22 | V |
| V_{SYS} | Supply voltage on V_{SYS} pin | 3.0 to 5.5 | |
| V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB} | CC pins | -0.3 to 5.5 | |
| $V_{VBUS_EN_SRC}$ $V_{VBUS_EN_SNK}$ V_{VBUS_SENSE} | High voltage pins | 0 to 22 | |
| V_{SCL}, V_{SDA} $V_{ALERT\#}$ V_{RESET} $V_{A_B_SIDE}$ | Operating voltage on I/O pins | 0 to 4.5 | |
| V_{CONN} | V_{CONN} voltage | 2.7 to 5.5 | A |
| I_{CONN} | V_{CONN} rated current (default = 0.35 A) | 0.1 to 0.6 | |
| T_A | Operating temperature | -40 to 105 | °C |

Note: The transient voltage on the CC1 and CC2 pins is allowed to drop to -0.3 during BMC communication.

8.3 Electrical and timing characteristics

Unless otherwise specified: $V_{DD} = 5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, all voltages are referenced to GND.

Table 30. Electrical characteristics

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|-----------------------|--|---|--------------------------|------|-------|------|------|
| I _{DD} (SRC) | Current consumption | Device idle as a SOURCE (not connected, no communication) | V _{SYS} @ 3.3 V | | 158 | | μA |
| | | | V _{DD} @ 5.0 V | | 188 | | |
| I _{DD} (SNK) | Current consumption | Device idle as a SINK (not connected, no communication) | V _{SYS} @ 3.3 V | | 113 | | |
| | | | V _{DD} @ 5.0 V | | 140 | | |
| I _{STDBY} | Standby current consumption | Device in standby (not connected, low power) | V _{SYS} @ 3.3 V | | 33 | | |
| | | | V _{DD} @ 5.0 V | | 53 | | |
| CC1 and CC2 pins | | | | | | | |
| I _{P-USB} | CC current sources | CC pin voltage, V _{CC} = -0.3 to 2.6 V, 40 °C < T _A < 105 °C | -20% | 80 | +20 % | uA | |
| I _{P-1.5} | | | -8% | 180 | +8 % | | |
| I _{P-3.0} | | | -8% | 330 | +8 % | | |
| V _{CCO} | CC open pin voltage | CC unconnected, V _{DD} = 3.0 to 5.5 V | 2.75 | | | V | |
| R _d | CC pull-down resistors | -40 °C < T _A < 105 °C | -10% | 5.1 | +10 % | kΩ | |
| V _{CCDB-1.5} | CC pin voltage in dead battery condition | External I _P = 180 μA applied into CC, V _{DD} = 0 V, dead-battery function enabled | | | 1.2 | V | |
| V _{CCDB-3.0} | | External I _P = 330 μA applied into CC, V _{DD} = 0 V, dead-battery function enabled | | | 2.0 | | |
| R _{INCC} | CC input impedance | Pull-up and pull-down resistors off | 200 | | | kΩ | |
| V _{TH0.2} | Detection threshold 1 | Max R _a detection by DFP at I _P = I _{P-USB} , min I _{P-USB} detection by UFP on R _d , min CC voltage for connected UFP | 0.15 | 0.20 | 0.25 | V | |
| V _{TH0.4} | Detection threshold 2 | Max R _a detection by DFP at I _P = I _{P-1.5} | 0.35 | 0.40 | 0.45 | | |
| V _{TH0.66} | Detection threshold 3 | Min I _{P-1.5} detection by UFP on R _d | 0.61 | 0.66 | 0.70 | | |
| V _{TH0.8} | Detection threshold 4 | Max R _a detection by DFP at I _P = I _{P-3.0} | 0.75 | 0.80 | 0.85 | | |
| V _{TH1.23} | Detection threshold 5 | Min I _{P-3.0} detection by UFP on R _d | 1.16 | 1.23 | 1.31 | | |
| V _{TH1.6} | Detection threshold 6 | Max R _d detection by DFP at I _P = I _{P-USB} and I _P = I _{P-1.5} | 1.50 | 1.60 | 1.65 | | |

Table 30. Electrical characteristics (continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|--|--|-------------------|-------------------------|--------------------|------|
| V _{TH2.6} | Detection threshold 7 | Max R _d detection by DFP at I _{P-3.0} , max CC voltage for connected UFP | 2.45 | 2.60 | 2.75 | V |
| V _{CONN} protection | | | | | | |
| R _{VCONN} | VCONN path resistance | I _{VCONN} = 0.2 A, | 0.25 | 0.5 | 0.975 | Ω |
| I _{OCP} | Overcurrent protection | Programmable current limit threshold (from 100 mA to 600 mA by step of 50 mA) | 85 | 100 | 125 | mA |
| | | | 300 | 350 | 400 | |
| | | | 550 | 600 | 650 | |
| V _{OVP} | Output-over voltage protection | | 5.9 | 6 | 6.1 | V |
| V _{UVP} | Input undervoltage protection | Low UVLO threshold | 2.6 | | 2.7 | |
| | | High UVLO threshold (default) | 4.6 | | 4.8 | |
| VBUS monitoring and driving | | | | | | |
| V _{THUSB} | V _{BUS} presence threshold | V _{SYS} = 3.0 to 5.5 V | 3.8 | 3.9 | 4.0 | V |
| V _{THOV} | V _{BUS} safe 0 V threshold (vSafe0V) | V _{SYS} = 3.0 to 5.5 V | 0.5 | 0.6 | 0.7 | |
| | | Programmable threshold | 0.8 | 0.9 | 1.0 | |
| | | Programmable threshold from 0.6 V to 1.8 V | 1.1 | 1.2 | 1.3 | |
| | | Default V _{THOV} = 0.6 V | 1.7 | 1.8 | 1.9 | |
| R _{DISUSB} | V _{BUS} discharge resistor | | 600 | 700 | 800 | Ω |
| T _{DISUSB} | V _{BUS} discharge time to 0V | Default T _{DISPARAM} = 840 ms, the co-efficient T _{DISPARAM} is programmable by NVM | 70 ⁽¹⁾ | 84 ⁽¹⁾ | 100 ⁽¹⁾ | ms |
| | V _{BUS} discharge time to PDO | Default T _{DISPARAM} = 200 ms, the co-efficient T _{DISPARAM} is programmable by NVM | 20 ⁽¹⁾ | 24 ⁽¹⁾ | 28 ⁽¹⁾ | |
| V _{MONUSBH} | V _{BUS} monitoring high voltage threshold | V _{BUS} = nominal target value, default V _{MONUSBH} = V _{BUS} + 10 %, the threshold limit is programmable by NVM from +5 % to +20 % | | V _{BUS} + 10 % | | V |
| V _{MONUSBL} | V _{BUS} monitoring low voltage threshold | V _{BUS} = nominal target value, default V _{MONUSBL} = V _{BUS} - 10 %, the threshold limit is programmable by NVM from -20 % to -5 % | | V _{BUS} - 10 % | | |
| Digital input/output (SCL, SDA, ALERT#, A_B_SIDE) | | | | | | |
| V _{IH} | High level input voltage | | 1.2 | | | V |
| V _{IL} | Low level input voltage | | | | 0.35 | |
| V _{OL} | Low level output voltage | I _{oh} = 3 mA | | | 0.4 | |

Table 30. Electrical characteristics (continued)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|--------------------------|------------------------|------|------|------|------|
| 20 V open drain outputs (VBUS_EN_SRC, VBUS_EN_SNK) | | | | | | |
| V _{OL} | Low level output voltage | I _{oh} = 3 mA | | | 0.4 | V |

1. T_{DISPARAM}

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.1 QFN24 EP 4x4 mm package information

Figure 11. QFN24 EP 4x4 mm package outline

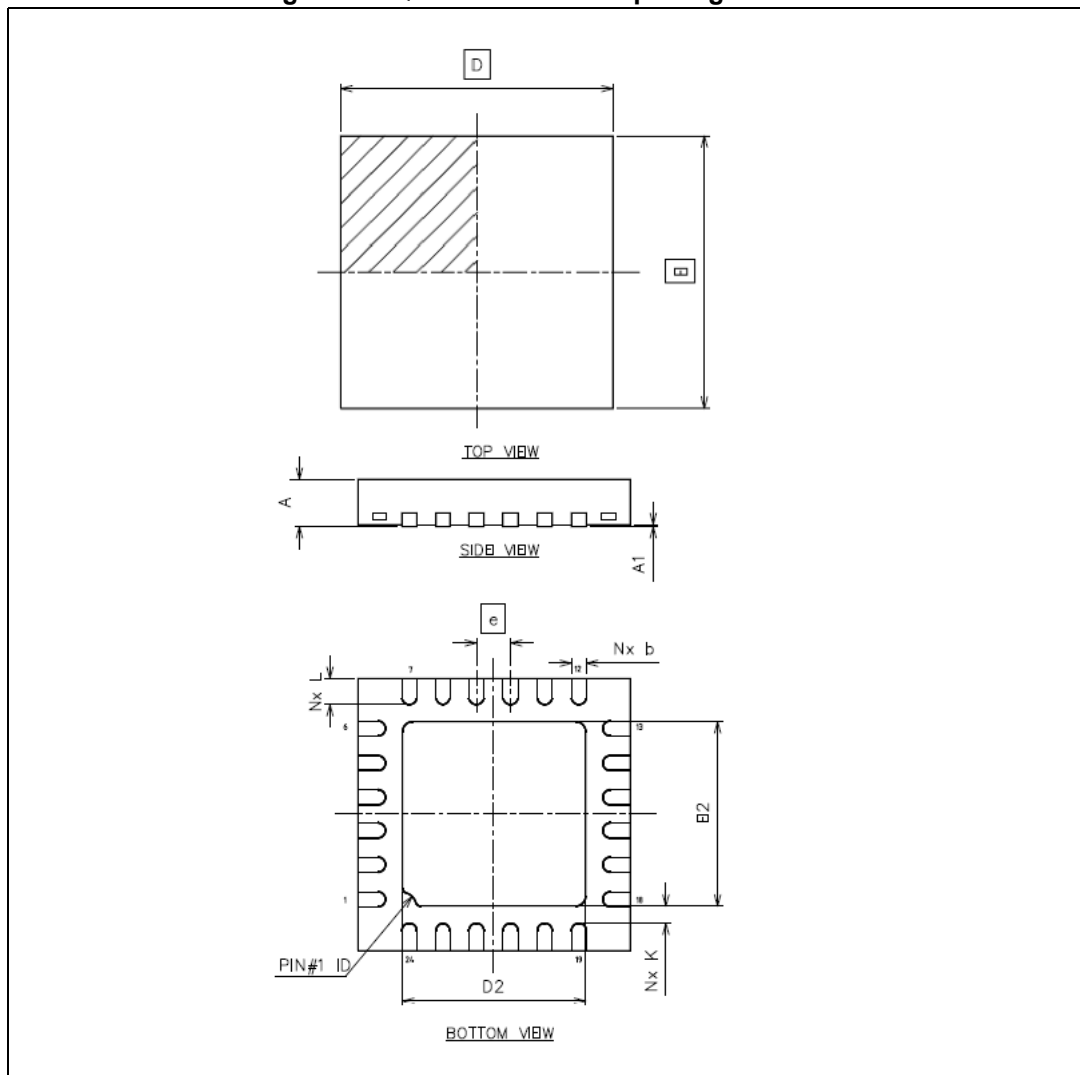
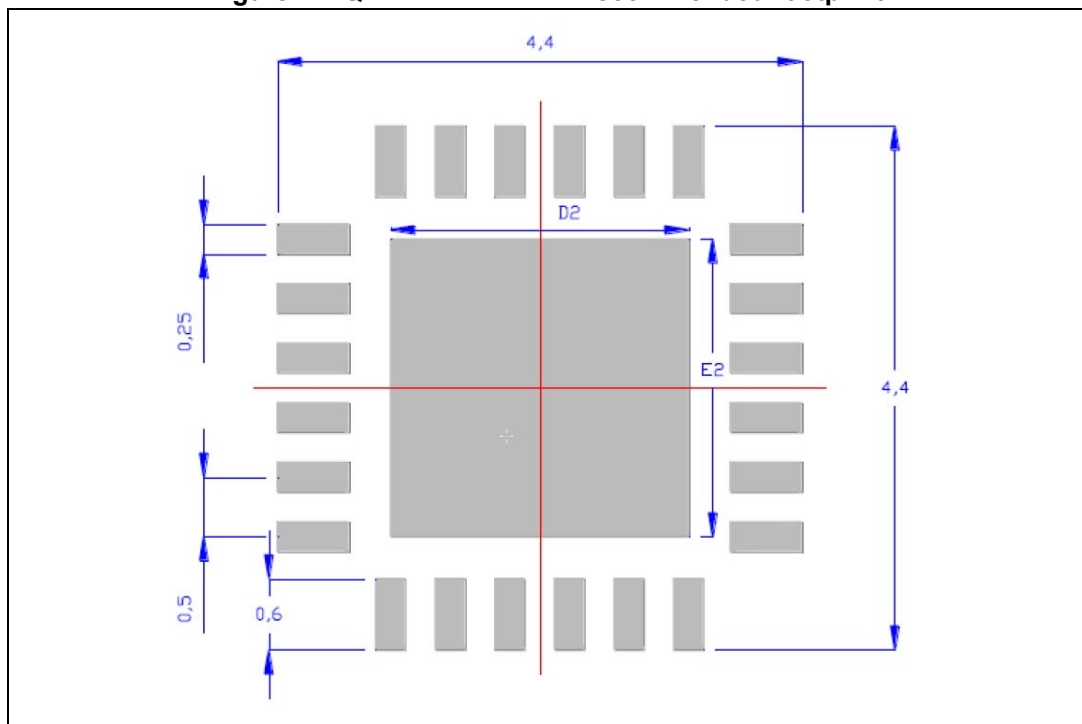


Table 31. QFN24 EP 4x4 mm mechanical data

| Ref. | Millimeters | | | Inches | | |
|------|-------------|------|------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D | 3.95 | 4.00 | 4.05 | 0.156 | 0.157 | 0.159 |
| D2 | 2.55 | 2.70 | 2.80 | 0.100 | 0.106 | 0.110 |
| E | 3.95 | 4.00 | 4.05 | 0.156 | 0.157 | 0.159 |
| E2 | 2.55 | 2.70 | 2.80 | 0.100 | 0.106 | 0.110 |
| e | 0.45 | 0.50 | 0.55 | 0.018 | 0.020 | 0.022 |
| K | 0.15 | — | — | 0.006 | — | — |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

Figure 12. QFN24 EP 4x4 mm recommended footprint



9.2 Thermal Information

Table 32. Thermal information

| Symbol | Parameter | Value | Unit |
|-----------------|--|-------|------|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 37 | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | 5 | |

9.3 Packing information

Figure 13. Reel information

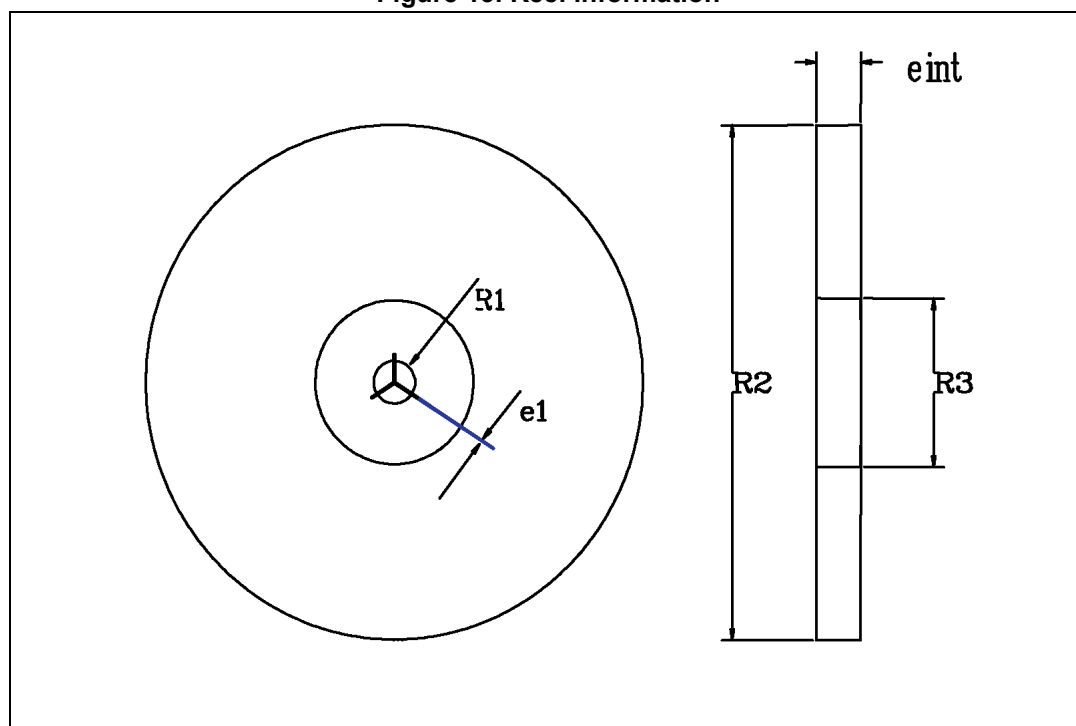


Table 33. Tape dimensions

| Package | Pitch | Carrier width | Reel |
|--------------|-------|---------------|------|
| QFN24 EP 4x4 | 8 mm | 12 mm | 13" |

10 Terms and abbreviations

Table 34. List of terms and abbreviations

| Term | Description |
|-----------------|---|
| Accessory modes | Audio adapter accessory mode. It is defined by the presence of Ra/Ra on the CC1/CC2 pins. |
| | Debug accessory mode. It is defined by the presence of Rd/Rd on CC1/CC2 pins in source power role or Rp/Rp on CC1/CC2 pins in sink power role. |
| DFP | Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically, the ports on a HOST or the ports on a hub to which devices are connected. In its initial state, the DFP sources V_{BUS} and V_{CONN} , and supports data. |
| DRP | Dual-role port. A port that can operate as either a source or a sink. The port's role may be changed dynamically. |
| Sink | Port asserting Rd on the CC pins and consuming power from the V_{BUS} ; most commonly a device. |
| Source | Port asserting Rp on the CC pins and providing power over the V_{BUS} ; most commonly a host or hub DFP. |
| UFP | Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks the V_{BUS} and supports data. |

11 Revision history

Table 35. Document revision history

| Date | Revision | Changes |
|-------------|----------|-----------------|
| 27-Jan-2017 | 1 | Initial release |



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