

April 2009

HCPL0700, HCPL0701, HCPL0730, HCPL0731 Low Input Current High Gain Split Darlington Optocouplers

Single Channel: HCPL0700, HCPL0701, Dual Channel: HCPL0730, HCPL0731

Features

- Low input current: 0.5mA
- Superior CTR: 2000%
- Superior CMR 10 kV/µs
- CTR guaranteed 0°C to 70°C
- U.L. Recognized (file# E90700)
- VDE 0884 recognized (file# 136616)– approval pending for HCPL0730/0731
- BSI recognized (file# 8661, 8662) - HCPL0700/0701 only

Applications

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- µP bus isolation
- Current loop receiver

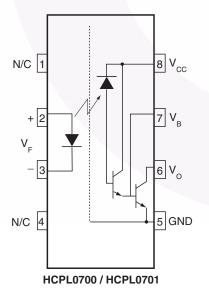
Description

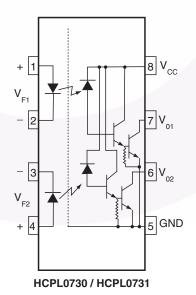
The HCPL0700, HCPL0701, HCPL0730 and HCPL0731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector housed in a compact 8-pin small outline package. The HCPL0730 and HCPL0731 devices have two channels per package for optimum mounting density.

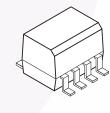
The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler.

The combination of a very low input current of 0.5mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

Schematics







Truth Table

LED	Vo
ON	LOW
OFF	HIGH

Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Paramet	Value	Units	
T _{STG}	Storage Temperature	-40 to +125	°C	
T _{OPR}	Operating Temperature		-40 to +85	°C
	Reflow Temperature Profile (Refe	r to page 12)		
EMITTER				
I _F (avg)	DC/Average Forward Input Curre	nt	20	mA
I _F (pk)	Peak Forward Input Current (50%	duty cycle, 1 ms P.W.)	40	mA
I _F (trans)	Peak Transient Input Current - (≤	1 μs P.W., 300 pps)	1.0	А
V _R	Reverse Input Voltage	Reverse Input Voltage		
P _D	Input Power Dissipation		35	mW
DETECTOR				
I _O (avg)	Average Output Current (Pin 6)		60	mA
V_{EBR}	Emitter-Base Reverse Voltage	Emitter-Base Reverse Voltage HCPL0700/HCPL0701		V
V_{CC}, V_{O}	Supply Voltage, Output Voltage	HCPL0700/HCPL0730	-0.5 to 7	V
		HCPL0701/HCPL0731	-0.5 to 18	
P_{D}	Output power dissipation		100	mW

Electrical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Individual Component Characteristics

Symbol	Parameter	Test Conditions		Device	Min.	Тур.*	Max	Unit
EMITTER								
V _F	Input Forward	I _F = 1.6mA	T _A = 25°C	HCPL0700/01	1.0	1.25	1.7	V
	Voltage			HCPL0730/31		1.35		
				All			1.75	
BV _R	Input Reverse Breakdown Voltage	$T_A = 25$ °C, $I_R = 10\mu A$		All	5.0			
DETECTO	R				•			
I _{OH}	Logic High Output	$I_F = 0$ mA, $V_O = V_{CC} = 0$	18V	HCPL0701/31		0.01	100	μΑ
	Current	$I_F = 0$ mA, $V_O = V_{CC} = 3$	7V	HCPL0700/30		0.01	250	
I _{CCL}	Logic Low Supply	$I_F = 1.6$ mA, $V_O = $ Open, $V_{CC} = 18V$		HCPL0700/01		0.4	1.5	mA
	Current $I_{F1} = I_{F2} = 1.6 \text{mA}, V_{CC} = 7 \text{V}$		= 7V	HCPL0730		0.8	3	
		V _{O1} = V _{O2} = Open, V _{CC} = 18V		HCPL0731		1		
I _{CCH}	Logic High	I _F = 0mA, V _O = Open,	$V_{CC} = 18V$	HCPL0700/01			10	μΑ
Supply Current	Supply Current	$I_{F1} = I_{F2} = 0, V_{CC} = 7V$		HCPL0730		0.001	20	
		$V_{O1} = V_{O2} = Open, V_{C0}$	_C = 18V	HCPL0731		0.01		

Transfer Characteristics

Symbol	Parameter	Test Conditions	Device	Min.	Тур.*	Max.	Unit
CTR	COUPLED	$I_F = 0.5 \text{mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V}$	HCPL0701/31	400		5000	%
	Current Transfer	I _F = 1.6mA,	HCPL0700	300		2600	
	Ratio (Note 1, 2)	$V_{O} = 0.4 \text{ V},$ $V_{CC} = 4.5 \text{ V}$	HCPL0701	500		2600	
		V _{CC} = 4.5 V	HCPL0730	300		5000	
			HCPL0731	500		5000	
V _{OL}	Logic Low Output	$I_F = 0.5 \text{mA}, I_O = 2 \text{mA}, V_{CC} = 4.5 \text{V}$	HCPL0701			0.4	V
	Voltage	I _F = 1.6mA, I _O = 8mA, V _{CC} = 4.5V	HCPL0731			0.4	
	$I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V$				0.4		
		$I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V$				0.4	
		$I_F = 1.6 \text{mA}, I_O = 4.8 \text{mA}, V_{CC} = 4.5 \text{V}$	HCPL0700/0730			0.4	

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Min.	Тур.*	Max.	Unit
I _{I-O}	Input-Output Insulation Leakage Current	Relative humidity = 45%, $T_A = 25$ °C, $t = 5$ s, $V_{I-O} = 3000$ VDC (Note 4)			1.0	μА
V _{ISO}	Withstand Insulation Test Voltage	$R_H \le 50\%$, $T_A = 25^{\circ}C$, $I_{I-O} \le 2\mu A$, $t = 1$ min. (Note 4, 5)	2500			V _{RMS}
R _{I-O}	Resistance (Input to Output)	V _{I-O} = 500 VDC (Note 4)		10 ¹²		Ω

^{*}All typicals at $T_A = 25^{\circ}C$

Electrical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Switching Characteristics $(V_{CC} = 5V)$

Symbol	Parameter	Test Con	ditions	Device	Min.	Тур.*	Max.	Unit
T _{PHL}	Propagation Delay			HCPL0701			30	μs
	Time to Logic Low (Note 2) (Fig. 14)						120	
	(Note 2) (Fig. 14)		$T_A = 25^{\circ}C$	HCPL0701		3	25	
				HCPL0731		5	100	
		$R_L = 270 \Omega, I_F =$	12mA	HCPL0701			2	
				HCPL0731			3	
			$T_A = 25^{\circ}C$	HCPL0701		0.3	1	
				HCPL0731		0.4	2	
		$R_L = 2.2 \text{ k}\Omega, I_F =$	1.6mA	HCPL0700			15	
				HCPL0730/0731			25	
		T _A = 25°C	T _A = 25°C	HCPL0700		1	10	
			HCPL0730/0731		2	20		
T _{PLH}	Time to Logic High	$R_L = 4.7 \text{ k}\Omega, I_F =$	0.5mA	HCPL0701/31			90	μs
			$T_A = 25^{\circ}C$	HCPL0701/31		12	60	
	(Note 2) (Fig. 14)	$R_L = 270 \Omega, I_F = 12 \text{mA}$		HCPL0701			10	
				HCPL0731			15	
			T _A = 25°C	HCPL0701	\	1.6	7	
				HCPL0731		1.6	10	
		$R_L = 2.2 \text{ k}\Omega, I_F =$	1.6mA	HCPL0700/30/31			50	
			$T_A = 25^{\circ}C$	HCPL0700/30/31		7	35	
ICM _H I	Common Mode Transient Immunity at Logic High	$I_F = 0mA$, $IV_{CM}I = 10 V_{P-P}$, $T_A = 25^{\circ}C$, $R_L = 2.2k\Omega$ (Note 3) (Fig. 15)		ALL	1,000	10,000		V/µs
ICM _L I	Common Mode Transient Immunity at Logic Low	I _F = 1.6mA, IV _{CM} T _A = 25°C, R _L = 2 (Note 3) (Fig. 15)	2.2 kΩ	ALL	1,000	10,000		V/µs

^{*}All typicals at $T_A = 25^{\circ}C$

Notes:

- Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
- 2. Pin 7 open. Use of a resistor between pins 5 and 7 will decrease gain and delay time.
- 3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0V$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8 \ V$).
- 4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
- 5. 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

Typical Performance Curves Fig. 1 Propagation Delay vs. Temperature (HCPL0700, HCPL0701) $V_{CC} = 5 \text{ V}$ $I_F = 0.5 \text{ mA}$ $R_L = 4.7 \text{ k}\Omega$ 1/f = 50 µst_p - PROPAGATION DELAY (μs) 25

-60

-40

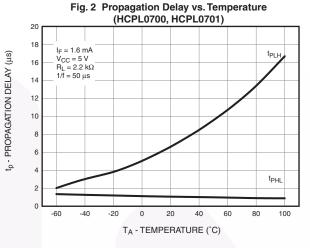
-20

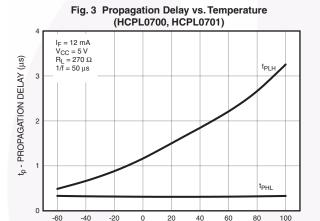
t_{PLH}

tpHI

80

100





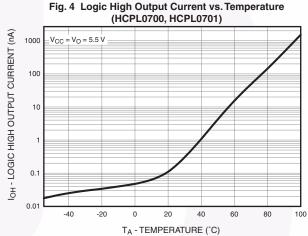
TA - TEMPERATURE (°C)

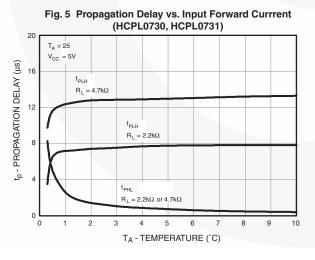
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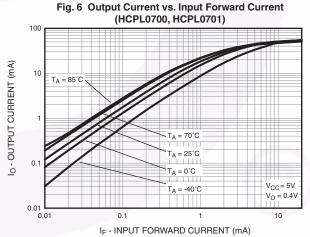
T_A - TEMPERATURE (°C)

40

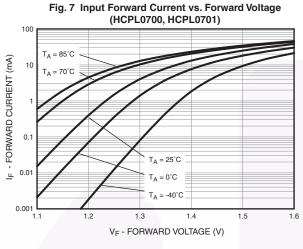
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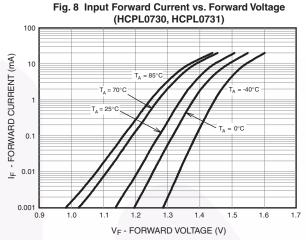






Typical Performance Curves (Continued)





(HCPL0700, HCPL0701) I_{CCL} - LOGIC LOW SUPPLY CURRENT (mA) Logic Low Supply Current vs. Input Forward Current 0.4 0.2 0.1 0.0 0.0 0.2 0.8 1.0 1.6 IF - INPUT FORWARD CURRENT (mA)

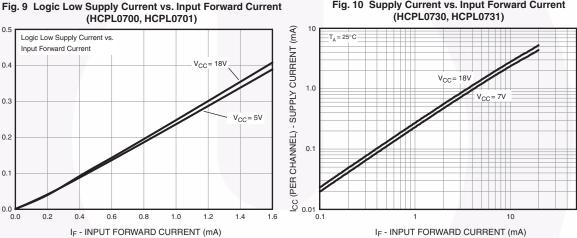
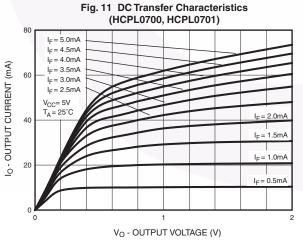
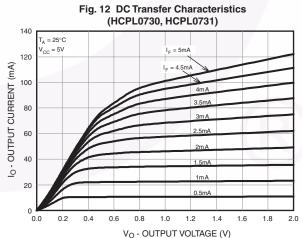


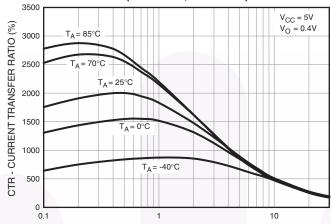
Fig. 10 Supply Current vs. Input Forward Current





Typical Performance Curves (Continued)

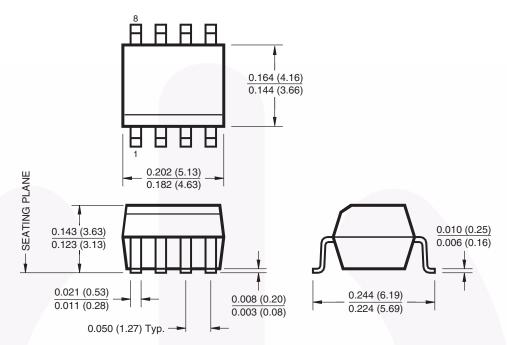
Fig. 13 Current Transfer Ratio vs. Input Forward Current (HCPL0700, HCPL0701)



Test Circuits Noise Shield Pulse Generator tr = 5ns Z₀ = 50 V Pulse Generator tr = 5ns Z_O= 50 V R∟Ş **0.1** μF **V**01 10% DUTY CYCLE 7 Ş R∟ l/f < 100 μS 10% D.C. I/f< 100μs CL = 15 pF 6 3 6 3 **0.1** μF MONITOR I_F Monitor GND 5 5 CL = 15 pF GND Test Circuit for HCPL-0700 and HCPL-0701 Test Circuit for HCPL-0730 and HCPL-0731 Fig. 14 Switching Time Test Circuit Noise Shield 8 8 RL > 2 7 2 7 **0.1** μF 3 6 3 6 VF2 0.1 μF GND 4 5 4 5 Pulse Gen Test Circuit for HCPL-0700 and HCPL-0701 Test Circuit for HCPL-0730 and HCPL-0731 Switch at A: I F= 0 mA Switch at B : I F= 1.6 mA Fig. 15 Common Mode Immunity Test Circuit

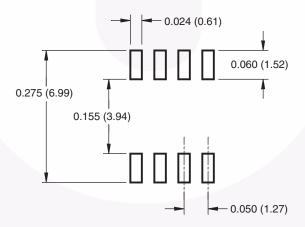
Package Dimensions

8-pin SOIC Surface Mount



Lead Coplanarity: 0.004 (0.10) MAX

Recommended Pad Layout



Dimensions in inches (mm).

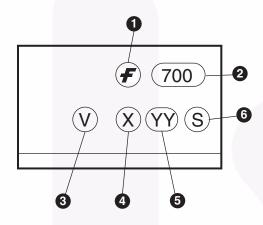
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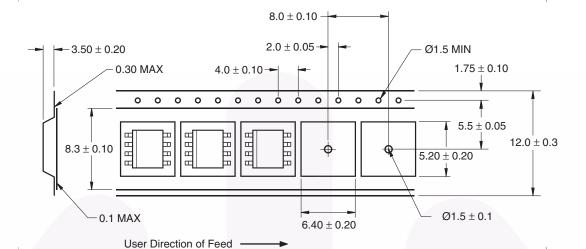
Option	Part Number Example	Description
V	HCPL0700V	VDE 0884
R2	HCPL0700R2 Tape and reel (2500 units per reel)	
R2V	HCPL0700R2V	VDE 0884, Tape and reel (2500 units per reel)

Marking Information



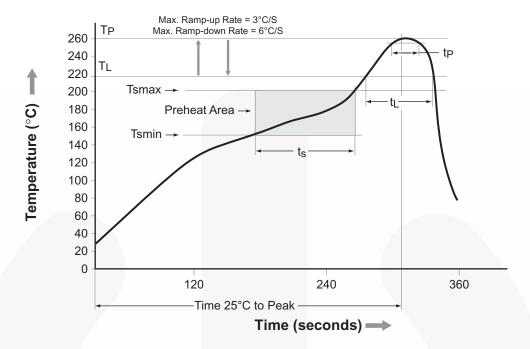
Definiti	ons		
1	Fairchild logo		
2	Device number		
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)		
4	One digit year code, e.g., '3'		
5	Two digit work week ranging from '01' to '53'		
6	Assembly package code		

Carrier Tape Specification



Dimensions in mm

Reflow Profile



Profile Freature	Pb-Free Assembly Profile		
Temperature Min. (Tsmin)	150°C		
Temperature Max. (Tsmax)	200°C		
Time (t _S) from (Tsmin to Tsmax)	60-120 seconds		
Ramp-up Rate (t _L to t _P)	3°C/second max.		
Liquidous Temperature (T _L)	217°C		
Time (t _L) Maintained Above (T _L)	60–150 seconds		
Peak Body Package Temperature	260°C +0°C / -5°C		
Time (t _P) within 5°C of 260°C	30 seconds		
Ramp-down Rate (T _P to T _L)	6°C/second max.		
Time 25°C to Peak Temperature	8 minutes max.		





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Definition of Terms

Deminition of Terms		
Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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