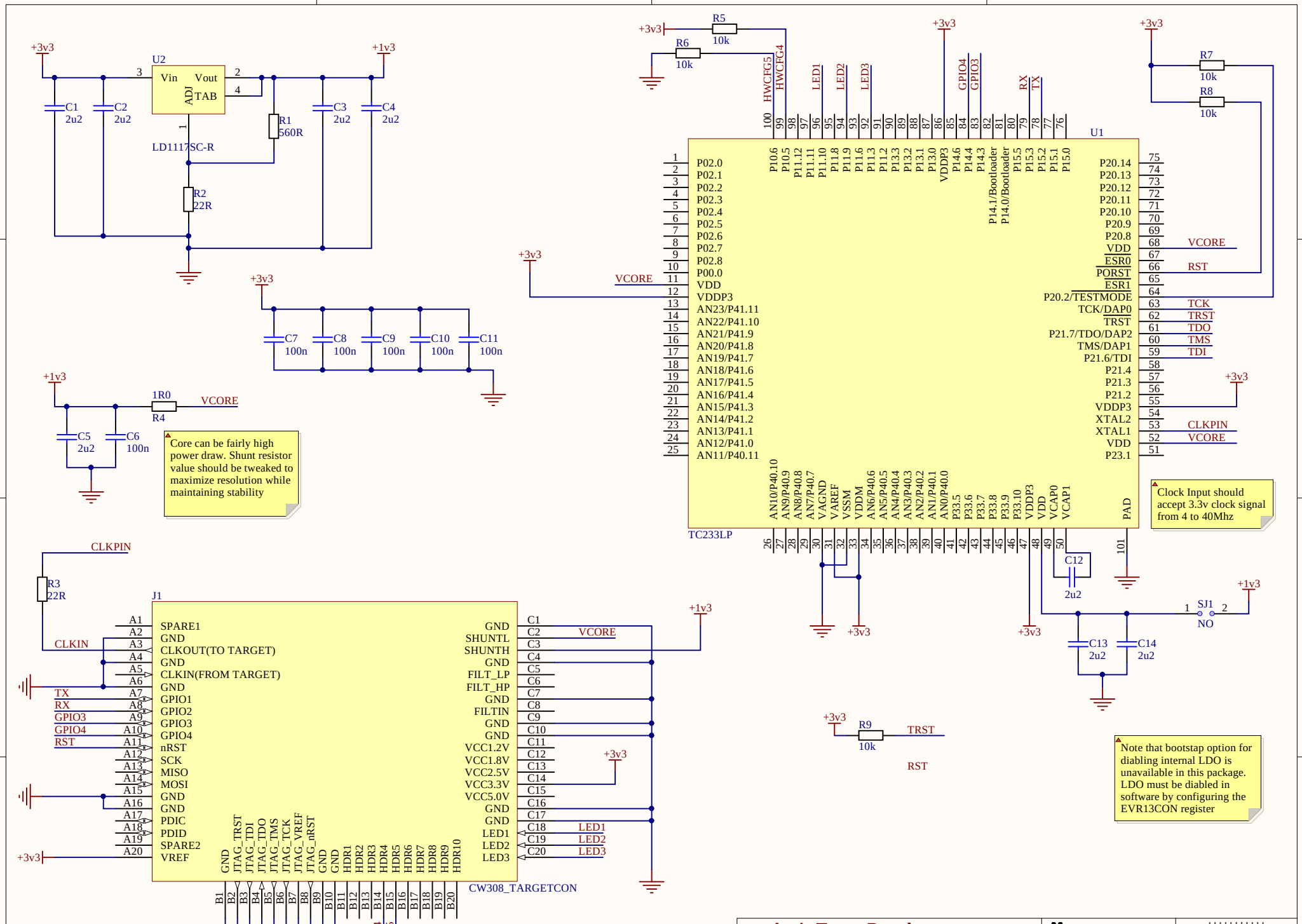
U2
LD1117SC-R
Vin
Vout
ADJ
TAB
C1 2u2
C2 2u2
C3 2u2
C4 2u2
R1 560R
R2 22R
+3v3
+1v3
C7 100n
C8 100n
C9 100n
C10 100n
C11 100n
1R0
R4
VCORE
C5 2u2
C6 100n
Core can be fairly high power draw. Shunt resistor value should be tweaked to maximize resolution while maintaining stability
R5 10k
R6 10k
R7 10k
R8 10k
U1
TC233LP
HWCFG5
HWCFG4
LED1
LED2
LED3
GPIO4
GPIO3
RX
TX
P14.1/Bootloader
P14.0/Bootloader
P02.0
P02.1
P02.2
P02.3
P02.4
P02.5
P02.6
P02.7
P02.8
P00.0
VDD
VDDP3
AN23/P41.11
AN22/P41.10
AN21/P41.9
AN20/P41.8
AN19/P41.7
AN18/P41.6
AN17/P41.5
AN16/P41.4
AN15/P41.3
AN14/P41.2
AN13/P41.1
AN12/P41.0
AN11/P40.11
P20.14
P20.13
P20.12
P20.11
P20.10
P20.9
P20.8
ESR0
PORST
ESR1
P20.2/TESTMODE
TCK/DAP0
TRST
P21.7/TDO/DAP2
TMS/DAP1
P21.6/TDI
P21.4
P21.3
P21.2
XTAL2
XTAL1
P23.1
TCK
TRST
TDO
TMS
TDI
CLKPIN
AN10/P40.10
AN9/P40.9
AN8/P40.8
AN7/P40.7
VAGND
VAREF
VSSM
VDDM
AN6/P40.6
AN5/P40.5
AN4/P40.4
AN3/P40.3
AN2/P40.2
AN1/P40.1
AN0/P40.0
P33.5
P33.6
P33.7
P33.8
P33.9
P33.10
VCAP0
VCAP1
PAD
C12 2u2
C13 2u2
C14 2u2
SJ1
NO
Clock Input should accept 3.3v clock signal from 4 to 40Mhz
R9 10k
TRST
RST
Note that bootstap option for diabling internal LDO is unavailable in this package. LDO must be diabled in software by configuring the EVR13CON register
R3 22R
CLKIN
J1
CW308_TARGETCON
SPARE1
GND
CLKOUT(TO TARGET)
CLKIN(FROM TARGET)
GPIO1
GPIO2
GPIO3
GPIO4
nRST
SCK
MISO
MOSI
PDIC
PDID
SPARE2
VREF
SHUNTL
SHUNTH
FILT_LP
FILT_HP
FILTIN
VCC1.2V
VCC1.8V
VCC2.5V
VCC3.3V
VCC5.0V
JTAG_TRST
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG_VREF
JTAG_nRST
HDR1
HDR2
HDR3
HDR4
HDR5
HDR6
HDR7
HDR8
HDR9
HDR10
Title: Aurix Target Board
Approved: NO
Rev: 02
Project: Aurix Target
License: GPL
Date: 03/03/2019
Time: 4:14:59 PM
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