
PCB Layout Guide for CEC1702

<i>Author: Tom Tse Microchip Technology Inc.</i>
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INTRODUCTION

This application note provides information on design considerations for a printed circuit board (PCB) for the Microchip CEC1702 device.

The design of the PCB requires care to provide good supply and ground paths; in addition, other design issues are addressed in this document.

The functional blocks in the CEC1702 have different requirements for routing and external connections, which are also outlined in this application note.

Please see [References](#) for device-level information such as V_{CC1} power planes, and mechanical package information for the 84-Pin WFBGA.

This document includes the following topics:

- [Section 1.0, "General Layout Considerations," on page 2](#)
- [Section 2.0, "Miscellaneous Considerations," on page 8](#)
- [Section 3.0, "JTAG Design and Layout Guide," on page 15](#)

Audience

This document is written for a reader that is familiar with hardware design. The goal of this application note is to provide information about sensitive areas of the CEC1702 PCB layout.

References

The following documents should be referenced when using this application note. Please contact your Microchip representative for availability.

- Microchip CEC1702 Data Sheet
- Microchip CEC1702 EVB Reference Schematic
- I²C-bus specification and user manual, Rev. 6 - 4 April, 2014 or later (see www.nxp.com/documents/user_manual/UM10204.pdf)

Package Information

The CEC1702 device is currently available in the following package:

- CEC1702 for 84-pin, WFBGA

1.0 GENERAL LAYOUT CONSIDERATIONS

This section describes layout considerations for the CEC1702 device. This includes the following topics:

- [Section 1.1, "Decoupling Capacitors," on page 2](#)
- [Section 1.2, "32.768kHz Crystal Oscillator," on page 4](#)
- [Section 1.3, "CAP Pins, AVSS/GND Connection," on page 5](#)
- [Section 1.4, "PCB Mounted Analog Power Supply Filter for PLL Usage," on page 5](#)
- [Section 1.5, "BGA Package PCB Layout Considerations," on page 6](#)

1.1 Decoupling Capacitors

This section includes the following topics:

- [Section 1.1.1, "CEC1702 WFBGA Capacitors," on page 2](#)

Decoupling capacitors should be placed as close to the chip as possible to keep series inductance low. When the capacitors are mounted on the bottom side of the PCB, the capacitors are connected to the ground plane from the bottom layer directly using the shortest path to the device. Each VCC pin should have a 0.1 μF capacitor located as close to the pin as possible. Bypass capacitors should be placed close to the supply pins of the CEC1702 with short and wide traces.

The CEC1702 has an integrated voltage regulator to supply the core circuitry. Decoupling this regulator requires a critical capacitor of 1 μF on the CAP pin. ESR of this 1 μF capacitor, including the routing resistance, must be less than 100 mOhm.

Capacitors may carry large currents that generate magnetic fields, inducing noise on nearby traces. Sensitive traces such as the 32kHz crystal should be separated by at least five times the trace width from decoupling capacitors when possible.

Connecting decoupling caps to power and ground planes using two vias per pad will reduce series inductance.

- [FIGURE 1-1: on page 3](#) shows decoupling for the CEC1702 84-pin WFBGA.

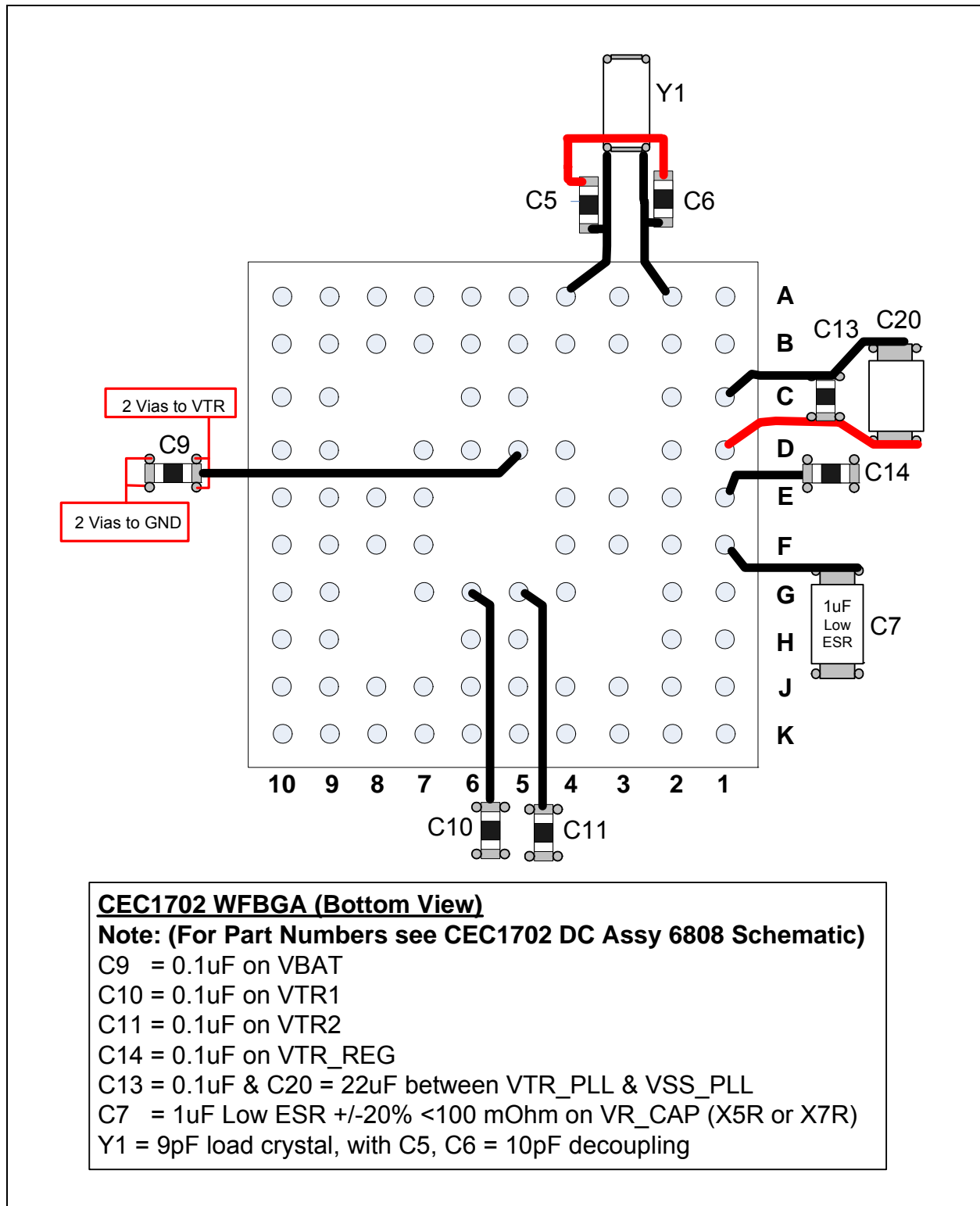
The VCC pin decoupling capacitors can use any typical 16V 10% Ceramic. See also the CEC1702 EVB Schematics and Bill of Materials.

1.1.1 CEC1702 WFBGA CAPACITORS

- [Figure 1-1](#) shows decoupling for the CEC1702 84-pin WFBGA package.

Note: The capacitors can use any typical 16V 10% ceramic.
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FIGURE 1-1: CEC1702 DECOUPLING IN 84-PIN WFBGA PACKAGE



1.2 32.768kHz Crystal Oscillator

This section describes specific layout and design considerations for the 32.768kHz crystal oscillator; this can be used to source the internal 32kHz clock domain, in lieu of the silicon oscillator or an external pin. The crystal implementation is required to support the RTC function within the CEC1702.

1.2.1 32.768KHZ CRYSTAL OSCILLATOR LAYOUT

The CEC1702 32kHz crystal oscillator is designed to generate an synchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5 μ W typical), stability and minimum jitter using a general purpose parallel resonant 32kHz crystal. For a suggested part number, please see the CEC1702 EVB schematic (see [References](#)).

This unique low power crystal oscillator drive circuit means that a standard inverter crystal layout should not be used. The design has been characterized to allow a variation of 4pF to 18pF on each pin. Based on the following load capacitance calculation, Microchip recommends 10pf load capacitors with a crystal that has a 9pf CI rating. Other than these capacitors, no additional external components are required for normal operation of the clock circuit.

$$\text{Effective Load Capacitance} = C1 = \frac{[C11 + C_{pin_xtal2}][C12 + C_{pin_xtal1}]}{C11 + C_{pin_xtal2} + C12 + C_{pin_xtal1}} + C_{brd}$$

Where:

- C12 is the cap from pin XTAL1 to ground.
- C13 is the cap from pin XTAL2 to ground.
- Cpin_xtal2 is the pin capacitance of pin XTAL2. This is estimated to be 5pf ([Note 1-1](#)).
- Cpin_xtal1 is the pin capacitance of pin XTAL1. This is estimated to be 3pf ([Note 1-1](#)).
- Cbrd is estimated at 1.5pF.

Note 1-1 At the time of publication, the CEC1702 silicon has not been characterized. Please check with your Microchip FAE for final pin capacitance values after silicon validation is complete. Any variation from the estimates provided here could change the crystal CI value requirement.

1.2.2 CRYSTAL ACCURACY

The accuracy of the 32kHz input translates directly into accuracy of the internal clock and the functions in the CEC1702 using the 32kHz: 32KHZ_OUT, week timer, hibernation timers, and so forth.

The accuracy, with regard to actual error in time can be illustrated as such: +/-1ppm of error in frequency corresponds to 32.768 kHz x 1ppm x 10^{-6} = +/-0.032768 Hz. This translates into ~1 μ sec/sec or ~+/-0.086 sec/day.

Based on customer RTC accuracy timer requirements, Microchip recommends using a +/-20ppm crystal. This would equal approximately +/-2 sec/day, other factors discounted.

For arguments sake, it is safe to say that stray capacitance is difficult to calculate exactly. So, as an exercise in completeness, this calculation describes the effect of each picofarad of additional capacitance over/under the crystal C_{load} value:

$$ppm/pF = \frac{C_1 \times 10^6}{2(C_0 + C_L)^2}$$

where C_0 is the shunt capacitance, C_1 is the motional capacitance and C_L is the load capacitance of the chosen crystal (these numbers can be found in the crystal data sheet). For example, using a crystal with C_0 = 0.8pF, C_1 = 0.0019pF, C_L = 12.5pF, we get a shift of 5.37ppm/pF. So, in terms of time, each pF of added/subtracted capacitance is approximately 5.37 x 0.086 = +/-462 msec/day for this particular crystal.

This example is meant to illustrate the magnitude of the potential error. In practice, slight capacitance mismatch does not equate to many seconds a day.

In all applications, the power and ground traces should be short, and run close and parallel as far as is possible, with large spacing to adjacent traces. On no account should any connection be made from VDD or VSS_PLL to board power planes; only connect as described above.

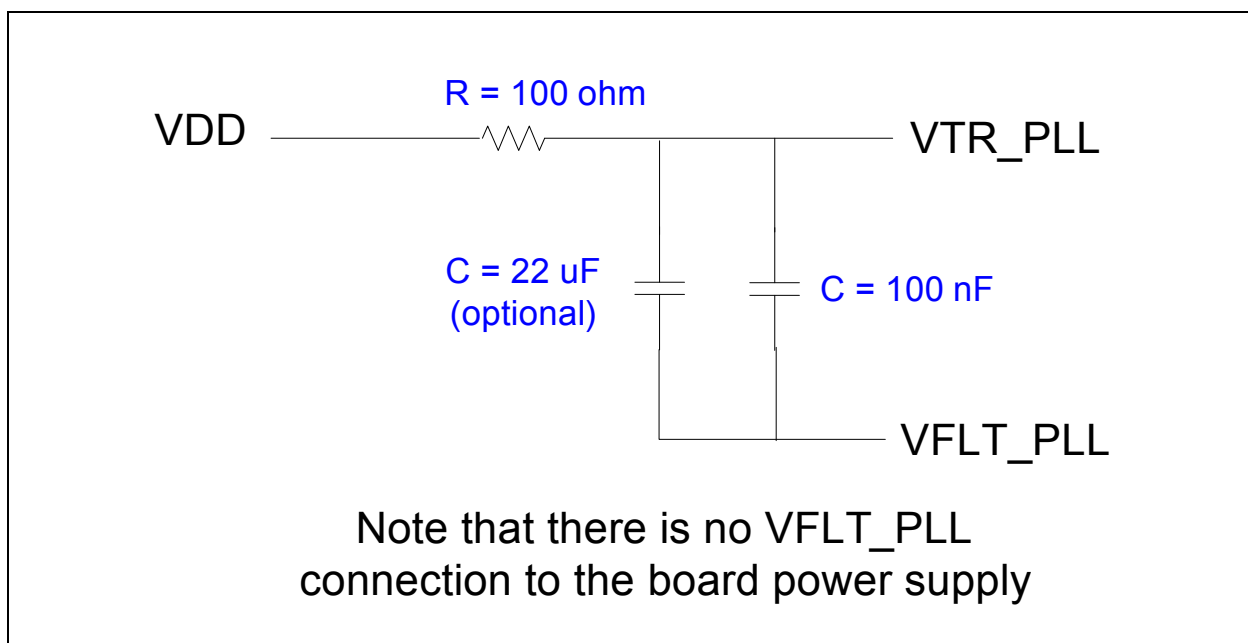
1.4.1 REAL WORLD COMPONENT SELECTION

Throughout the attenuating frequency range, there should be no resonant non-absorptions. This means that the series element will either be a resistor or a very poor (i.e. resistive) inductor.

Having got the series element with the most impedance as we can, the filter requires the highest value high frequency capacitor we can find in a small package (often 100nF). In applications with a low PLL reference frequency and environment with significant low frequency components, it is often beneficial to add a large value capacitor such as an electrolytic which fits nicely on the board (often 22uF).

The Figure 1-3 as shown below is reference schematic represents both the circuitry and the device placement. The component values are only illustrative.

FIGURE 1-3: POWER SUPPLY FILTER FOR VTR_PLL



1.5 BGA Package PCB Layout Considerations

The CEC1702 devices have BGA lead-free RoHS-Compliant package as follows:

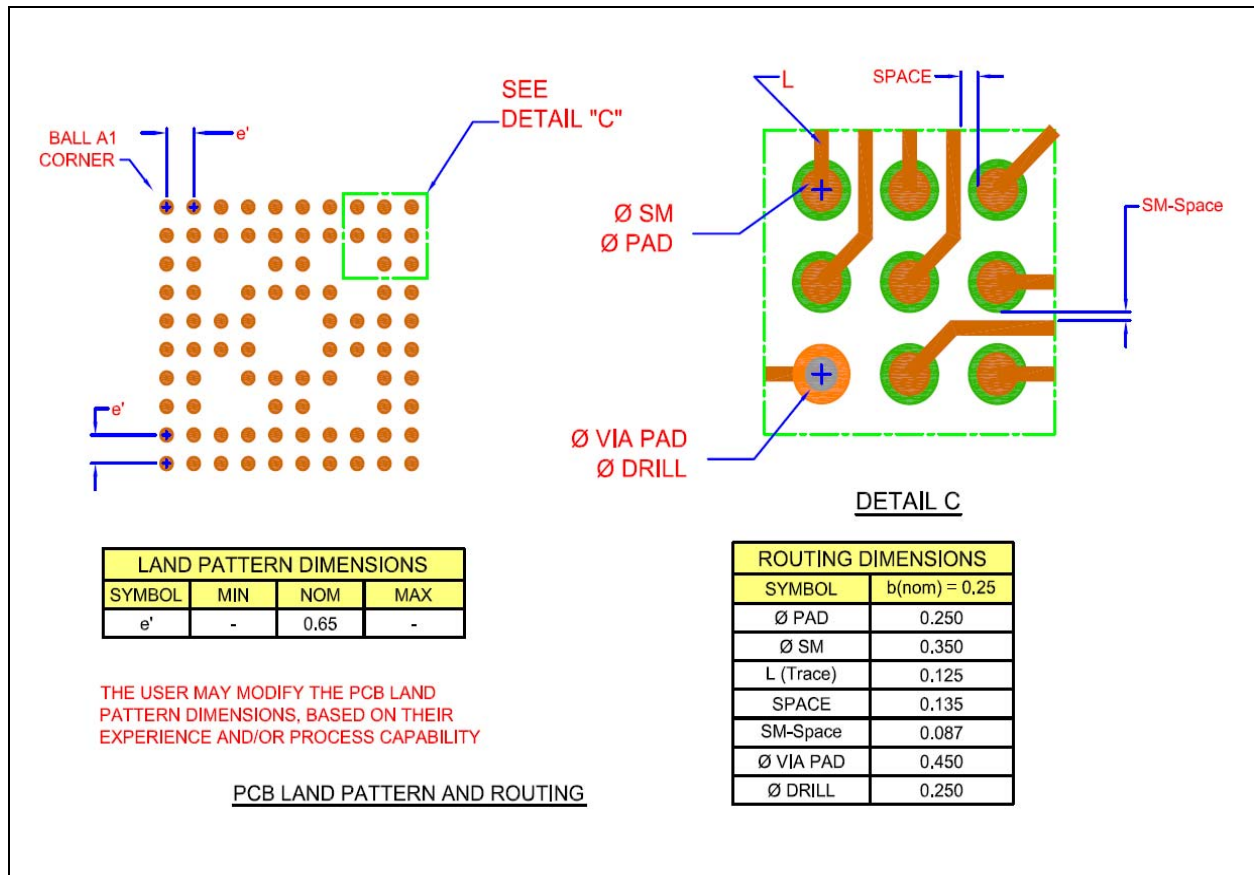
- 84-pin WFBGA: 7mm x 7mm, 0.65mm ball pitch

Note: Please refer to the latest data sheet for most up-to-date PCB LAND pattern information.

The following list summarizes BGA routing guidelines, but it is understood that final layout is process- dependent and your design should reflect your needs:

- Through-hole vias technology is not recommended for pitches less than 0.8mm (unless the ball matrix is depopulated in the center)
- NSMD ball pads for pitches 0.8mm – 0.4mm
- Solder Mask to be 1:1 scale of the land size, when routing 0.5mm pitch ball pads
- μ Vias – next generation PCB technology for tighter pitches
- Eliminate through-hole vias
- Increase routing density & enhance electrical performance
- Decrease routing layers
- Provide fan-out solutions for multiple layers (stacked Vias)

FIGURE 1-4: LAND PATTERN DIMENSIONS, 84-WFBGA, 0.65MM BALL PITCH



2.0 MISCELLANEOUS CONSIDERATIONS

This section covers a variety of layout topics:

- [Section 2.1, "Strapping Options," on page 8](#)
- [Section 2.2, "Battery Circuit," on page 8](#)
- [Section 2.3, "EOS Considerations," on page 9](#)
- [Section 2.4, "ADC Input Layout Requirements," on page 10](#)
- [Section 2.5, "SPI Flash Implementation," on page 11](#)
- [Section 2.6, "1MHz Pullup Resistor Requirement," on page 13](#)
- [Section 2.7, "5V Tolerant Pins," on page 13](#)
- [Section 2.8, "1.8V Capability," on page 13](#)
- [Section 2.9, "Power Switch Input," on page 14](#)
- [Section 2.10, "VCI_IN Pins when Used as GPIO," on page 14](#)

2.1 Strapping Options

[Table 2-1](#) describes the CEC1702 strap option pins.

TABLE 2-1: CEC1702 STRAP OPTIONS

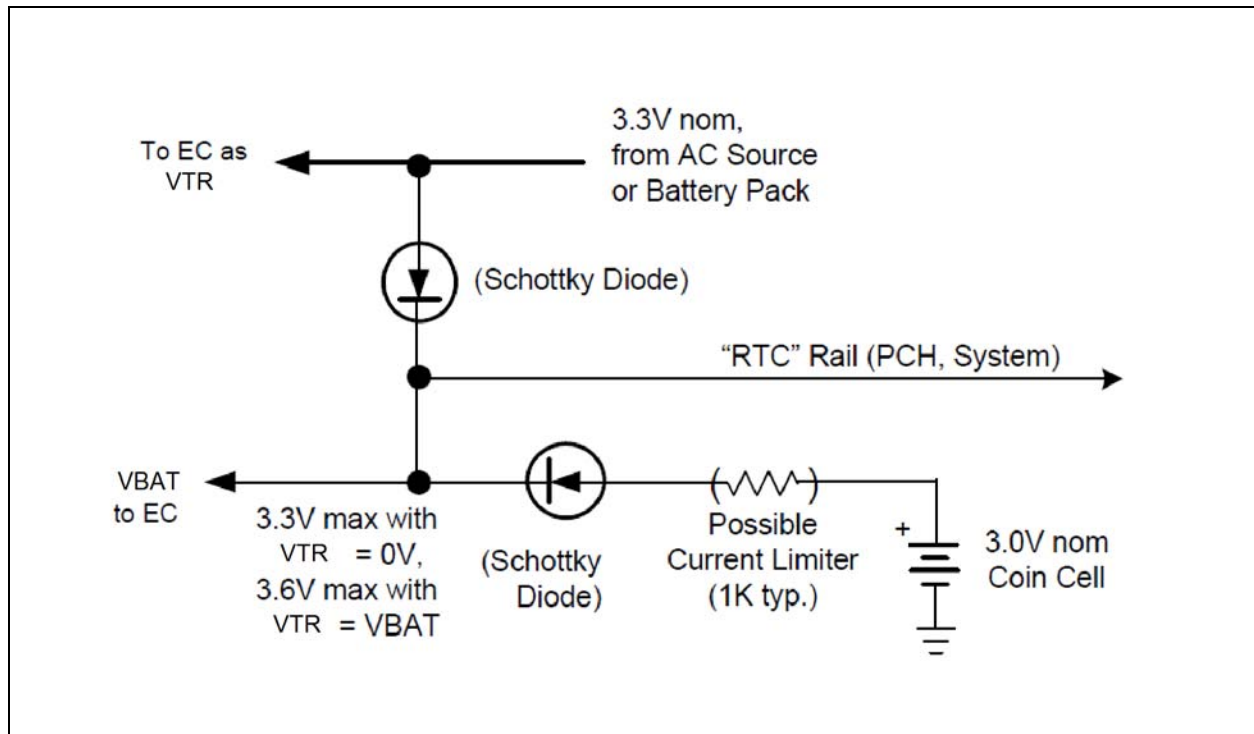
GPIO	Strap Name	Description	Pull High	Pull Low
GPIO171	TAP Controller Select Strap	This strap option is sampled on VTR power up, and is not affected by a Watchdog Timer reset. If any of the CEC1702 JTAG TAP controllers are used, GPIO171 must be configured as an output to a VTR-powered external function. GPIO171 may only be configured as an input when the JTAG TAP controllers are not needed or when an external driver does not violate the Slave Select Timing.	(Default) Internal pull high selects Boundary Scan TAP Controller	External pull Low, selects Debug TAP Controller
		See the CEC1702 Data Sheet, "Tap Controller Select Strap Option," for further details. This pin MUST be pull-low for normal operation.		

2.2 Battery Circuit

Please see the Power Sources section of the CEC1702 Data Sheet.

For the battery circuitry requirement, VBAT must always be present if VTR is present. The following circuit is recommended to fulfill this requirement.

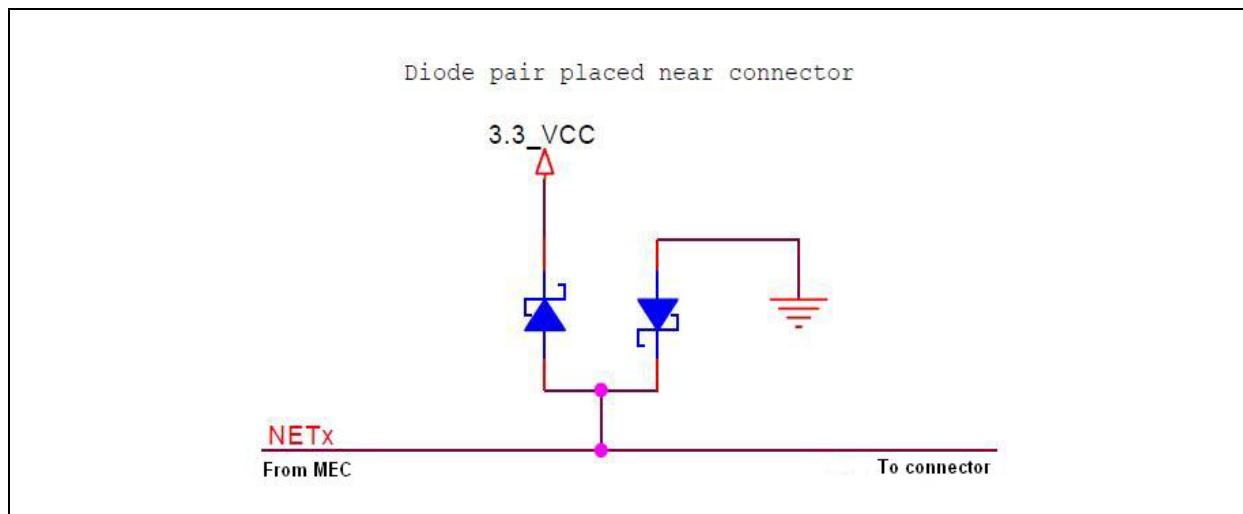
FIGURE 2-1: RECOMMENDED BATTERY CIRCUIT



2.3 EOS Considerations

For SMBus signals that terminate external to the main system board (for example, Smart Battery) the designer should take care in protecting these signals from EOS (Note 2-1) and ESD (Note 2-2). Please refer to the SMBus 2.0 specification, section 3.1.2.2 for appropriate guidelines. The specification recommends a series protection resistor and an optional ESD transorb on these nets. In addition to the SMBus specification recommendation, past experience shows that using 2 high speed diodes on each SMBus trace (instead of the transorb in the SMBus spec) is an effective way to improve immunity to EOS and ESD events. A Schottky diode pair is a good example. Figure 2-2 shows the suggested circuit implementation for each net that goes to a connector.

FIGURE 2-2: SCHOTTKY DIODE PAIR EXAMPLE



It should also be noted that any other signal that goes to an external connector should also be considered for EOS/ESD susceptibility. For instance, an ID pin (tied to a GPIO) that might seem benign, but is routed near high voltage sources could suffer transient EOS events. A similar protection scheme should be considered for these nets.

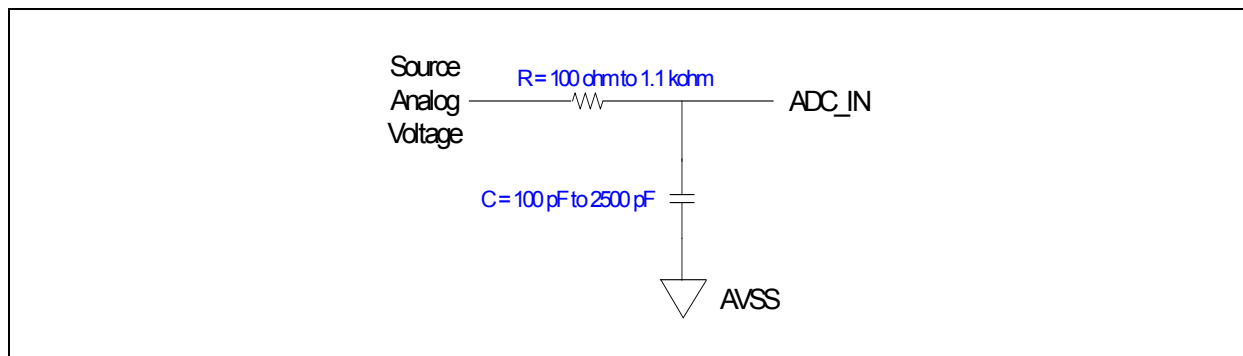
Note 2-1 EOS is defined as damage to the part caused by the application of voltages (to any pin) beyond the power supply rails, usually forward biasing internal protection diodes and resulting in high levels of current flow. This typically induces open failures by damaging the metal inside the part. EOS is typically a low voltage, high current situation.

Note 2-2 ESD is the applied reverse bias to the PN junction -- heat due to power dissipation melts the silicon in the part. ESD is typically a high transient voltage spike with low current situation.

2.4 ADC Input Layout Requirements

- It is suggested that the Analog-Digital Converter (ADC) Source AVSS reference connects to the CEC1702 AVSS via a low noise AVSS island, which is shown in [Figure 1-2](#).
- It is suggested that a low pass filter, see [Figure 2-3](#), be used on each ADC input of CEC1702. Filter components below are a good starting point, the R should have value between 100 ohm to 1.1 kohm and the C should have value between 100pF to 2500pF. The RC values are based on high frequency cut off desired for the application, $F = 1 / (2\pi * RC)$

FIGURE 2-3: ADC INPUT LOW PASS FILTER



- It is recommended that the ADC nets are spaced at least 20 mils from any high speed switching signals to prevent cross talk that could add noise.

2.5 SPI Flash Implementation

The CEC1702 SPI flash interface enables the embedded controller (EC) access to an external SPI flash device. The CEC1702 Data Sheet and Boot ROM Application Note have more details on detail information (see [References on page 1](#)). This section describes specific PCB layout design considerations to setup this feature.

Note: The SPI Flash Interface of CEC1702 can be selected either 3.3V or 1.8V. The QSPI0 interface is on VTR2 power rail.

TABLE 2-1: SPI INTERFACE SIGNALS

Generic Pin Signal Name	Pin Signal Function name	CEC1702 Pin Number	Pin Function Signal Description
SPICLK	QSPI0_CLK	K6	Shared SPI Clock
SPI_CS#	QSPI0_CS#	K7	Shared SPI Chip Select
IO0 / MOSI	QSPI0_IO0 / QSPI0_MOSI	K5	Shared SPI Data I/O 0.
	Note: Also used as SPI_MOSI when the interface is used in single wire mode.		
IO1 / MISO	QSPI0_IO1 / QSPI0_MISO	K3	Shared SPI Data I/O 1.
	Note: Also used as SPI_MISO when the interface is used in single wire mode.		
IO2	QSPI0_IO2	K4	Shared SPI Data I/O 2
	Note: Only used in Quad Mode. Also can be used by firmware as WP.		
IO3	QSPI0_IO3	K2	Shared SPI Data I/O 3
	Note: Only used in Quad Mode. Also can be used by firmware as HOLD.		

2.5.1 SPI FLASH INTERFACE

Figure 2-4 is topology for implementing the CEC1702 SPI flash for a SPI flash device. The detection of the SPI flash device is determined by the GPIO055 (QSPI0_CS#) in the Boot Rom. See Table 2-2 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-4: SPI FLASH ON QSPI0 FLASH I/F (GPIO55 = 1)

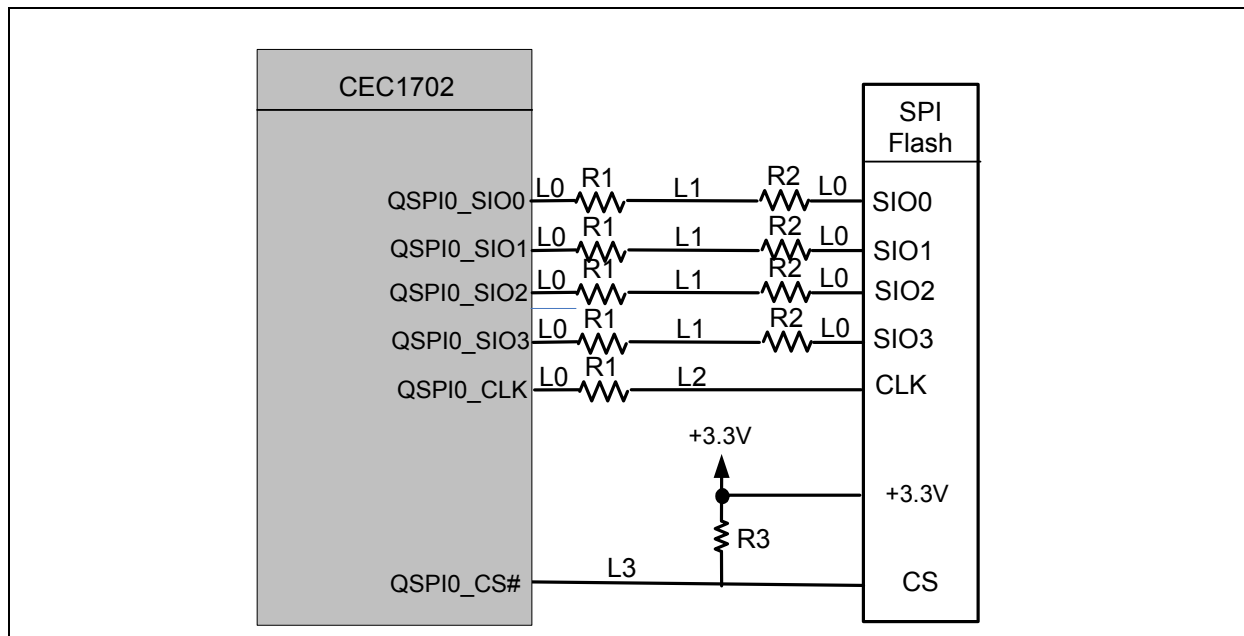


TABLE 2-2: CEC1702 SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between CEC1702 or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	The PCB trace between terminating resistors on the IO lines.	1-inch to 10-inch
L2	The PCB trace from CEC1702 or R1 resistor to SPI flash.	1-inch to 10-inch
L3	PCB trace from CEC1702 to SPI flash for chip select.	$L3 = L0 + L1$
R1	These resistors are between the trace and the CEC1702.	25 ohm, see also Note 2-3
R2	This resistor is on the IO lines between the SPI flash and trace.	45 ohm, see Note 2-3.
R3	This is a Pull-High resistor (to +3.3V) for SPI CS connections. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-3 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the CEC1702 (-0.3V min. to $V_{CC1} + 0.3V$ max).

2.5.2 SPI FLASH IMPLEMENTATION RECOMMENDATIONS

The following recommendations are for SPI Flash Implementations.

- The CEC1702 SPI memory interface has serial flash device compatibility requirements that are defined in the CEC1702 Data Sheet. Please make sure the selected SPI flash meets these requirements.
- SPI_CLK must be 20mils spacing from any other high frequency (>1GHz) signal.
- The SPI flash parts should support operating at 12MHz for the ROM code loader, and up to 48MHz clock speed in RAM code loading.
- The designer should follow the SPI interface host design guidelines.
- IBIS models are available to aid in simulating the SPI system topology.
- The chip select CS# signals should have weak pullup resistors to the same power rail as the SPI flash. The pullup resistor value should meet the rise time requirements of the SPI flash.
- The characteristic impedance of the PCB trace should be 50 ohms +/-15% at 50MHz operating frequency.
- Within the SPI flash device, Schmitt trigger inputs are assumed on both the clock line and IO data lines.
- The output drivers for the SPI flash chip select pins should be programmed as open-drain using the GPIO Pin Control registers.
- The SPI Data IO traces should be length-matched to the CLK lines within 0.100-inch.
- Signal Integrity should be checked for each SPI part on your BOM.

2.5.3 SPI FLASH EXTERNAL PROGRAMMER

The SPI Flash must be programmed externally using a suitable programmer, such as Dediprog's SF100 (<http://www.dediprog.com/pd/spi-flash-solution/sf100>).

Provisions for a programming header for the SPI flash are recommended if the SPI is not socketed.

2.6 1MHz Pullup Resistor Requirement

Please refer to the I²C-bus specification and user manual as indicated in the section [References on page 1](#) for more information.

2.7 5V Tolerant Pins

There are ten 3.3V/5V tolerant (over-voltage) pins on the CEC1702. Please see the CEC1702 Data Sheet section 2.5.7 for more information.

Note: Pins with over-voltage protection may be pulled up externally to 5V supply. It is recommended to select strong pull-up resistor value (less than 10k ohms) that keep the pull-up voltage on the pin less than 3.8V and above 4.5V. If the voltage is between 3.8V and 4.5V, the pad current will be higher (~65uA nominal).
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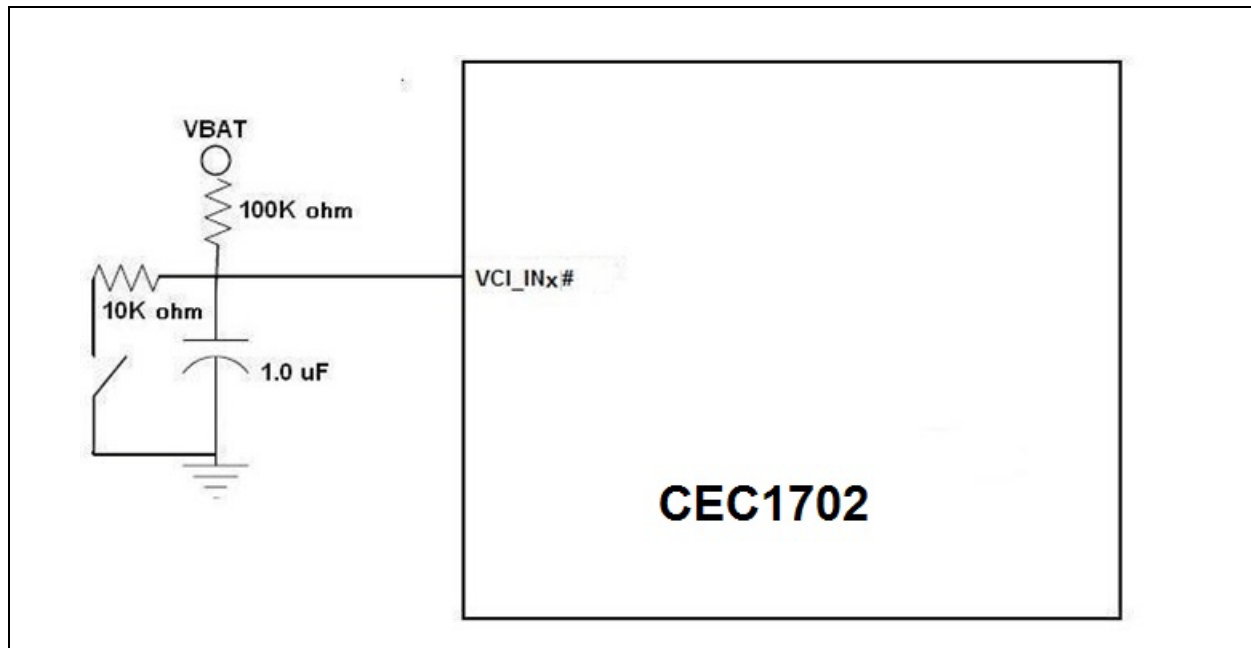
2.8 1.8V Capability

There are two voltage supply regions for all GPIO pins powered by VTR1 and VTR2. Each region may be either 3.3V or 1.8V. Please refer to the CEC1702 Data Sheet section 2 for more information.

2.9 Power Switch Input

For the VBAT-powered power switch inputs (VCI_INx#) there is a specific requirement for the input circuit as illustrated in [Figure 2-5](#). The resistors can use any typical 1/10W, +/- 1% carbon, thick, metal, or thin film. The capacitors can use any typical 16V 10% ceramic. Unused VCI pins should be pulled up to VBAT via a 100K resistor. Please refer to the CEC1702 EVB Schematics and Bill of Materials.

FIGURE 2-5: VBAT-POWERED CONTROL INPUT CIRCUIT



2.10 VCI_IN Pins when Used as GPIO

All the VCI_IN pins can be used as GPIOs. In addition to programming the alternate function field in the GPIO Control register for the GPIO function the firmware must also disable the VCI input. To disable the VCI input the firmware must clear (i.e., set to '0') both the VCI_BUFFER_EN bit in the VCI BUFFER ENABLE REGISTER and the IE bit in the VCI INPUT ENABLE REGISTER.

3.0 JTAG DESIGN AND LAYOUT GUIDE

This section provides general hardware information for using the CEC1702 JTAG interface and working with JTAG master and slaves.

This document includes the following topics:

- [Section 3.1, "CEC1702 JTAG Capabilities," on page 15](#)
- [Section 3.2, "General PCB Layout Considerations for JTAG," on page 15](#)
- [Section 3.3, "Pin Connections," on page 15](#)
- [Section 3.4, "JTAG Internal Pull-Up," on page 17](#)
- [Section 3.5, "JTAG Reset," on page 17](#)

3.1 CEC1702 JTAG Capabilities

CEC1702 devices have the following debug capabilities:

- JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
- Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
- Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
- Accessed via 4-wire JTAG or 2-wire ARM SWD (Default)
- Comprehensive ARM-Standard Trace Support: Full DWT, ITM, ETM, TPIU functionalities

3.2 General PCB Layout Considerations for JTAG

Please follow the PCI Specification's Routing and Layout Guidelines for the JTAG interface signals to support the JTAG interface speed up to 33MHz.

- In order to improve the clock transmission line's signal integrity, the following is recommended:
 - Keep the clock traces as straight as possible
 - Use arc-shaped traces instead of right-angle bends
 - Do not use multiple signal layers
 - Do not use vias to reduce impedance change and reflection
 - Place a ground plane next to the outer layer to minimize noise effect
 - Terminate clock signals to minimize reflection
- The JTAG cable that attaches to the CEC1702 motherboard has a standard 20-pin 0.1" spacing female connector on it. Normally, the CEC1702 motherboard just has a 20-pin 0.1" spacing pin strip on the board to mate with it.
- If the CEC1702 motherboard design does not have the space for a 20-pin male pin strip, then the board designer can place a 6 pin header on the motherboard and build a 6-pin to 20-pin adapter cable to attach to the 20-pin female connector on the JTAG cable. This is shown in Figure 3-1, "6-Pin to 20-Pin Adapter Board (w/ BOM)".

3.3 Pin Connections

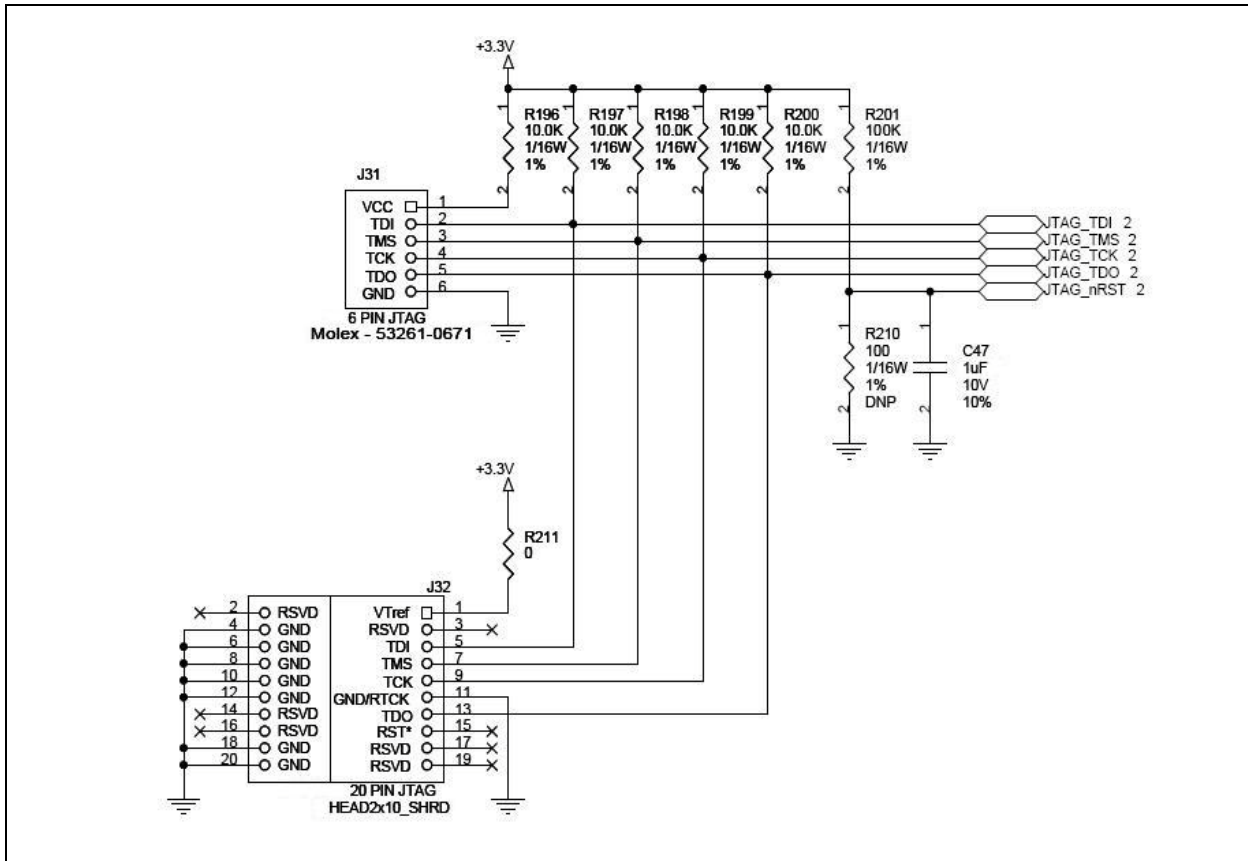
3.3.1 4-WIRE JTAG CONNECTION

Six signals are the minimum number required on the motherboard side; these are described in [Table 3-1](#) and illustrated in [FIGURE 3-1: 6-Pin to 20-Pin Adapter Board \(w/ BOM\) on page 16](#).

TABLE 3-1: CEC1702 4-WIRE JTAG PINS

Name	JTAG Cable Connection
VTR	The motherboard VTR is always 3.3V. It is recommended to add a 49-ohm series resistor for motherboard protection. The JTAG cable senses the voltage level on this line and drives the JTAG logic levels to the same voltage level from the target system.
TDI	Test Data In
TMS	Test Mode Select
CLK	Test Clock
TDO	Test Data Out
GND	Motherboard ground connect

FIGURE 3-1: 6-PIN TO 20-PIN ADAPTER BOARD (W/ BOM)



- Note 1:** The 10K pullups that are shown in [Figure 3-1](#) are used on CEC1702 JTAG inputs to prevent them from floating when the JTAG cable is not attached.
- 2:** The CEC1702 JTAG RST# pin connects to a 100K pullup to always enable the JTAG interface. Board design can provide pads for a pullup and pulldown for this pin in motherboard layout.
- 3:** In order to prevent potential damage, use a keyed connector to avoid plugging the cable in backward which would result in a short between VTR and ground.
- 4:** Add zero-ohm resistors to the JTAG link if there is a JTAG chain is used.

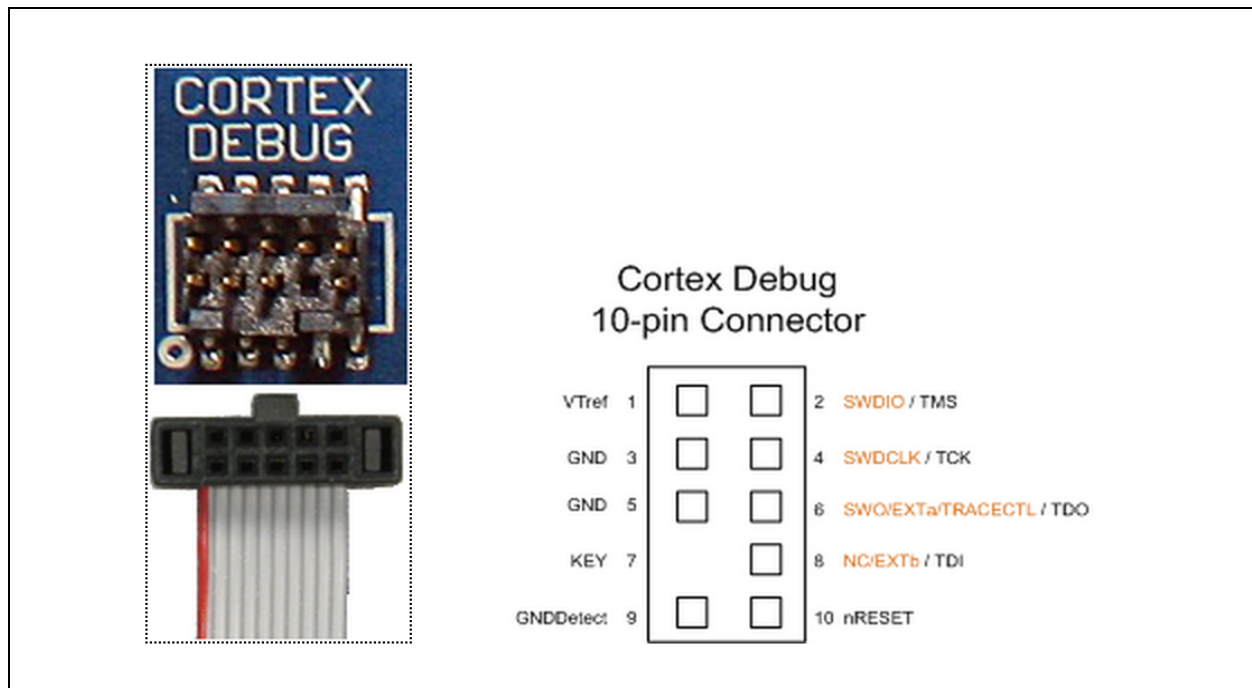
3.3.2 2-WIRE JTAG CONNECTION

Five signals are the minimum number required on the motherboard side; these are described in [Table 3-2](#).

TABLE 3-2: CEC1702 2-WIRE JTAG PINS

Name	JTAG Cable Connection
VTR	The motherboard VTR is always 3.3V.
SWDCLK	Use on JTAG_CLK pin if selected.
SWO	Use on JTAG_TDO pin if selected.
SWDIO	Use on JTAG_TMS pin if selected.
GND	Motherboard ground connect

The [Figure 3-2](#) shows the standard ARM Cortex 10 pins connector (a Samtec FTSH-105-01 w/ pin 7 removed).

FIGURE 3-2: 10-PIN CORTEX DEBUG (0.05") CONNECTOR

3.4 JTAG Internal Pull-Up

The firmware can select which debug pins to enable the internal pull-high. Default is disabled. Please see the CEC1702 Data Sheet DEBUG ENABLE REGISTER (4000_FC20h) for more information.

3.5 JTAG Reset

When the JTAG_RST# pin is not asserted (logic'1'), the JTAG_TDI, JTAG_TDO, JTAG_TCK, JTAG_TMS signal functions in the JTAG interface are unconditionally routed to the JTAG interface; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the JTAG_TDI, JTAG_TDO, JTAG_TCK, JTAG_TMS signal functions in the JTAG interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers cannot route the JTAG interface to the pins. The system board designer should terminate this pin in all functional states using jumpers, pullup or pulldown resistors, and so forth.

JTAG registers are set to their initial values by the assertion of the JTAG_RST# pin. The JTAG_RST# pin must be held low while the CEC1702 devices are powering up so the registers can be set to their proper default values. If JTAG_RST# is high during power up, the JTAG registers may be set to unpredictable values. This can trigger unwanted test modes and the system may not run correctly. As a result, the JTAG_RST# pin must be held low for at least 5.00 msec when applying VTR power.

Note: For more details on the JTAG_RST# pin, in particular JTAG_RST# functionality with respect to VTR power up events, as well as RESETI# reset input pin transitions, see the JTAG section in the CEC1702 Data Sheet.

The minimum required JTAG signals as shown in [Table 3-1](#) does not include the JTAG_RST# signal. There are several options to handle the absence of this pin as followed:

- Production Mode with JTAG Port Disable:
 - Hold the JTAG_RST# pin low with pulldown resistor to disable the JTAG port. Add a pullup resistor option (do not populate) for potential failure analysis to allow use of the JTAG interface. In this case, the JTAG_RST# pin must be manually held low at least 5.00 msec on power up.

- Production Mode with JTAG Port Enable:

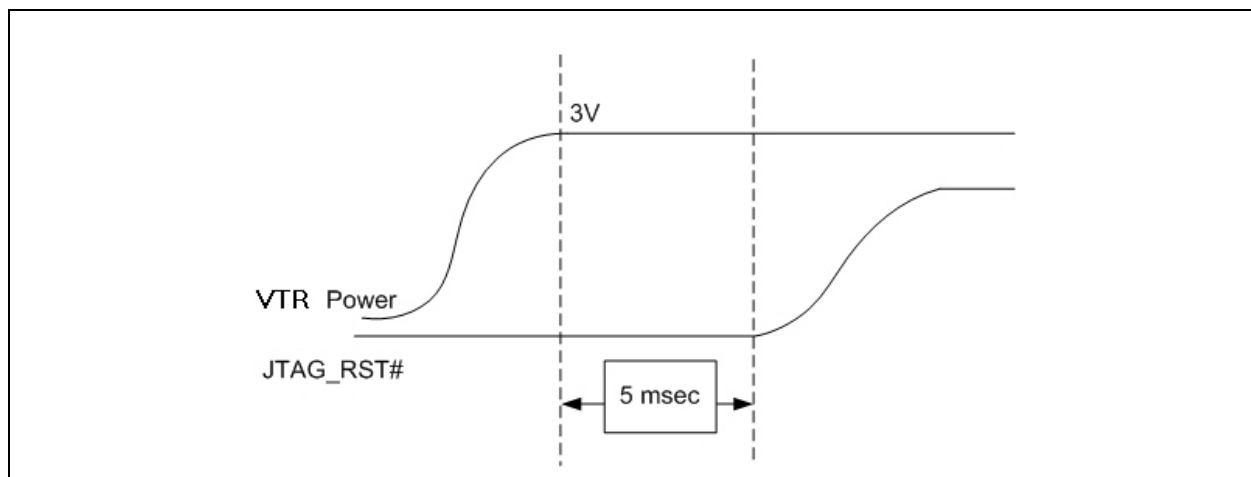
- Add a jumper to hold the JTAG_RST# line low during power up, then remove the jumper in order to ensure that it meets the 5.00 msec timing requirement.

Optionally, put in hardware Resistor-Capacitor (RC) circuitry to force the JTAG_RST# signal low for at least 5.00 msec. For example:

1. Use a CEC1702 EVB with external power supply which shows the rise time less than 100 μ s.
2. RC = 100K ohms resistor pullup to VTR and 1 μ F capacitor.
3. The rising timing of VTR related to the JTAG_RST# signal is shown in [Figure 3-3](#); the falling time should be a reverse of the rising time.

Note: The RC values need to be changed in order to compensate for the power supply time to provide a 5.00 msec reset pulse, measured from VTR = 3.3V to JTAG_RST# = 0.8V.

FIGURE 3-3: VTR VS. JTAG RISING TIME



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002402A (03-15-17)		Initial Release

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