Koruza-CM

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Version Revision:

v0.3 - 30.03.2017.

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

Koruza	www.koruza.net
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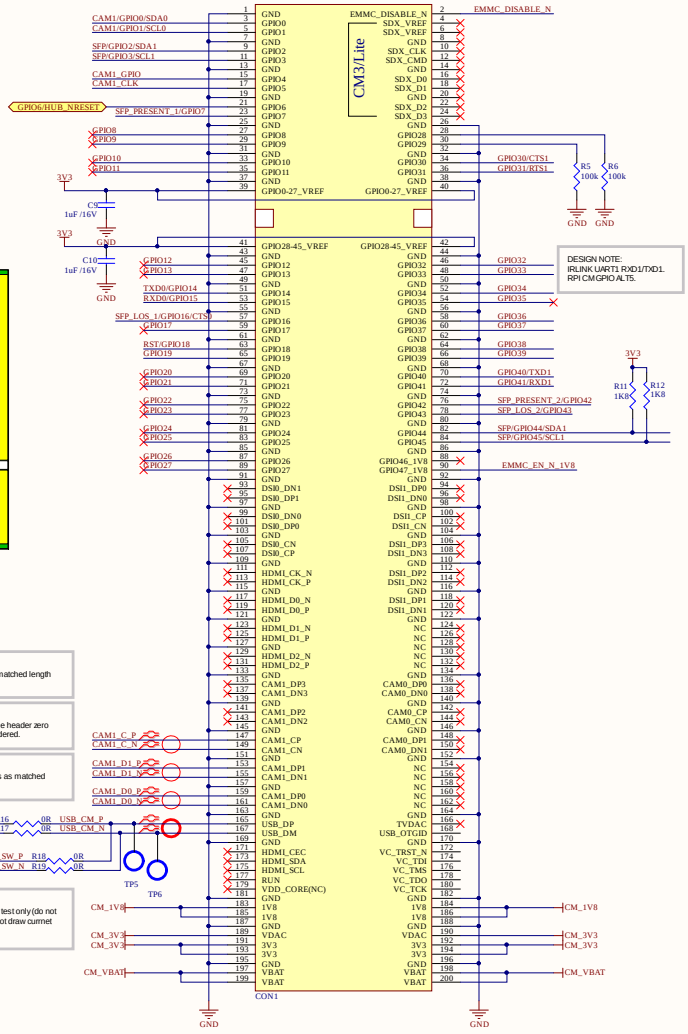
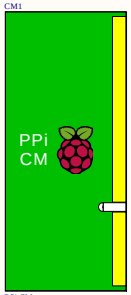
KORUZA-CM

www.koruza.net



CM1



RPi CM

DESIGN NOTE:
IRLINK UART1 RXD1/TXD1.
RPI CM GPIO ALTS.

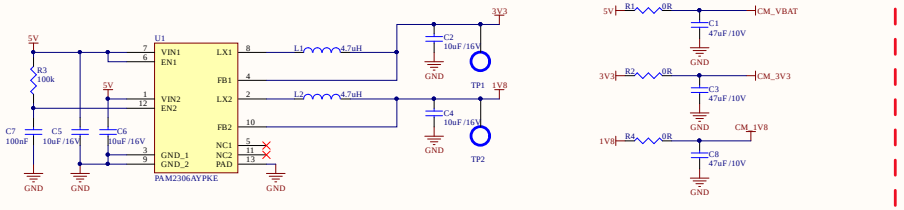
DESIGN NOTE:
Route red ringed signals as matched length 100R differential pair

DESIGN NOTE:
For USB to be connected to the header zero ohm resistors need to be soldered.

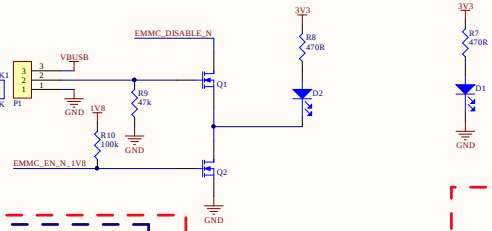
DESIGN NOTE:
Route red bold-ringed signals as matched length 90R differential pair.

DESIGN NOTE:
VDD_CORE used for module test only (do not use in normal operation, do not draw current form this part)

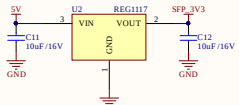
Power



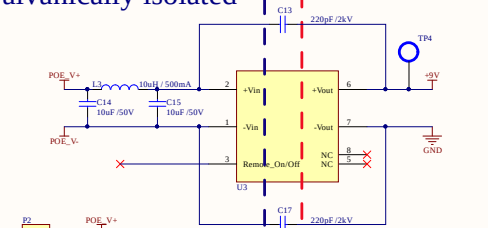
DESIGN NOTE:
Jumper position:
3-2 = USB BOOT ENABLED
2-1 = USB BOOT DISABLED

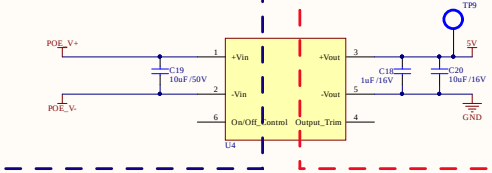


SFP Power supplay



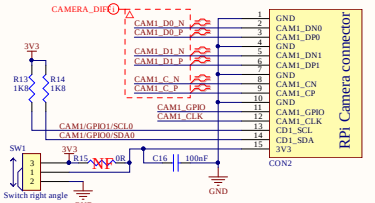
Galvanically isolated



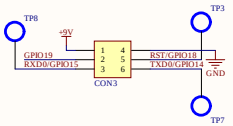


DESIGN NOTE:
This board supports 3V3 voltage level on the IO pins.
It is powered with passive PoE, +24V, and it is galvanically isolated, due to two isolated DC-DC converters.

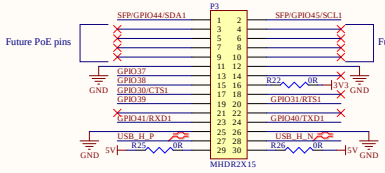
Koruza Camera connector



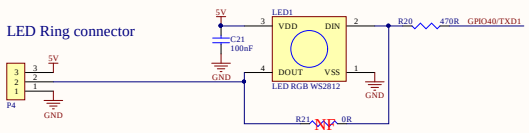
Koruza move driver connector



Koruza GPIO connector



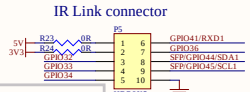
LED Ring connector



DESIGN NOTE:
If RGB LED is soldered, zero ohm resistor should not be fited.

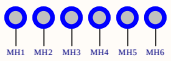
LAYOUT NOTE:
LED Ring connector need to be paced on the front edge of the board, to be easy accessible.

IR Link connector



DESIGN NOTE:
IRLINK UART1 RXD1/TXD1.
GPIO 32/33

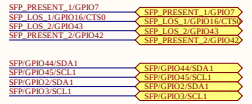
Mounting holes



Mounting holes 7.4mm pad 3.2mm drill
BOARD MOUNTING HOLES
ONE IN EACH CORNER

Fiducials

Fiducials 2x TOP



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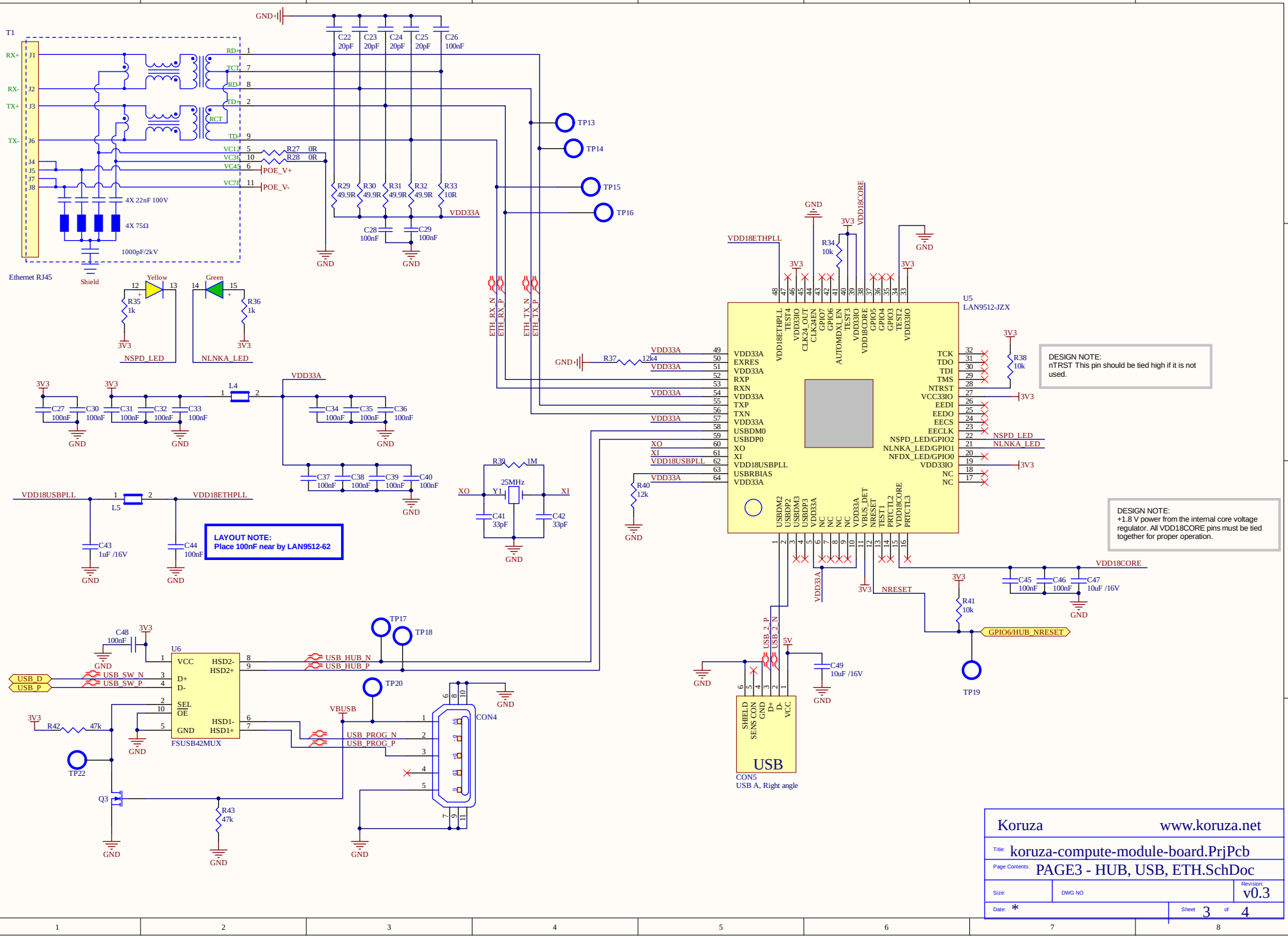

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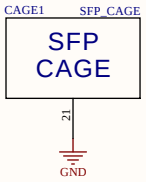
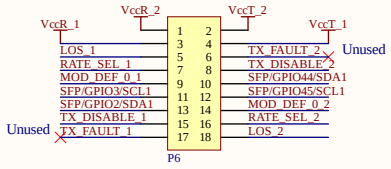
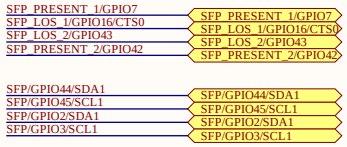
Rigid to Flex PCB connection

SFP Cage Rigid to flex connector

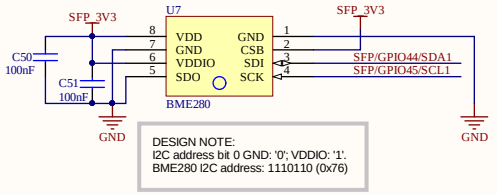


Koruza SFP rigid to flex GPIO connector

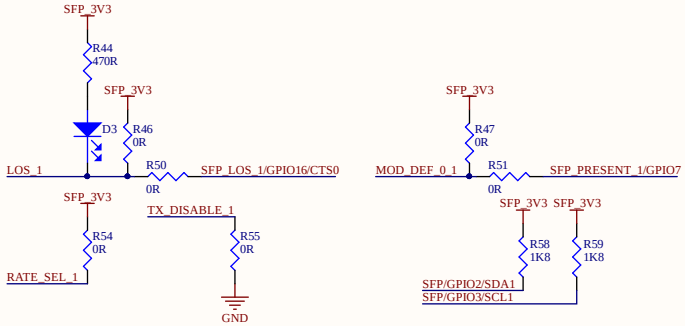




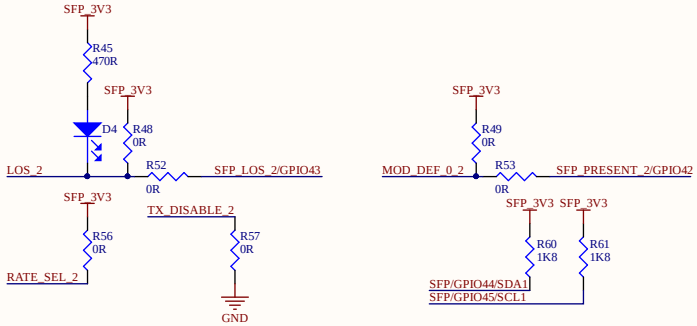
Environment sensor
Temperature, humidity, presure



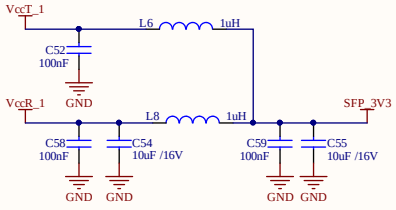
SFP1 GPIO config



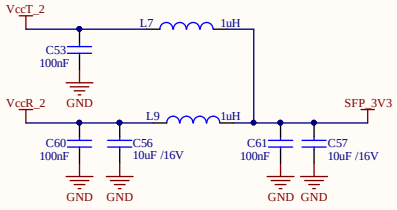
SFP2 GPIO config



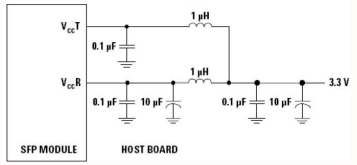
SFP1 Power filtering network



SFP2 Power filtering network



DESIGN NOTE:
Note: Inductors with DC resistance of less than 1 © should be used in order to maintain the required voltage at the SFP input pin at 3.3V. When the recommended supply filtering circuit is used, hot plugging of the SFP transceiver module will result in an inrush current of no more than 30 mA greater than the steady state value.



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