Koruza-CM

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Version Revision:

v0.2 - 09.03.2017.
v0.3 - 30.03.2017.
v0.3.1 - 05.05.2017.

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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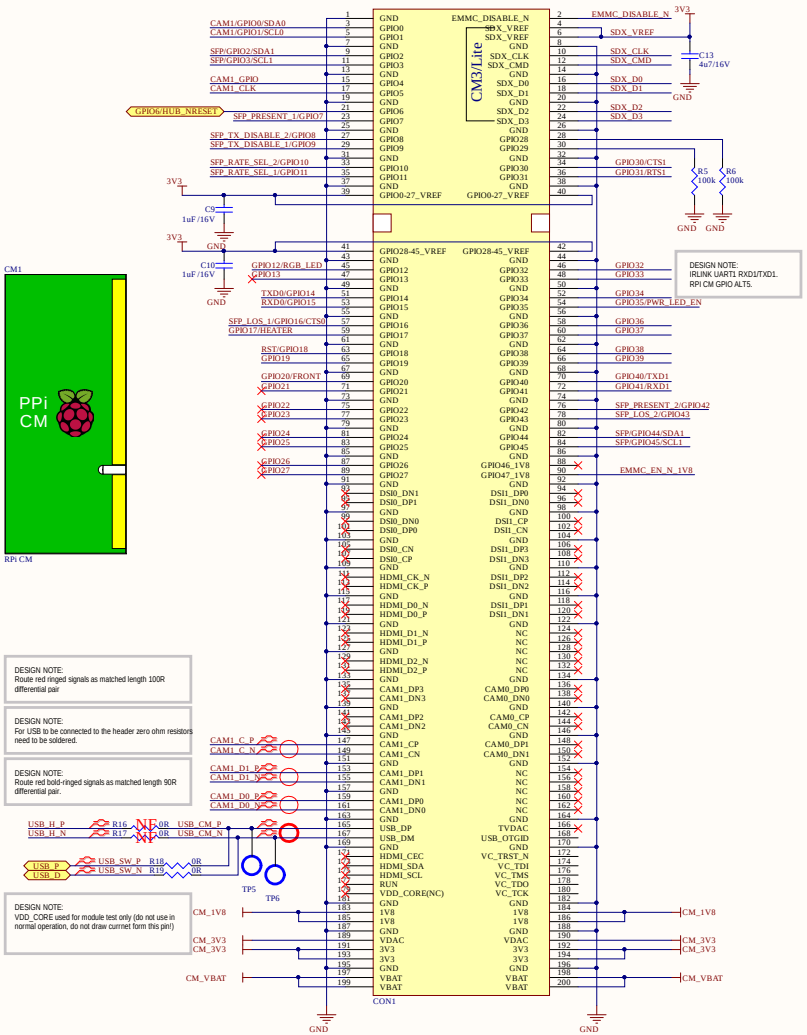
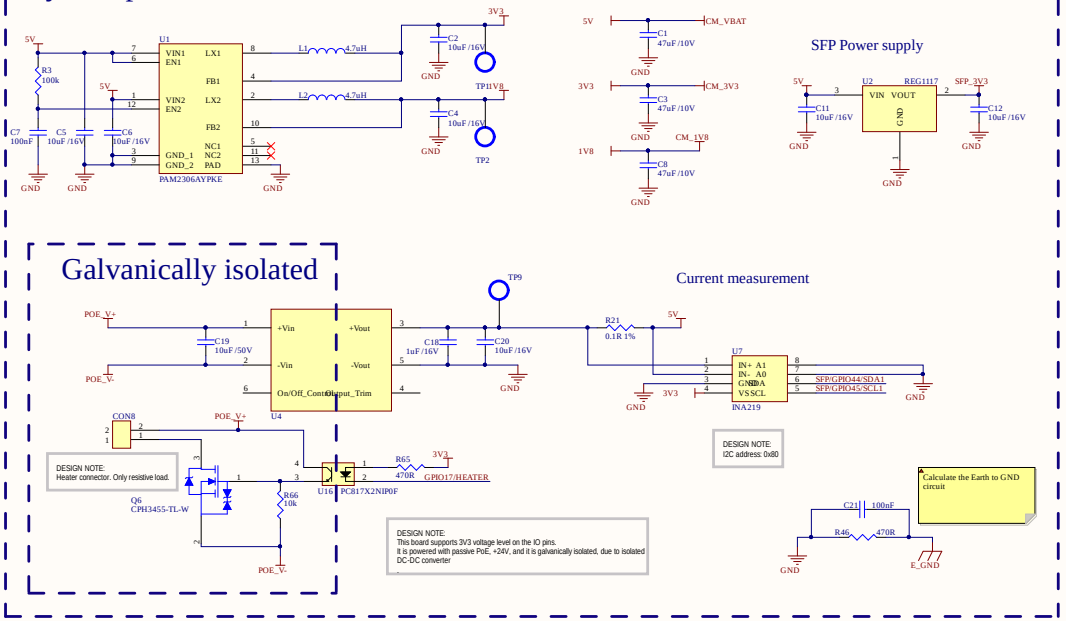
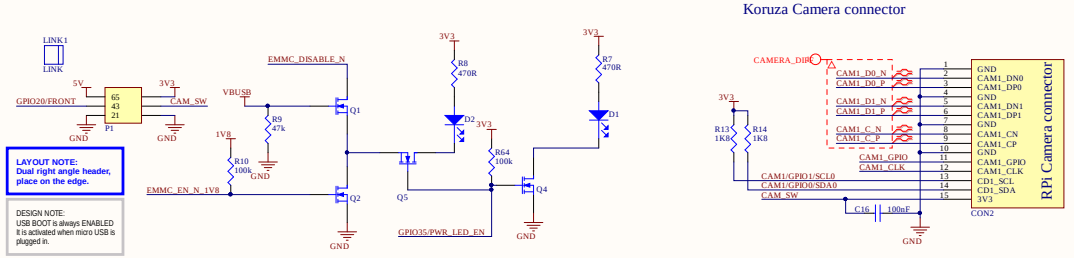


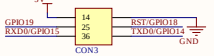
System power



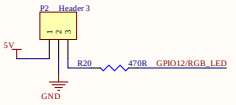
Koruza Camera connector



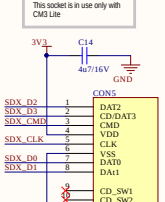
Koruza move driver connector



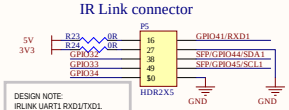
RGB Status LED



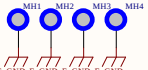
Micro SD card socket



IR Link connector

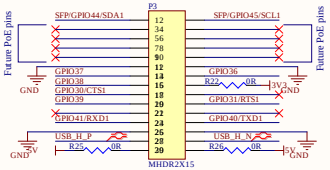


Mounting holes



Fiducials

Koruza GPIO connector



Koruza GPIO connector - GPIO Pins Alternative Function Assignment

	Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
GPIO30	Low	<reserved>	SA3	PCM_DIN	CTS0		CTS1
GPIO31	Low	<reserved>	SA2	PCM_DOUT	RTS0		RTS1
GPIO36	High	SPI0_CE0_N	SD0	TXD0	<reserved>		
GPIO37	Low	SPI0_MISO	SD1	RXD0	<reserved>		
GPIO38	Low	SPI0_MOSI	SD2	RTS0	<reserved>		
GPIO39	Low	SPI0_SCLK	SD3	CTS0	<reserved>		
GPIO40	Low	PWM0	SD4		<reserved>	SPI2_MISO	TXD1
GPIO41	Low	PWM1	SD5	<reserved>	<reserved>	SPI2_MOSI	RXD1
GPIO44	-	GPCLK1	SDA0	SDA1	<reserved>	SPI2_CE1_N	
GPIO45	-	PWM1	SCL0	SCL1	<reserved>	SPI2_CE2_N	

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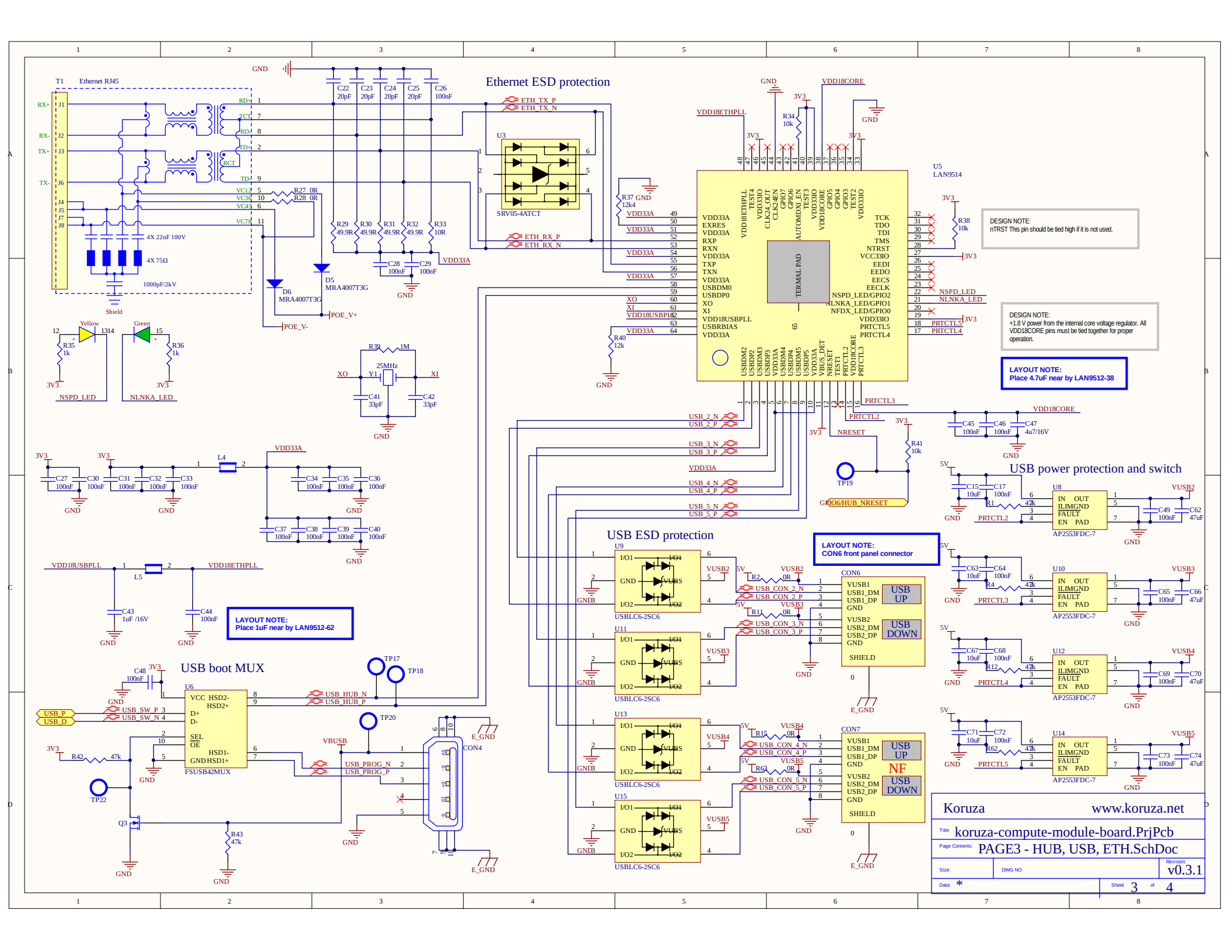
Ethernet ESD protection
USB power protection and switch
USB boot MUX
USB ESD protection
T1 Ethernet RJ45
U5 LAN9514
U3 SRV05-4ATCT
U6 FSUSB42MUX
U8 AP2553FDC-7
U9 USBLC6-2SC6
U10 AP2553FDC-7
U11 USBLC6-2SC6
U12 AP2553FDC-7
U13 USBLC6-2SC6
U14 AP2553FDC-7
U15 USBLC6-2SC6
CON4
CON6
CON7
Q3
Y1 25MHz
L4
L5
TP17
TP18
TP19
TP20
TP22
LAYOUT NOTE: Place 1uF near by LAN9512-62
LAYOUT NOTE: Place 4.7uF near by LAN9512-38
LAYOUT NOTE: CON6 front panel connector
DESIGN NOTE: nTRST This pin should be tied high if it is not used.
DESIGN NOTE: +1.8 V power from the internal core voltage regulator. All VDD18CORE pins must be tied together for proper operation.
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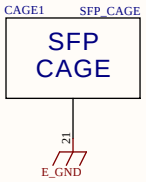
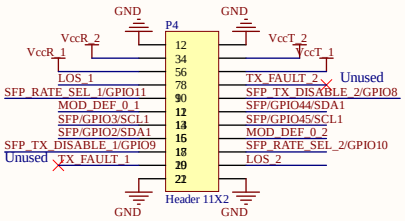
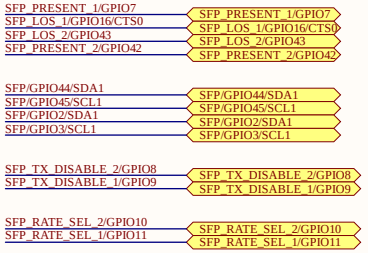
Rigid to Flex PCB connection

SFP Cage Rigid to flex connector

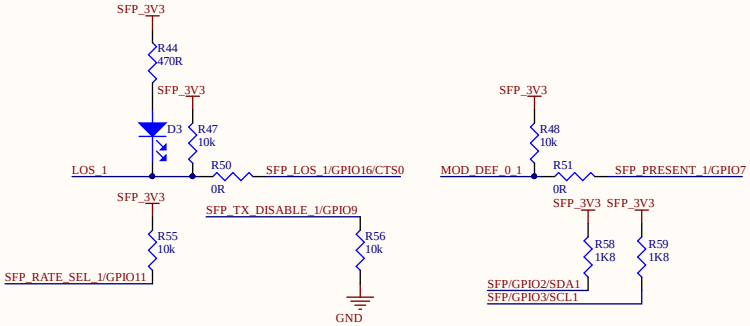


Koruza SFP rigid to flex GPIO connector

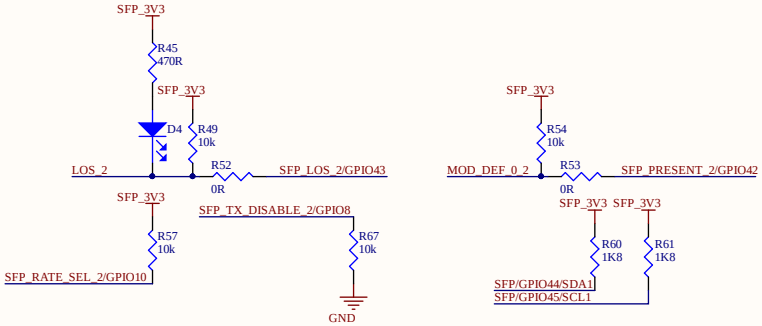




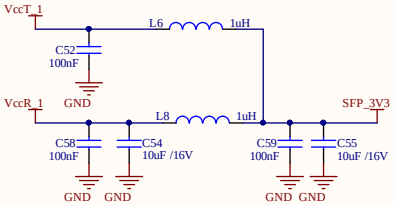
SFP1 GPIO config



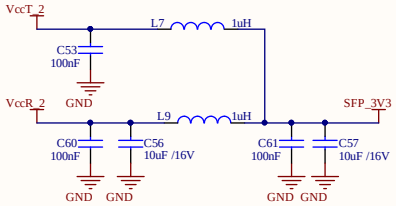
SFP2 GPIO config



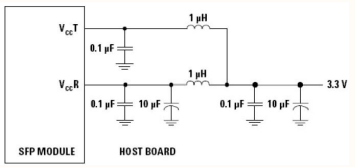
SFP1 Power filtering network



SFP2 Power filtering network



DESIGN NOTE:
Note: Inductors with DC resistance of less than 1Ω should be used in order to maintain the required voltage at the SFP input pin at 3.3V. When the recommended supply filtering circuit is used, hot plugging of the SFP transceiver module will result in an inrush current of no more than 30 mA greater than the steady state value.



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