
STM32
CubeMX

1. Description

1.1. Project

Project Name	TIM_basic
Board Name	custom
Generated with:	STM32CubeMX 6.0.1
Date	11/30/2020

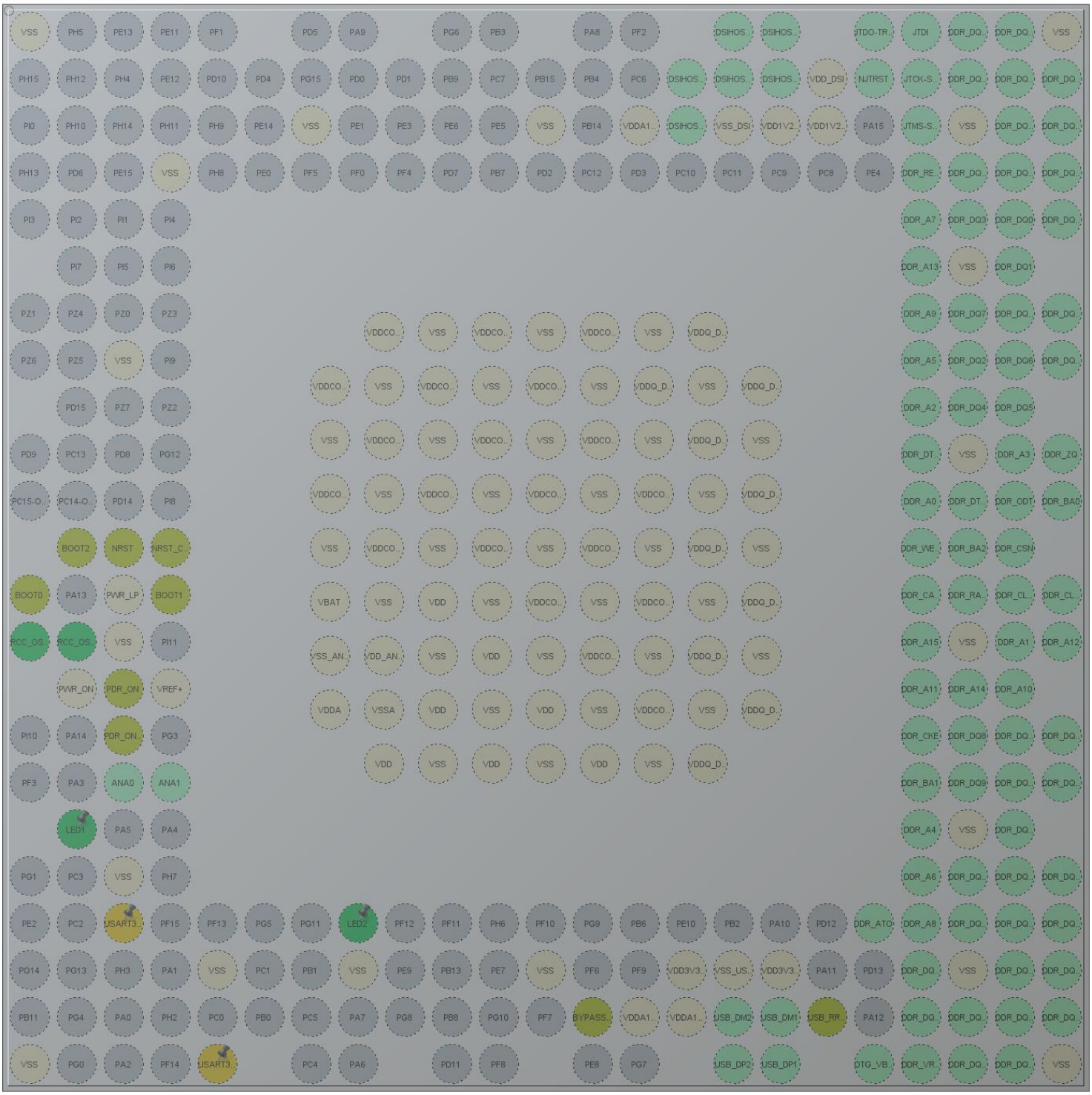
1.2. MCU

MCU Series	STM32MP1
MCU Line	STM32MP157
MCU name	STM32MP157AACx
MCU Package	TFBGA361
MCU Pin number	361

1.3. Core(s) information

Core(s)	ARM Cortex-A7 ARM Cortex-M4

2. Pinout Configuration



TFBGA361 (Top view)

3. Pins Configuration

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A23	VSS	Power		
B18	VDD_DSI	Power		
C7	VSS	Power		
C12	VSS	Power		
C14	VDDA1V8_DSI	Power		
C16	VSS_DSI	Power		
C17	VDD1V2_DSI_PHY	Power		
C18	VDD1V2_DSI_REG	Power		
C21	VSS	Power		
D4	VSS	Power		
F21	VSS	Power		
H3	VSS	Power		
K21	VSS	Power		
M2	BOOT2	Boot		
M3	NRST	Reset		
M4	NRST_CORE	Reset		
N1	BOOT0	Boot		
N3	PWR_LP	Power		
N4	BOOT1	Boot		
P1	PH0-OSC_IN	I/O	RCC_OSC_IN	
P2	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
P3	VSS	Power		
P21	VSS	Power		
R2	PWR_ON	Power		
R3	PDR_ON	MonoIO		
R4	VREF+	Power		
T3	PDR_ON_CORE	MonoIO		
V2	PG2 *	I/O	GPIO_Output	LED1
V21	VSS	Power		
W3	VSS	Power		
Y3	PB10 **	I/O	USART3_TX	
Y8	PB5 *	I/O	GPIO_Output	LED2
AA5	VSS	Power		
AA8	VSS	Power		
AA12	VSS	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
AA15	VDD3V3_USBHS	Power		
AA16	VSS_USBHS	Power		
AA17	VDD3V3_USBFS	Power		
AA21	VSS	Power		
AB13	BYPASS_REG1V8	MonoIO		
AB14	VDDA1V8_REG	Power		
AB15	VDDA1V1_REG	Power		
AB18	USB_RREF	MonoIO		
AC1	VSS	Power		
AC5	PB12 **	I/O	USART3_RX	
AC23	VSS	Power		
1A2	VDDCORE	Power		
1A3	VSS	Power		
1A4	VDDCORE	Power		
1A5	VSS	Power		
1A6	VDDCORE	Power		
1A7	VSS	Power		
1A8	VDDQ_DDR	Power		
1B1	VDDCORE	Power		
1B2	VSS	Power		
1B3	VDDCORE	Power		
1B4	VSS	Power		
1B5	VDDCORE	Power		
1B6	VSS	Power		
1B7	VDDQ_DDR	Power		
1B8	VSS	Power		
1B9	VDDQ_DDR	Power		
1C1	VSS	Power		
1C2	VDDCORE	Power		
1C3	VSS	Power		
1C4	VDDCORE	Power		
1C5	VSS	Power		
1C6	VDDCORE	Power		
1C7	VSS	Power		
1C8	VDDQ_DDR	Power		
1C9	VSS	Power		
1D1	VDDCORE	Power		
1D2	VSS	Power		
1D3	VDDCORE	Power		

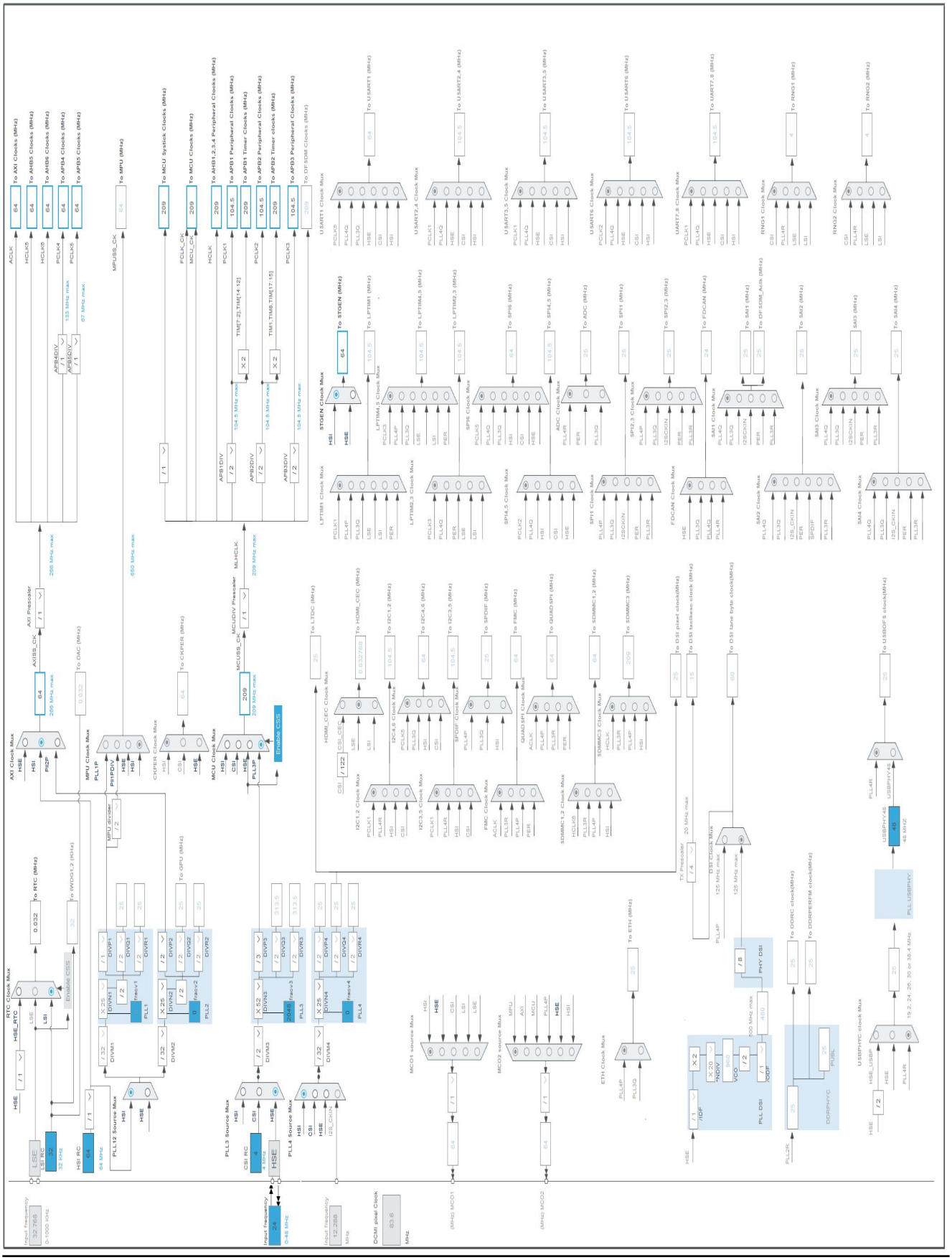
Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1D4	VSS	Power		
1D5	VDDCORE	Power		
1D6	VSS	Power		
1D7	VDDCORE	Power		
1D8	VSS	Power		
1D9	VDDQ_DDR	Power		
1E1	VSS	Power		
1E2	VDDCORE	Power		
1E3	VSS	Power		
1E4	VDDCORE	Power		
1E5	VSS	Power		
1E6	VDDCORE	Power		
1E7	VSS	Power		
1E8	VDDQ_DDR	Power		
1E9	VSS	Power		
1F1	VBAT	Power		
1F2	VSS	Power		
1F3	VDD	Power		
1F4	VSS	Power		
1F5	VDDCORE	Power		
1F6	VSS	Power		
1F7	VDDCORE	Power		
1F8	VSS	Power		
1F9	VDDQ_DDR	Power		
1G1	VSS_ANA	Power		
1G2	VDD_ANA	Power		
1G3	VSS	Power		
1G4	VDD	Power		
1G5	VSS	Power		
1G6	VDDCORE	Power		
1G7	VSS	Power		
1G8	VDDQ_DDR	Power		
1G9	VSS	Power		
1H1	VDDA	Power		
1H2	VSSA	Power		
1H3	VDD	Power		
1H4	VSS	Power		
1H5	VDD	Power		
1H6	VSS	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1H7	VDDCORE	Power		
1H8	VSS	Power		
1H9	VDDQ_DDR	Power		
1J2	VDD	Power		
1J3	VSS	Power		
1J4	VDD	Power		
1J5	VSS	Power		
1J6	VDD	Power		
1J7	VSS	Power		
1J8	VDDQ_DDR	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	TIM_basic
Project Folder	E:\STM32CubeIDE\workspace_1.4.0\embedfire\10TIM_basic\TIM_basic
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_MP1 V1.2.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-A7

Rank	Function Name	IP Instance Name

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ETZPC_Init	ETZPC
4	MX_TIM6_Init	TIM6

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32MP1
Line	STM32MP157
MCU	STM32MP157AACx
Datasheet	DS12504_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

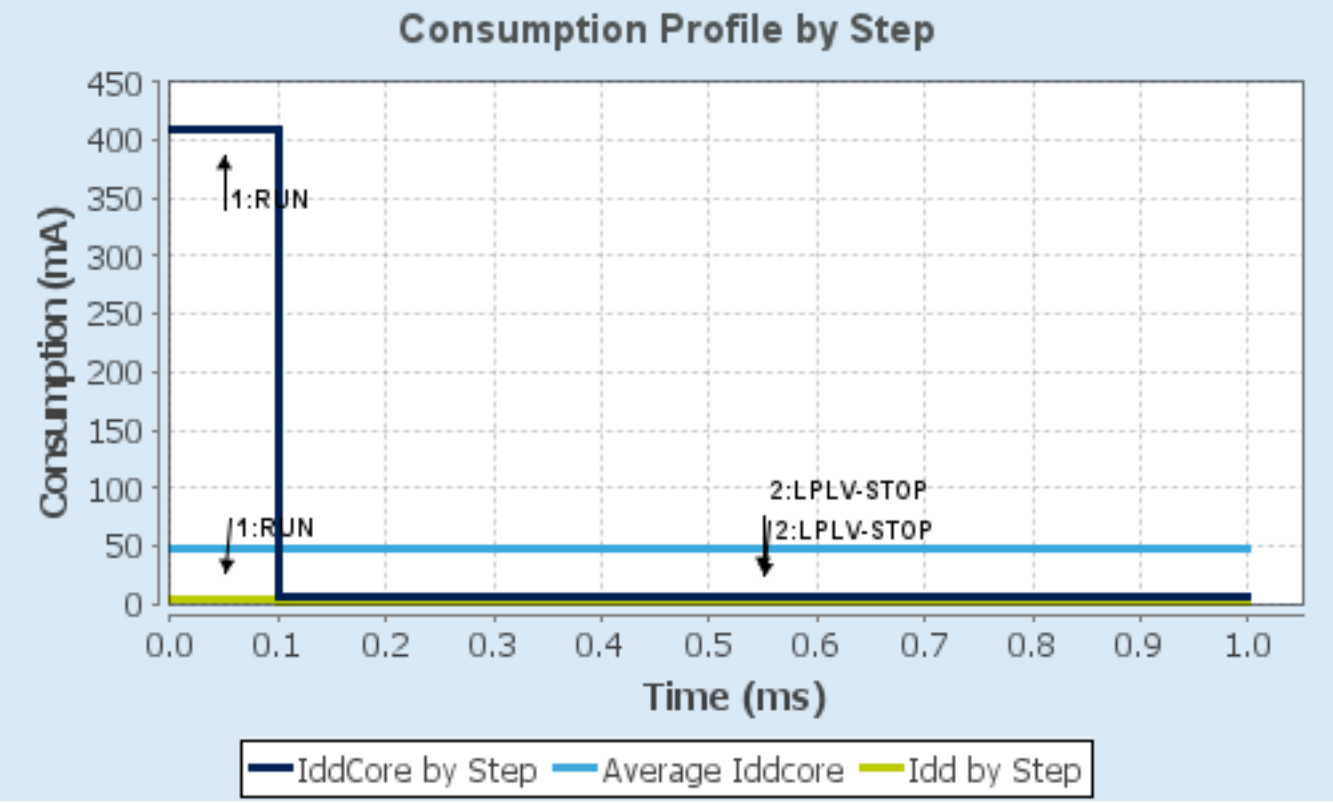
6.4. Sequence

Step	Step1	Step2
Mode	RUN	LPLV-STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Vdd Core	1.25	0.85
MPU0 Mode	P0RUN	P0STOP
MPU1 Mode	P1RUN	P1STOP
MCU Mode	CRUN	CSTOP
Fetch Type	SRAM	NA
MPU0/MPU1 Frequency	648 MHz	0 Hz
Clock Configuration	HSE HSI LSI PLL ALL_IPs_ON	ALL CLOCKS OFF
MCU Frequency	210 MHz	0 Hz
AXI Frequency	264 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Idd Core	410 mA	6.05 mA
Idd	3.7 mA	0.83 mA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	46.44 mA
Battery Life	1 month, 1 day, 20 hours	Average DMIPS	0.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
450
400
350
300
250
200
150
100
50
0
1:RUN
1:RUN
2:LPLV-STOP
2:LPLV-STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
IddCore by Step
Average Iddcore
Idd by Step

7. IPs and Middleware Configuration

7.1. BSEC

mode: Activated

7.2. ETZPC

mode: Activated

7.3. GIC

7.4. GPIO

7.5. HSEM

mode: Activated

7.6. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.6.1. Parameter Settings:

Core(s) Settings:

Context(s):	Boot ROM Boot loader Cortex-A7 secure Cortex-A7 non secure Cortex-M4
Initialized Context:	Boot ROM
Power Domain:	

Spread spectrum mode:

PLL1 CSG mode	DISABLED
PLL2 CSG mode	DISABLED
PLL3 CSG mode	DISABLED
PLL4 CSG mode	DISABLED

RCC Parameters:

TIM Group1 Prescaler Selection	Disabled
TIM Group2 Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16

HSI Calibration Value	16
HSI clock calibration feature	Enable
CSI clock calibration feature	Enable
Periodic calibration Value	60

System Parameters:

VDD voltage (V)	3.3

PLL1 configuration:

User defined configuration	FALSE

7.7. RTC

mode: Activate Clock Source

7.7.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 secure
Power Domain:	

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.8. SYS

Timebase Source: SysTick

7.9. TAMP

mode: Activated

7.10. TIM6

mode: Activated

7.10.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4

Initialized Context:	Cortex-M4
Power Domain:	

Counter Settings:

Prescaler (PSC - 16 bits value)	**20900-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**5000-1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a		Boot ROM* Boot loader Cortex-A7	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a		Boot ROM* Boot loader Cortex-A7	
Single Mapped Signals	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low			
	PB12	USART3_RX	Alternate function	No pull-up and no pull-down	n/a			
GPIO	PG2	GPIO_Output	Output Push Pull	**Pull-up ***	**Medium ***	LED1	Cortex-M4	
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED2	Cortex-M4	

* Initialized context

8.2. DMA configuration

nothing configured in DMA service

8.3. MDMA configuration

nothing configured in DMA service

8.4. NVIC configuration

8.4.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM6 global interrupt	true	0	0
RCC global interrupt	unused		
FPU global interrupt	unused		
HSEM interrupt 2	unused		
Cortex-A7 send event interrupt through EXTI line 66	unused		
RCC wake-up interrupt	unused		

8.4.2. NVIC Code generation

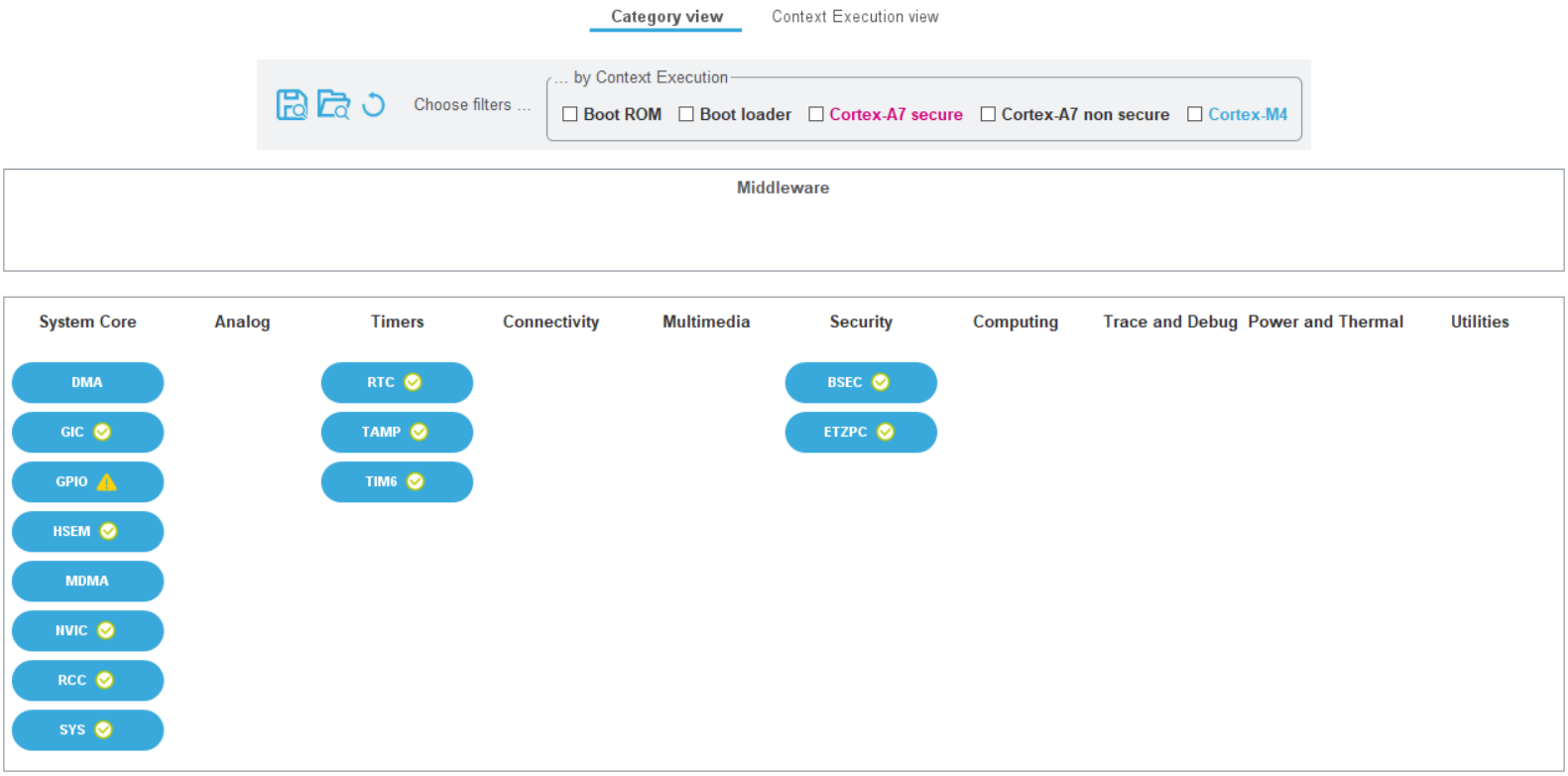
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Pre-fetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
TIM6 global interrupt	true	true	true

*** User modified value**

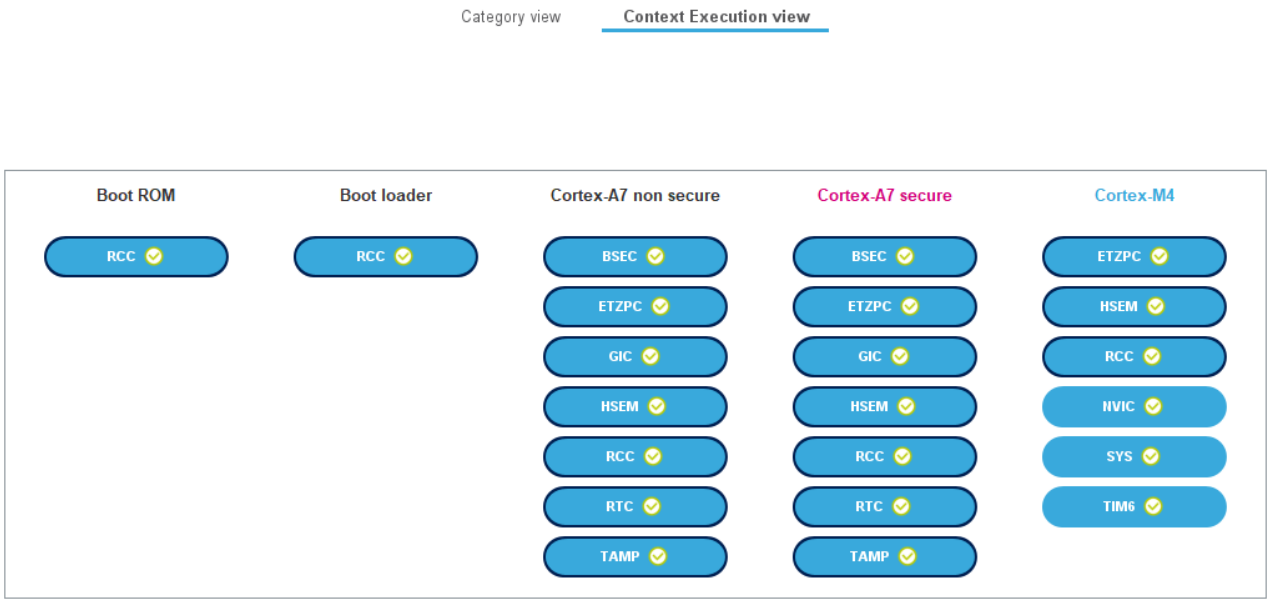
9. System Views

9.1. Category view

9.1.1. Current



9.2. Context Execution view



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00489389.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00327659.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00596687.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00516256.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00389996.pdf
Application note	http://www.st.com/resource/en/application_note/DM00449434.pdf
Application note	http://www.st.com/resource/en/application_note/DM00462392.pdf
Application note	http://www.st.com/resource/en/application_note/DM00505673.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00560967.pdf
Application note	http://www.st.com/resource/en/application_note/DM00595472.pdf
Application note	http://www.st.com/resource/en/application_note/DM00561921.pdf
Application note	http://www.st.com/resource/en/application_note/DM00589815.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00564136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00681502.pdf
Application note	http://www.st.com/resource/en/application_note/DM00693021.pdf

Application note http://www.st.com/resource/en/application_note/DM00713831.pdf