AMPAK Technology Inc.

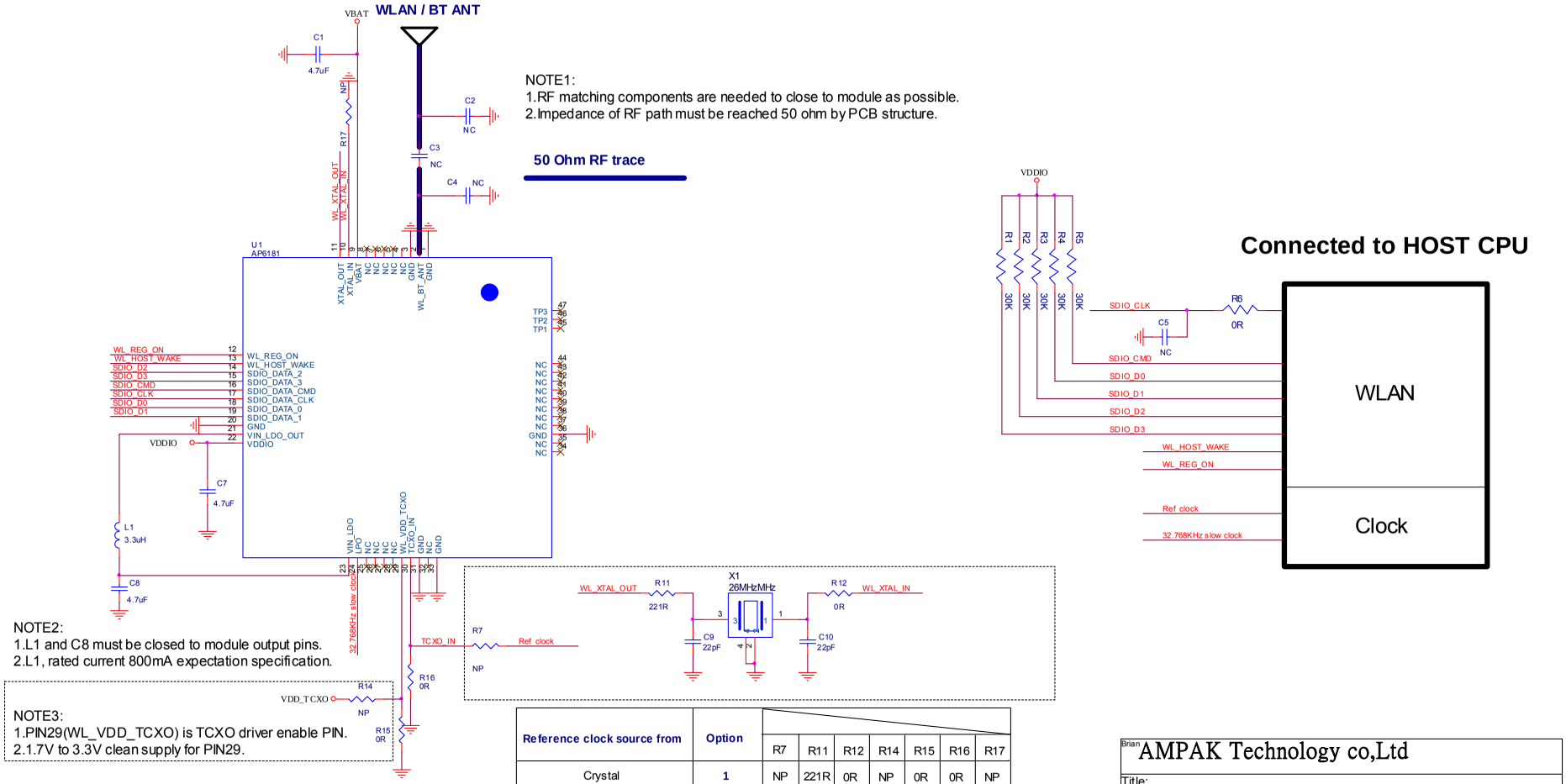
Advanced Module Packaging Solution

正基科技股份有限公司

Revision History

Date	Revision Content	Revised By	Version
2012/10/01	- Initial released	Joe	1.0

AP6181 reference design circuit



Reference clock source from	Option	R7	R11	R12	R14	R15	R16	R17
Crystal	1	NP	221R	0R	NP	0R	0R	NP
System clock (Should be met spec. of Table3)	2	0R	NP	NP	0R	NP	NP	0R

Brian AMPAK Technology co,Ltd		
Title:		
Size: C	File: AP6181 reference design	Sheet: 1 of 1
Directory: <design name>		Rev: 01
Design: Joe	Appvd: Brian	Now date: 2012.10.1 Present date:

Note: Peripheral components highlight

Item	Qty	Reference	Value	Description	Vendor
1	3	C1,C7,C8	4.7uF	Capacitor 4.7uF 10V 10%(K) X5R 0805 T=1.25mm	Murata, WALSIN
2	2	C9,C10	22pF	Capacitor 22pF 50V 0.25P(C) NPO 0402 T=0.5mm	Murata, WALSIN
3	1	L1	3.3uH	Power Inductor (HF) 3.3uH 2.5*2.0mm Rated current 800mA	Murata, TDK
4	1	R11	221R	Resistor 221 ohm 1/16W 5% 0402	YAGEO, WALSIN
5	5	R1,R2,R3,R4,R5	30K	Resistor 30K ohm 1/16W 5% 0402	YAGEO, WALSIN
6	4	R6,R12,R15,R16	0R	Resistor 0 ohm 1/16W 5% 0402	YAGEO, WALSIN
7	1	X1	26MHz	XTAL 26MHz+/-20ppm CL=16pF, ESR 60ohm(Max.) 3.2x2.5x0.55mm SMD -30~+85℃	HOSONIC, TAI-SAW
8	1	U1	AP6181	Module AP6181 WLBGA-44 802.11b/g/n 12x12 mm -30~+85℃	AMPAK

Table1. BOM

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	±30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1600 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

Table2. 32.768KHz clock requirements and performance

Peripheral interface highlight

❖ Power Source: A single host power supply can be used (including VBAT ranging from 3.0V to 4.8V) for AP6210 module and external VDDIO ranging from 1.71V to 3.6V supplies for GPIO by host power. Power topology is shown as below figure.

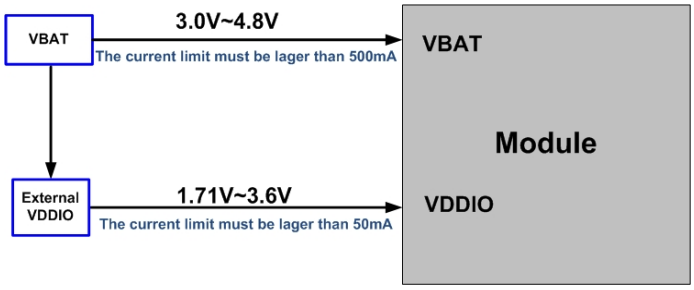


Figure1. Power topology

❖ Reference clock: About reference clock, as an alternative to a crystal, an external system clock can be used as the frequency reference, provided that it meets the phase noise requirements listed in table3 for WiFi requirements.

		Crystal			Reference clock shared from HOST system			
Parameter	*Conditions/Notes*	*Min*	*Typ*	*Max*	*Min*	*Typ*	*Max*	*Units*
Frequency	–	Between 12 MHz and 52 MHz[a]						
Crystal load capacitance	–	–	12	–				pF
ESR	–	–	–	60				Ω
Input Impedance (OSCIN)[b]	Resistive				30k	100k	–	Ω
	Capacitive				–	–	7.5	pF
Input Impedance (WRF_TCXO_IN)	Resistive				30k	100k	–	Ω
	Capacitive				–	–	4	pF
OSCIN input voltage	AC-coupled analog signal				400	–	1200	mV_{p-p}
OSCIN input low level	DC-coupled digital signal				0	–	0.2	V
OSCIN input high level	DC-coupled digital signal				1.0	–	1.36	V
WRF_TCXO_IN input voltage	DC-coupled analog signal[c]				400	–	TCXO_VDD[d]	mV_{p-p}
Frequency tolerance Initial + over temperature	–	−20	–	20	−20	–	20	ppm
Duty cycle	26 MHz clock				40	50	60	%
Phase Noise[e, f] (IEEE 802.11 b/g)	26 MHz clock at 1 kHz offset				–	–	−119	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	−129	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	−134	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	−139	dBc/Hz
Phase Noise[e, f] (IEEE 802.11n, 2.4 GHz)	26 MHz clock at 1 kHz offset				–	–	−124	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	−134	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	−139	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	−144	dBc/Hz

Table3. Crystal and eternal system clock requirements and performance for WiFi

❖ WIFI SDIO: Using external pull up resistors depends on the SDIO supply voltage. For 1.8V, the resistance range is 30~82KΩ. For 2.6V, it range from 21~41 KΩ. For 3.3V, it range from 15~35 KΩ on the four data lines and the CMD line as the following circuitry.

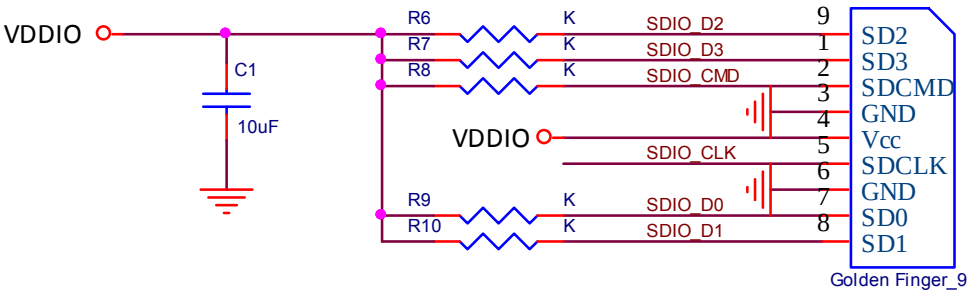


Figure2.