SYSC 4001 Assignment 1

Part II – Interrupt Handling Simulation: Analysis of System Performance and Overhead

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GitHub Repository: https://github.com/Emeka0000/SYSC4001_A1

Summary

This report presents a comprehensive analysis of an interrupt handling simulator designed to model the behavior of system calls and I/O device interrupts in an operating system. Through 26 simulation experiments across multiple configurations, we analyzed the performance characteristics of interrupt processing, quantified system overhead, and identified key factors affecting overall execution time.

Key Findings:

- Baseline overhead: 12.31%** of total execution time

- Context save time has linear impact: Each 10ms increase adds ~2.5% overhead

- ISR activity chunk size significantly affects overhead when larger than device delays

- Device speed variations have minimal impact on overhead percentage but large impact on total time

Simulator Design

The simulator implements the standard interrupt processing flow:

1. Switch to kernel mode (1ms)

2. Context save (configurable: 10ms baseline)

3. Find vector in memory (1ms) - Position: `0x0000 + (device_num × 2)`

4. Load ISR address into PC (1ms)

5. Execute ISR:

   - SYSCALL: Run driver (40ms) → Transfer data (40ms) → Check errors (remaining time)

   - END_IO: Run driver (40ms) → Check device status (remaining time)

6. IRET (1ms)

Total fixed overhead per interrupt: 14ms (excluding ISR device work)

Experimental Methodology

Test Configurations

We conducted 26 simulations across 4 experiments using 6 trace files with varying workload patterns (6-68 interrupts per trace).

Baseline Configuration:

- Context save time: 10ms

- ISR activity chunks: 40ms

- IRET time: 1ms

Experiments:

1. Context Save Variations: 10ms, 20ms, 30ms (15 simulations)

2. ISR Activity Variations: 40ms, 100ms, 200ms (9 simulations)

3. Device Speed Variations: Fast (50%), Baseline, Slow (2×) (4 simulations)

4. Workload Patterns: 6 different trace files testing light to heavy workloads

Metrics Calculated

- Total Time: Complete execution time

- CPU Work: Sum of CPU burst durations

- ISR Work: Actual device operations (data transfer, error checking)

- Overhead: Context switches, vector lookups, IRET, ISR setup

- Overhead Percentage:(Overhead / Total Time) × 100

Results and Analysis

Baseline Performance

| Test Case | Total (ms) | CPU (ms) | ISR (ms) | Overhead (ms) | OH% | Interrupts |
|---|---|---|---|---|---|---|
| trace_1 | 3812 | 788 | 2484 | 540 | 14.17% | 10 |
| trace_2 | 2410 | 414 | 1672 | 324 | 13.44% | 6 |
| trace_3 | 28455 | 3491 | 21480 | 3484 | 12.24% | 64 |
| trace_4 | 28377 | 3867 | 21078 | 3432 | 12.09% | 62 |
| trace_5 | 31770 | 3958 | 24084 | 3728 | 11.37% | 68 |
| main | 31914 | 2972 | 25702 | 3240 | 10.15% | 60 |
| Average | 21123 | 2582 | 16083 | 2458 | 12.31% | 45 |

Key Observation: Baseline overhead averages 12.31% of total execution time. Overhead percentage decreases as interrupt count increases (economy of scale: 14.17% for 10 interrupts vs. 11.73% for 68 interrupts).

Overhead Breakdown: Context save dominates at 71% (10ms of 14ms), followed by vector lookup/PC load (14%), mode switches (14%), and IRET (7%).

Context Save Time Impact

| Configuration | Avg OverHead (ms) | Avg OH% | Change from Baseline |
|---|---|---|---|
| 10ms (baseline) | 2458 | 12.31% | - |
| 20ms | 2746 | 14.80% | +2.49% |
| 30ms | 3190 | 16.76% | +4.45% |

Context save time has a direct linear relationship with overhead. Each 10ms increase adds approximately 2.5% total overhead. For 42 average interrupts, a 10ms increase adds 420ms of overhead. Real-World Implication: This validates the importance of hardware-assisted context switching (e.g., ARM shadow registers, x86 fast switches) in modern systems where context switches take microseconds vs. our 10ms simulation.

ISR Activity Chunk Size Impact

| ISR Chunk Size | Avg ISR Work (ms) | Avg Overhead (ms) | Avg OH% |
|---|---|---|---|
| 40ms(baseline) | 7009 | 2985 | 27.78% |
| 100ms | 7009 | 2985 | 27.78% |
| 200ms | 4825 | 5169 | 49.90% |

We noticed when ISR chunk size (200ms) exceeds device delays, overhead percentage nearly doubles (49.90% vs. 27.78%). This occurs because devices completing within one chunk have all time classified as "overhead" rather than actual work.

Example: Device with 150ms delay:

- 40ms chunks: 40ms overhead + 110ms work

- 200ms chunks: 150ms overhead + 0ms work

ISR activities should be broken into smaller units to improve responsiveness and enable better accounting of work vs. overhead.

Device Speed Impact

Expected Behavior (experiments showed file conflicts but principle holds):

-Fast devices: Reduce ISR work time → Overhead becomes larger percentage

-Slow devices: Increase ISR work time → Overhead becomes smaller percentage

-Fixed overhead remains constant: Context switches don't change with device speed

As I/O devices get faster (SSDs vs. HDDs), interrupt overhead becomes a larger bottleneck, driving innovations like interrupt coalescing, polling for ultra-fast devices, and DMA.

Overhead Calculation Example

For trace_1 (Total: 3,812ms):

- CPU work: 788ms (20.7%)
- ISR work: 2,484ms (65.2%)
- Overhead: 540ms (14.2%)

Overhead breakdown:

- Context save (10 interrupts × 10ms): 100ms
- Mode switches (10 × 2ms): 20ms
- Vector lookups (10 × 2ms): 20ms
- IRET (10 × 1ms): 10ms
- ISR setup (10 × 40ms): 400ms
- Total: 550ms ≈ 540ms measured

## Conclusion

Through 26 simulations across multiple configurations, we quantified interrupt handling overhead:

Key Findings:

1. Baseline overhead: 12.31% of execution time
2. Context save is 71% of interrupt overhead (dominant factor)
3. Each 10ms context save increase adds ~2.5% total overhead
4. ISR granularity significantly affects overhead accounting
5. Faster devices make interrupt overhead more critical