

# STORMING THE GATES: REFET Combined with Stable Stochastic Signal Generation for Post Deterministic Logic Gates

Version 1.2

A Simple Hybrid System to Aid Exotic Quantum Technology Development and Implementation

White Paper

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## Introduction

Modern electronic systems have traditionally treated noise as an adversary to be mitigated or filtered out. This paradigm is inverted by the Reliability-Failure Effect Transistor (REFET) approach, which leverages inherent quantum-scale unpredictability in ordinary MOSFETs, operated at their reliability edge, to generate robust, controlled, non-Gaussian stochastic signals. When configured alongside a conventional stable stochastic signal source, such as an ion chamber from a common smoke detector, new classes of logic gates arise. These hybrid configurations form the basis of low-cost, versatile, and powerful post-deterministic logic gates, with direct applications for affordable quantum technology verification and research.

## REFET Fundamentals

A typical REFET device uses a readily available N-channel MOSFET, biased just below breakdown to amplify quantum and atomic-level phenomena, leading to measurable stochastic charge carrier activity. Over time, these activities manifest as broadband, non-Gaussian noise and stochastic bursts, which, under proper circuit conditions, are stable and reproducible. A REFET's output is shaped by intrinsic quantum fluctuations, distinguishing it from traditional thermal or digital noise sources.

By pairing a REFET with a stable stochastic generator—sourced, for example, from an ionization chamber component confirmed to comply with NIST random standards—the resulting circuit achieves dual independent entropy sources. One source (the ion chamber) provides a continuous, relatively unbiased background noise. The other (REFET) delivers metastable, quantum-origin entropy events when suitably triggered.

## Example Logic Gates Realized via Hybrid Stochastic Configuration

### 1. Physical XOR (Exclusive-Or) Gate:

Configuration:

Connect outputs from both the stable ion chamber and the REFET device to a

high-speed analog comparator or pulse monitoring circuit.

Define a coincidence window using a timing circuit (e.g., monostable multivibrator or microcontroller timer input).

Achievement:

The gate outputs “true” (logic high) only when a burst event is detected from one source but not both within the coincidence window.

Physically, this means that only non-simultaneous stochastic events propagate as “positive” logical events, embodying a non-deterministic, entropy-driven XOR.

2. Physical AND Gate:

Configuration:

Both stochastic outputs are monitored by a time window circuit.

Achievement:

The gate produces a “true” output only when both sources trigger an event within the predefined coincidence interval.

This physically implements the logical AND gate through detection of simultaneous independent random events.

3. Physical NOT Gate:

Configuration:

Use stable noise as a reference and trigger REFET events to invert the state.

Achievement:

An event from the REFET in the absence of a stable source event within the timing window triggers a “true” NOT state; otherwise, the output remains “false.”

4. Physical OR Gate:

Configuration:

Monitor inputs from both sources and output “true” if either fires within the interval.

Achievement:

An event from either the stable or triggerable source, or both, registers as logical “true,” matching the classical OR but realized with non-deterministic events.

5. Stochastic Majority and Parity (Bell-Type) Gates:

Configuration:

Use multiple REFET and stable channel pairs in parallel, with a summing logic or voting circuit (analog or digital microcontroller aggregation).

Achievement:

Output follows the majority or parity of firing among all input pairs, providing probabilistic, robust logic suitable for error-detecting and quantum analog operations such as Bell-type measurements.

How These Gates are Achieved

The essential mechanism is coincidence detection over user-defined time intervals. By using comparators and timing circuits, the random and burstlike nature of stochastic events from both stable and triggerable sources are translated into classical logic pulse outputs. This allows not just direct logic computation, but enables higher-level probabilistic, cryptographic, and verification processes, all without digitally pre-selecting outcomes or filtering entropy out. Logic circuits developed under these principles are easily validated empirically, robust to environmental fluctuations, and provide physical randomness directly at the logic gate level.

## Applications for Quantum Testing and Verification

With these gates, hybrid stochastic logic can be deployed for:

- In-line environmental and process state monitoring of quantum systems, precluding deterministic failures.
- Physical random number generation and entropy validation in research and cryptographic tasks.
- Cross-verification of quantum state claims, enabling low-cost reliability audits for entanglement or superposition testing.
- Development of secure, dynamically reconfigurable “physical logic memory” and unclonable signatures.
- Rapid, parallelizable device validation across multiple quantum experiments, democratizing quantum-class technology access.

## System Implementation

A standard build uses commodity N-MOSFETs (such as IRF540Z), low noise bias circuitry, a high-resistance load, and amplifier. For the stable source, an ion chamber with suitable interface electronics provides the baseline. All logic gates described are created with simple analog components or microcontroller digital acquisition of comparator outputs, ensuring reproducibility and ease of adoption.

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