International Roadmap Devices & Systems (IRDS) More Moore Update for Defect Definitions at the Yield Workshop

November 7, 2023

ROADMAP SUMMARIES

IRDS MORE MOORE ROADMAP

Cloud and edge computing w/ **intelligent connectivity** at all levels driving System Scaling

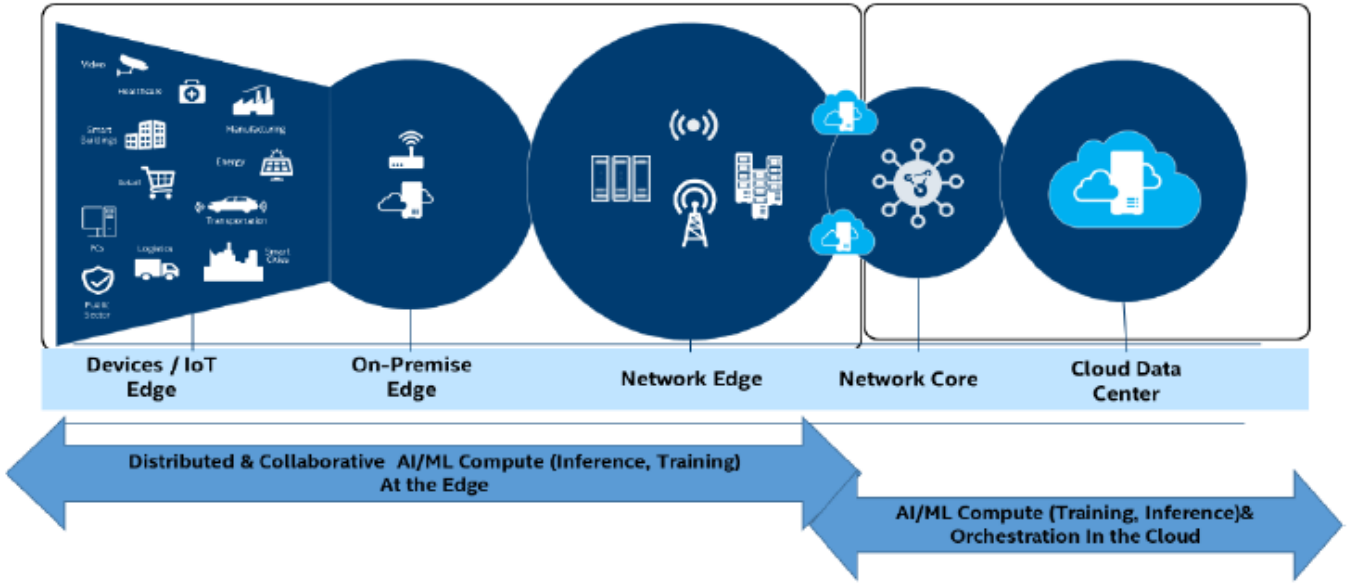
- Device-interconnect-memory technologies for mobile and cloud+HPC computing
  - Mobile computing - additional functionality, biometrics, and display/camera/sensing for increased consumer value
  - Cloud+HPC computing - 2.5D/3D integration to scale memory bandwidth / power and latency
- Convergence of edge and cloud computing by 5G/6G and distributed AI

Big Data and abundant computing power are pushing computing to the **Cloud**

Micro (data) servers
Increasing data on cloud requires high-density memories

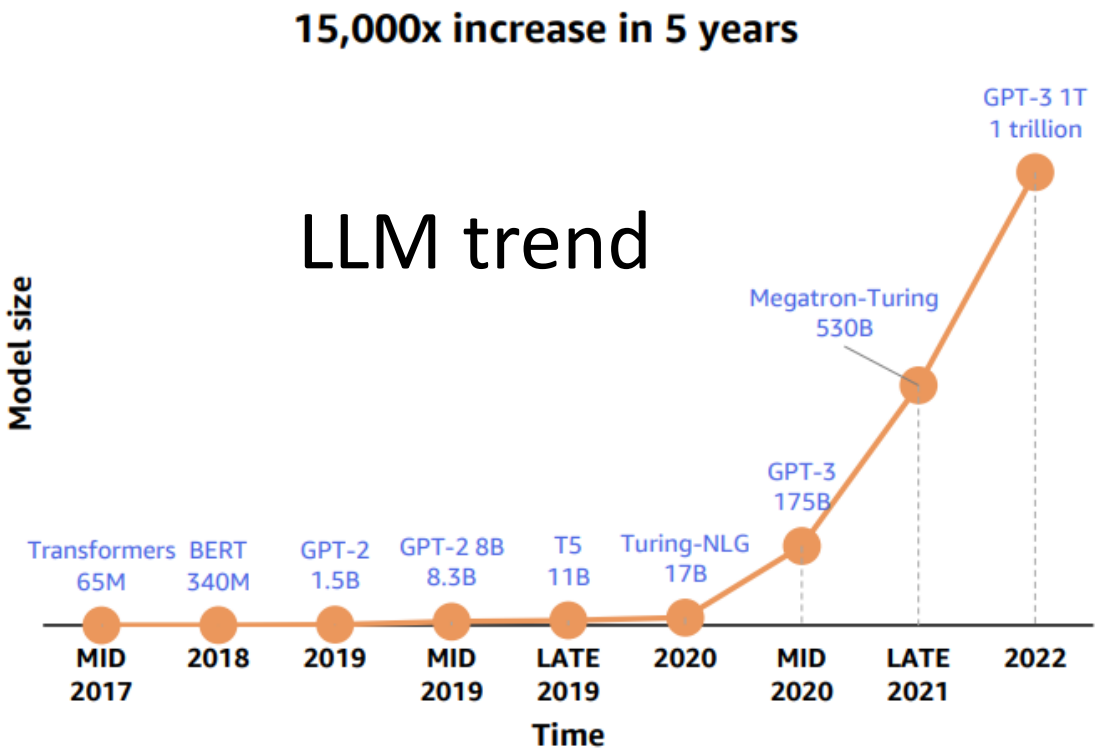
Instant Data generated by sensors and users are pushing computing to the **Edge**

Mobile computing
AI at edge requires fast and high-density memories



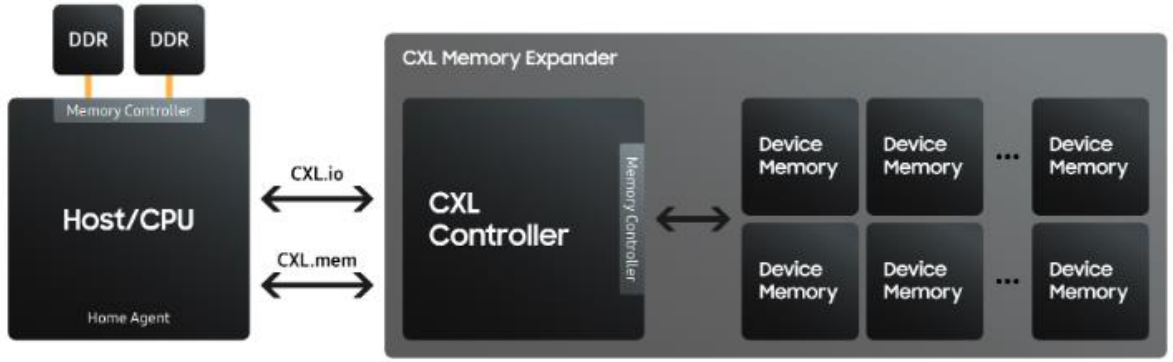
Source: 5G At the Edge, 5G Americas, 2019

Growing need for memory bandwidth and capacity and efficient data transfer



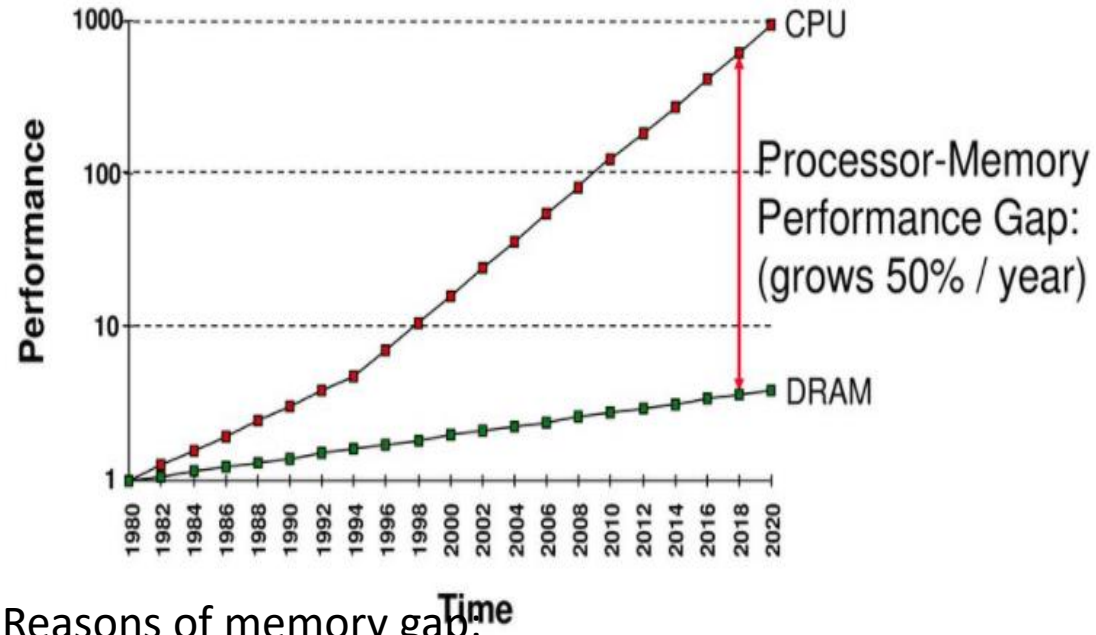
Source: AWS@2022

- ChatGPT Token ~ Word,
- Basic chat: 5 tokens/sec (~reading speed), requiring delivering 175B int8 parameters in 200ms
- BW=875GB/sec required
  - Capacity: 8 HBM3 memories needed
  - Bandwidth: 8*819GB/sec (8192 IOs)
- Need for memory and compute coherency



Source: Samsung

Memory wall addressed by SLI: Protocol, I/O, and interconnect



Reasons of memory gap:

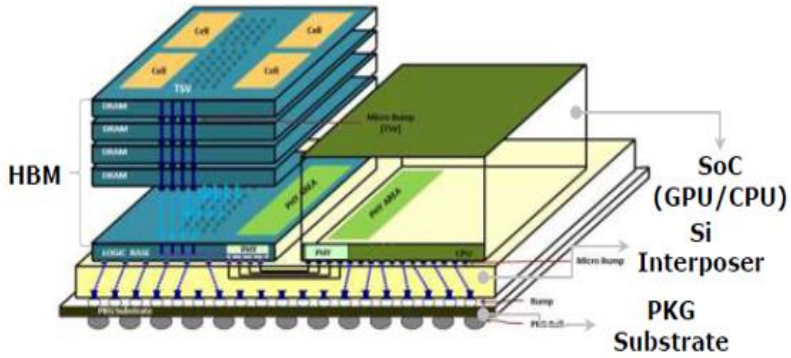
1. Power wall (energy/bit delta in compute and DRAM)
2. Slow IO bandwidth scaling vs compute area efficiency
3. DRAM data re-use in compute getting worse

Mitigation:

1,2: Compute-in/near-memory

2 => High-bandwidth memory

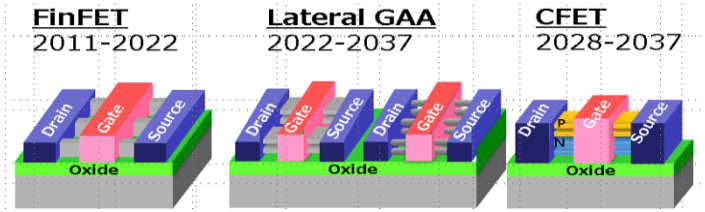
3 => Large cache such as 3D-SRAM and novel NoC fabrics



IO speed and bandwidth scaling much faster than CPU speed

Source: SK Hynix and Rambus

2 complementing routes for system scaling



2D scaling for energy-efficient computing at scaled area

2022 — Nanosheet

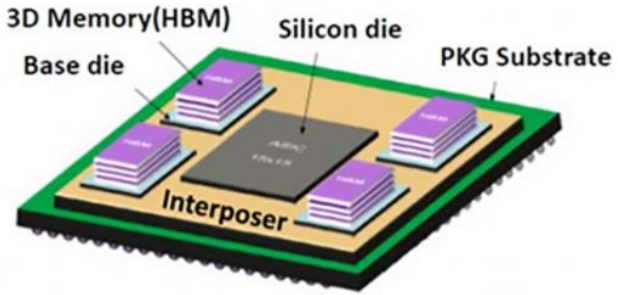
2028 — CFET SRAM

2031+ — Logic-on-Logic (Sequential-3D) 3D-SRAM

Classical 2D scaling

2020

System-technology-co-optimization
e.g. System Infrastructure to boost scaling



2022 — Memory (SRAM) On Logic

2025 — 3D-Memory on Logic Backside metal

2028 — Backside Devices Extreme stacking

2031+ — Domain-specific chiplets on active interposer (e.g. decap, memory, NOC, IO, ESD, VR)

Source: Edited from IRDS 2023 More Moore roadmap

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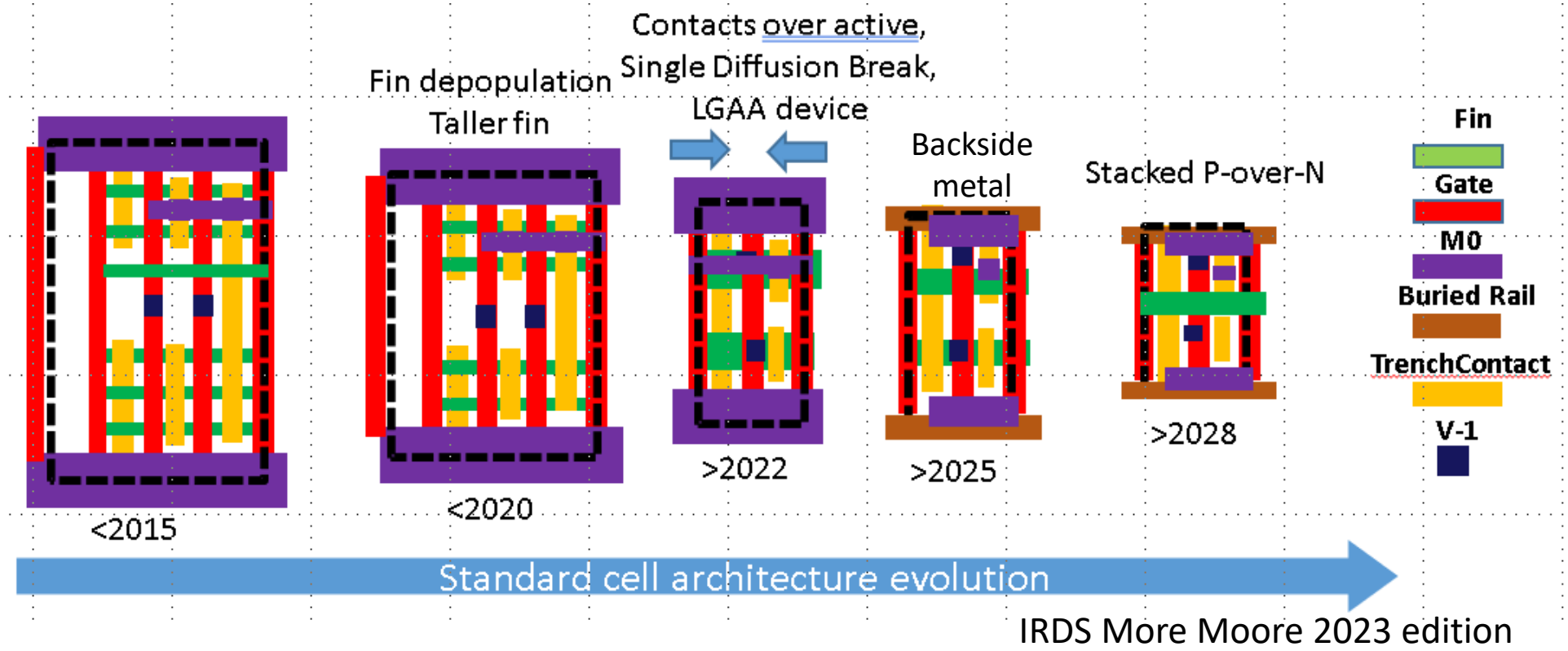
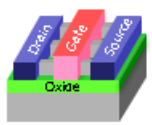
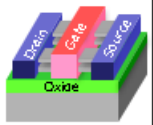
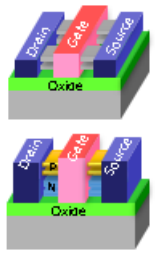
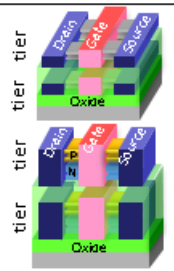
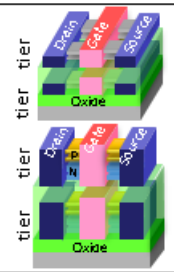
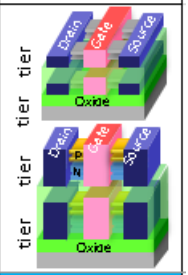
Buried power rail by >2025 and CFET by >2028



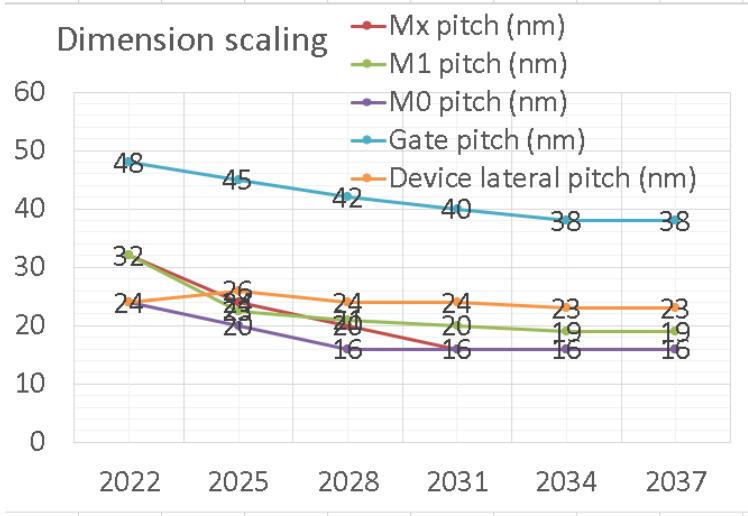
IRDS More Moore 2023 edition

- Front-side and back-side wafer processing
- High-aspect ratio vias and metallization at the backside

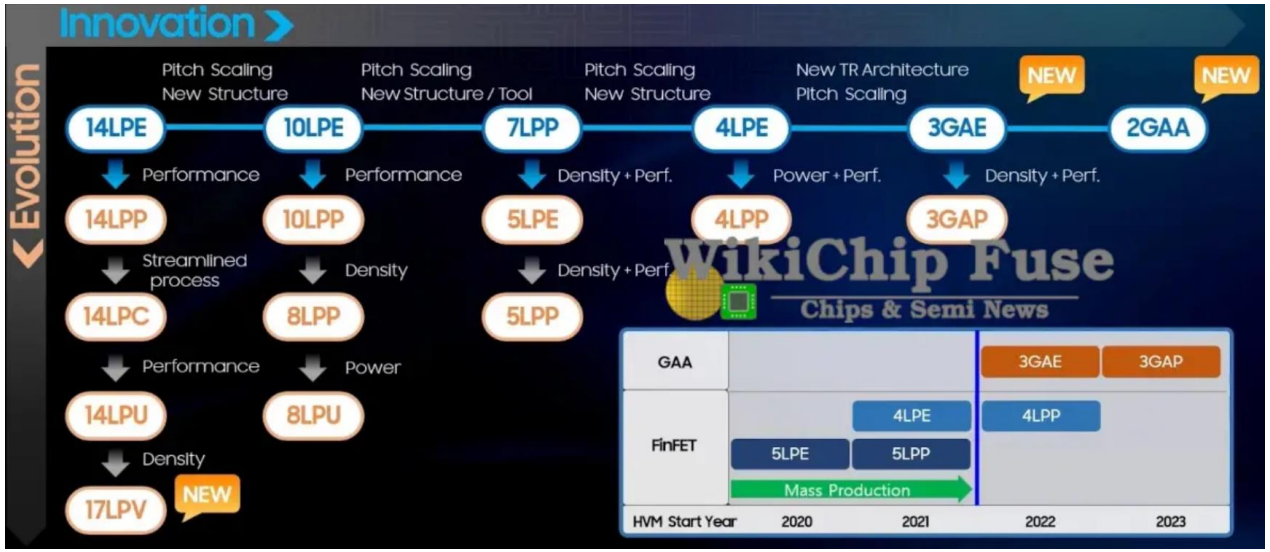
Logic ground rules – IRDS More Moore Logic

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
						
LOGIC DEVICE GROUND RULES						
Mx pitch (nm)	32	24	20	16	16	16
M1 pitch (nm)	32	23	21	20	19	19
M0 pitch (nm)	24	20	16	16	16	16
Gate pitch (nm)	48	45	42	40	38	38
Lg: Gate Length - HP (nm)	16	14	12	12	12	12
Lg: Gate Length - HD (nm)	18	14	12	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	19	20	18	18	18
Device architecture key ground rules						
Device lateral pitch (nm)	24	26	24	24	23	23
Device height (nm)	48	52	48	64	60	56
FinFET Fin width (nm)	5.0					
Footprint drive efficiency - finFET	4.21					
Lateral GAA vertical pitch (nm)		18.0	16.0	16.0	15.0	14.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0
Number of vertically stacked nanosheets on one device		3	3	4	4	4
LGAA width (nm) - HP		30	30	20	15	15
LGAA width (nm) - HD		15	10	10	6	6
LGAA width (nm) - SRAM		7	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	4.50	5.47	5.00	4.75
Device effective width (nm) - HP	101.0	216.0	216.0	208.0	160.0	152.0
Device effective width (nm) - HD	101.0	126.0	96.0	128.0	88.0	80.0
PN seperation width (nm)	45	40	20	15	15	10

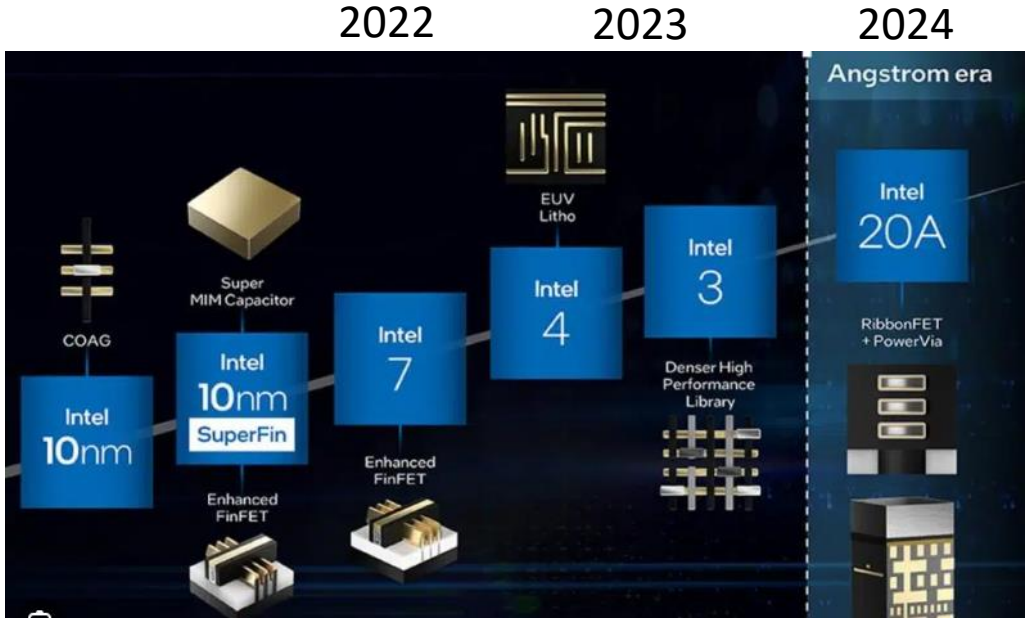
- M0 pitch critical to sustain cell area scaling
- Lg scaling saturating around 10-12nm
- 3 discrete GAA widths in SoC: HP, HD, SRAM but choosing which width to assign still flexible in GAA
- Device height, device width, and device vertical pitch critical for overall PPA scaling



Device technology roadmaps



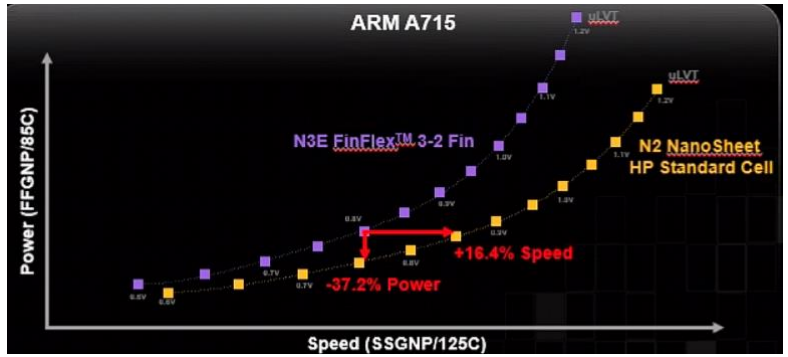
Samsung roadmap, Source: WikiChip



Intel roadmap

Production	2018	2019	2020	2021	2022	2023	2024	2025	2026
High-end (Premium Mobile, Data Center Server, AI Accelerator, Game, ADAS)	N7	N7+	N5	N5P N7A	N4	N3 N4P/N4X	N3E N5A	N2 N3P/N3X	N2P/N2X N3A

TSMC roadmap



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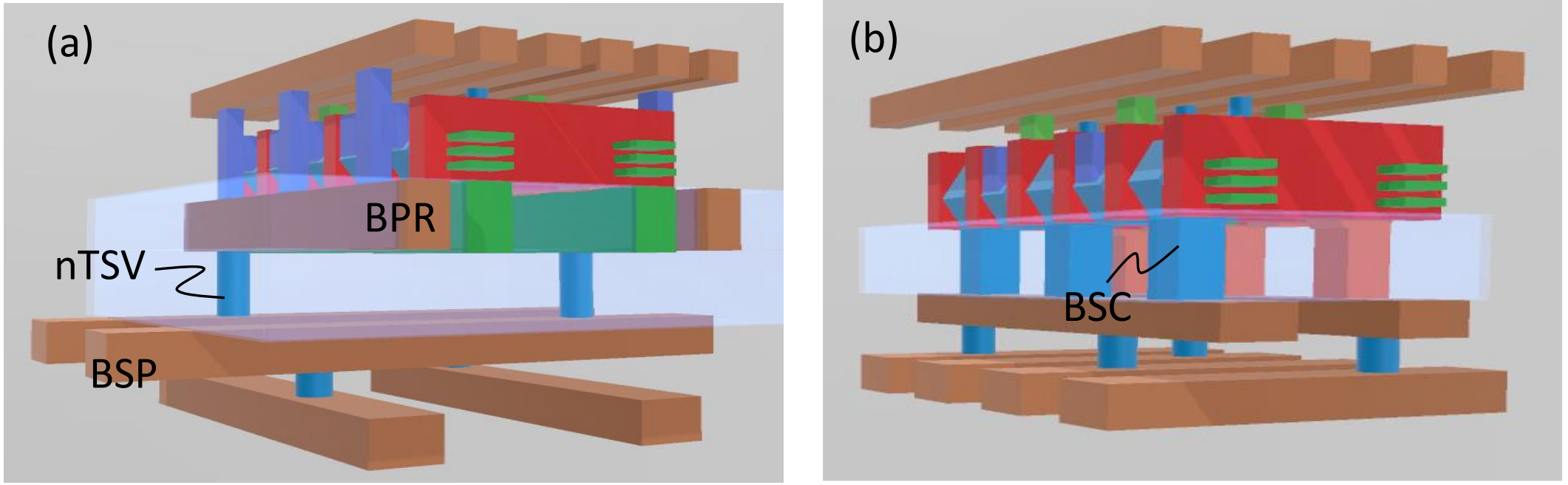
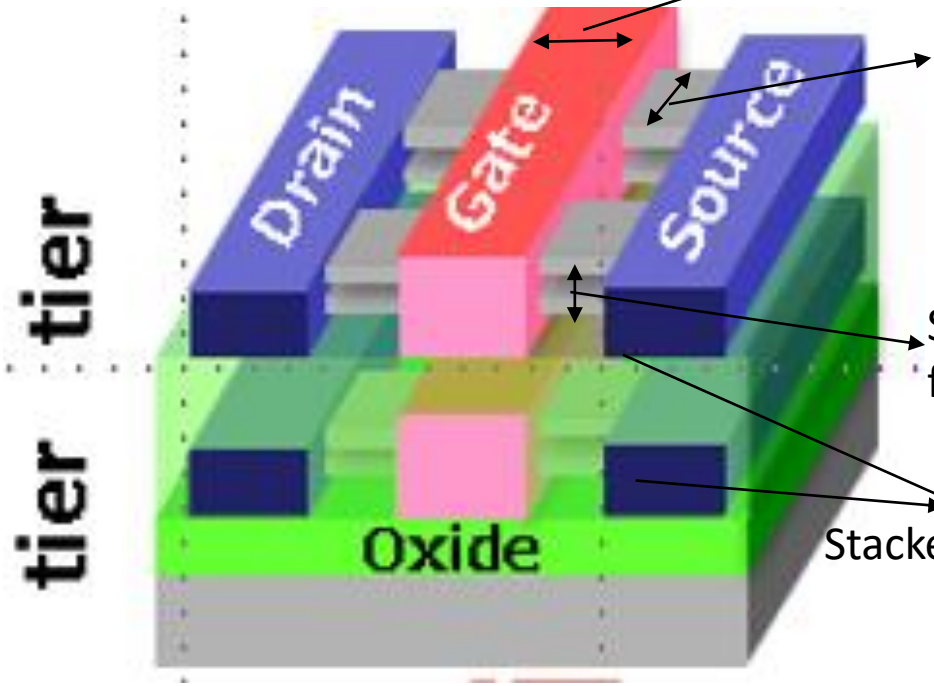
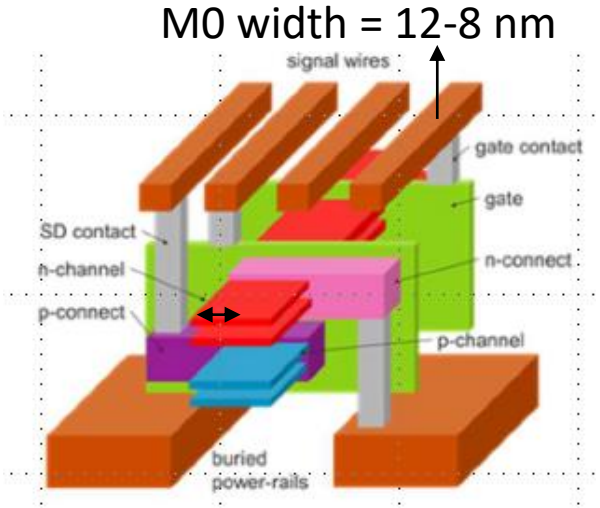
Backside power connection schemes



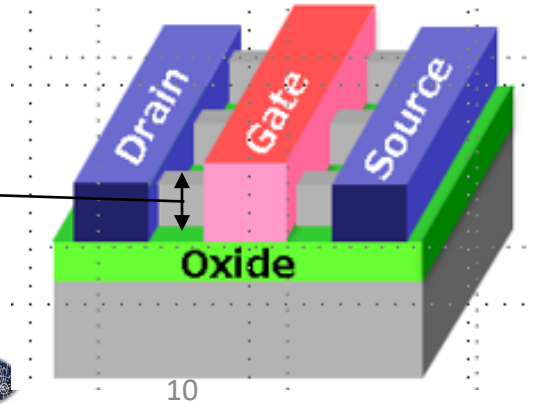
Two different Back Side Power (BSP) schemes as focal point:
(a) BPR+nTSV, (b) BSC (Back Side Contact)

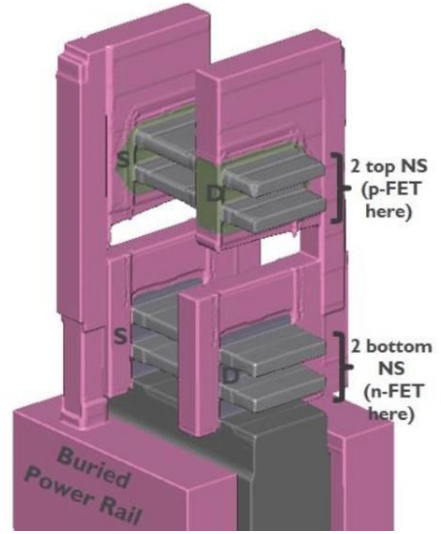
Critical dimensions across 2022-2037





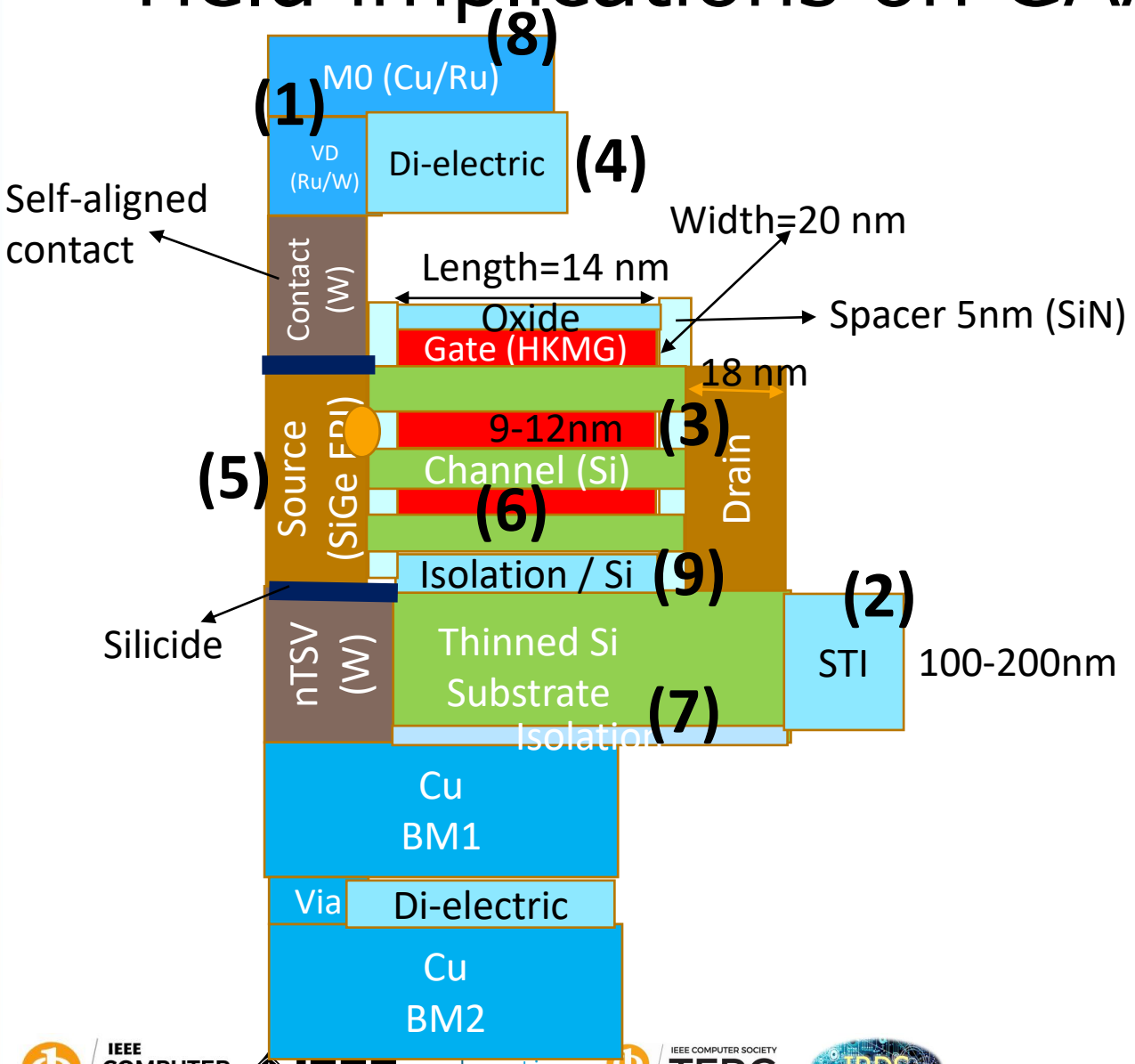
Source: TEL@IEDM-2021





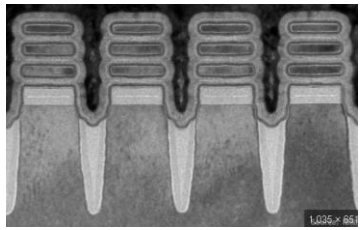
Source: imec@IEEE J. EDS-2020

Yield implications on GAA+Backside Metallization

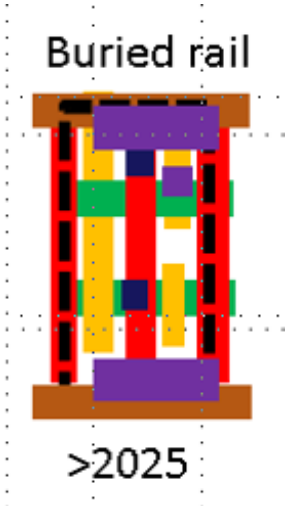


1. Local Interconnect
2. STI di-electric
3. Inner spacer
4. ILD
5. Source/drain EPI
6. Gate stack
7. Water thinning
8. BEOL
9. Bottom transistor isolation

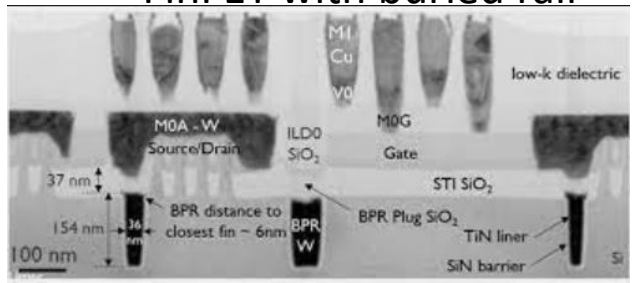
GAA with bottom device isolation



Source: IBM



FinFET with buried rail



Source: IMEC

Critical modules and steps in the GAA w/ BS metal

- MOL (middle-of-line) direct metal etch
- MOL ILD fill
- STI di-electric fill
- Inner spacer
- GAA bottom transistor isolation
- Source drain module – front and back side
- Gate stack
- Extension and junction engineer
- Backside surface control

Blue: Impacting device reliability as well

Defect mechanism analysis

- Critical module
- Critical process step
- Characterization of module: 1) Materials/physics, 2) Material property, 3) Integration in process/device, 4) Image reference
- Litho mask layer
- Failure mechanism definition
- Condition under which failure might occur: 1) Surface chemistry, 2) Environment, 3) Contaminant type
- Potential causes of failure
- Defect density
- Facility related (yes/no)

Yield defect definition and failure mode/mechanism

Process Defectivity Risk Analysis Steps:	(1) Critical Module, Unit Step with high chance of failure due to defectivity caused by contamination	(2) Critical Process Step in which defect may occur	(3) Characterization of Module					(4) Litho mask reference	(5) Failure Mechanism Definition (e.g. Electrical, reliability, material selectivity, obstruction)	(6) Conditions under which failure may occur			(7) Potential causes of failure under conditions of manufacturing process	(8) Defect Density	(9) Is it facility-related?		Defect Density as	Comments	AMC	Gas	Chemistry	UPW	Potential failure mechanism
			Material s/Physics	Dimensions	Material Property (if failure is material selectivity concerned)	Integration in process/device	Image Ref. #			Surface Chemistry	Environment	Contaminant Type										
Information Source:	MM	MM	MM	MM	MM	MM	MM	MM	MM	MM/Tool or Unit Step Experts	Unit Step Experts	MM	Process Experts	Process Experts	Process Experts							
	Local Interconnect (MOL), Subtractive Etch	Etch		3nm CD, 54nm tall		Ru/W patterning etch, RIE plasma etch, Cl2/O2	1	Metal mask (M0)	Creating opens, hardmask (SiN to O2 selectivity) oxidation	CVD/PVD, CMP	Wet+Dry	Metal particle or metal ions/Contaminant at bottom and top of the trench	short between two metal lines due to particle or dielectric impurity		Chemical purity		1e10 at/cm2	oxygen and moisture in the ambient air. Si-O-Si, Si-H and Si-OH species. very dilute solutions of HF, in de-ionized water, DI, or dilute					Creating opens, hardmask (SiN to O2 selectivity) oxidation, Systematic portion is only Cl2/O2 etchant
	STI di-electric fill	Flowable CVD		40nm gap, 90nm tall		STI Gap Fill in GAA	2	Active/OD mask (OD)	Reliability - Leakage, Creating leakage source, low-quality STI, height variation in di-electric		Wet+Dry	Halide anion, metallic ion										Creating leakage source, low-quality STI, height variation in di-electric
	GAA Inner Spacer	Flowable CVD		6nm tall, 5nm gap space		Inner spacer	3/3b	S/D mask (MetalC)	Reliability - TDDB Creating leakage source, low-quality STI, height variation in di-electric		Wet or Dry	Halide anion, metalic ion	Changing width of inner spacer (defect induced depth variation), Excessive Etch	Contamination affects process control (etch effectiveness)	Possibly, complex sources, difficult to control affecting material selectivity	This problem is likely going to be resolved via litho complex solutions						Creating leakage source, low-quality STI, height variation in di-electric
	GAA Inner Spacer	Flowable CVD		6nm tall, 5nm gap space		Inner spacer	3/3b	S/D mask (MetalC)	Electrical - Failed EPI to Si connection	EPI to Si interface	TBC	Carbon, oxygen (for Si)	Contaminant prevents EPI growth	challenges to remove contamination without affecting dielectric	No, lower risk for gas contamination than the process							
	GAA Bottom Isolation	pre-epi gate clean		10nm thick		selective SiGe removal followed by SiO2 deposition	3		HCl - hot carrier injection (failure mode), metal contamination or uncontrolled doppant	SiO2 or different	Wet and Dry	Any contamination will impact	Higher risk: mobile ions, (OH-) interface									
	ILD fill	Flowable CVD		3nm CD, 54nm tall		High-AR metal gap fill	4	Metal mask (M0)	Reliability - TDDB Creating leakage source, low-quality STI, height variation in di-electric		Wet	Halide anion, metallic ion										Creating leakage source, low-quality STI, height variation in di-electric
	Source Drain and Gate Stack	Dry Etch		6nm tall, 5nm gap space		Front and Back Side EPI	5	S/D mask (MetalC)	Positively ionized carbons at the interface acting as additional positive charges affecting the inversion to n-channel		Wet+Dry	Carbon, oxygen	residual from dry etch, leaving molecular contamination - needs to be removed pre epi	challenges to remove contamination with high efficiency without affecting dielectric	No, lower risk for gas contamination than the process		5e13 at/cm2	last step, air break after the cleaning				Deterioration of device performance is explained by means of which the positively ionized carbons at the interface acting as additional positive charges affecting the inversion to n-channel.
	Source Drain	Dry Etch		14nm wide, 30nm long		Front and Back Side EPI	5	S/D mask (MetalC)	Flouride detoriating the silicide quality		Wet+Dry	Ionic (fluoride)	residual from dry etch, leaving molecular contamination - needs to be removed pre epi	challenges to remove contamination without affecting dielectric	No, lower risk for gas contamination than the process		5e10 at/cm2					
	Gate stack	Std Clean		12nm long * 15nm wide * 6 nm thick		GAA RMG at narrower vertical space - **Dipole (La02) + HfO2**	6	Gate mask	Reliability - BTI Mobile ions in the gate di-electric causing Vt shift		Wet+Dry	Mobile metallic ions, organic contamination	Treshold voltage, Reliability + Yield risks; dilute HF pre-gate clean - high risk of contamination.	TBC based on the reliability model	UPW and DHF contamination risk		2e10 at/cm2	1) gate or contact metallization; 2) oxidation and annealing furnaces and gases; 3) diffusion furnaces and gases; 4) photoresist bake; 5) incomplete resist stripping; and 6) contaminated chemicals used in wafer cleaning.				The mobile ions often enter the gate oxide through the interface between the gate (usually metal or polysilicon) and the gate oxide (usually SiO2). Some of the ions then drift to the Si-SiO2 interface under the influence of electric fields created by voltages applied to the gate. Given the high mobility of these ions in SiO2, they can drift under field assistance even at room temperature. Na+ exhibits the greatest mobility due to its small atomic radius. K is
				12nm long * 15nm		GAA RMG at vertical space -			Reliability - BTI (TDDB also?) Changing the k-value of gate di-	TiN, Aluminum,	surface prep with HCl, clean Wet + Dry deposition		Air exposure in transition to ALD (humidity/moisture				2e10	Ca, Fe, Ni, Cu, Zn. One is direct binding to the silicon surface by charge exchange between a metal ion and a hydrogen atom attached to the surface of the Si substrate; this type of impurity is not easily removed during the wet cleaning process. The other mechanism is that the oxide and metallic impurities form simultaneously on the surface; such metallic impurities can be removed by etching the				

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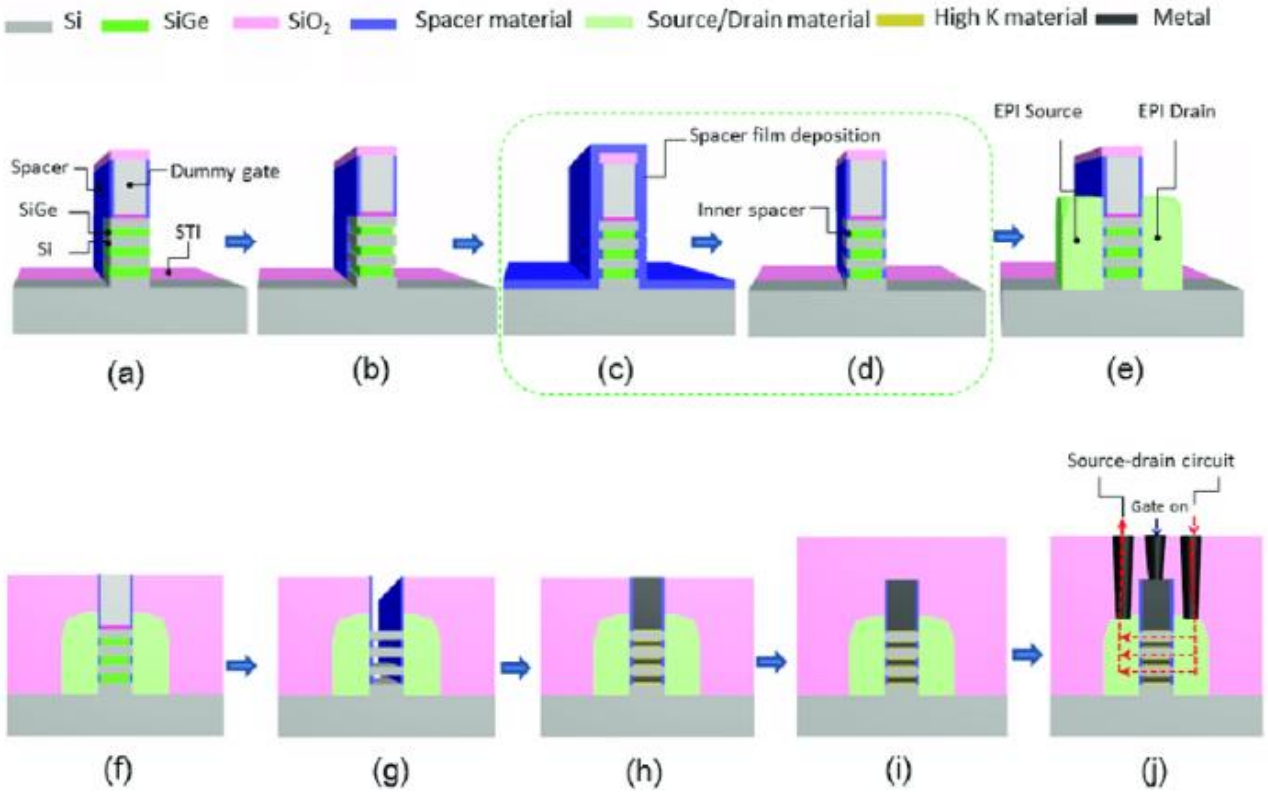
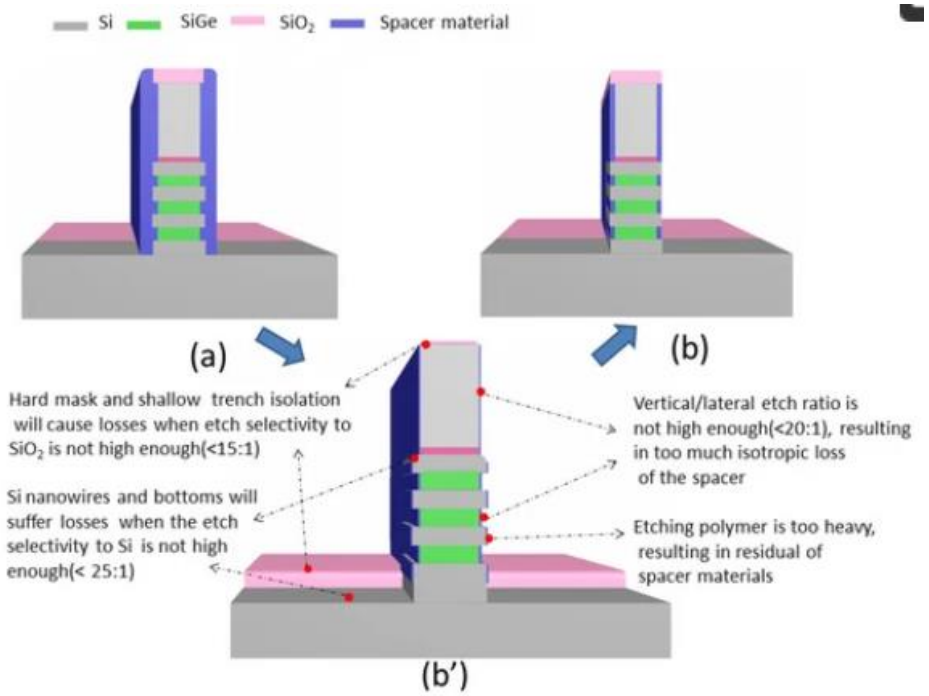
GAA integration flow with inner spacer integration



Source: Chinese Academy of Sciences@MDPI/Nanomaterials2020

SiGe side Etchback - CF4/O2/He gas ICP
Inner spacer fill – LPCVD Depi
Spacer etch back to reveal channel - CH2F2/O2/CH4/Ar gas ICP

Multiple depo/etchback steps
Inner spacer di-electric needs to withstand multiple down-stream process steps



Inner spacer defect definition

(1) Critical Module, Unit Step with high chance of failure due to defectivity caused by contamination	**(2) Critical Process Step** in which defect may occur	**(3) Characterization of Module**					**(4) Litho mask reference**	**(5) Failure Mechanism Definition** (e.g. Electrical, reliability, material selectivity, obstruction)
		Materials /Physics	Dimensions	Material Property (if failure is material selectivity concerned)	Integration in process/device	Image Ref. #		
GAA Inner Spacer	Flowable CVD		6nm tall, 5nm gap space		Inner spacer	3/3b	S/D mask (MetalC)	Reliability - TDDB Creating leakage source, low-quality STI, height variation in di-electric

(6) Conditions under which failure may occur			**(7) Potential causes of failure** under conditions of manufacturing process	**(8) Defect Density**	**(9) Is it facility-related?**
Surface Chemistry	Environment	Contaminant Type			
	Wet or Dry	Halide anion, metalic ion	Changing width of inner spacer (defect induced depth variation), Excessive Etch	Contamination affects process control (etch effectiveness)	Possibly, complex sources, difficult to control affecting material selectivity

Deep-dive to GAA gate stack – IBM@IEDM2020

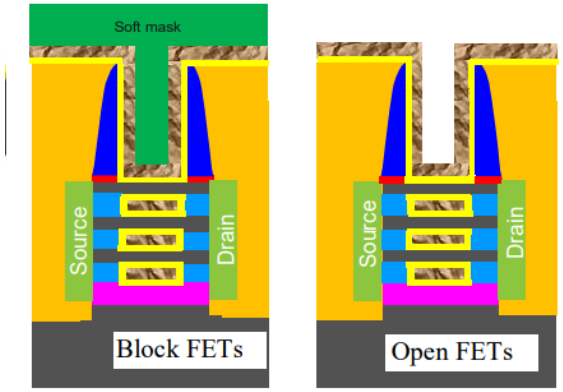
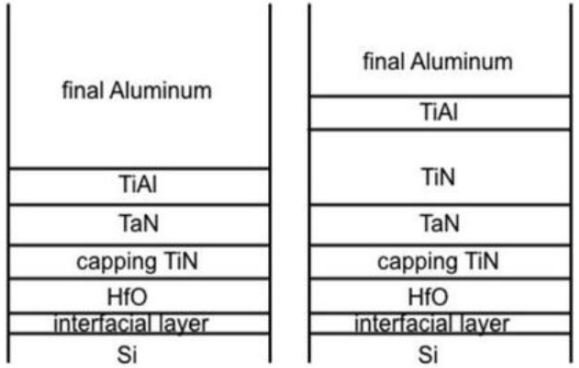


Fig. 2. Schematic for block FETs and open FETs in NS RMG patterning with soft mask (y-direction view).



Source: Erben@CMOS2018

Figure 7.
Gate stack of NMOS transistor (left) and a PMOS transistor (right).

Multi-Vt Schemes		ULVT	SLVT	LVT	RVT
A	nFET	nWFM+Dipole (t1+ t2+t3)	nWFM++Dipole (t2+t3)	nWFM+Dipole (t3)	nWFM
	pFET	pWFM	pWFM+Dipole (t3)	pWFM+Dipole (t2+t3)	pWFM+Dipole (t1+ t2+t3)
B	nFET	nWFM+Dipole (t1+t2)	nWFM+Dipole (t2)	nWFM	pWFM2+Dipole (t1+t2)
	pFET	pWFM1	pWFM1+Dipole (t2)	pWFM1+Dipole (t1+t2)	pWFM2
C	nFET	nWFM2+Dipole (t1)	nWFM2	nWFM1(t1)	nWFM1
	pFET	pWFM1	pWFM1+Dipole (t1)	pWFM2	pWFM2+Dipole (t1)

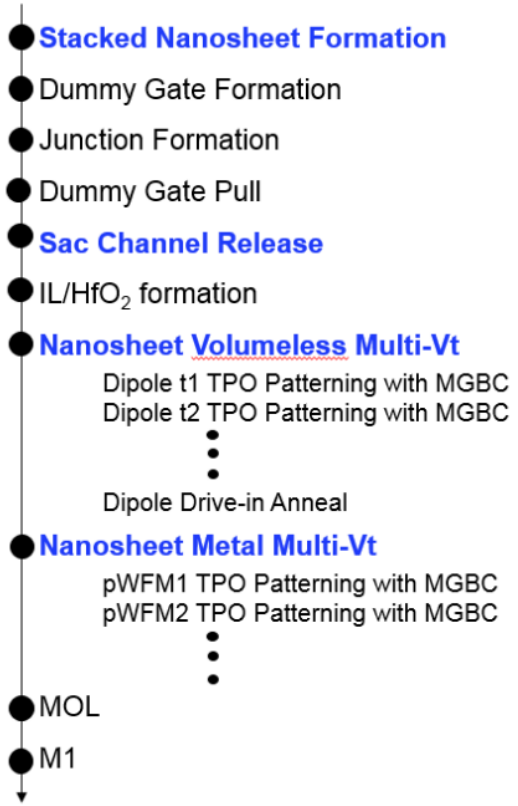


Fig. 17. Nanosheet multi-Vt process flow with volumeless multi-Vt module and metal multi-Vt module for NS technology multi-Vt offering.

GAA gate stack defect definition

(1) Critical Module, Unit Step with high chance of failure due to defectivity caused by contamination	(2) Critical Process Step in which defect may occur	(3) Characterization of Module					(4) Litho mask reference	(5) Failure Mechanism Definition (e.g. Electrical, reliability, material selectivity, obstruction)
		Materials/ Physics	Dimensions	Material Property (if failure is material selectivity concerned)	Integration in process/device	Image Ref. #		
Gate stack	Std Clean		12nm long * 15nm wide * 6 nm thick		GAA RMG at narrower vertical space - **Dipole (LaO2) + HfO2**	6	Gate mask	Reliability - BTI Mobile ions in the gate di-electric causing Vt shift

(6) Conditions under which failure may occur			(7) Potential causes of failure under conditions of manufacturing process	(8) Defect Density	(9) Is it facility-related?
Surface Chemistry	Environment	Contaminant Type			
	Wet+Dry	Mobile metallic ions, organic contamination	Treshold voltage, Reliability + Yield risks; dilute HF pre-gate clean - high risk of contamination.	TBC based on the reliability model	UPW and DHF contamination risk