CS 6210 Fall 2015 Midterm

Name:_____GT Number:

Note:

1. **Write your name and GT number AT LEAST on the first page.**
2. The test is **CLOSED BOOK** and **NOTES**.
3. Please provide the answers in the space provided. You can use scratch paper (provided by us) to figure things out (if needed) but you get credit **only** for what you put down in the space provided for each answer.
4. For conceptual questions, **concise bullets** (**not wordy sentences**) are preferred. **YOU DON'T HAVE TIME TO WRITE WORDY SENTENCES…**
5. While it is NOT REQUIRED, where appropriate use figures to convey your points (a figure is worth a thousand words!)
6. **Illegible answers are wrong answers.**
7. **DON'T GET STUCK ON ANY SINGLE QUESTION…FIRST PASS: ANSWER QUESTIONS YOU CAN WITHOUT MUCH THINK TIME; SECOND PASS: DO THE REST.**

Good luck!

Question number	Points earned	Running total
1 (0 min) (Max: 1 pts)		
2 (12 min) (Max: 24 pts)		
3 (12 min) (Max: 22 pts)		
4 (12 min) (Max: 28 pts)		
5 (7 min) (Max: 15 pts)		
6 (5 min) (Max: 10 pts)		
Total (48 min) (Max: 100 pts)		

1. (0 min, 1 point) (This is a freebie, you get 1 point regardless)
   The Pittsburgh Steelers quarterback for the next several weeks
   (a) Ben Roethlisberger
   (b) Mike Tomlin
   (c) Matt Ryan
   (d) Michael Vick
   (e) I have no idea what you are talking about
   (f) I will pretend I have no idea lest you think I am doing anything but prepping for this exam

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

OS Structures

2. (**12 min**, 24 points)

(a) (4 points) (General)

Enumerate the **four** different types of program discontinuities that can occur during the execution of a process with a **short** sentence explaining what each one of the discontinuities is.

(b) (4 points) (SPIN)

SPIN implements logical protection domains using Modula-3 objects. Name two key features of Modula-3 that help SPIN accomplish its extensibility goals without sacrificing memory protection. (Two concise bullets please)

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(c) (8 points) (Exokernel) (Concise bullets please)
(i) What is the role played by the “software TLB” data structure?

(ii) What is the role played by the “processor environment” data structure?

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(d) (8 points) (Liedtke's L3 Microkernel)
In a microkernel-based design of an OS, every service lives in its own address space and they may have to cross protection boundaries (border crossing) to complete a system call from an application. Name two tricks suggested by Liedtke to make border crossing cheap in a microkernel-based design of an OS. Identify the architectural assists that make such tricks possible. (Concise 4 bullets, 2 for tricks and 2 for architectural assists)

Virtualization
3. (**12 min**, 22 points)
(a) (2 points) (General)
Answer True/False with justification:
In a virtualized setting, the hypervisor knows at all times the specific process within a guest OS that is currently running on the processor.

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(b) (5 points) (para virtualization)
Using a specific example, show why mutual exclusion locks are not needed to access the I/O ring data structure that is shared between the guest OS and the hypervisor.

(c) (5 points) (Ballooning)
Ballooning is a mechanism employed by the hypervisor to reclaim memory from one VM and give it to another “needy” VM. What information does the hypervisor need to keep in order to make sane decisions about reclaiming memory from the VMs?

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(d) (5 points) (Full Virtualization)
In a non-virtualized environment on an Intel-like architecture, the page table (PT) is a data structure set up by the OS and used by the processor architecture upon a TLB miss, thus ensuring that address translation occurs at hardware speeds.

Recall that with full virtualization, the guest OS keeps a PT data structure for each process. However, this is an illusion since what the guest OS "thinks" as a physical page is in fact mapped to a machine page (which is the real page frame in the physical memory of the processor).

Conceptually on every memory access, the VPN has to be converted to PPN which in turn has to be converted to MPN to do the actual memory access. Clearly, this is untenable from a performance perspective. In the absence of page faults, how is the conversion of VPN to MPN accomplished in a fully virtualized setting so that the translation occurs at hardware speeds?

Name:_____GT Number:

(e) (5 points)(Page sharing across VMs)
To reduce the memory pressure of competing VMs in a virtualized setting, "VM oblivious page sharing" is often employed. Upon finding an exact match of the MPN contents belonging to two different VMs, the hypervisor "fixes up" the mappings for the two VMs to point to the same MPN. What data structures are modified (and how) by the hypervisor to accomplish this page sharing?

Synchronization, Communication, and Scheduling in Parallel Systems

4. (**12 mins**, 28 points)
(a) (2 points) (**Answer True/False with justification**)
Memory consistency model is irrelevant and inconsequential in an NCC NUMA shared memory multiprocessor.

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(b) (4 points)
Consider the following lock algorithm:

```
while ((L == locked) or (T&S(L) == locked))
{
      while (L == locked); /* spin */
      Delay (d[P_i]));
}
```

Why is this algorithm expected to perform better under high contention compared to a simple **spin-on-read** algorithm on cache coherent multiprocessor? (Concise bullets please)

(c) (4 points)
Recall that Anderson's array-based queuing lock algorithm expects an atomic operation **fetch-and-inc** for its implementation. If a cache-coherent multiprocessor architecture has only an atomic **test-and-set** instruction is it still worthwhile implementing Anderson's lock algorithm as opposed to a simple **spin-on-read** algorithm? Explain your answer. (Concise bullets please)

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(d) (4 points)
Recall that the centralized and tree-based counting barriers require an atomic read-modify-write (RMW) operation for their implementation on a shared memory multiprocessor. How is it that the MCS barrier implementation does not require an atomic RMW operation for its implementation?

(e) (4 points)
Recall that light-weight RPC (LRPC) is for cross-domain calls within a single host without going across the network. The kernel allocates A-stack in physical memory and maps this into the virtual address space of the client and the server.

A particular call implemented by the server has the following prototype:

```
int server_procedure (char *client_buffer);
```

The prototype expects a pointer to the client buffer. How is this client-server interaction accomplished in the LRPC paradigm while maintaining the address space protection guarantees for the client and the server processes? (Concise bullets please)

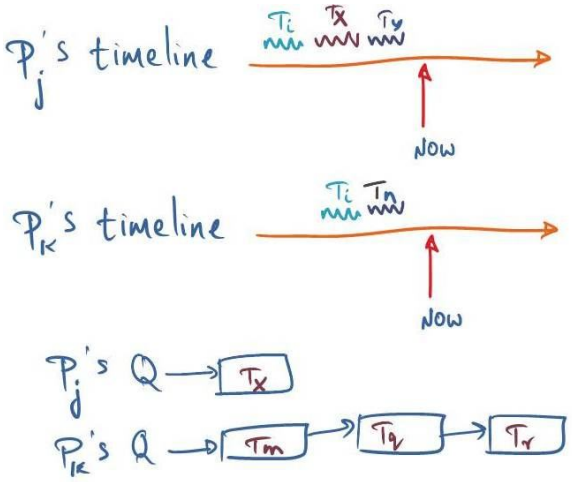
CS 6210 Fall 2015 Midterm

Name:_____GT Number:

(f) (5 points)
Consider a multiprocessor running data intensive workloads (i.e., all the processes have fairly large working sets and are compute intensive).

Answer True/False with justification:
For such an environment, a "fixed processor" scheduling algorithm will be the most effective one.

(g) (5 points)
In a multiprocessor, the following is the state of the processors (P_k and P_j) on which T_i ran previously. It is ready to run "Now".



Which processor would you schedule Ti on and why?

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

Parallel System Case Studies

5. (7 mins, 15 points)

(a) (5 points) (**Answer True/False with justification**)

Imagine a shared memory multiprocessor executing independent processes on the different processors. Simultaneously, all the processes experience page faults. Does servicing these simultaneous page faults lead to serialization? Explain your answer with concise bullets.

(b) (5 points)

You are implementing a subsystem using the Tornado clustered object paradigm on top of a cache coherent NUMA shared memory multiprocessor. You have decided to replicate a particular object on each node of the multiprocessor to increase the concurrency for that system service. During execution, one of the nodes makes a modification to its local replica.

Answer True/False with Justification:

The replicas on the other processors will automatically get updated since the multiprocessor is cache coherent.

(c) (5 points)

What is “page cache” in a traditional operating system?

CS 6210 Fall 2015 Midterm

Name:_____GT Number:

Communication in Distributed Systems

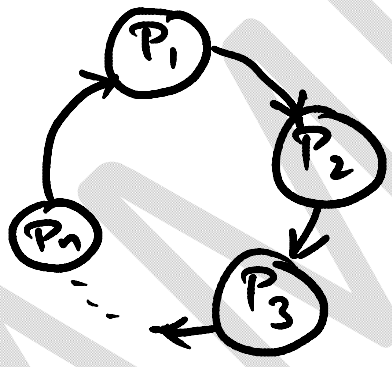
6. (**5 mins**, 10 points)

(a) (5 points)

Assume that messages arrive out-of-order in a distributed system. Does this violate the "happened before" relation? Justify your answer with an example.

(b) (5 points)

Imagine that the nodes of a distributed system are inter-connected by a one-directional ring topology as shown below.



Using Lamport's logical clock, sketch an efficient algorithm for implementing distributed mutual exclusion with fairness. Assume that there is no loss of messages in the network.