Temas:

- Osciladores
- Clock source selection
- PLL
- Divisores de Clock
- Divisores APB
- Power Control

Esquema general

Se desarrollará todo lo referido al siguiente esquema, explicando las fuentes de clock, y las manipulaciones que pueden hacerse con cada una de las fuentes de clock.

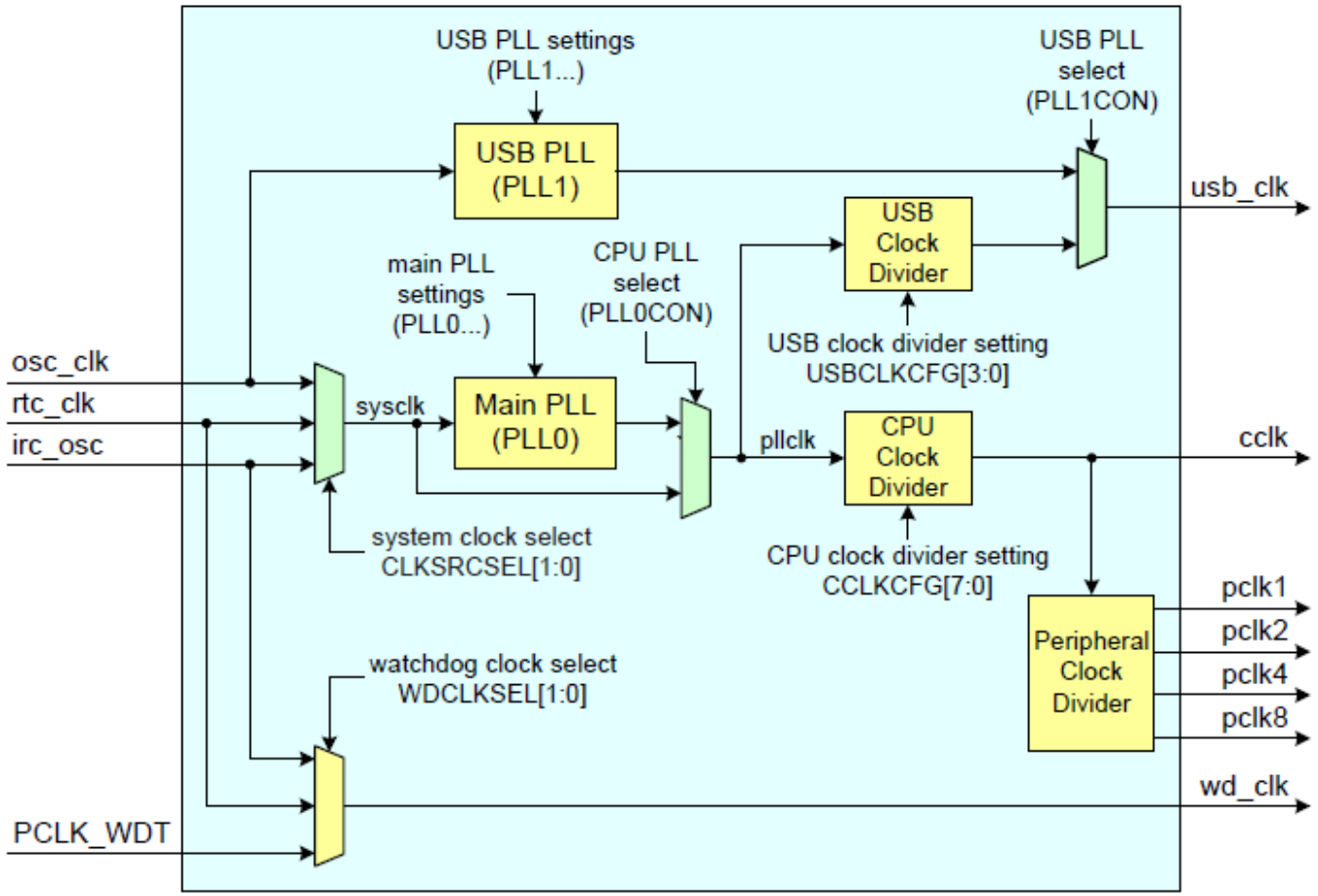


Fig 7. Clock generation for the LPC176x/5x

Registros asociados a este bloque

Table 14. Summary of system control registers

Name	Description	Access	Reset value	Address
Clock source selection				
CLKSRCSEL	Clock Source Select Register	R/W	0	0x400F C10C
Phase Locked Loop (PLL0, Main PLL)				
PLL0CON	PLL0 Control Register	R/W	0	0x400F C080
PLL0CFG	PLL0 Configuration Register	R/W	0	0x400F C084
PLL0STAT	PLL0 Status Register	RO	0	0x400F C088
PLL0FEED	PLL0 Feed Register	WO	NA	0x400F C08C
Phase Locked Loop (PLL1, USB PLL)				
PLL1CON	PLL1 Control Register	R/W	0	0x400F C0A0
PLL1CFG	PLL1 Configuration Register	R/W	0	0x400F C0A4
PLL1STAT	PLL1 Status Register	RO	0	0x400F C0A8
PLL1FEED	PLL1 Feed Register	WO	NA	0x400F C0AC
Clock dividers				
CCLKCFG	CPU Clock Configuration Register	R/W	0	0x400F C104
USBCLKCFG	USB Clock Configuration Register	R/W	0	0x400F C108
PCLKSEL0	Peripheral Clock Selection register 0.	R/W	0	0x400F C1A8
PCLKSEL1	Peripheral Clock Selection register 1.	R/W	0	0x400F C1AC
Power control				
PCON	Power Control Register	R/W	0	0x400F C0C0
PCONP	Power Control for Peripherals Register	R/W	0x03BE	0x400F C0C4
Utility				
CLKOUTCFG	Clock Output Configuration Register	R/W	0	0x400F C1C8

Osciladores

Los integrados LPC176x cuentan con 3 osciladores independientes, el oscilador principal, un oscilador RC y un RTC

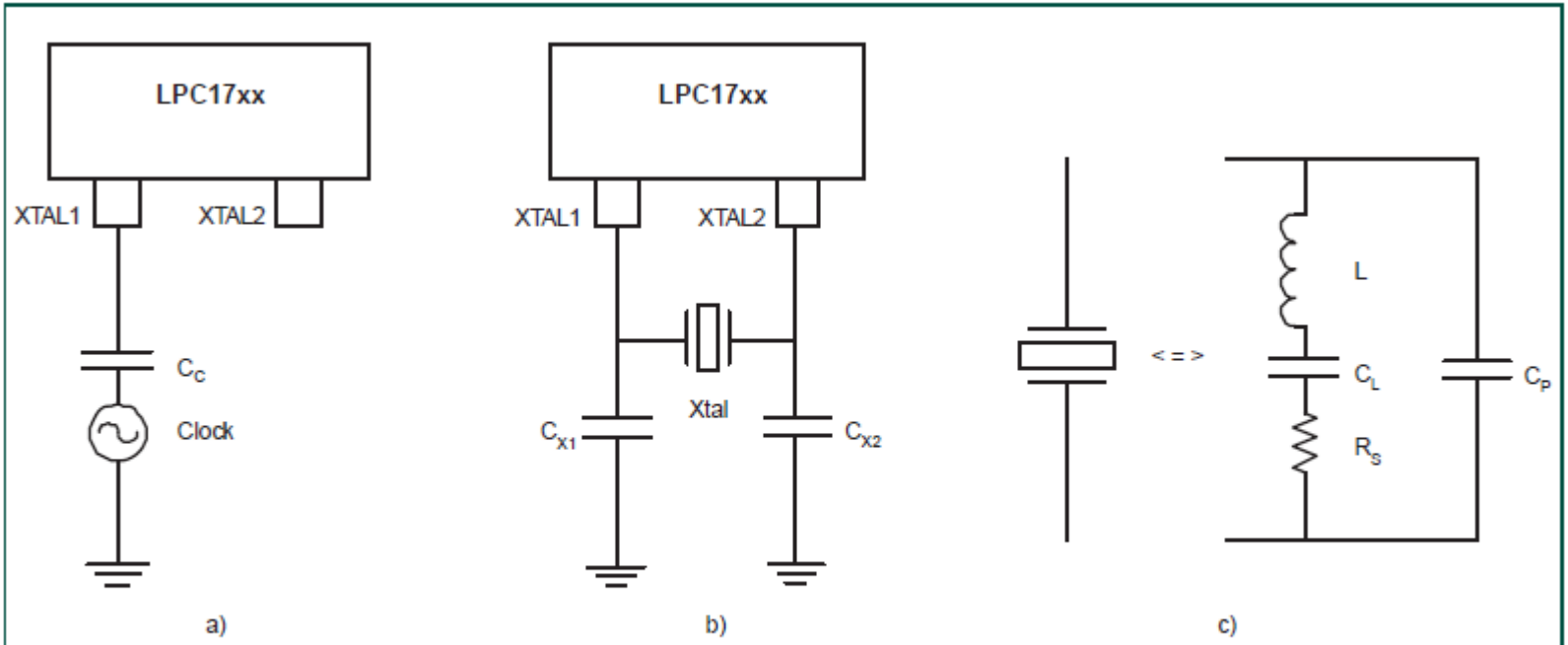


Fig 8. Oscillator modes and models: a) slave mode of operation, b) oscillation mode of operation, c) external crystal model used for $C_{X1}/_{X2}$ evaluation

Osciladores

Contamos con el registro CLKSRCSEL para seleccionar la fuente de clock

Table 17. Clock Source Select register (CLKSRCSEL - address 0x400F C10C) bit description

Bit	Symbol	Value	Description	Reset value
1:0	CLKSRC		Selects the clock source for PLL0 as follows:	0
		00	Selects the Internal RC oscillator as the PLL0 clock source (default).	
		01	Selects the main oscillator as the PLL0 clock source. **Remark:** Select the main oscillator as PLL0 clock source if the PLL0 clock output is used for USB or for CAN with baudrates > 100 kBit/s.	
		10	Selects the RTC oscillator as the PLL0 clock source.	
		11	Reserved, do not use this setting.	
		Warning: Improper setting of this value, or an incorrect sequence of changing this value may result in incorrect operation of the device.		
31:2	-	0	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

PLL (Bucle enganchado en fase)

PLL (Bucle enganchado en fase)

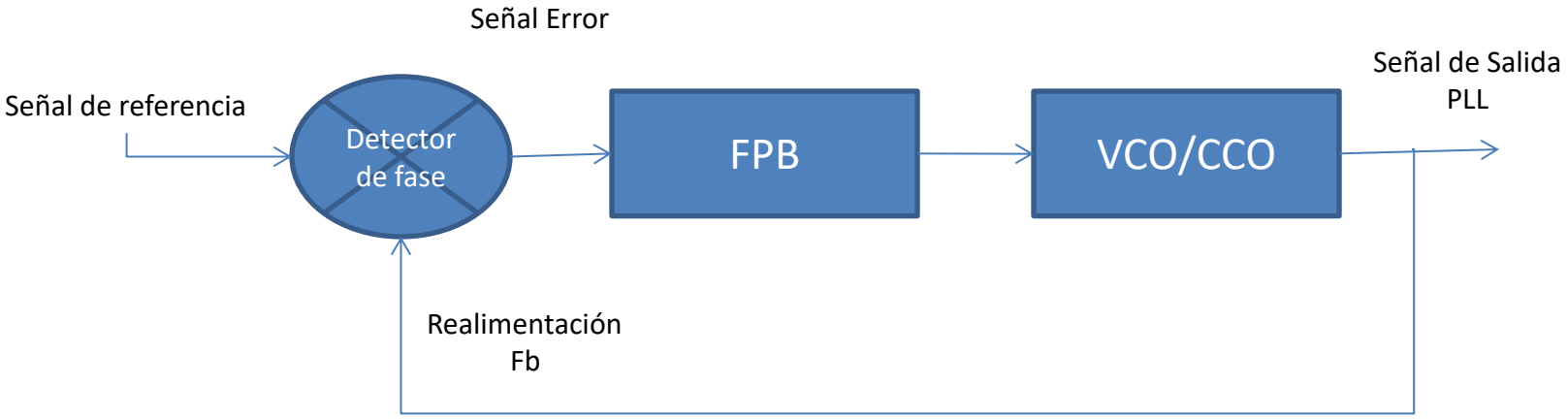
El objeto de un PLL es tomar una frecuencia proveniente de un cristal externo y mediante una realimentación (bucle) conseguir multiplicar la frecuencia del cristal hasta un valor deseado.

Los cristales son estables en el orden de los 10Mhz-20Mhz

El módulo PLL del LPC1769
Admite frecuencias de entrada desde 32khz hasta 25Mhz

Frecuencia máxima de trabajo del core 120Mhz

Diagrama de Bloques



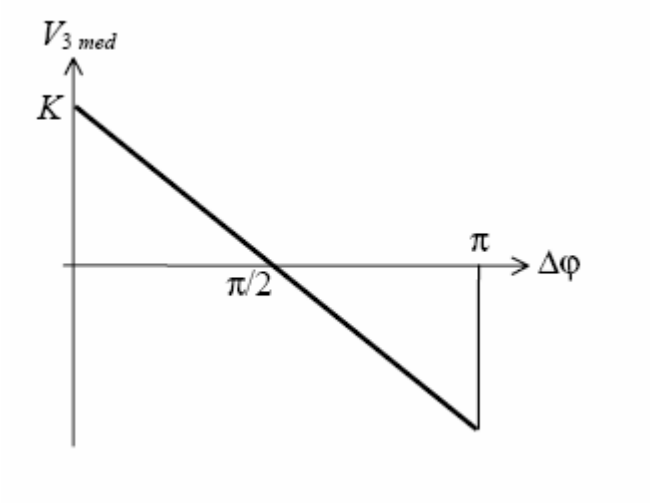
El detector de fase detecta las diferencias de fase entre la señal de referencia y la de realimentación (Fb) y da una tensión de salida (señal Error) Proporcional a esta diferencia. Verror=Kd (Φref- ΦFb)

El Bloque VCO/CCO es un Oscilador controlado por tensión /corriente que controlaremos con la señal error, Proveniente del Detector de fase.

El filtro pasa bajos cumple varias funciones. Una de ellas es la de filtrar ruido.

Detector de Fase

Como ya s mencionó, El detector de fase nos da como salida una tensión proporcional a la diferencia de fase entre la señal de referencia y la de realimentación



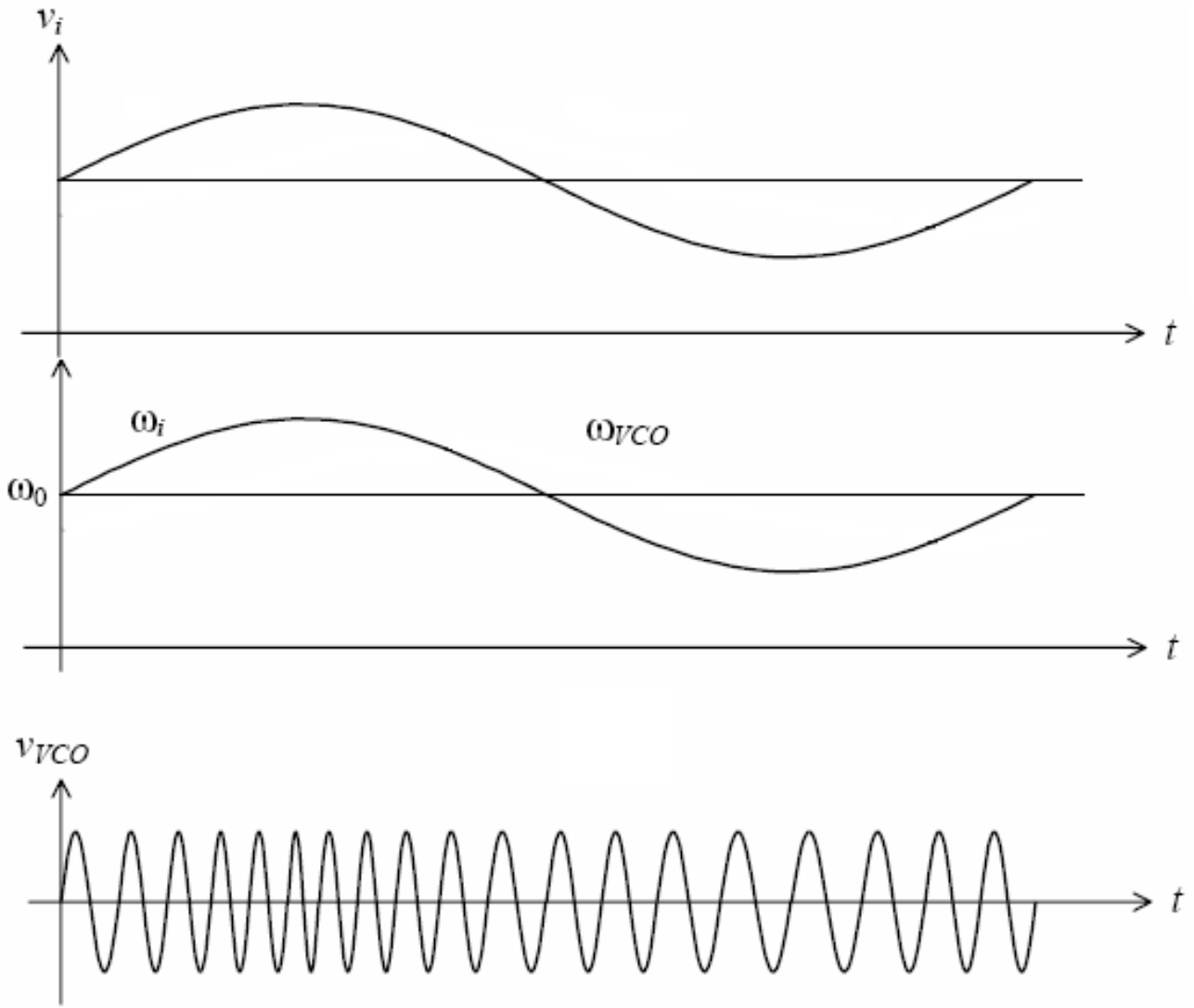
$$Verror = Kd\,(\Phi ref - \Phi Fb) = K * \Delta\Phi$$

VCO/CCO

Función de transferencia=Salida/Entrada
Frecuencia /tensión
Frecuencia/corriente

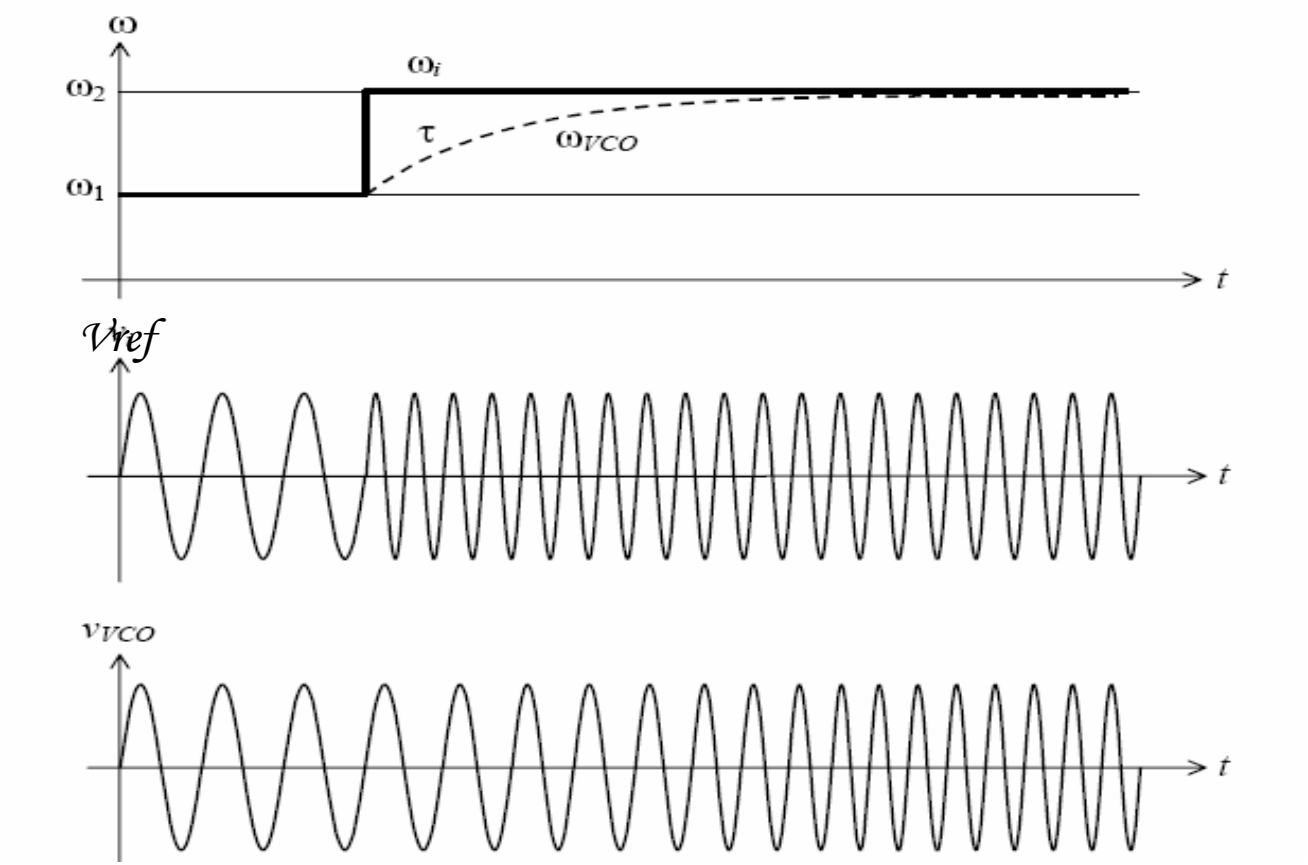
El VCO/CCO trabaja en una frecuencia central

VCO/CCO

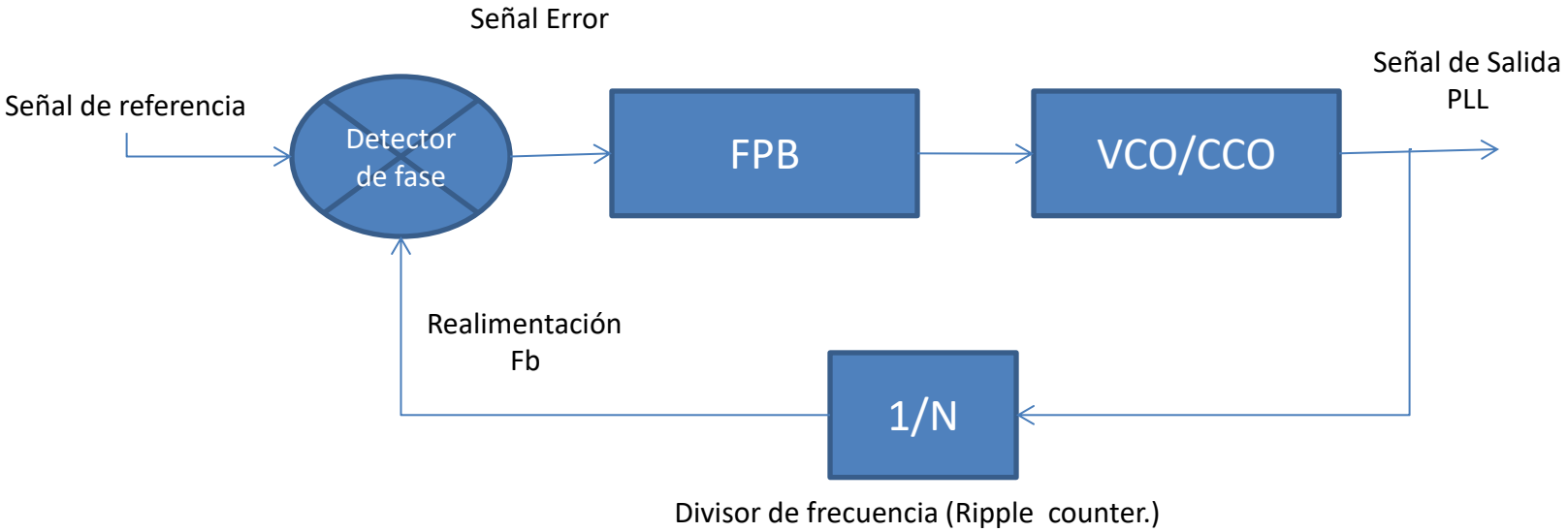


Tiempo de respuesta

El PLL tiene un tiempo de respuesta debido a los retardos propios de cada bloque individual y al filtro pasabajos.



Multiplicación de Frecuencias



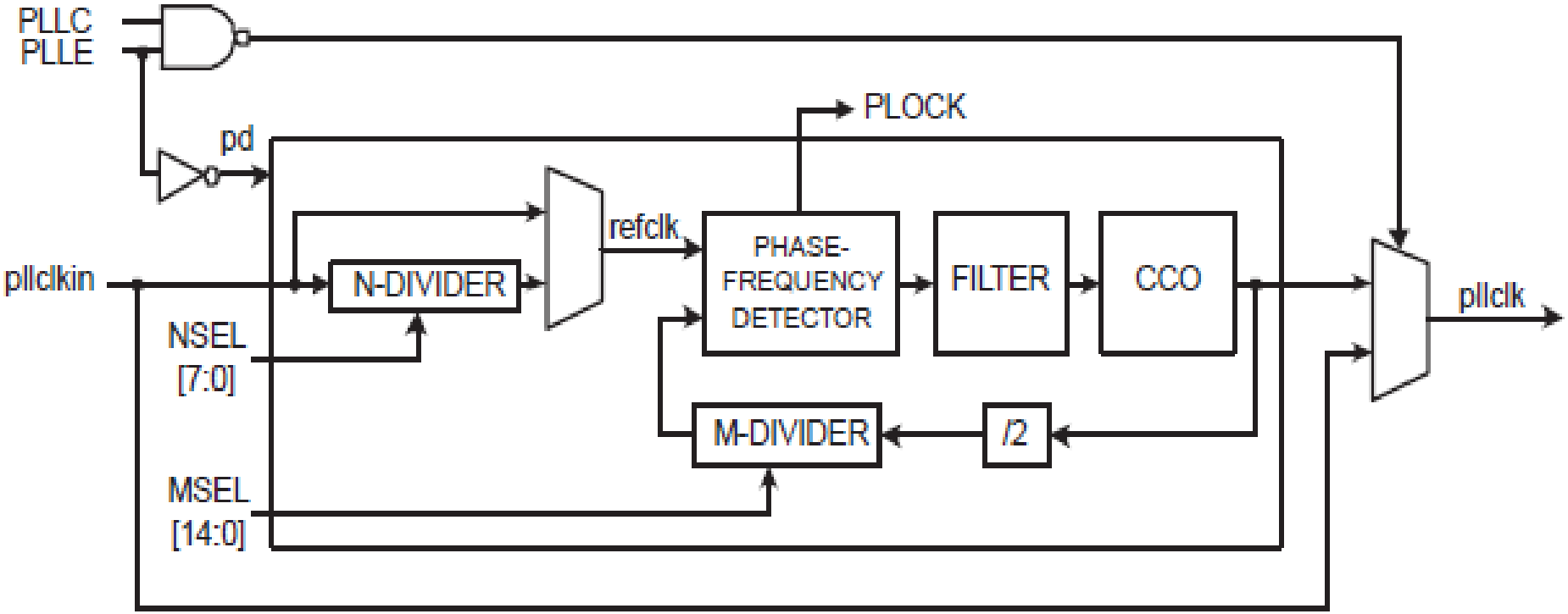
Sabemos dividir frecuencias:

- El PLL se encuentra originalmente enganchado en fase
- Dividimos la frecuencia de la señal de salida por N (Ripple counter.)
- El detector notará la diferencia de frecuencias.
- La señal error dejará de ser cero indicándole al VCO/CCO que aumente la frecuencia.
- La frecuencia del VCO/CCO incrementará N veces de modo que cuando esta sea dividida por N sea igual a la frecuencia de la señal de referencia.
- Luego del transitorio, el PLL está nuevamente enganchado en fase.

Ejemplo:
Fref=1Mhz
N=4
Ffb=Fvco/4
Si el PLL está enganchado en fase
Ffb=Fref y
ΦFb=Φref
Por lo tanto
Fvco=4*Fref

PLL LPC1769

Diagrama de bloques del PLL0



PLL0 must be set up, enabled, and Lock established before it may be used as a clock source. When switching from the oscillator clock to the PLL0 output or vice versa, interr

PLL LPC1769

PLL Control Register

Table 19. PLL Control register (PLL0CON - address 0x400F C080) bit description

Bit	Symbol	Description	Reset value
0	PLLE0	PLL0 Enable. When one, and after a valid PLL0 feed, this bit will activate PLL0 and allow it to lock to the requested frequency. See PLL0STAT register, Table 22.	0
1	PLLC0	PLL0 Connect. Setting PLLC0 to one after PLL0 has been enabled and locked, then followed by a valid PLL0 feed sequence causes PLL0 to become the clock source for the CPU, AHB peripherals, and used to derive the clocks for APB peripherals. The PLL0 output may potentially be used to clock the USB subsystem if the frequency is 48 MHz. See PLL0STAT register, Table 22.	0
31:2	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

PLL LPC1769

PLL0 Configuration Register

Table 20. PLL0 Configuration register (PLL0CFG - address 0x400F C084) bit description

Bit	Symbol	Description	Reset value
14:0	MSEL0	PLL0 Multiplier value. Supplies the value "M" in PLL0 frequency calculations. The value stored here is M - 1. Supported values for M are 6 through 512 and those listed in Table 21. **Note:** Not all values of M are needed, and therefore some are not supported by hardware. For details on selecting values for MSEL0 see Section 4.5.10 "PLL0 frequency calculation".	0
15	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
23:16	NSEL0	PLL0 Pre-Divider value. Supplies the value "N" in PLL0 frequency calculations. The value stored here is N - 1. Supported values for N are 1 through 32. **Note:** For details on selecting the right value for NSEL0 see Section 4.5.10 "PLL0 frequency calculation".	0
31:24	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

PLL LPC1769

PLL0 Configuration Register

El valor de M puede variar de 6 a 512 y los valores de la tabla 21

Table 21. Multiplier values for PLL0 with a 32 kHz input

Multiplier (M)	Pre-divide (N)	Fcco
4272	1	279.9698
4395	1	288.0307
4578	1	300.0238
4725	1	309.6576
4807	1	315.0316
5127	1	336.0031
5188	1	340.0008
5400	1	353.8944
5493	1	359.9892
5859	1	383.9754
6042	1	395.9685
6075	1	398.1312
6104	1	400.0317
6409	1	420.0202
6592	1	432.0133
6750	1	442.3680
6836	1	448.0041
6866	1	449.9702
6958	1	455.9995
7050	1	462.0288
7324	1	479.9857
7425	1	486.6048
7690	1	503.9718
7813	1	512.0328
7935	1	520.0282
8057	1	528.0236
8100	1	530.8416
8545	2	280.0026
8789	2	287.9980
9155	2	299.9910
9613	2	314.9988
10254	2	336.0031
10376	2	340.0008
10986	2	359.9892
11719	2	384.0082
12085	2	396.0013
12207	2	399.9990
12817	2	419.9875
12817	3	279.9916
13184	2	432.0133
13184	3	288.0089
13672	2	448.0041
13733	2	450.0029
13733	3	300.0020
13916	2	455.9995
14099	2	461.9960
14420	3	315.0097
14648	2	479.9857
15381	2	504.0046
15381	3	336.0031
15564	3	340.0008
15625	2	512.0000
15869	2	519.9954
16113	2	527.9908
16479	3	359.9892
17578	3	383.9973
18127	3	395.9904
18311	3	400.0099
19226	3	419.9984
19775	3	431.9915
20508	3	448.0041
20599	3	449.9920
20874	3	455.9995
21149	3	462.0070
21973	3	480.0075
23071	3	503.9937
23438	3	512.0109
23804	3	520.0063
24170	3	528.0017

PLL LPC1769

PLL0 Status Register

Table 22. PLL Status register (PLL0STAT - address 0x400F C088) bit description

Bit	Symbol	Description	Reset value
14:0	MSEL0	Read-back for the PLL0 Multiplier value. This is the value currently used by PLL0, and is one less than the actual multiplier.	0
15	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
23:16	NSEL0	Read-back for the PLL0 Pre-Divider value. This is the value currently used by PLL0, and is one less than the actual divider.	0
24	PLLE0_STAT	Read-back for the PLL0 Enable bit. This bit reflects the state of the PLEC0 bit in PLL0CON (see Table 19) after a valid PLL0 feed. When one, PLL0 is currently enabled. When zero, PLL0 is turned off. This bit is automatically cleared when Power-down mode is entered.	0
25	PLLC0_STAT	Read-back for the PLL0 Connect bit. This bit reflects the state of the PLLC0 bit in PLL0CON (see Table 19) after a valid PLL0 feed. When PLLC0 and PLLE0 are both one, PLL0 is connected as the clock source for the CPU. When either PLLC0 or PLLE0 is zero, PLL0 is bypassed. This bit is automatically cleared when Power-down mode is entered.	0
26	PLOCK0	Reflects the PLL0 Lock status. When zero, PLL0 is not locked. When one, PLL0 is locked onto the requested frequency. See text for details.	0
31:27	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

PLL LPC1769

PLL0 Status Register

Table 23. PLL control bit combinations

PLLC0	PLLE0	PLL Function
0	0	PLL0 is turned off and disconnected. PLL0 outputs the unmodified clock input.
0	1	PLL0 is active, but not yet connected. PLL0 can be connected after PLOCK0 is asserted.
1	0	Same as 00 combination. This prevents the possibility of PLL0 being connected without also being enabled.
1	1	PLL0 is active and has been connected as the system clock source.

PLL LPC1769

PLL0 Feed Register para que surtan los cambios en los registros mencionados previamente es necesario ingresar la secuencia 0xAA, 0x55 en el registro PLL0 Feed

Table 24. PLL Feed register (PLL0FEED - address 0x400F C08C) bit description

Bit	Symbol	Description	Reset value
7:0	PLL0FEED	The PLL0 feed sequence must be written to this register in order for PLL0 configuration and control register changes to take effect.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

1. Write the value 0xAA to PLL0FEED.
2. Write the value 0x55 to PLL0FEED.

PLL LPC1769

Secuencia para programar PLL página 47 User Manual

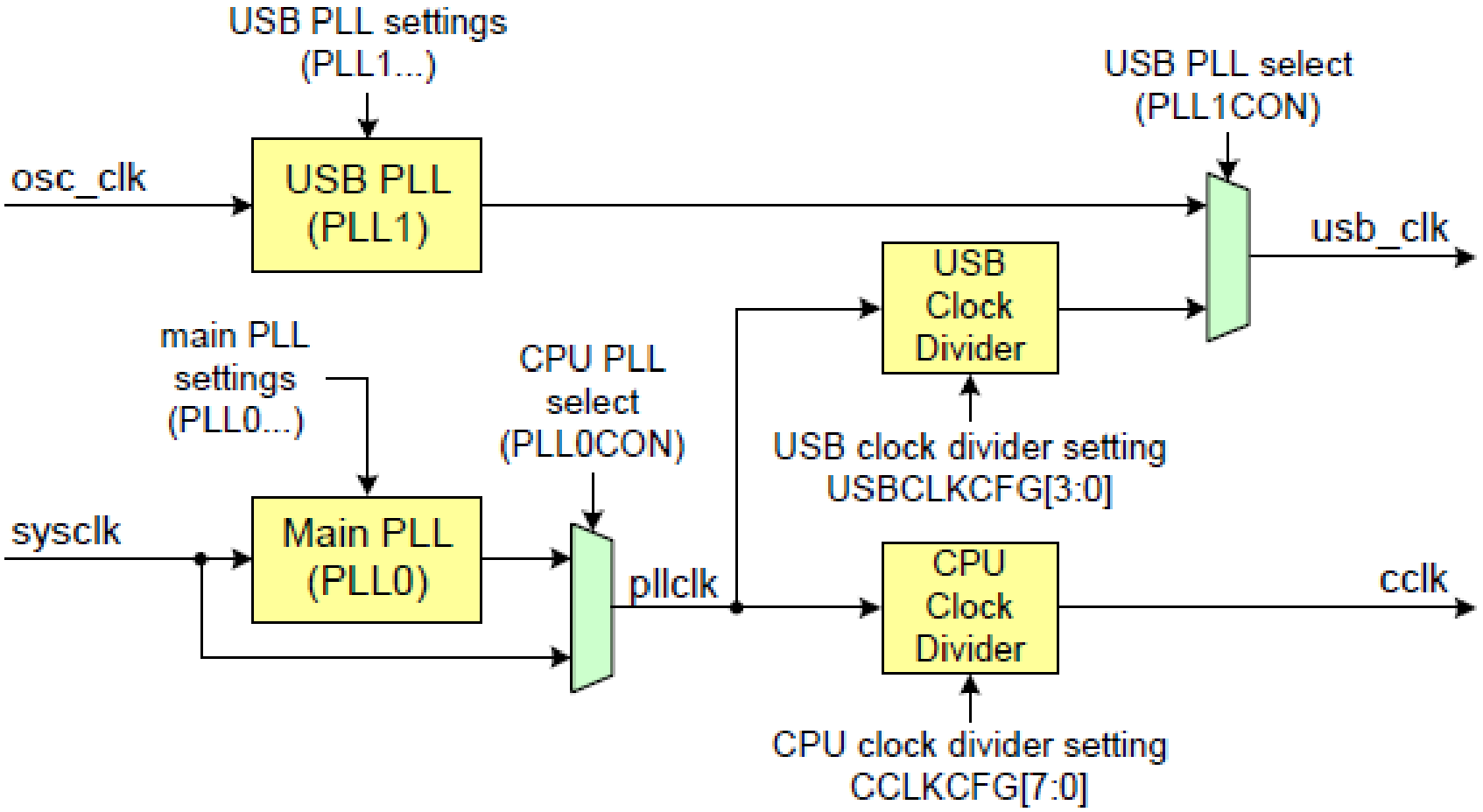
4.5.13 PLL0 setup sequence

The following sequence must be followed step by step in order to have PLL0 initialized and running:

It is very important not to merge any steps above. For example, do not update the PLL0CFG and enable PLL0 simultaneously with the same feed sequence.

Divisores de Clock

A los fines de obtener mayor flexibilidad contamos con un divisor de frecuencia, a la salida del PLL.



Divisores de Clock

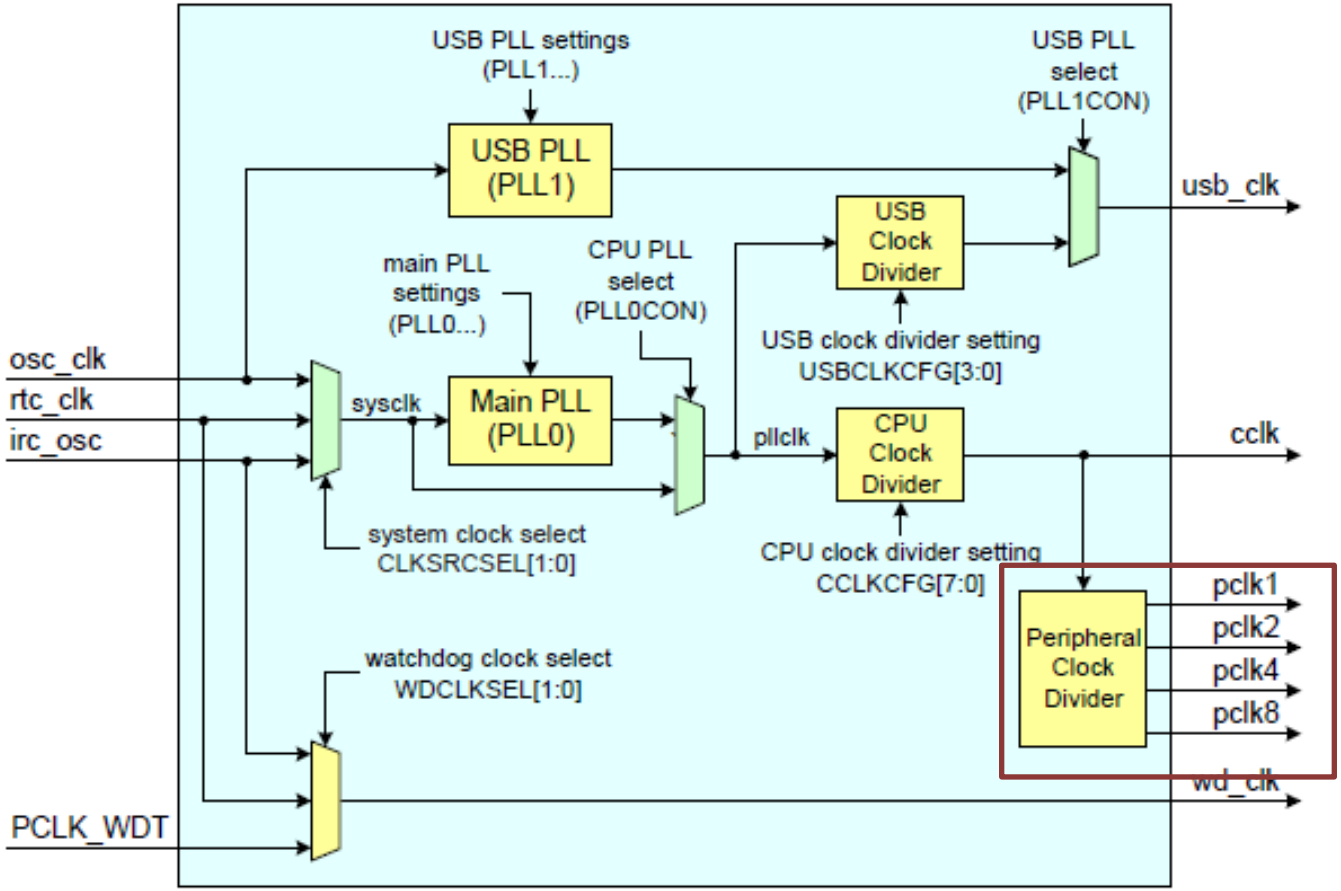
A los fines de obtener mayor flexibilidad contamos con un divisor de frecuencia, a la salida del PLL.

Table 38. CPU Clock Configuration register (CCLKCFG - address 0x400F C104) bit description

Bit	Symbol	Value	Description	Reset value
7:0	CCLKSEL		Selects the divide value for creating the CPU clock (CCLK) from the PLL0 output.	0x00
		0	pllclk is divided by 1 to produce the CPU clock. This setting is not allowed when the PLL0 is connected, because the rate would always be greater than the maximum allowed CPU clock.	
		1	pllclk is divided by 2 to produce the CPU clock. This setting is not allowed when the PLL0 is connected, because the rate would always be greater than the maximum allowed CPU clock.	
		2	pllclk is divided by 3 to produce the CPU clock.	
		3	pllclk is divided by 4 to produce the CPU clock.	
		4	pllclk is divided by 5 to produce the CPU clock.	
		:	:	
		255	pllclk is divided by 256 to produce the CPU clock.	
31:8	-		Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Divisores APB

Contamos también con divisores del bus APB



Divisores APB

Contamos también con divisores del bus APB

Table 40. Peripheral Clock Selection register 0 (PCLKSEL0 - address 0x400F C1A8) bit description

Bit	Symbol	Description	Reset value
1:0	PCLK_WDT	Peripheral clock selection for WDT.	00
3:2	PCLK_TIMER0	Peripheral clock selection for TIMER0.	
5:4	PCLK_TIMER1	Peripheral clock selection for TIMER1.	
7:6	PCLK_UART0	Peripheral clock selection for UART0.	
9:8	PCLK_UART1	Peripheral clock selection for UART1.	
11:10	-	Reserved.	
13:12	PCLK_PWM1	Peripheral clock selection for PWM1.	
15:14	PCLK_I2C0	Peripheral clock selection for I2C0.	
17:16	PCLK_SPI	Peripheral clock selection for SPI.	
19:18	-	Reserved.	
21:20	PCLK_SSP1	Peripheral clock selection for SSP1.	
23:22	PCLK_DAC	Peripheral clock selection for DAC.	
25:24	PCLK_ADC	Peripheral clock selection for ADC.	
27:26	PCLK_CAN1	Peripheral clock selection for CAN1.[1]	
29:28	PCLK_CAN2	Peripheral clock selection for CAN2.[1]	
31:30	PCLK_ACF	Peripheral clock selection for CAN acceptance filte	

Table 41. Peripheral Clock Selection register 1 (PCLKSEL1 - address 0x400F C1AC) bit description

Bit	Symbol	Description	Reset value
1:0	PCLK_QEI	Peripheral clock selection for the Quadrature Encoder Interface.	00
3:2	PCLK_GPIOINT	Peripheral clock selection for GPIO interrupts.	00
5:4	PCLK_PCB	Peripheral clock selection for the Pin Connect block.	00
7:6	PCLK_I2C1	Peripheral clock selection for I2C1.	00
9:8	-	Reserved.	NA
11:10	PCLK_SSP0	Peripheral clock selection for SSP0.	00
13:12	PCLK_TIMER2	Peripheral clock selection for TIMER2.	00
15:14	PCLK_TIMER3	Peripheral clock selection for TIMER3.	00
17:16	PCLK_UART2	Peripheral clock selection for UART2.	00
19:18	PCLK_UART3	Peripheral clock selection for UART3.	00
21:20	PCLK_I2C2	Peripheral clock selection for I2C2.	00
23:22	PCLK_I2S	Peripheral clock selection for I2S.	00
25:24	-	Reserved.	NA
27:26	PCLK_RIT	Peripheral clock selection for Repetitive Interrupt Timer.	00
29:28	PCLK_SYSCON	Peripheral clock selection for the System Control block.	00
31:30	PCLK_MC	Peripheral clock selection for the Motor Control PWM.	00

Divisores APB

Contamos también con divisores del bus APB

Table 40. Peripheral Clock Selection register 0 (PCLKSEL0 - address 0x400F C1A8) bit description

Bit	Symbol	Description	Reset value
1:0	PCLK_WDT	Peripheral clock selection for WDT.	00
3:2	PCLK_TIMER0	Peripheral clock selection for TIMER0.	
5:4	PCLK_TIMER1	Peripheral clock selection for TIMER1.	
7:6	PCLK_UART0	Peripheral clock selection for UART0.	
9:8	PCLK_UART1	Peripheral clock selection for UART1.	
11:10	-	Reserved.	
13:12	PCLK_PWM1	Peripheral clock selection for PWM1.	
15:14	PCLK_I2C0	Peripheral clock selection for I2C0.	
17:16	PCLK_SPI	Peripheral clock selection for SPI.	
19:18	-	Reserved.	
21:20	PCLK_SSP1	Peripheral clock selection for SSP1.	
23:22	PCLK_DAC	Peripheral clock selection for DAC.	
25:24	PCLK_ADC	Peripheral clock selection for ADC.	
27:26	PCLK_CAN1	Peripheral clock selection for CAN1.[1]	

Table 41. Peripheral Clock Selection register 1 (PCLKSEL1 - address 0x400F C1AC) bit description

Bit	Symbol	Description	Reset value
1:0	PCLK_QEI	Peripheral clock selection for the Quadrature Encoder Interface.	00
3:2	PCLK_GPIOINT	Peripheral clock selection for GPIO interrupts.	00
5:4	PCLK_PCB	Peripheral clock selection for the Pin Connect block.	00
7:6	PCLK_I2C1	Peripheral clock selection for I2C1.	00
9:8	-	Reserved.	NA
11:10	PCLK_SSP0	Peripheral clock selection for SSP0.	00
13:12	PCLK_TIMER2	Peripheral clock selection for TIMER2.	00
15:14	PCLK_TIMER3	Peripheral clock selection for TIMER3.	00
		r UART2.	00
		r UART3.	00
		r I2C2.	00
		r I2S.	00
			NA
		r Repetitive Interrupt Timer.	00
		r the System Control block.	00
		r the Motor Control PWM.	00

Table 42. Peripheral Clock Selection register bit values

PCLKSEL0 and PCLKSEL1 individual peripheral's clock select options	Function	Reset value
00	PCLK_peripheral = CCLK/4	00
01	PCLK_peripheral = CCLK	
10	PCLK_peripheral = CCLK/2	
11	PCLK_peripheral = CCLK/8, except for CAN1, CAN2, and CAN filtering when "11" selects = CCLK/6.	

Power Control

Registros asociados al Power Control Block

Table 43. Power Control registers

Name	Description	Access	Reset value[1]	Address
PCON	Power Control Register. This register contains control bits that enable some reduced power operating modes of the LPC176x/5x. See Table 44.	R/W	0x00	0x400F C0C0
PCONP	Power Control for Peripherals Register. This register contains control bits that enable and disable individual peripheral functions, allowing elimination of power consumption by peripherals that are not needed.	R/W		0x400F C0C4

Power Control

Registros asociados al Power Control Block

Table 46. Power Control for Peripherals register (PCONP - address 0x400F C0C4) bit description

Bit	Symbol	Description	Reset value
0	-	Reserved.	NA
1	PCTIM0	Timer/Counter 0 power/clock control bit.	1
2	PCTIM1	Timer/Counter 1 power/clock control bit.	1
3	PCUART0	UART0 power/clock control bit.	1
4	PCUART1	UART1 power/clock control bit.	1
5	-	Reserved.	NA
6	PCPWM1	PWM1 power/clock control bit.	1
7	PCI2C0	The I^2C0 interface power/clock control bit.	1
8	PCSPI	The SPI interface power/clock control bit.	1
9	PCRTC	The RTC power/clock control bit.	1
10	PCSSP1	The SSP 1 interface power/clock control bit.	1
11	-	Reserved.	NA
12	PCADC	A/D converter (ADC) power/clock control bit. **Note:** Clear the PDN bit in the AD0CR before clearing this bit, and set this bit before setting PDN.	0
13	PCCAN1	CAN Controller 1 power/clock control bit.	0
14	PCCAN2	CAN Controller 2 power/clock control bit.	0