Emilio A. Magaña

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EDUCATION

Bachelor of Science in Electrical and Computer Engineering Graduated June 2021

Oregon State University (OSU)

- USA-GPA: 3.52/4.0, **DE-GPA: 1.63 (Gut)**
- **Computer Science Minor**
- *Related Coursework:* Digital Logic Design, VLSI, CMOS, Computer Architecture, Data Structures.

EXPERIENCE

Product Engineer Oct. 2021 - Jan. 2024

Lattice Semiconductor | Hillsboro, OR | Python, SystemVerilog, R, Electrical Lab Equipment

- Main role consisted of validating and characterizing IP.
  - Wrote documentation of methodology for both validation and characterization.
  - Worked closely with all aspects of FPGA IP's, mainly on: I/O, PLL, OSC.
  - **Developed behavioral patterns** through our in-house design software.
  - **In charge of** bring-up, maintenance, and **automatization of benches**.
  - Created statistical visuals between specification and performance of IP.
- Worked with customer issues/JIRA (internal and external) in providing solutions and data.
- Small Projects involving: BSCAN/JTAG, Thermal Studies.

Teacher's Assistant/Head TA Jan. 2019 - Mar. 2019

OSU, Electrical and Computer Engineering Department | Corvallis, OR

- Coordinated lab sessions for ECE 112: Introduction to Electrical and Computer Engineering.

PROJECTS

Portfolio Website

Personal | TypeScript, React.js, Next.js, TailwindCSS, Git

- **Designed** a personal website **using Next.js** to self-introduce and be a root to all socials and future projects.
- Deployed using Vercel for developing serverless functionality, when handling api calls.

Wild Oasis

Personal | TypeScript, React.js, Supabase, TanStack, React Router, styled-components

- Designed a property booking website to act as an AirBnb clone, for authenticated users managing lodgings, guests, and bookings of property.
- Supabase is used for managing all information.
- Deployed using Netlify.

High Voltage Peripherals

Capstone | Eagle CAD, LTspice

- Capstone Project was done with the Global Formula Racing (GFR) Team at OSU, a International Formula Student team in conjunction with DHBW Ravensburg, as part of the ePowertrain sub-team.
- **Designed and Functionally tested** the Direct Current Link (DCL) and Brake System Plausibility Device (BSPD) for both Formula Student (FS) and Formula Society of Automotive Engineers (FSAE) 2021 Competitions.
  - Under FS rules:
    - The DCL discharged the vehicle's current **2627% faster** than the allotted maximum given time.
    - The BSPD **rebooted the car 11.6s** after no implausibility being present (reboot must be > 10s).
  - Under FSAE rules:
    - The DCL discharged the vehicle's current **50% faster** than the allotted maximum given time.
    - The BSPD was not to be used.

TECHNICAL SKILLS

Languages: TypeScript, Python, CSS, SystemVerilog, R, Go
Frameworks/Libraries: React.js, Next.js, Node.js, TailwindCSS, TanStack, React Router, styled-components
Tools: Vite, Git, Supabase, Electrical Lab Equipment, Eagle CAD, LTspice, Cadence
Conversational Languages: Spanish (Fluent, Oregon Seal Of Biliteracy, C1), German (Conversational)