Emilio A. Magaña

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EDUCATION

Bachelor of Science in Electrical and Computer Engineering Graduated June 2021

Oregon State University

- GPA: 3.52/4.0
- Computer Science Minor
- *Related Coursework:* Digital Logic Design, VLSI, CMOS, Computer Architecture, Signal and Systems.

EXPERIENCE

Product Engineer Oct. 2021 - Jan. 2024

Lattice Semiconductor | Hillsboro, OR | Python, SystemVerilog, R

- Main role consisted of validating and characterizing IP.
  - Wrote documentation of methodology for both validation and characterization.
  - Worked closely with all aspects of FPGA IP's, mainly on: I/O, PLL, OSC.
  - Developed behavioral patterns through our in-house design software.
  - In charge of bring-up, maintenance, and automatization of benches.
  - Created statistical visuals between specification and performance of IP.
- Worked with customer issues/JIRA (internal and external) in providing solutions and data.
- Small Projects involving: BSCAN/JTAG, Thermal Studies.

Teacher's Assistant/Head TA Jan. 2019 - Mar. 2019

OSU, ECE Department | Corvallis, OR

- Coordinated lab sessions for ECE 112: Introduction to Electrical and Computer Engineering.

PROJECTS

Portfolio Website

Personal Project | TypeScript, React.js, TailwindCSS, Next.js

- Designed a personal website to act as a root to all socials and future projects and give a self-introduction.
- Used Next.js for developing serverless functionality, when handling api calls.

High Voltage Peripherals

Global Formula Racing | Eagle CAD, LTspice

- Capstone Project was done with the Global Formula Racing (GFR) Team at Oregon State, a International Formula Student team in conjunction with DHBW Ravensburg, as part of the ePowertrain sub-team.
- Designed and Functionally tested the DC-Link (DCL) and Brake System Plausibility Device (BSPD) for both FS and FSAE 2021 Competitions.
  - Under FS rules:
    - The DCL discharged the vehicle's current **2627% faster** than the allotted maximum given time.
    - The BSPD **rebooted the car 11.6s** after no implausibility being present (reboot must be > 10s).
  - Under FSAE rules:
    - The DCL discharged the vehicle's current **50% faster** than the allotted maximum given time.
    - The BSPD was not to be used.

SCARA Robot Arm

Junior Design Project | Python, Eagle CAD

- Programmed a SCARA Robot Arm, with three other classmates, capable of drawing a 10-inch straight line within 2.5 seconds and being able to sort a single layer of coins using an Arduino, a Jetson Nano, and a custom made PCB.
- Contributed in the coding of the SCARA's motion, using Python and Arduino Ide.

TECHNICAL SKILLS

Languages: TypeScript, Python, CSS, Go, SystemVerilog, R
Frameworks/Libraries: React.js, Next.js, TailwindCSS, Node.js
Tools: Vite, Git, Supabase, Eagle CAD, Cadence, LTspice, Electrical Lab Equipment
Conversational Languages: Spanish (Fluent, Oregon Seal Of Biliteracy), German (Conversational)