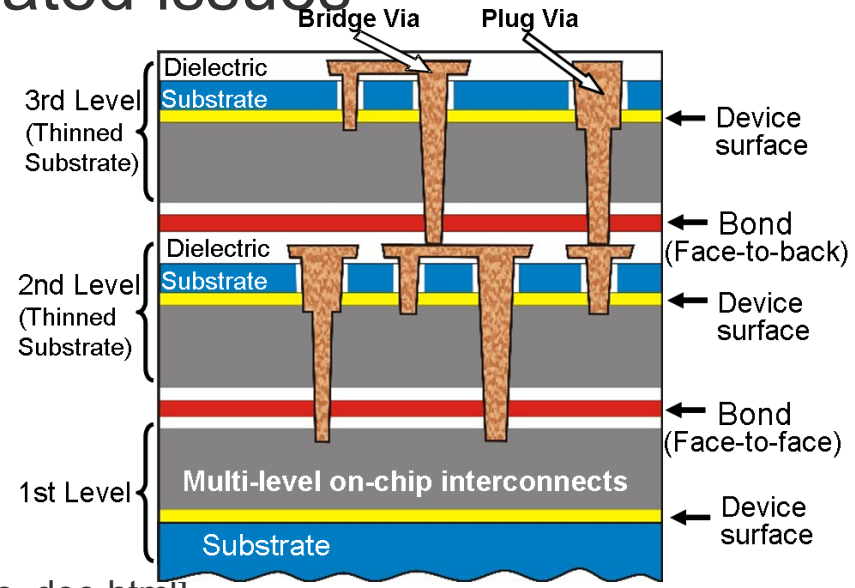
EE 382M Final Project: Monolithic 3D IC Standard Cell Library

Emily Bragg, Tengchieh Huang
2014-12-08

Technology Intro: 3D ICs

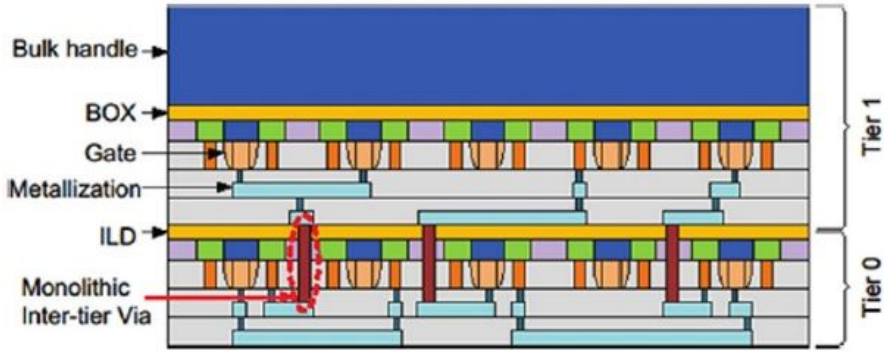
- Stacking silicon layers
- Introduces many complicated issues
- Need connections between layers
- Difficult to design
  - TSVs



[image from http://www.process-evolution.com/3d-ics_doe.html]

+ Monolithic?

- No large TSVs
- Monolithic Inter-tier Via -> 1% of TSV size (~70nm)
- Builds layers up sequentially



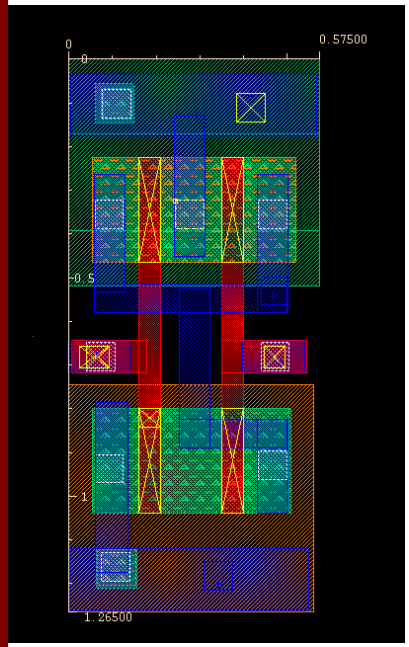
[image from Qualcomm presentation, June 2014]

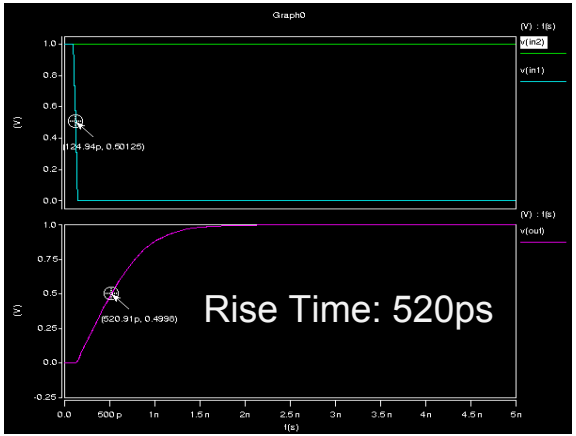
Motivations

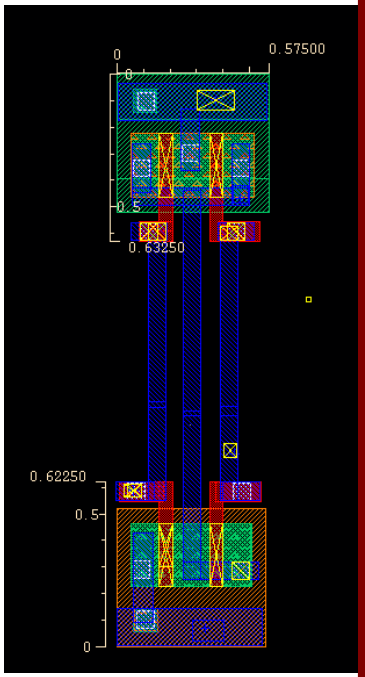
- Area
  - Potential gains of ~40%
- Ease of Design
  - Doesn’t require awareness of TSVs to combine these cells

Design Process

- Designed 2D and 3D versions of each cell
- Used long wires to simulate the additional resistance of a MIV
- Simulated and compared the two designs







NAND2 Design Process

Timing Results

cell names	rising time(ps)	falling time (ps)
INV	383.5	249.72
BUF	394.09	270.84
NAND2	396	219
NAND3	413	213
NAND4	435.65	212
NOR2	419.79	262.17
NOR3	454.44	279.22
NOR4	488.38	301.18
AND2	404.23	168.23
AND3	414.82	163.74
AND4	427.33	158.24
AOI21	432.26	228.9
AOI22	362.22	238.24
OAI21	469.83	229.28
OAI22	446.02	184.48

Table 7: Post-layout Simulation for 2D cells

cell names	rising time(ps)	falling time(ps)
INV	400.1	263.35
BUF	410.3	283.51
NAND2	409.25	227.25
NAND3	428.65	221.3
NAND4	451.14	223.65
NOR2	436.55	273.12
NOR3	471.58	290.01
NOR4	506.42	312.27
AND2	418.83	187.3
AND3	429.62	180.12
AND4	441.7	172.4
AOI21	438.23	232
AOI22	357.76	240.43
OAI21	471.77	232.6
OAI22	450.39	186.41

Table 8: Post-layout Simulation for 3D cells

Area Results

cell names	area in 2D(um$\hat{2}$)	area in 3DMI(um$\hat{2}$)	difference percentage
INV	0.4151	0.2352	42.6
BUF	0.8483	0.4828	43.5
INV_CHAIN			
NAND2	0.7242	0.4531	37.5
NAND3	1.0356	0.5946	43.5
NAND4	1.3523	0.7229	46.5
NOR2	0.7943	0.5304	29.4
NOR3	1.2288	0.8661	29.5
NOR4	1.7825	1.3195	26
AND2	1.1866	0.7102	41
AND3	1.5595	0.88	43.6
AND4	1.9815	1.179	40.5
OR2	1.3298	0.844	36.5
OR3	1.4506	1.2953	10.7
OR4	2.1974	1.792	18.4
AOI21	1.125	0.6244	44.2
AOI22	1.675	0.9165	45.3
OAI21	1.1306	0.6242	44.8
OAI22	1.9163	0.9237	51.6

Table 4: Total Area Comparison

Constraints

Software!

- 3D ICs are new technology
- NCSU 45NM 3DPDK only supports TSV-based
- Need more advanced tools to properly layout

Future Work

1) Software library that supports monolithic integration
2) Additional cells
3) Determine the average area improvement after routing overhead

Questions?