EE382M: VLSI I
Monolithic 3D IC Basic Cell Library

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1 Introduction

3D integrated circuits (3DICs) are one potential advancement that will allow circuit designers to save area by having different parts of a design on different layers of silicon which are then bonded together. There are several different styles of 3DIC technology, but we will be focusing on monolithic 3DICs. We designed a standard cell library for 3DIC technology, and simulated the cells to determine the performances differences as compared to the standard version of each cell.

2 Technology Background

2.1 3D ICs

There are two common types of 3D ICs. The more common variety, which the library we plan to use was designed for, uses Through-Silicon Vias (TSVs) to connect layers, with each layer typically having full transistors. This allows vertical logic, but requires careful planning so as to ensure that the layers line up. Another issue with this approach is that a single TSV is very large relative to the cells it connects; at a 45nm technology node, the minimum width of a TSV is 6000nm [3]. This obviously cannot be used for fine-grained modifications to a design, and must be planned for when the design is initially made.

2.2 Monolithic 3D ICs

One way of avoiding the problem with TSV is through monolithic 3D IC technology. This technology is also a vertical technology, but it builds up very thin layers of devices instead of bonding them together. Instead of having TSVs, monolithic integration has 'monolithic inter-tier vias' (MIV). These MIVs, at 70nm, are a similar size to the contacts used at a 45nm technology node [2], and thus can be used to design individual cells across multiple layers. They additionally have negligible parasitic capacitance. Because a significant portion of cell area comes from the necessary separation between the pwell and the nwell, by splitting the pull-up network and pull-down networks and putting each on a separate layer, we can achieve significantly smaller area without having to alter logic. We also considered doing the method presented in [1]; however, due to the limitations of the tools, the advantages of these method (stacking cells on top of other cells by layers to reduce wire lengths and delays across designs) would be difficult to illustrate.

3 Specifications

3.1 Overview

We are designing a library of standard cells (listed in Table 1) for reducing area using monolithic 3D IC technology. Once completed, these cells should be able to be placed in a design andreduce the area by up to 40% in the ideal case. This also should allow for less area consumed by routing, as routing can be run in the layer that has less area dedicated to logic (typically the same layer as the NMOS, due to the smaller transistor widths).

Cell	Sizes
AND	2,3,4
OR	2,3, 4
NAND	2, 3,4
NOR	2, 3, 4
AOI	21, 22
OAI	21, 22
INV	N/A
BUF	N/A

Table 1: Cell Types and Sizes

3.2 Interface

The goal of cell design is to ensure that the inputs and outputs match identically with standard cell libraries of traditional technology. As such, each cell has the standard outputs. The primary difference is that the target library has VDD and GND rails stacked on separate layers, and as such they are not at opposing ends of the cell as they traditionally are in standard cells. All inputs and outputs come from the opposite side of the cell from the power and ground rails in our designs.

3.3 Design Targets

Our primary goal is area reduction, and we expect that using 3D IC technology can achieve area improvements approaching 50% in the ideal case. However, we expect most of our better gains to be around 40% less area, due to the overhead created by the MIVs. The best cases for area reduction come from gates that have equally sized PMOS and NMOS transistors; however, this is rarely the case (with size typically larger on the PMOS network), and even if it were, we could not achieve 50% area reduction due to the MIV area. We plan to create reference versions of all of the standard cells, and the power and timing requirements for the reference versions are our design targets for the power and timing requirements of the 3D versions.

4 Design

4.1 Basic Architecture

The most basic goal of our design is to achieve the functionality of each standard cell. Because we used the technique outlined in [2], the PMOS and NMOS networks remained the same as they were in the standard cell, except for removing the poly between and replacing it with a contact to metal1.

4.2 Toolset

NCSU has a library for 3D ICs that we initially considered using. However, while it does support multiple layers, it has no functionality for MIVs (focusing rather on TSV-based ICs). This meant two things for our design. Firstly, if we built our designs using the 3D IC library provided, there would be no way of achieving power and timing simulation, as TSV technology has radically different effects. Secondly, TSVs would dominate the area of any cell, and thus we would not be able to get valid area results either. The only advantage this path would have had would be for purposes of simulating the logic, which was basic and thus would not be important information.
We instead decided to utilize the standard 45nm NCSU libraries. While this does not support laying directly, we were able to simulate the effect of the MIV by separating the layers with a metal1 wire, with the length calculate to provide the same resistance as the MIV would, for power and timing simulations. Additionally, as the contacts connecting the poly to the wire are within 5nm of the size of a MIV, we can accurately measure the area. This approach allowed us to calculate the area, power, and timing achievable if we had tools that supported the technology.

4.3 Design Flow

To illustrate our procedure, here are the steps taken for a NAND2 gate.

1. Create a schematic (Fig. 1)
2. Generate the pins from the schematic
3. Create a layout for the standard cell (Fig. 2)
4. Take the standard cell layout and remove the interconnecting polysilicon
5. Add a 65nm by 3420nm metal1 connection between the poly contacts and the inputs. This size was chosen by calculating the wire length necessary, when created from a material with the resistivity of

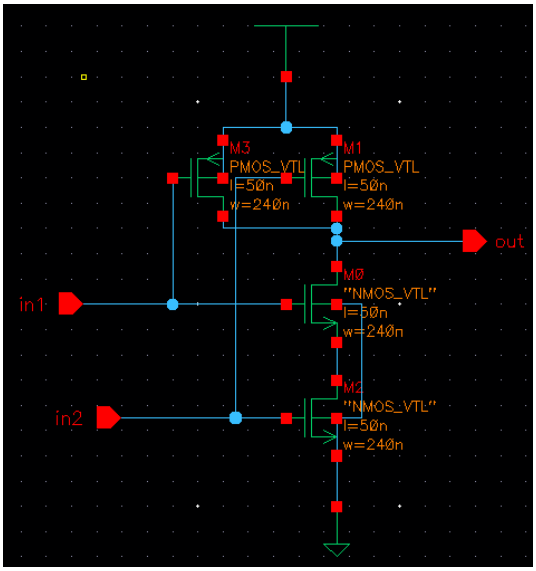

Figure 1: NAND2 Schematic

metal1 (.25Ω / square) [3], to simulate a MIV resistance of 20 Ω [2] . We chose 65nm width to minimize the required length. This is shown in Figure 3.

6. Measure each half of the cell (the 3D IC area is equal to the max of the two sizes)

7. Simulate the 3D version of the cell pre- and post- layout to determine the power and timing. Timing is shown for both rising and falling worst case scenarios for planar (Figures 4 and 5) and 3D (Figures 6 and 7) designs.

4.4 Optimization Techniques

We employed the standard optimization techniques used for standard cell libraries, as the pull-up and pull-down networks remain intact. These include sizing the transistors so that they are balanced, adding additional pins on the larger transistors to reduce the resistance from the contacts, and carefully routing the metal1 so as to avoid unnecessary area due to routing. The last one is particularly relevant, as space that would have been available between transistors due to minimum distances between wells is no longer available. One unique advantage that monolithic 3D IC technology gives us is the ability to reduce the length of the poly. As it notes in [2], the unit resistance of polysilicon is significantly higher than that of metal; by only having polysilicon on the transistor and not forming a wire between them, we can reduce the internal wire resistance. This counteracts the additional resistance provided by the MIV, producing what we anticipate to be a negligible timing difference.

4.5 Naming Conventions

Our naming conventions were to have either <CELLNAME><CELLSIZE>, for a standard version of a cell, or <CELLNAME><CELLSIZE>_3D, for the version that has the additional wiring to simulate a 3D IC.

4.6 Issue Tracking

We kept track of the cells through git, using it to track progress, bugs, to-do items, and notes on each design as we worked on them.

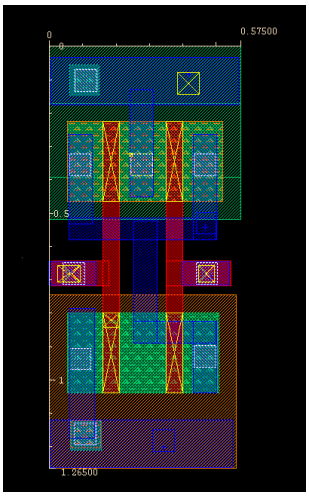

Figure 2: NAND2 Layout

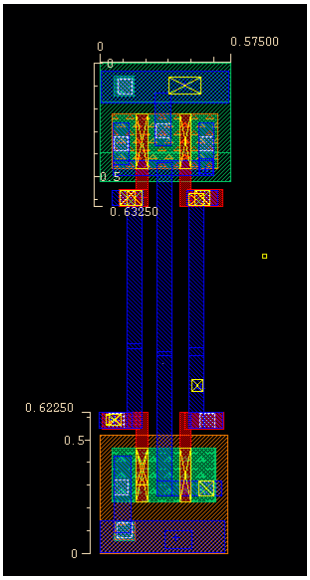

Figure 3: Simulated 3D NAND2 Layout - Middle wires shortened for figure visibility

5 User Document

5.1 Using 3DMI Standard Cells

The 3DMI standard library has similar design concept with conventional planar process standard library. The biggest difference is it separate NMOS and PMOS transistors into two layers, which can be used to reduce chip area, global wire routing length and even provide new way of circuit design. In this library, we put all the PMOS transistors and power rail (VDD) into the bottom layer, because normally PMOS transistors occupy larger area. For the bottom layer, we apply 4BM metal layer stack [Ultra High Density Logic Designs ...] which adds 3 metal layers to the bottom tier. In other word, there are total 4 local metal layers available on the bottom tier. It is a good choice because as we mentioned, in this library PMOS transistors are located in the bottom tier. With more local metal line, it could bring more convenience when routing in tight space. For each cell, there is always one side for the connection of inter-tier vias (MIVs). Therefore, routing should be more careful when wires are close to the edge. Another important thing is

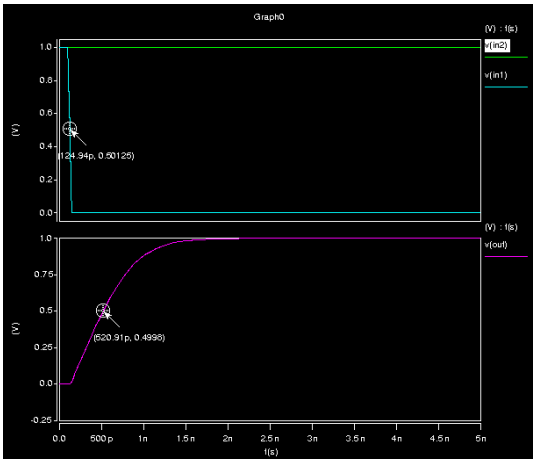

Figure 4: Worst-case NAND2 Rising Time

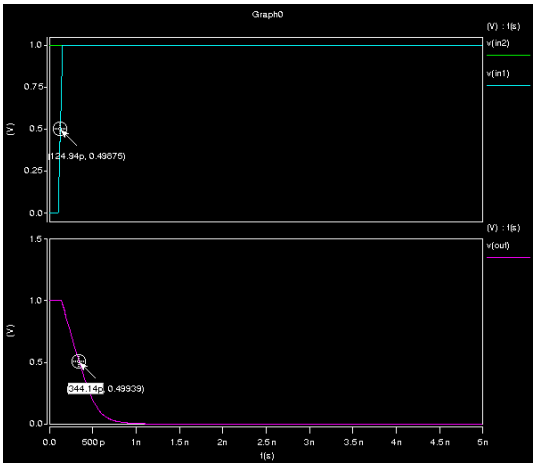

Figure 5: Worst-case NAND2 Falling Time

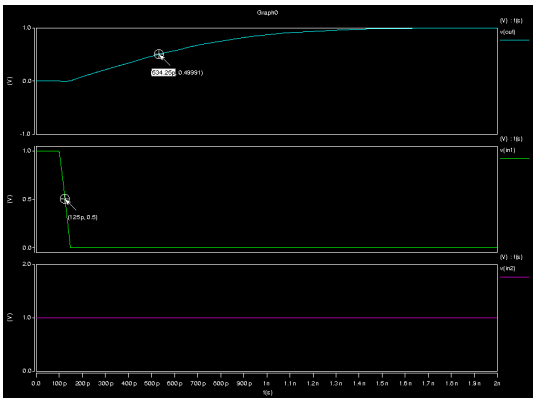

Figure 6: Worst-case NAND2_3D Rising Time

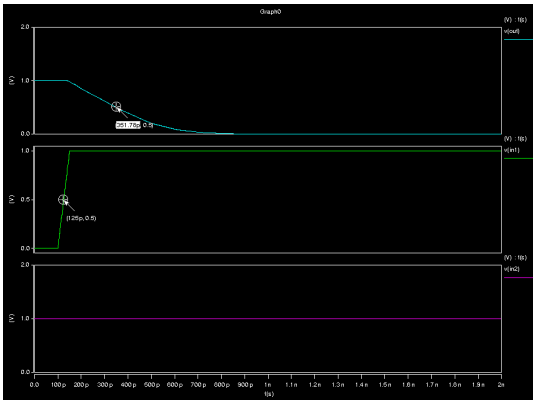

Figure 7: Worst-case NAND2_3D Falling Time

Category	Number of cells	Cell Names
buffer	3	INV, BUF, INV_CHAIN
logic	16	NAND2/3/4, NOR2/3/4,
		AND2/3/4, OR2/3/4,
		AOI21, OAI21, AOI22, OAI22

Table 2: 2D Cells Created

when choosing cells, some cells could be more favorable than others, especially for cells have similar NMOS and PMOS area, which will be discussed later.

5.2 Standard Cell List

We choose total 20 standard cells, including an inverter chain to test the potential problems caused by monolithic 3D integration. All of the cells should be sufficient for normal design, and could be useful for testing most of the circuits using 3DMI process. In order to compare the differences between 2D and 3D process, we construct both type with the same floorplanning mechanism which can help easily understand the advantages and disadvantages among two strategies.

5.3 Cell Area

One of the most obvious benefit of using 3D ICs is that they can reduce area of the chips or SoCs by stacking the circuits and growing vertically. Here we not only provide the cell area of monolithic 3D standard cells but also the cell area for 2D standard cells. Therefore, you can use the tables to calculate how much area could be saved by using 3DMI.

The following table provides the area of PMOS transistors and NMOS transistors in a single 3D standard cell. We can see which cells are more competitive when applied on 3D technology.

Category	Number of cells	Cell Names
buffer	3	INV_3D, BUF_3D, INV_CHAIN_3D
logic	16	NAND2/3/4_3D, NOR2/3/4_3D,
		AND2/3/4_3D, OR2/3/4_3D,
		AOI21_3D, OAI21_3D, AOI22_3D, OAI22_3D

Table 3: 3D Cells Created

cell names	area in 2D(um$\hat{2}$)	area in 3DMI(um$\hat{2}$)	difference percentage
INV	0.4151	0.2352	42.6
BUF	0.8483	0.4828	43.5
INV_CHAIN			
NAND2	0.7242	0.4531	37.5
NAND3	1.0356	0.5946	43.5
NAND4	1.3523	0.7229	46.5
NOR2	0.7943	0.5304	29.4
NOR3	1.2288	0.8661	29.5
NOR4	1.7825	1.3195	26
AND2	1.1866	0.7102	41
AND3	1.5595	0.88	43.6
AND4	1.9815	1.179	40.5
OR2	1.3298	0.844	36.5
OR3	1.4506	1.2953	10.7
OR4	2.1974	1.792	18.4
AOI21	1.125	0.6244	44.2
AOI22	1.675	0.9165	45.3
OAI21	1.1306	0.6242	44.8
OAI22	1.9163	0.9237	51.6

Table 4: Total Area Comparison

cell names	area of PMOS(um$\hat{2}$)	area of NMOS(um$\hat{2}$)	difference percentage
INV	0.2352	0.1925	22.2
BUF	0.4828	0.37	30.5
INV_CHAIN			
NAND2	0.4531	0.3516	28.9
NAND3	0.5946	0.5547	71.9
NAND4	0.7229	0.7031	28.2
NOR2	0.5304	0.336	57.9
NOR3	0.8661	0.4615	87.7
NOR4	1.3195	0.6867	92.1
AND2	0.7102	0.6137	15.7
AND3	0.8158	0.88	7.3
AND4	0.9675	1.179	17.9
OR2	0.844	0.5688	48.4
OR3	1.2953	0.6891	88
OR4	1.792	0.8112	121
AOI21	0.6244	0.4894	27.6
AOI22	0.9165	0.5694	61
OAI21	0.6242	0.5527	12.9
OAI22	0.9237	0.7056	30.9

Table 5: PMOS Area Comparison

cell names	rising time(ps)	falling time(ps)
INV	376.3	242.8
BUF	383.65	263.52
NAND2	383.94	212.3
NAND3	386.24	201.86
NAND4	390.49	197.51
NOR2	409.65	235.72
NOR3	431.36	263.98
NOR4	446.26	268.06
AND2	388.24	144.2
AND3	392.82	110.57
AND4	396.34	96.91
AOI21	411.6	219.26
AOI22	333	224.94
OAI21	446.27	218.06
OAI22	417.16	160.18

Table 6: Pre-layout Simulation

5.4 Cell Delay

The following table contains Presim, Postsim for both planar and monolithic 3D rising and falling time. Assume output capacitance is 50 fF. For 4BM metal layer stack we applied, the average resistance for a single stacked via is 20 ohms, and parasitic capacitance is 0.123 fF. After calculating and spice simulation, we found that metal 1 wire which is 3.42um long and 65 nm wide can fit the requirement well. As the extracted nettles files shows:

```
.subckt PM\_AND2\_OUT 3 7 8
c10 3 0 0.0371754f
r11 7 8 1.43133
r12 3 7 1.634
.ends

.subckt PM\_AND2\_3D\_OUT 4 8 12
c14 12 0 0.00285922f
c15 8 0 0.0134125f
c16 4 0 0.169493f
r17 12 14 0.220645
r18 12 13 0.0980645
r19 8 14 0.975333
r20 4 13 19.304
.ends
```

PM_AND2_OUT and PM_AND2_3D_OUT are the same net in an AND2 cell, and the only difference is PM_AND2_3D_OUT is connected to a 3.42 um metal 1 wire. You can find that C16 and r20 are quite close to our desired value. Since the parasitic resistance and capacitance of 3DMI stacking vias are not large, we think that it would be sufficient for the simulation.

6 Testing

Basic testing was the same as we learned in Lab 1. This includes ensure that all cells pass DRC and LVS, as well as that the simulations achieved the expected logic. Most of the bugs encountered through this were slight dimension errors on the DRC, created by the movement required to separate the PMOS and NMOS.

cell names	rising time(ps)	falling time (ps)
INV	383.5	249.72
BUF	394.09	270.84
NAND2	396	219
NAND3	413	213
NAND4	435.65	212
NOR2	419.79	262.17
NOR3	454.44	279.22
NOR4	488.38	301.18
AND2	404.23	168.23
AND3	414.82	163.74
AND4	427.33	158.24
AOI21	432.26	228.9
AOI22	362.22	238.24
OAI21	469.83	229.28
OAI22	446.02	184.48

Table 7: Post-layout Simulation for 2D cells

cell names	rising time(ps)	falling time(ps)
INV	400.1	263.35
BUF	410.3	283.51
NAND2	409.25	227.25
NAND3	428.65	221.3
NAND4	451.14	223.65
NOR2	436.55	273.12
NOR3	471.58	290.01
NOR4	506.42	312.27
AND2	418.83	187.3
AND3	429.62	180.12
AND4	441.7	172.4
AOI21	438.23	232
AOI22	357.76	240.43
OAI21	471.77	232.6
OAI22	450.39	186.41

Table 8: Post-layout Simulation for 3D cells

Additionally, careful design was needed to get the 4-input cells to pass DRC, as adding the contact often would put metal1 too close together. Simulation files are in the attached tarball.

7 Optimization

7.1 Optimizing Individual Cells

Individual cells were primarily optimized using prior knowledge, as the design process (as noted in Section 3) does not differ significantly from the standard process. The methods that we used have all been thoroughly investigated in Lab 1 of this semester, and thus are not shown in detail. We used multiple contacts for all of the cells that had transistors large enough to fit multiple contacts, to reduce the resistance. Additionally, all transistors were sized to have 2:1 PMOS:NMOS transistors, to minimize delay.

7.2 Using Monolithic 3D ICs to Optimize Full Designs

The more interesting problem is how to use these completed cells to optimize existing designs. There are several facets, which we will analyze here; without support from the tools, it is difficult or impossible to show these in an actual design.

1. **Total Area** The biggest optimization goal of using 3D ICs is to reduce area. In the instances of balanced networks, as is shown in Section 6, the area saving can approach $40 - 50$ % on individual cells. However, the more optimal the split between the two sections is, the less room is left for routing, and thus cells must be spaced out to allow for wires. If we assume an optimal gate (using the NAND2 numbers from above) that must route wires, the area savings goes down by 130nm for every second wire added (as they can be split between layers if there are an even number). For a NAND2 gate, that is equivalent to a third of the area savings for each additional wire.

2. **Routing** Another interesting case, and a more realistic one, is that the user has a balance of cell sizes and types. In this case, while the overall area savings are less, you can hide the routing overhead in the underutilized layer (typically with the NMOS, though the routing can also use MIVs to switch to the other layer if it becomes advantageous). This can help mitigate the pressure on routing. Designs have been found by [2] to approach 40% reduction in area, even with the additional difficulties of routing.

8 Cell Layouts

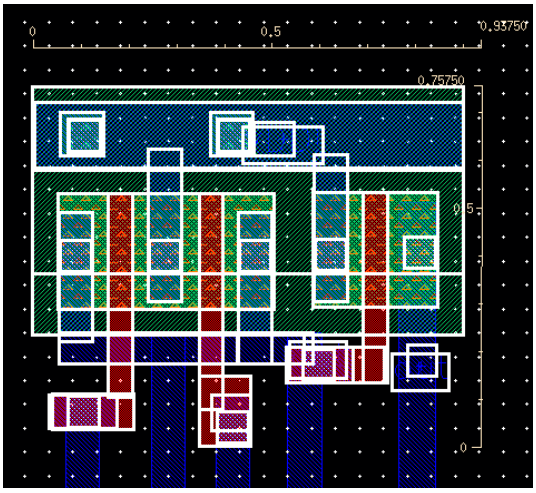

Figure 8: AND2 Pull-up Network

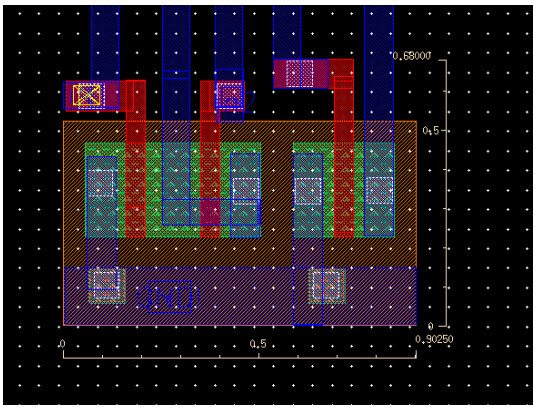

Figure 9: AND2 Pull-down Network

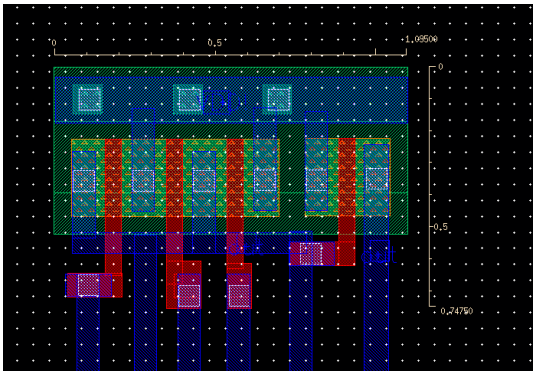

Figure 10: AND3 Pull-up Network

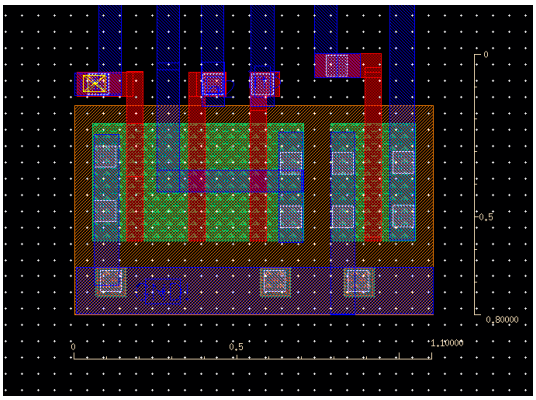

Figure 11: AND3 Pull-down Network

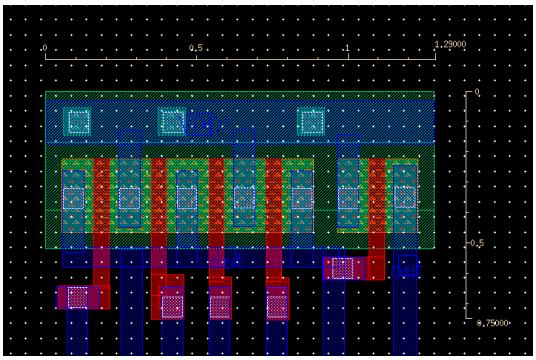

Figure 12: AND4 Pull-up Network

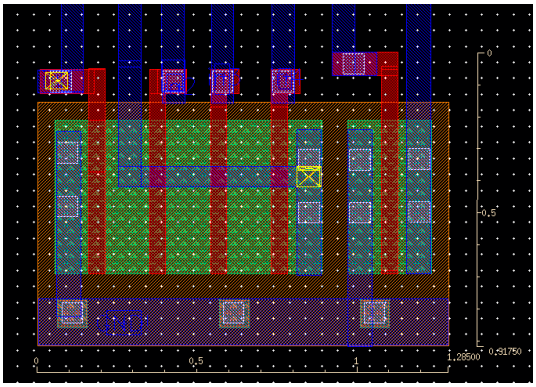

Figure 13: AND4 Pull-down Network

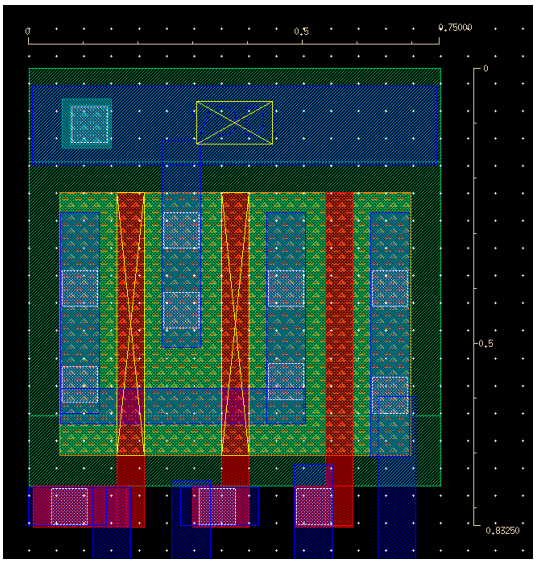

Figure 14: AOI21 Pull-up Network

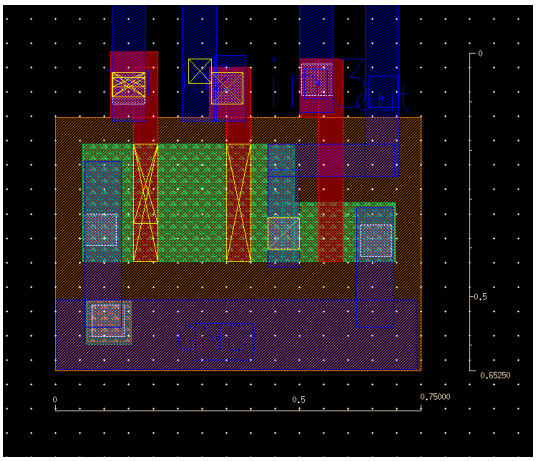

Figure 15: AOI21 Pull-down Network

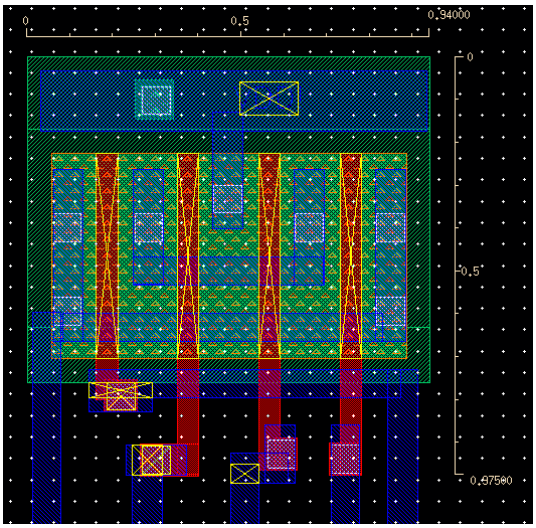

Figure 16: AOI22 Pull-up Network

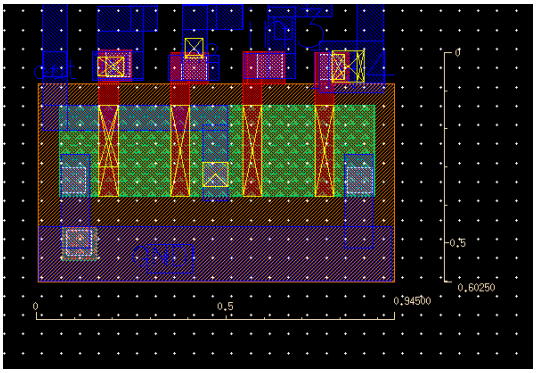

Figure 17: AOI22 Pull-down Network

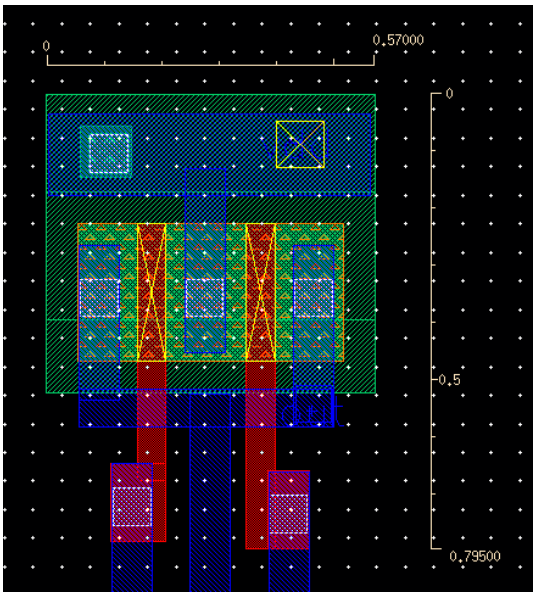

Figure 18: NAND2 Pull-up Network

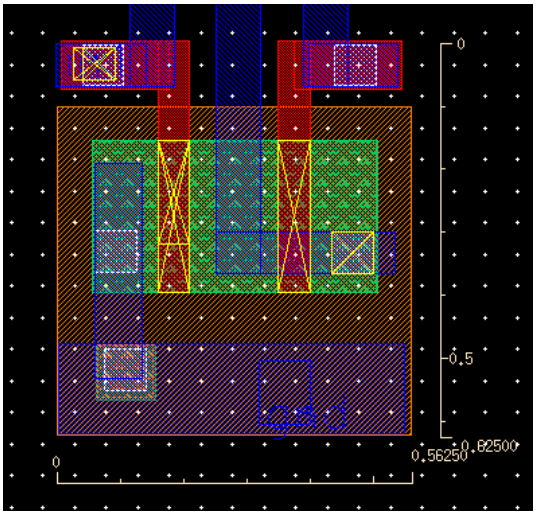

Figure 19: NAND2 Pull-down Network

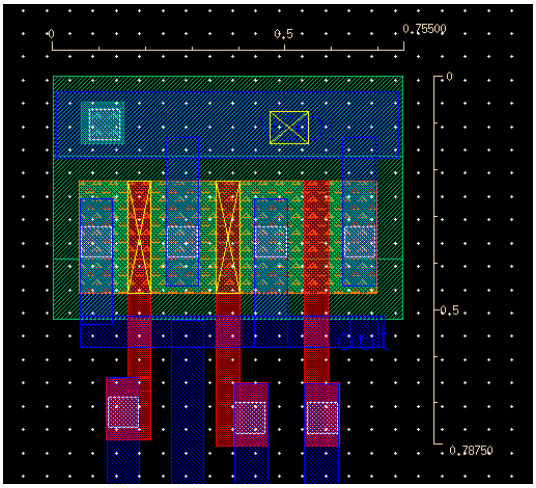

Figure 20: NAND3 Pull-up Network

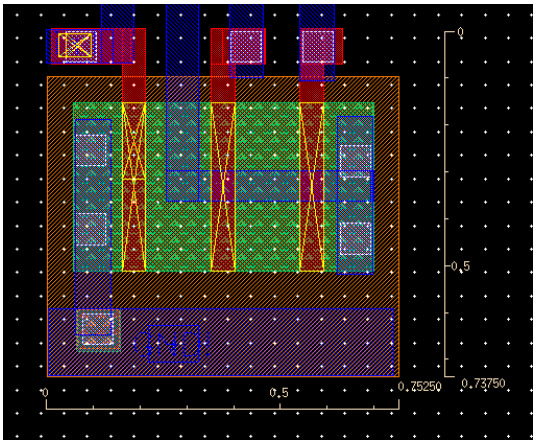

Figure 21: NAND3 Pull-down Network

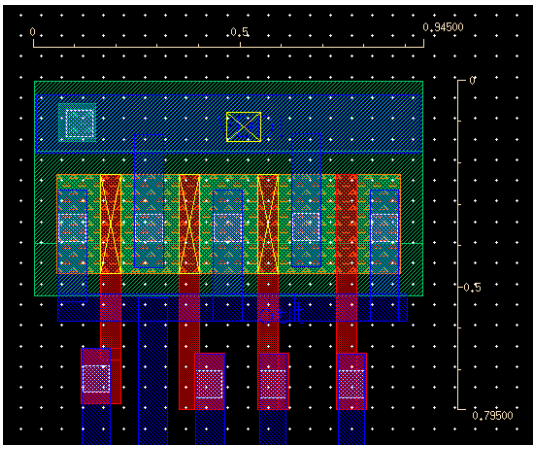

Figure 22: NAND4 Pull-up Network

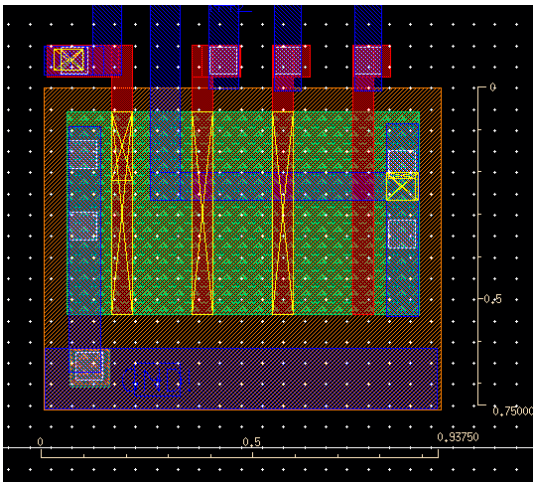

Figure 23: NAND4 Pull-down Network

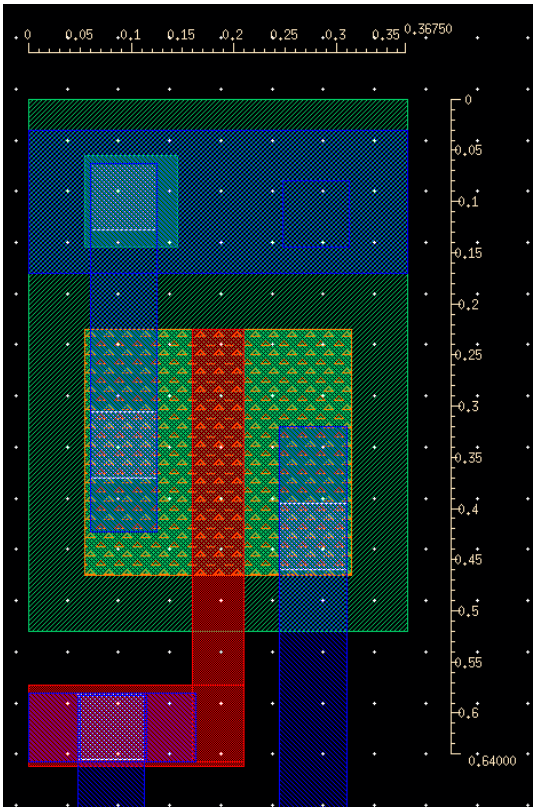

Figure 24: INV Pull-up Network

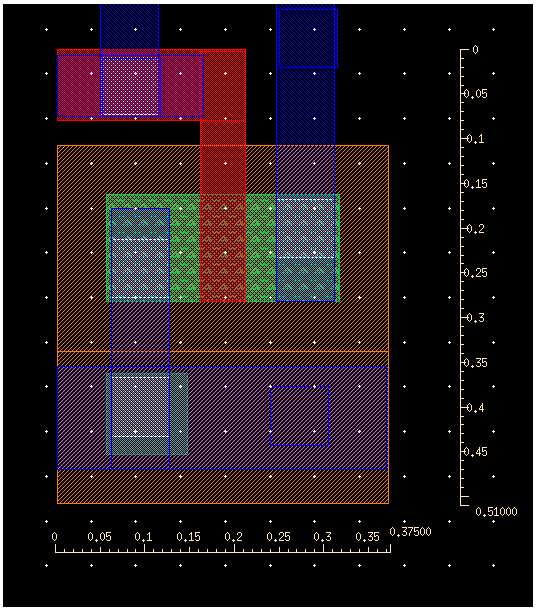

Figure 25: INV Pull-down Network

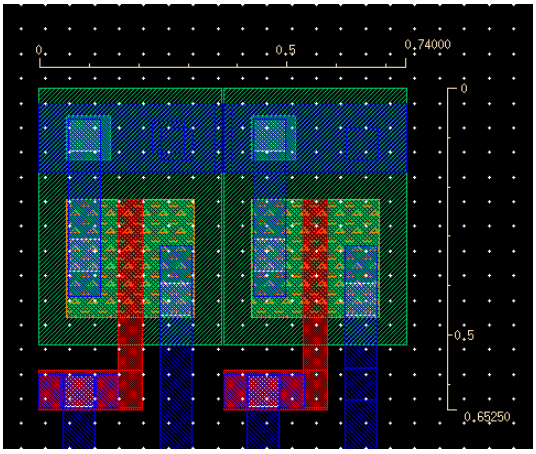

Figure 26: BUF Pull-up Network

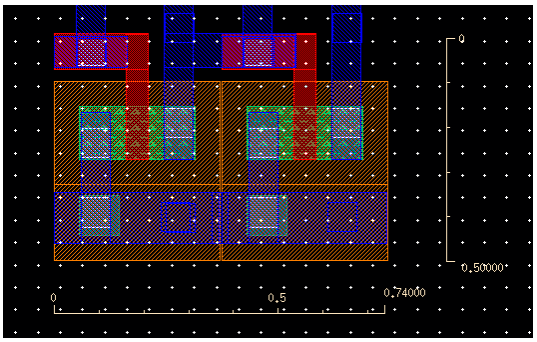

Figure 27: BUF Pull-down Network

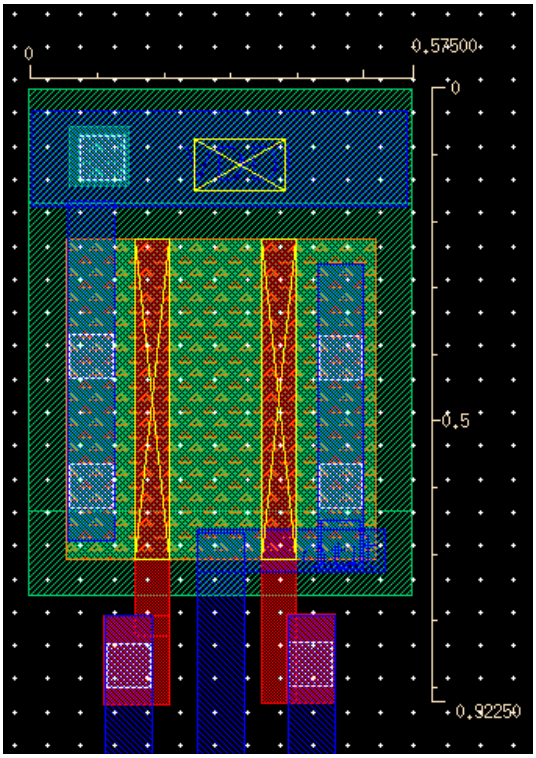

Figure 28: NOR2 Pull-up Network

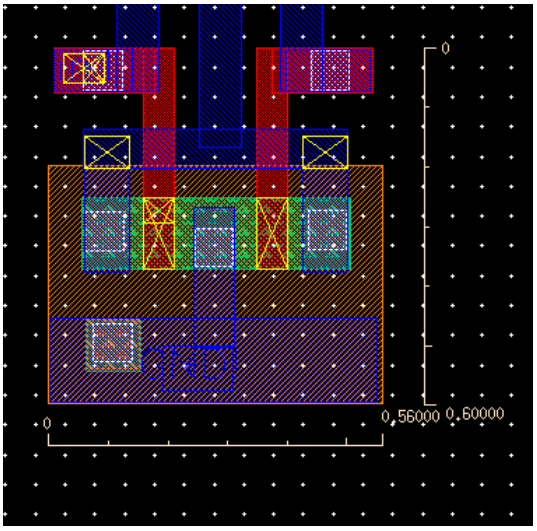

Figure 29: NOR2 Pull-down Network

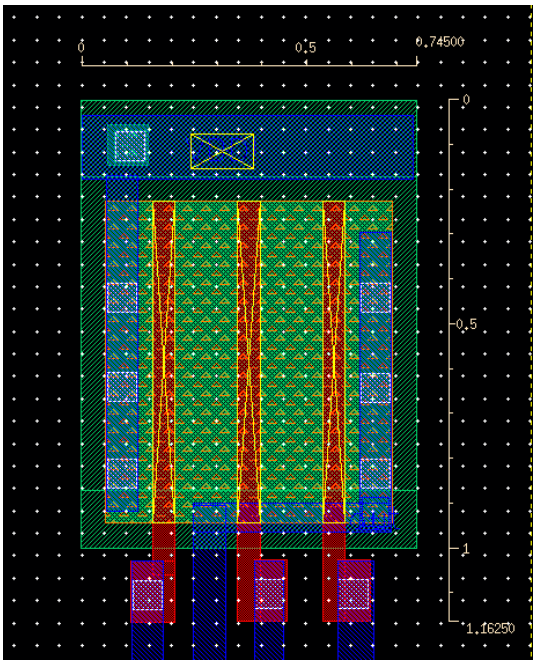

Figure 30: NOR3 Pull-up Network

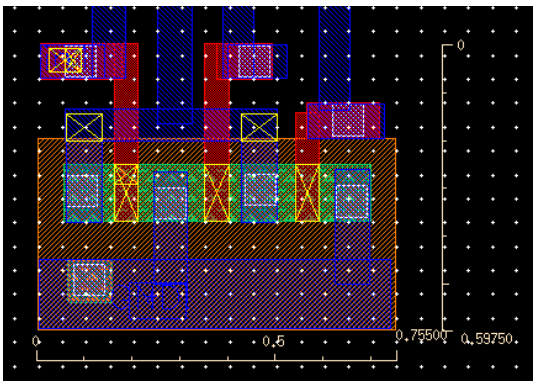

Figure 31: NOR3 Pull-down Network

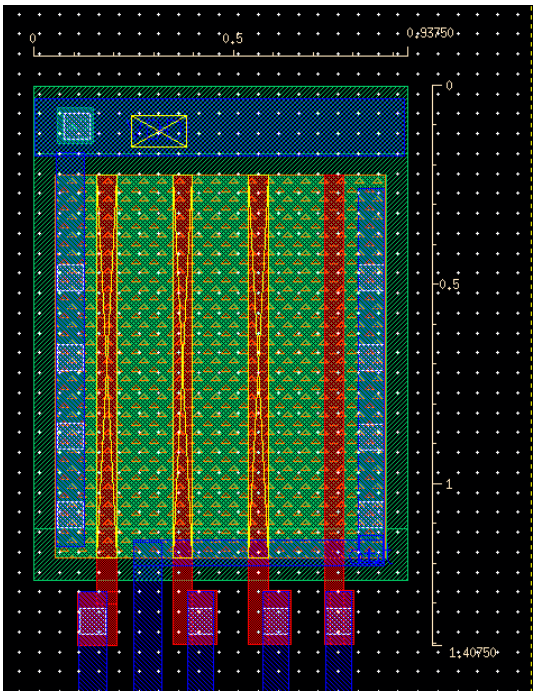

Figure 32: NOR4 Pull-up Network

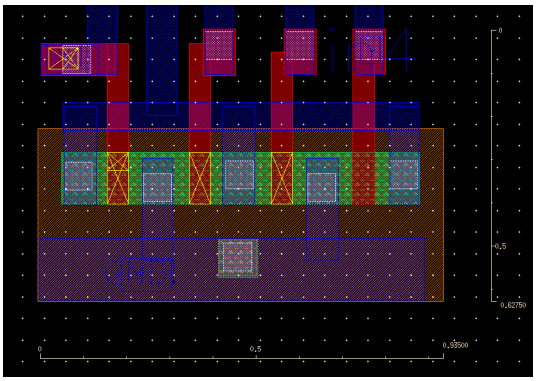

Figure 33: NOR4 Pull-down Network

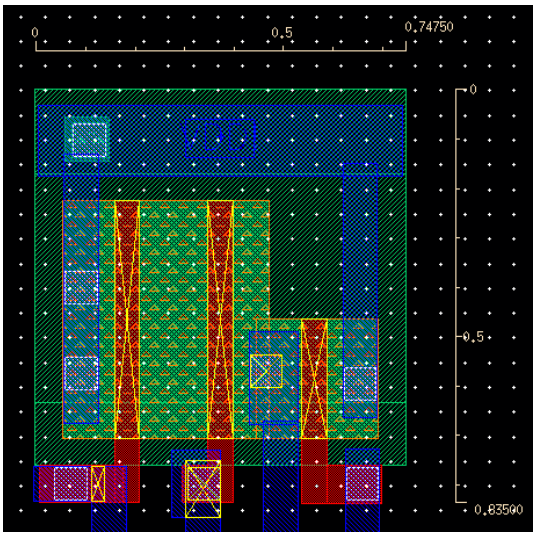

Figure 34: OAI21 Pull-up Network

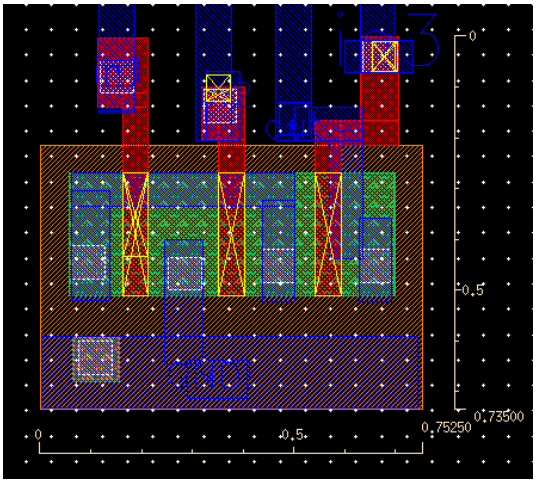

Figure 35: OAI21 Pull-down Network

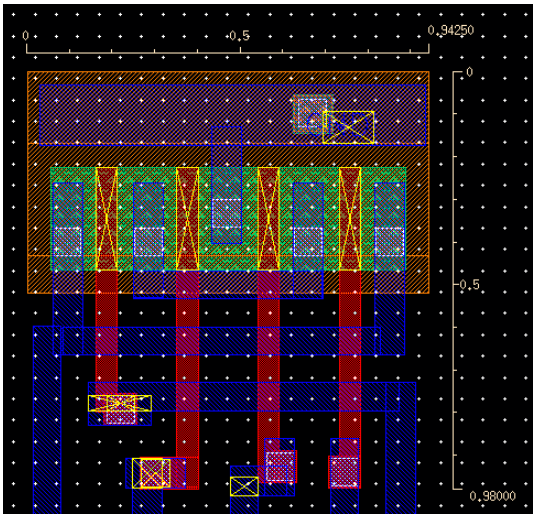

Figure 36: OAI22 Pull-up Network

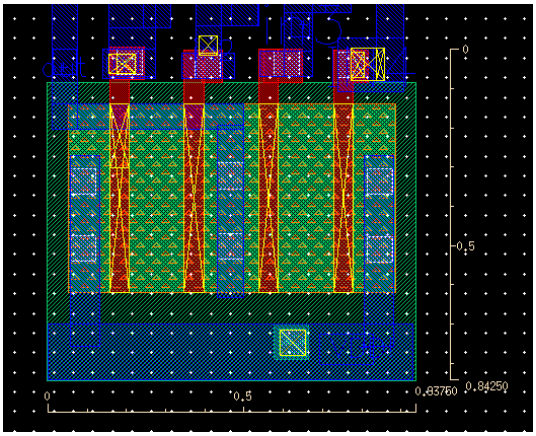

Figure 37: OAI22 Pull-down Network

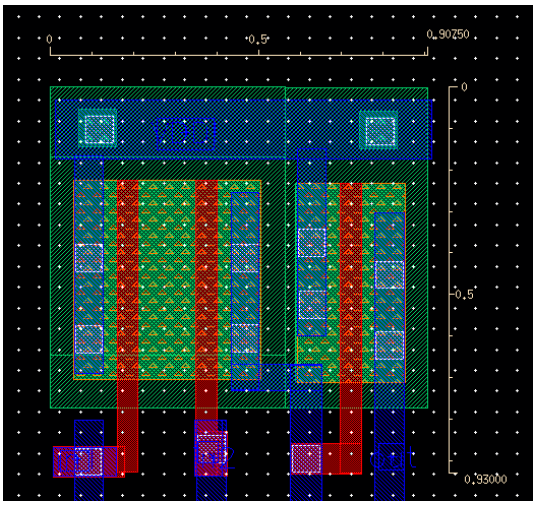

Figure 38: OR2 Pull-up Network

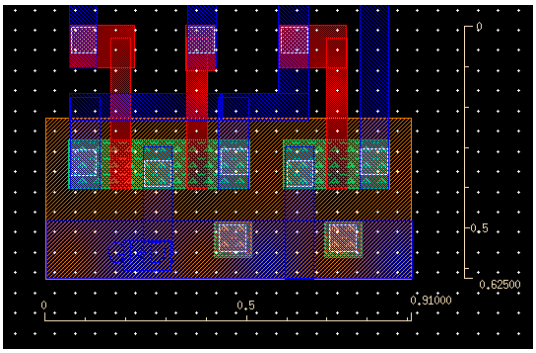

Figure 39: OR2 Pull-down Network

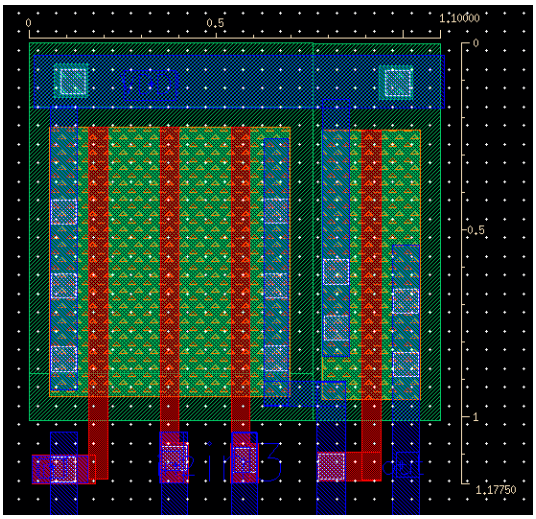

Figure 40: OR3 Pull-up Network

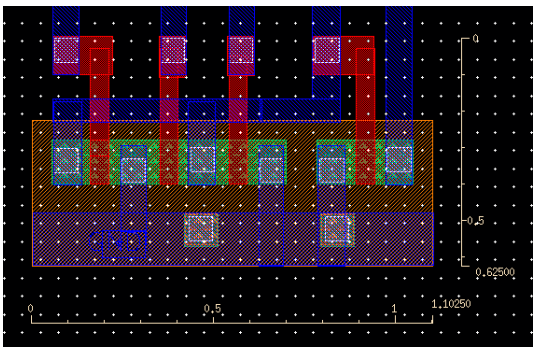

Figure 41: OR3 Pull-down Network

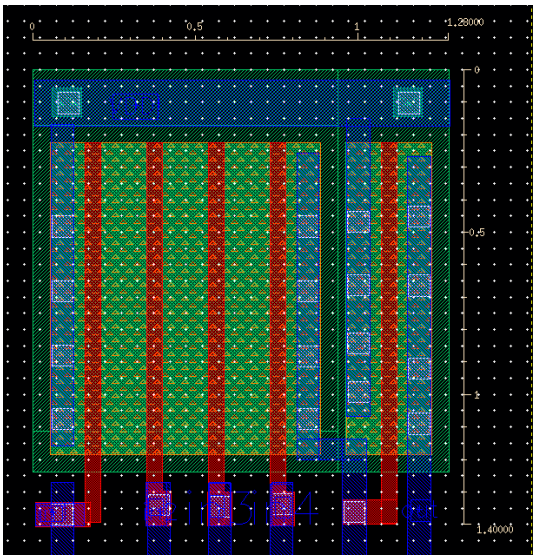

Figure 42: OR4 Pull-up Network

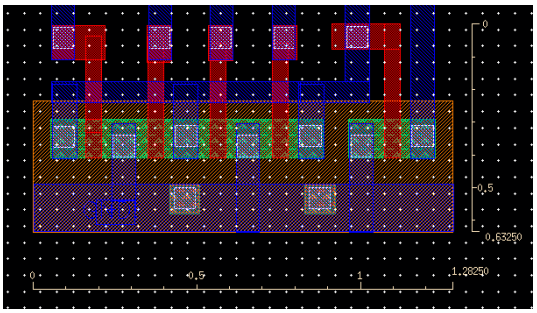

Figure 43: OR4 Pull-down Network

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[2] Young-Joon Lee, P. Morrow, and Sung Kyu Lim. Ultra high density logic designs using transistor-level monolithic 3d integration. In *Computer-Aided Design (ICCAD), 2012 IEEE/ACM International Conference on*, pages 539–546, Nov 2012.

[3] North Carolina State University. Electronic design automation (eda) wiki, 2012.