

VGA DRIVER INFO

The vgaDriverBuffer component is fairly complex in its construction, but simple to use. The screen is broken up into blocks of 16x16 pixels for a 640x480 resolution screen, resulting in a driver provides a 40x30 display. The coordinates of the top-left, top-right, bottom left and bottom right blocks are: (0,0), (39,0), (0,29), (39,29) respectively. This is shown in Figure 1.

The VGA hardware driver consists of three different sub-circuits, a clock divider (Vga_clk), a dual-ported memory(frameBuffer), and a VGA driver state-machine (Vga_out). An overview of this circuit is shown in Figure 2. This circuit allows color data (wd) to be stored into a frame buffer. The frame buffer holds the color data in memory, where each memory location in the frame buffer is mapped to pixels on the vga screen. The VGA driver state-machine is programmed to understand the timing of a VGA display, and reads from the appropriate location in the frame buffer when the "horizontal sync" and "vertical sync" (H, V) are at the correct pixel.

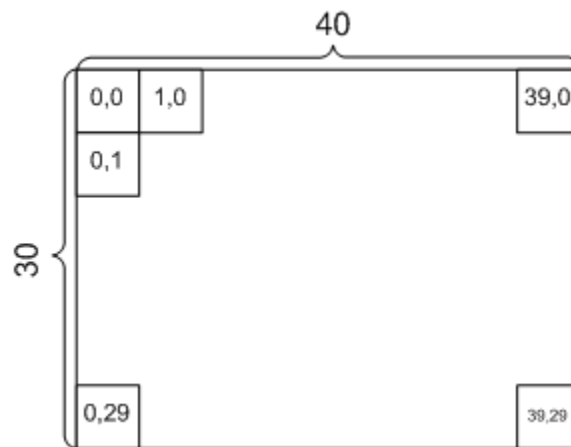


Figure 1. Screen Resolution

To write a color to the screen, you need to make sure that the write-enable is active (we), the write address is for a chosen pixel-block location (wa) and that the appropriate color is chosen (wd). You must have your Nexys2 board clock connected to the top-level of the circuit in Figure 2, and the HS, VS, Rout, Gout and Bout signals must be mapped to the pins that are connected to the VGA connector (see the included .ucf file for details).

For computing the address of a block of pixels, we need to take into account of a "guard band". The guard band is 24 blocks off the right of the display.

So the address computation for block (0,0) is 0
the address computation for block (1,0) is 1
the address computation for block (39,0) is 39
the address computation for block (0,1) is 64
the address computation for block (1,1) is 65
the address computation for block (2,0) is 128
the address computation for block (0,29) is $29 \times 64 + 0 = 1856$
the address computation for block (39,29) is $29 \times 64 + 39 = 1895$
the address computation for block (x,y) is $64y + x$

Color information is in the form of a byte, where the 3 msbs are red bits, the next 3 bits are green bits and the 2 lsbs are blue bits. This results in the bits of the wd signal to be represented by: RRRGGGBB. Having more red bits asserted and no other bits asserted, makes the block "more red", so "full red" is "11100000", "full blue" is "00000011", and full green is "00011100". You can mix colors: white is "11111111" black is "00000000".

A vgaTest entity is provided via the course website. This entity is a test block for making sure you understand how to use the vga driver, and should be synthesizable "out of the box". Please note the .ucf file for the pin locations. It is recommended that you first try this entity out prior to integrating the VGA driver to your RAT processor.

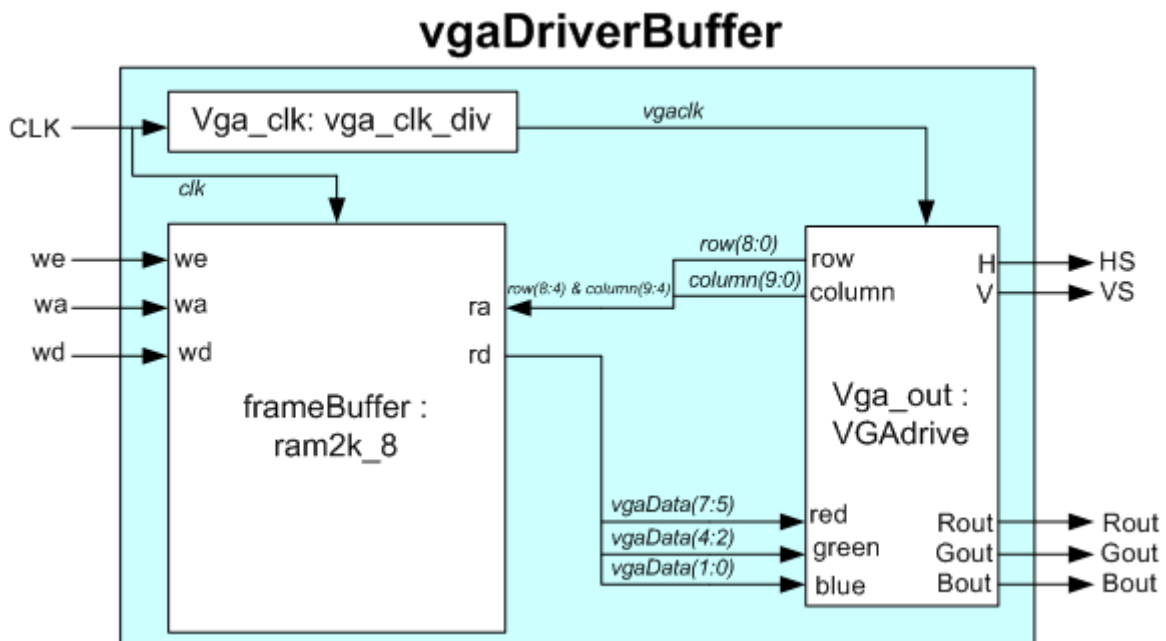


Figure 2. Supplied VGA driver block