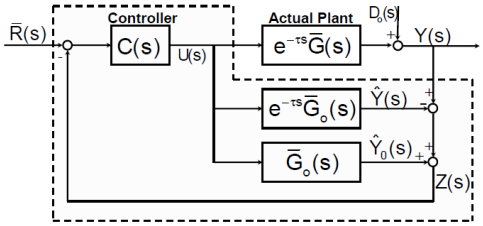
FROM LAST TIME…

Pole placement design

- Pole placement design
- Controller with integration
- PID via pole placement
- Smith predictor

$$\begin{bmatrix} a_{C(n-1)} \\ a_{C(n-2)} \\ \vdots \\ a_{C0} \\ b_{C(n-1)} \\ \vdots \\ b_{C0} \end{bmatrix} = \mathcal{S}^{-1} \begin{bmatrix} a^c_{2n-1} \\ a^c_{2n-2} \\ \vdots \\ a^c_n \\ a^c_{n-1} \\ \vdots \\ a^c_0 \end{bmatrix}$$

$$C(s) = \frac{b_{C2}s^2 + b_{C1}s + b_{C0}}{s^2 + a_{C1}s}$$



SISO DESIGN LIMITATIONS

Topics

- Free integrators
- Poles/Zeros

At the end of this section, students should be able to:

- Describe the connection between system order and steady-state error due to a reference or disturbance.
- Predict the effect of poles and zeros on closed-loop step response.
- Select appropriate closed-loop bandwidth based on poles and zeros.

SISO DESIGN LIMITATIONS

FREE INTEGRATOR EFFECTS

WHAT IS SYSTEM TYPE? WHY DOES IT MATTER?

$$G(s) = \frac{N(s)}{s^i \overline{D}(s)}$$

	Steady-State System Error		
Type	**Step**	**Ramp**	**Parabolic**
0	finite	∞	∞
1	0	finite	∞
2	0	0	finite
3	0	0	0

OPEN LOOP INTEGRATORS

Lemma 8.1 (System Types for Reference Command)

- For a stable CL system with one-DOF controller configuration, assume that open-loop TF has i free integrators or i poles at the origin, i.e.,

$$D_G(s)D_C(s) = s^i \bar{D}_G(s)\bar{D}_C(s), \qquad i \geq 1$$
$$\bar{D}_G(0)\bar{D}_C(0) = c_0 \neq 0$$
$$N_G(0)N_C(0) = c_1 \neq 0$$

- Then, for a step output disturbance or step reference command, the error $e(t)$ satisfies

$$\lim_{t\to\infty} e(t) = 0, \qquad \forall i \geq 1$$
$$\int_0^\infty e(t)dt = 0, \qquad \forall i \geq 2$$

OPEN LOOP INTEGRATORS

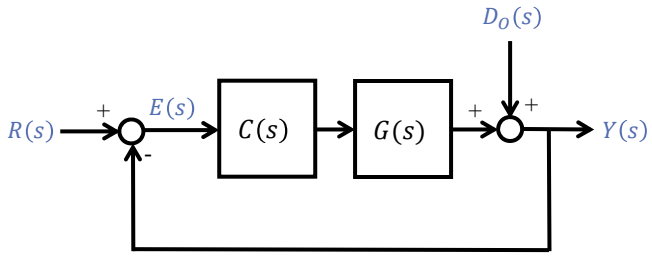
Lemma 8.1 (continued)

- Also, for a negative unit ramp output disturbance or a positive unit ramp reference command, the error $e(t)$ satisfies

$$\lim_{t\to\infty} e(t) = \frac{c_0}{c_1}, \qquad \text{for } i = 1$$
$$\lim_{t\to\infty} e(t) = 0, \qquad \forall i \geq 2$$
$$\int_0^\infty e(t)dt = 0, \qquad \forall i \geq 3$$

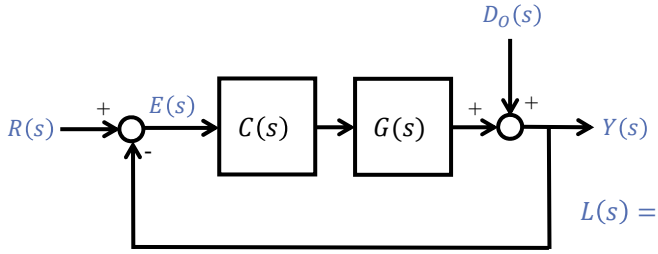
Q: *Is it possible to design a one-DOF controller to reject a ramp output disturbance that also has the property that the step response does not have any overshoot?*

LET'S VERIFY WITH A SIMPLE EXAMPLE



$$C(s) = K_P \qquad G(s) = \frac{623}{s(s+3.5)}$$

LET'S VERIFY WITH A SIMPLE EXAMPLE



$$L(s) = \frac{K_P 623}{s(s+3.5)}$$

$$G_{ER}(s) = -G_{ED_o}(s) = \frac{1}{1+L(s)} = \frac{s(s+3.5)}{s(s+3.5)+623K_P}$$

$$e_R(\infty) =$$

DETERMINE THE UNIT STEP RESPONSE AND APPLY FVT

$$G_{ER}(s) = -G_{ED_o}(s) = \frac{s(s+3.5)}{s(s+3.5)+623K_P}$$

$$e_R(\infty) = \lim_{s\to 0} sE(s)$$

$$e_D(\infty) = \lim_{s\to 0} sE(s) =$$

OPEN LOOP INTEGRATORS

Lemma 8.2 (System Types for Input Disturbance)

- For a stable CL system with one-DOF controller configuration, assume that the controller TF has i free integrators or i poles at the origin, i.e.,

$$D_C(s) = s^i \bar{D}_C(s)$$
$$\bar{D}_C(0) = c_0 \neq 0$$
$$N_C(0) = c_1 \neq 0$$

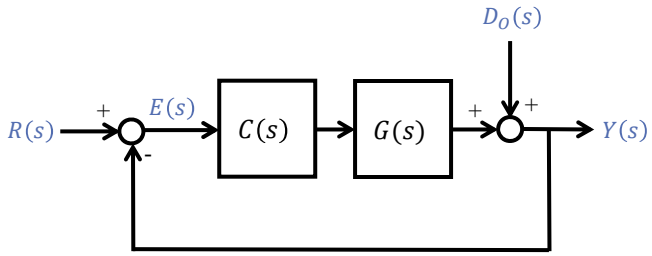
- Then, for a step input disturbance, the error $e(t)$ satisfies

$$\lim_{t\to\infty} e(t) = 0, \qquad \forall i \geq 1$$
$$\int_0^\infty e(t)dt = 0, \qquad \forall i \geq 2$$

- Also, for a negative unit ramp input, the error $e(t)$ satisfies

$$\lim_{t\to\infty} e(t) = \frac{c_0}{c_1}, \qquad \text{for } i = 1$$
$$\lim_{t\to\infty} e(t) = 0, \qquad \forall i \geq 2$$
$$\int_0^\infty e(t)dt = 0, \qquad \forall i \geq 3$$

CONSIDER A MORE GENERAL EXAMPLE



$$C(s) = \frac{N_C(s)}{s^i D_C(s)} \qquad G(s) = \frac{N_G(s)}{s^j D_G(s)}$$

- Controller transfer function has i free integrators
- Open-loop transfer function has k free integrators

DETERMINE THE RAMP INPUT DISTURBANCE RESPONSE AND APPLY FVT

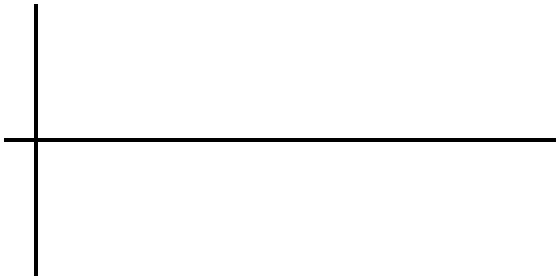
$$E(s) = S_{io}(s)D_i(s) \qquad S_{io}(s) = \frac{G}{1+CG} = \frac{s^i D_C(s)N_G(s)}{s^k D_C(s)D_G(s) + N_C(s)N_G(s)}$$

$$e(\infty) = \lim_{s\to 0} sE(s) \quad = \lim_{s\to 0} sS_{io}(s)D_i(s)$$

- For $i = 1$:

$$e(\infty) = \lim_{s\to 0} \frac{D_C(s)N_G(s)}{s^k D_C(s)D_G(s) + N_C(s)N_G(s)}$$

WHAT DOES IT MEAN THAT THE INTEGRAL OF ERROR IS ZERO?



- If the error overshoots, so must the plant output!
- Later we show that overshoot of step responses can be avoided with a two-DOF control system

TO SUMMARIZE

Want zero steady-state error to a step reference?

- Controller or plant must have at least one free integrator

Want zero steady-state error to a step input disturbance?

- Controller must have at least one free integrator

How to design for zero steady-state error?

- Select appropriate number of free integrators
- Embed free integrators into controller
- Apply pole-placement design

SISO DESIGN LIMITATIONS

POLE/ZERO EFFECTS

GENERAL EFFECT OF OPEN LOOP POLES/ZEROS

Lemma 8.3

- For stable CL system with poles located to the left of $-\alpha$ for some $\alpha > 0$, assume that the controller has at least one pole at origin. Then, for any uncancelled plant zero z_0 or pole p_0 that is to the right of CL poles (i.e., $Re\{z_0\} > -\alpha$ or $Re\{p_0\} > -\alpha$), we have
  1. For a positive unit reference step or a negative unit step output disturbance, the error $e(t)$ satisfies

$$\int_0^\infty e(t)e^{-z_0 t}dt = \frac{1}{z_0}$$
$$\int_0^\infty e(t)e^{-p_0 t}dt = 0$$

  2. For a positive unit step reference and for z_0 in RHP (unstable zero),

$$\int_0^\infty y(t)e^{-z_0 t}dt = 0$$

  3. For a negative unit step input disturbance,

$$\int_0^\infty e(t)e^{-z_0 t}dt = 0 \qquad \int_0^\infty e(t)e^{-p_0 t}dt = \frac{D_C(p_0)}{p_0 N_C(p_0)}$$

GENERAL EFFECT OF OPEN LOOP POLES/ZEROS

Observations

- A real minimum-phase (LHP) zero to the right of all CL poles produces overshoot in the step response

- A real nonminimum-phase (RHP) zero always produces undershoot in the step response. The amount of undershoot grows as the zero approaches the origin

- Any real open-loop pole to the right of all CL poles will produce overshoot in a one-DOF control architecture

HOW DO WE DESIGN USING THESE OBSERVATIONS?

1. The *CL bandwidth* should in practice be set *less* than the *smallest nonminimum-phase (RHP) zero* to avoid large undershoot in step response

2. It is advisable to set CL bandwidth *greater* than *real part* of any *unstable pole* to avoid large overshoot

3. To avoid overshoot produced by *minimum-phase* plant or controller zeros, cancel them outside the loop in a two-DOF design using the poles of prefilter $H(s)$.

CONSIDER AN EXAMPLE…

Given nominal plant:

$$G(s) = \frac{(s - z_G)}{s(s - p_G)}$$

Choose CL poles: $p_{1d}^c = p_{2d}^c = p_{3d}^c = -1$

Design lead/lag controller: $C(s) = \frac{K(s - z_c)}{(s - p_C)}$

$$z_C = \frac{1}{K_C z_G} \qquad K_C = \frac{3 + 1/z_G + 3p_G + p_G^2}{p_G - p_z}$$
$$p_C = K_C - 3 - p_G$$

HERE ARE RESULTS FOR 5 CASES OF PLANT POLES/ZEROS

	Case 1	Case 2	Case 3	Case 4	Case 5
	$p_G = -0.2$ $z_G = -0.8$	$p_G = -0.8$ $z_G = -0.2$	$p_G = -0.8$ $z_G = 0.8$	$p_G = 0.2$ $z_G = 0.8$	$p_G = 0.8$ $z_G = 0.2$
K_C	1.98	6.27	-1.56	-8.15	18.4
p_C	-0.82	4.07	-3.76	-11.4	14.6
z_C	-0.63	-0.8	-0.8	-0.15	0.27

- Which cases fail rule 1 and will undershoot?
- Which cases fail rule 2 and will overshoot?

Slow OL LHP pole → small overshoot

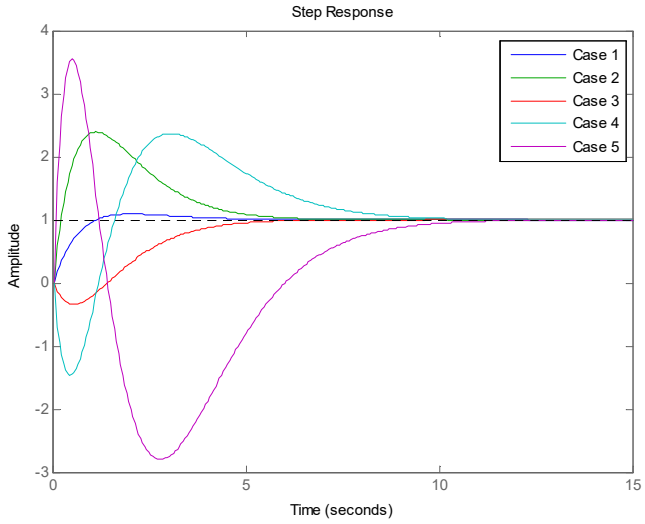
RHP zero → big undershoot
Slow LHP pole → small overshoot

RHP zero → undershoot
RHP pole → bigger overshoot

	Case 1	Case 2	Case 3	Case 4	Case 5
	$p_G = -0.2$ $z_G = -0.8$	$p_G = -0.8$ $z_G = -0.2$	$p_G = -0.8$ $z_G = 0.8$	$p_G = 0.2$ $z_G = 0.8$	$p_G = 0.8$ $z_G = 0.2$
K_C	1.98	6.27	-1.56	-8.15	18.4
p_C	-0.82	4.07	-3.76	-11.4	14.6
z_C	-0.63	-0.8	-0.8	-0.15	0.27

Slow LHP zero → big overshoot

RHP zero → undershoot
Slow RHP pole → big overshoot



IMAGINARY POLES/ZEROS

Corollary 8.1

- Consider the stable CL system in Lemma 8.3. Then, for a unit step reference input,
  - If plant has a pair of zeros at $\pm j\omega_0$, then

$$\int_0^\infty e(t)\cos(\omega_0 t)\,dt = 0$$
$$\int_0^\infty e(t)\sin(\omega_0 t)\,dt = \frac{1}{\omega_0}$$

  - If plant has a pair of poles at $\pm j\omega_0$, then

$$\int_0^\infty e(t)\cos(\omega_0 t)\,dt = 0$$
$$\int_0^\infty e(t)\sin(\omega_0 t)\,dt = 0$$

SLOW IMAGINARY ZEROS

Example 8.6

- Assume ω_0 is small when compared to CL bandwidth:

$$t_s \leq \frac{\pi}{\omega_0}$$

- Estimated Error Bound from Corollary 8.1:

$$e_{max} \geq \frac{1}{1-\cos(\omega_0 t_s)} \quad \rightarrow \infty \quad as \quad \omega_0 t_s \rightarrow 0$$

Maximum error will be very large if one tries to make CL bandwidth greater than the position of the resonant zeros (or imaginary zeros)

CONSIDER AN EXAMPLE…

Given:

$$G(s) = \frac{100s^2 + 1}{s^2(s+1)}$$

You chose desired poles at:

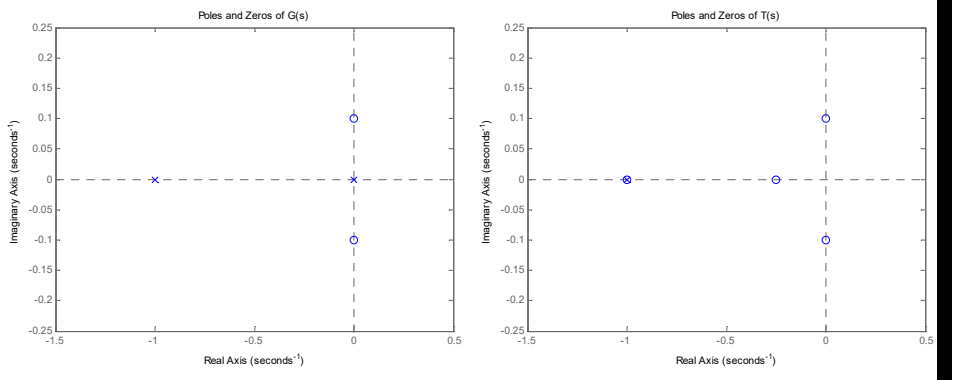
$$p_{1d} = p_{2d} = p_{3d} = p_{4d} = -1$$

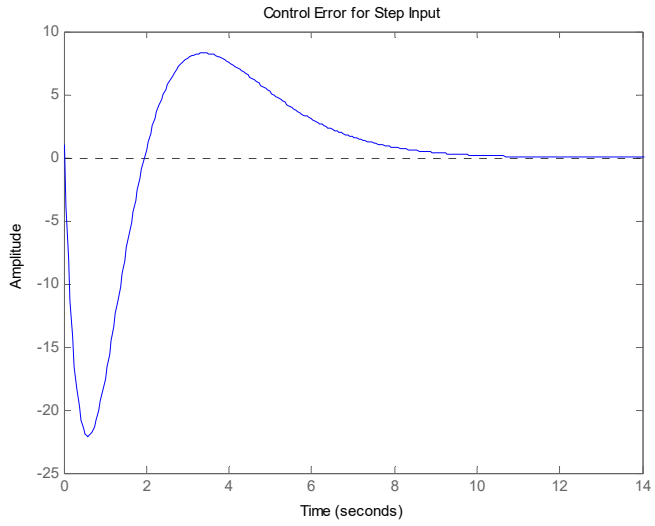
Producing the controller :

$$C(s) = \frac{(s+1)(4s+1)}{s^2 - 396s - 94}$$

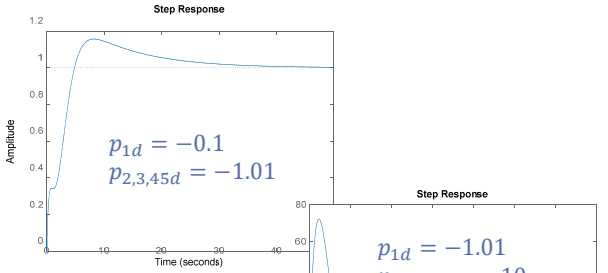
What is the resulting performance?

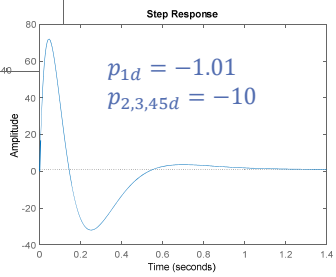
$$T(s) = \frac{400(s+1)(s+0.25)(s^2+0.01)}{(s+1)^5}$$

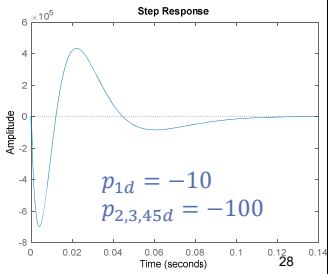




TEST SEVERAL SETS OF DESIRED CLOSED-LOOP POLES







$$G(s) = \frac{s^2 + 1}{s^2(s+1)}$$

Zeros: $\pm j1$

COMING UP

Frequency-Domain Design Limitations

- Bode's integral constraints on sensitivity
- Integral constraints on complementary sensitivity
- Poisson integral constraint on sensitivity
- Poisson integral constraint on complementary sensitivity

Summary of Design Limitations

Architectural Issues

- Internal Model Principle
- Feedforward
- Cascade Control