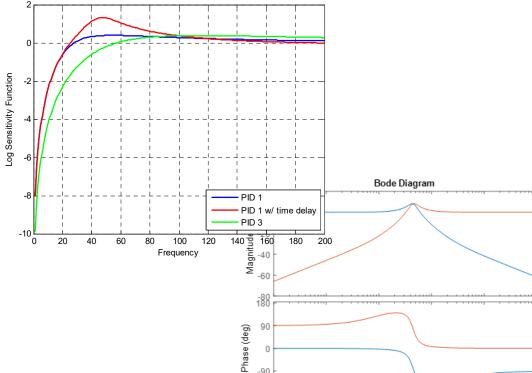
# FROM LAST TIME...

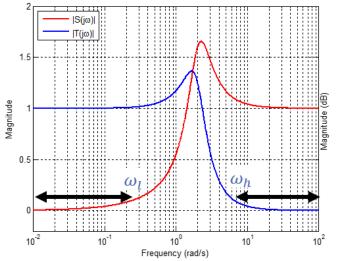
# **Frequency-Domain Design Limitations**

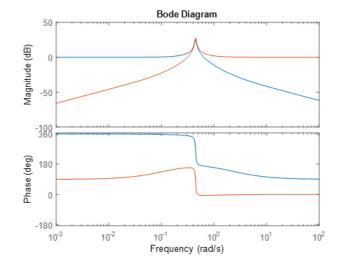
- Bode's Integral Constraints
- Poisson Integral Constraints



-180

10<sup>-3</sup>





Frequency (rad/s)

10<sup>1</sup>

10<sup>2</sup>

# **SUMMARY OF DESIGN LIMITATIONS**

# **Topics**

- Fundamental Design Trade-offs
- Limitations
- Remedies

### At the end of this section, students should be able to:

- Identify design trade-offs.
- Identify limitations due to physical components.

# HOW DO WE QUANTIFY CLOSED-LOOP PERFORMANCE?

- Various aspects of performance cannot be addressed independently via SISO design
- Must have a thorough understanding of fundamental SISO design limitations to come up with realistic performance specifications

# DISTURBANCE REJECTION PROPERTY

$$Y_D(s) = S(s)[D_O(s) + G(s)D_i(s)]$$
  $S(s) = 1 - T(s)$ 

$$S(s) = 1 - T(s)$$

# Disturbances are rejected only at frequencies where

$$|S(j\omega)| \approx 0$$
 or  $|T(j\omega)| \approx 1$ 

To achieve acceptable performance in the presence of disturbances, it will generally be necessary to place a lower bound on the closed-loop bandwidth!

# **MEASUREMENT NOISE EFFECT**

$$Y_M(s) = -T(s)N(s)$$

# Measurement noise is rejected only at frequencies where

$$|T(j\omega)| \approx 0$$

Given the fact that noise is typically dominated by high frequencies, there will be an upper limit on the bandwidth of closed-loop set by measurement noise!

# **CONTROL EFFORT**

$$U(s) = S_u(s)[\bar{R}(s) - D_o(s) - N(s)]$$
  $S_u(s) = T(s)/G(s)$ 

Large control signals arise at frequencies where  $|T(j\omega)| \approx 1$  but  $|G(j\omega)| \ll 1$  which occurs when closed-loop is forced to be much more responsive than open-loop process

To avoid actuator saturation or slew rate problems, it will generally be necessary to place an upper limit on the closed-loop bandwidth!

# **MODELING ERROR EFFECT**

Robust Stability Theorem:  $|T_o(j\omega)||G_{\Delta}(j\omega)| < 1$ ,  $\forall \omega$ 

Robust Performance:  $|S_{\Delta}(j\omega)| = \left| \frac{1}{1 + T_o(j\omega)G_{\Delta}(j\omega)} \right| \approx 1$ ,  $\forall \omega$ 

**Design Constraint:**  $S_o(j\omega) + T_o(j\omega) = 1$ ,  $\forall \omega$ 

# For frequencies with significant modeling errors:

Being responsive to reference changes and against disturbances at frequencies with significant modeling errors jeopardize stability; note also that MME  $|G_{\Delta}(j\omega)|$  is normally significant at high frequencies

To achieve robust stability and acceptable performance in the presence of modeling errors, it will generally be desirable to place an upper limit on closed-loop bandwidth!

### STRUCTURAL LIMITATIONS VIA TIME DELAYS

# Best Attainable Ideal Sensitivity Functions for a delay of au

$$T_o^*(s) = e^{-s\tau}$$
  
 $S_o^*(s) = 1 - e^{-s\tau}$ 

 To achieve the above ideal result requires the use of Smith Predictor plus an ideal controller!

# **Practically Achievable Sensitivity Functions**

- For  $\eta\tau$  error of time delay, magnitude of MME  $|G_{\Delta}(j\omega)|$  approaches 1 at approximately a bandwidth of  $1/\eta\tau$ , and thus limits the achievable CL bandwidth to this order for robust stability.
  - Delays limit disturbance rejection by requiring that a delay occurs before the disturbance can be cancelled.
  - 2. Delays further limit the achievable CL bandwidth through the impact of modeling errors

# **SYSTEM TYPE**

# Want zero steady-state error to a step reference?

Controller or plant must have at least one free integrator

# Want zero steady-state error to a step input disturbance?

Controller must have at least one free integrator

Requirements on steady-state error to reference or input disturbance place requirements on controller structure

# **OPEN LOOP POLES/ZEROS**

### **Observations**

- A real minimum-phase (LHP) zero to the right of all CL poles produces overshoot in the step response
- A real nonminimum-phase (RHP) zero always produces undershoot in the step response. The amount of undershoot grows as the zero approaches the origin
- Any real open-loop pole to the right of all CL poles will produce overshoot in a one-DOF control architecture
- Imaginary zeros smaller than CL poles will produce overshoot
- 1. The CL bandwidth should in practice be set less than the smallest RHP zero to avoid large undershoot in step response
- 2. It is advisable to set CL bandwidth greater than real part of any unstable OL pole to avoid large overshoot
- 3. Maximum error will be very large if one tries to make CL bandwidth greater than the position of the imaginary zeros

# **WATER BED EFFECT (BODE)**

### Independent of controller design

- Low sensitivity in certain prescribed frequency bands will result in a sensitivity larger than one in other frequency bands
- Unstable (RHP) open-loop poles make sensitivity minimization more difficult
- Low complementary sensitivity in certain prescribed frequency bands will result in a complementary sensitivity larger than one in other frequency bands
- RHP open-loop zeros makes the allocation of complementary sensitivity in the frequency domain more difficult.

# **POISSON**

### **Observations**

- When one RHP zero approaches a RHP open-loop pole, sensitivity allocation in frequency domain becomes almost impossible.
- When CL bandwidth is large when compared to the speed of NMP (RHP) zero, there will be a large sensitivity peak
- When CL bandwidth is small compared to unstable RHP poles, there will be a large complementary sensitivity peak.
- Sharp transitions in the sensitivity frequency response, i.e.,  $\omega_l$  close to  $\omega_h$ , will contribute to large sensitivity peaks.

The design problem becomes more difficult when the system has fast RHP open-loop poles and slow RHP zeros, relative to CL bandwidth

# **SISO DESIGN LIMITATIONS (PART 2)**

# REMEDIES

# GIVEN THE LIMITATIONS IN SISO DESIGN, WHAT CAN WE ACTUALLY DO WITH ALL OF THEM?

- 1. Identify unachievable specifications
- Identify where additional effort would be fruitful or wasted

# For example, each of the following impose an upper limit on usable bandwidth:

- Actuator slew-rate and amplitude limits
- Model error
- Delays
- Right-half-plane or imaginary-axis zeros

# GIVEN THESE TRADE-OFFS AND LIMITATIONS, WHAT REMEDIES ARE AVAILABLE?

# WHAT CHANGES TO SENSOR SELECTION WILL HELP?

- More accurate or faster sensor
- Virtual sensor

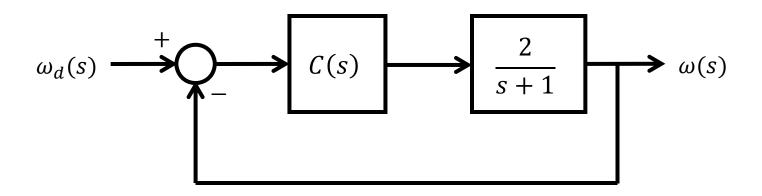
# WHAT CHANGES TO ACTUATOR SELECTION WILL HELP?

More powerful or faster actuators

### **LIMITATIONS AND REMEDIES**

# EXAMPLE: CHANGING PID STRUCTURE

# **SPEED CONTROL OF MOTOR**

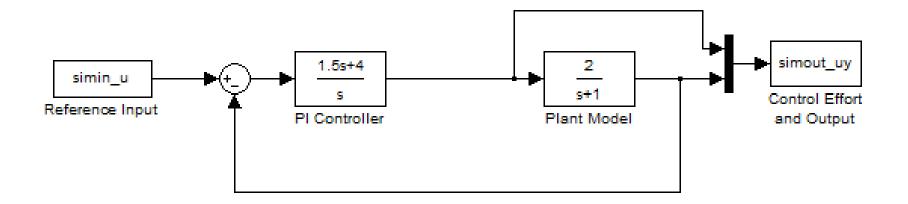


# **Performance Specifications:**

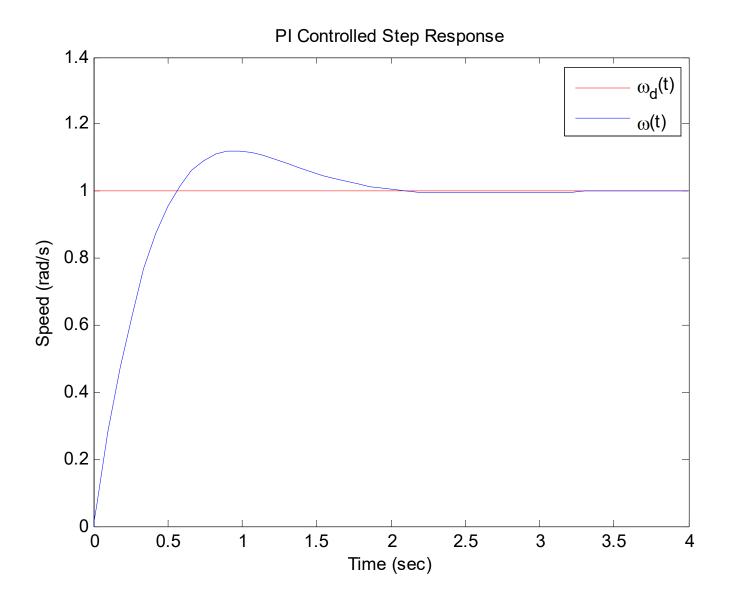
- Damping ratio = 0.707
- 2% Settling time = 2 sec.
- S.S. error to step inputs = 0

# **CHOOSE A PI CONTROLLER**

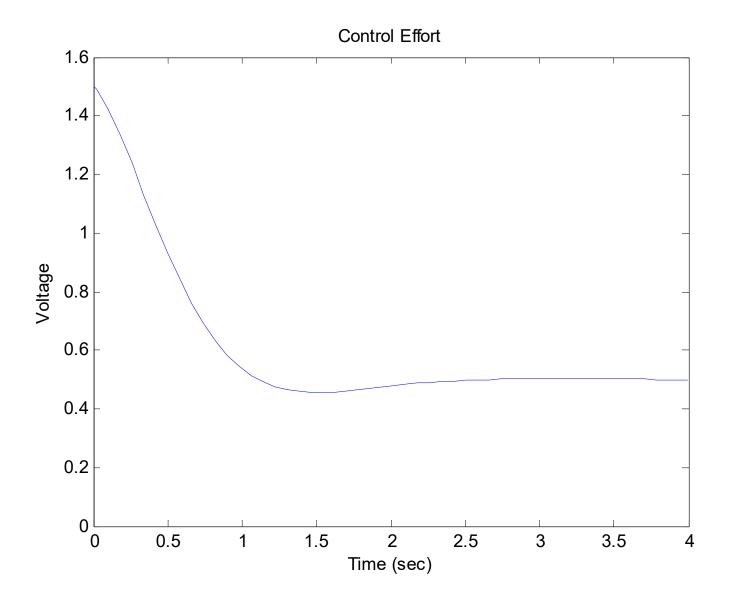
# **CREATE CONTROL LOOP IN SIMULINK**



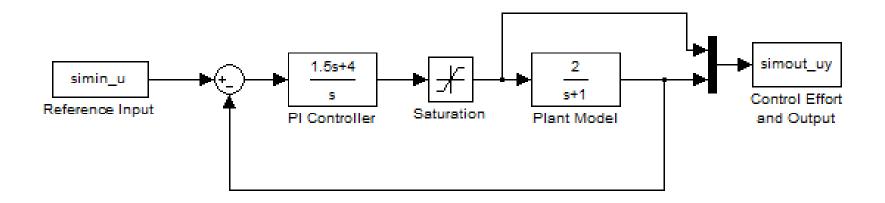
# **PI CONTROL**



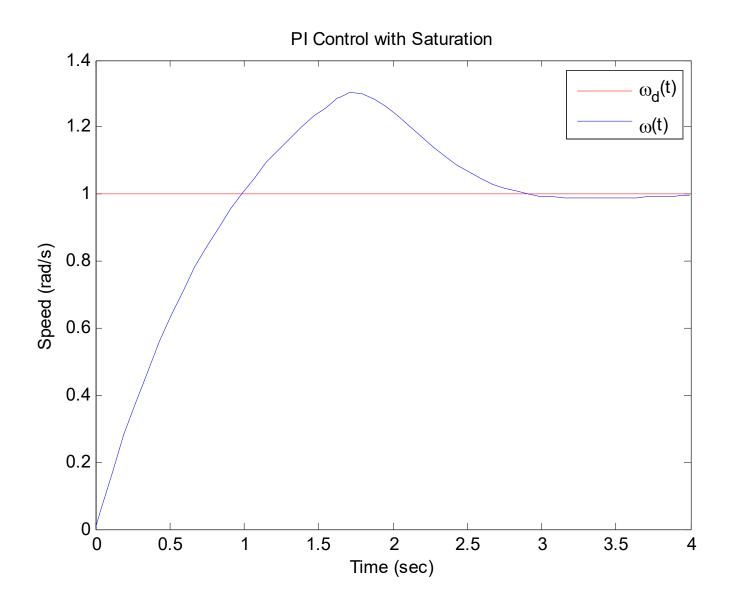
# **PI CONTROL**



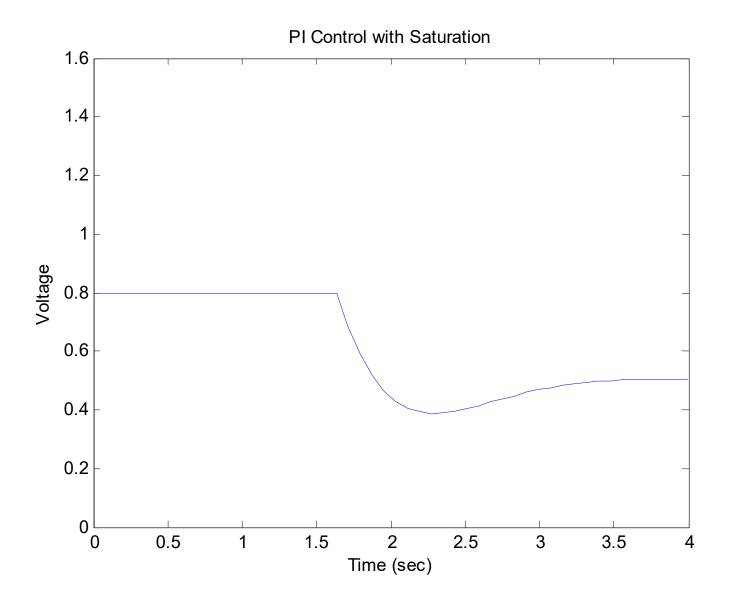
# ADD ACTUATOR SATURATION TO CONTROL LOOP IN SIMULINK



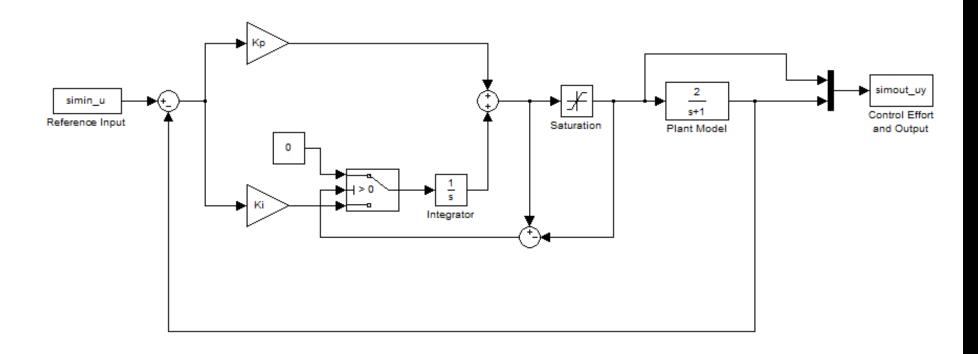
# PI CONTROL WITH SATURATION



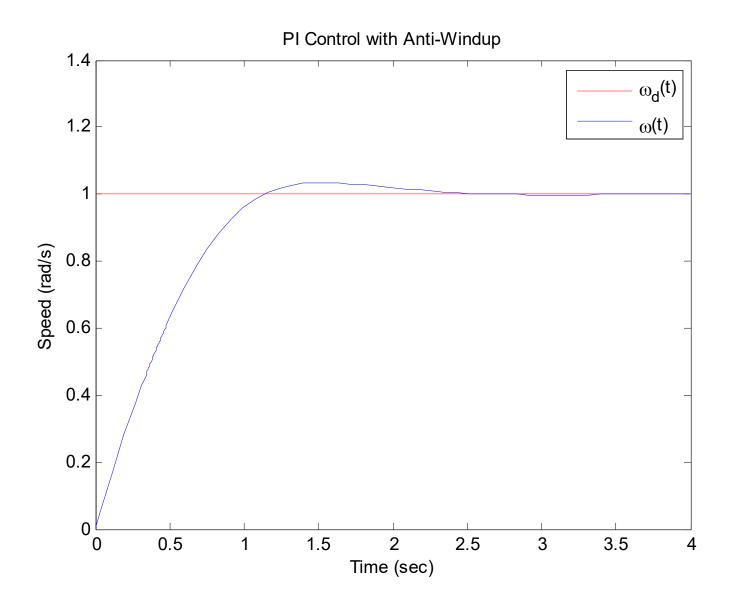
# PI CONTROL WITH SATURATION



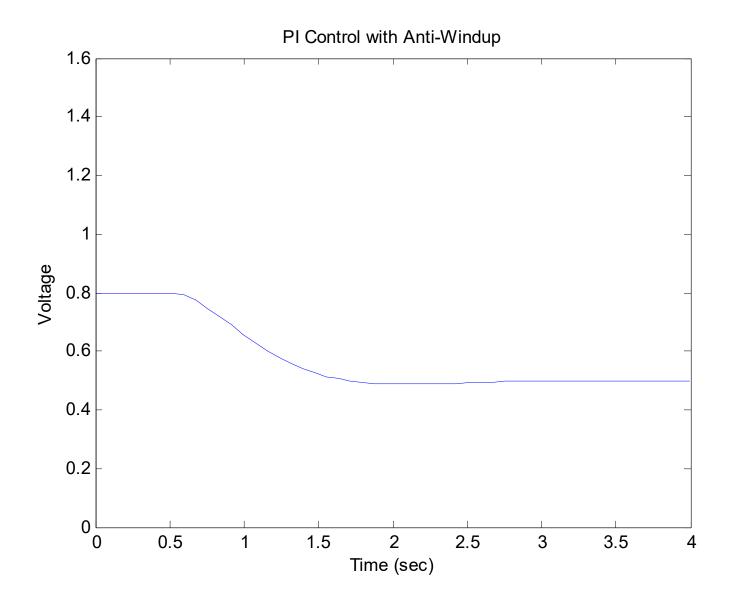
# ADD ANTI-WINDUP MECHANISM TO CONTROL LOOP IN SIMULINK



# PI CONTROL WITH ANTI-WINDUP



# PI CONTROL WITH ANTI-WINDUP



# **COMING UP...**

# **Architectural Issues**

- Internal Model Principle
- Feedforward
- Cascade Control

### **Midterm Exam!**