LAB 6: VerySimpleCPU

What To Do

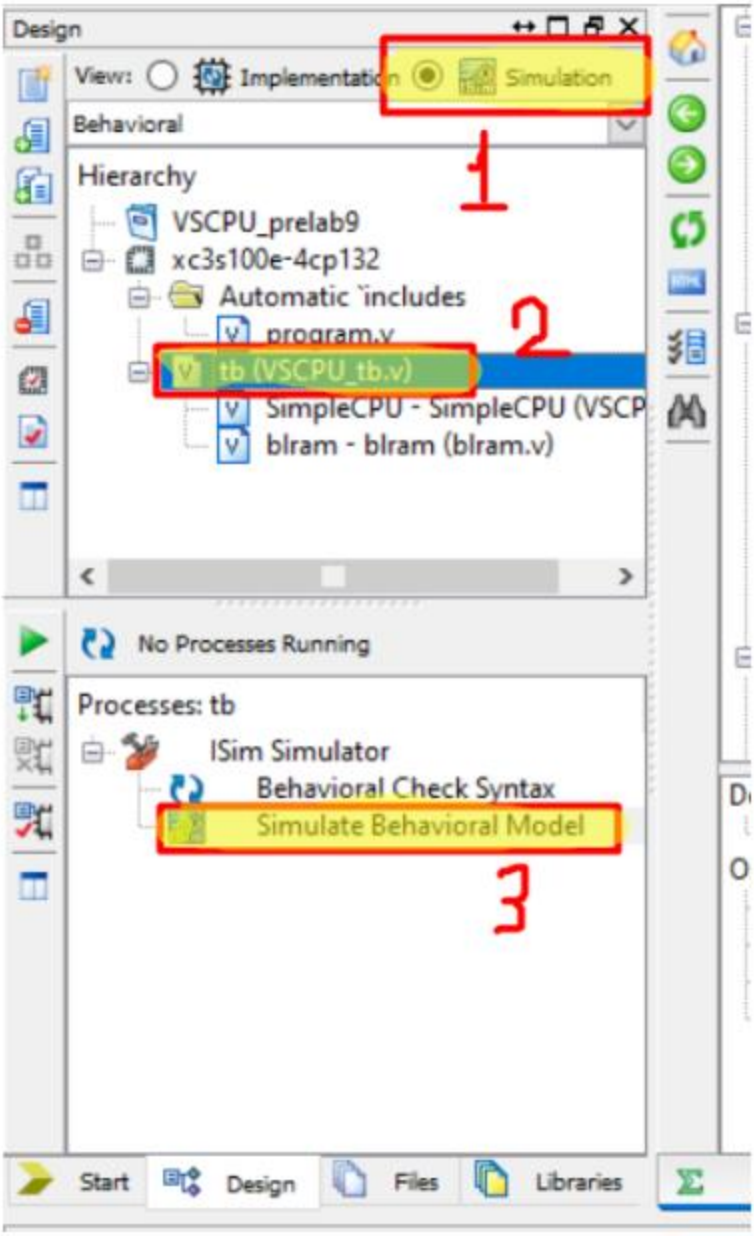
1. Download Lab6 files.
2. Create new project in Xilinx ISE Design Suite, name it “VSCPU_lab6” and add the design files using “add copy of source”. The files are in “VerilogTB” folder. They are: VSCPU_tb.v, blram.v and program.v.
3. Add “VSCPU.v” using “add copy of source” from your “**VSCPU_prelab6**” project folder. Right-click on **“SimpleCPU (VSCPU.v)”** on the left side panel and click on **“Set as Top Module”**.
4. Modify VSCPU.v file so that the CPU can also do **NAND, NANDi, CPI** and **CPIi** instructions. After this, our VSCPU Instruction Set will be complete.
5. Do “Synthesize – XST”. Make sure you get only **trivial warnings** such as below.

```
WARNING:Xst:916 - "SimpleCPU.v" line 22: Delay is ignored for synthesis.
WARNING:Xst:916 - "SimpleCPU.v" line 23: Delay is ignored for synthesis.
WARNING:Xst:916 - "SimpleCPU.v" line 24: Delay is ignored for synthesis.
WARNING:Xst:916 - "SimpleCPU.v" line 25: Delay is ignored for synthesis.
WARNING:Xst:916 - "SimpleCPU.v" line 26: Delay is ignored for synthesis.
WARNING:Xst:915 - Message (916) is reported only 5 times for each module.
WARNING:Xst:643 - "SimpleCPU.v" line 128: The result of a 32x14-bit
multiplication is partially used. Only the 32 least significant bits are used.
If you are doing this on purpose, you may safely ignore this warning.
Otherwise, make sure you are not losing information, leading to unexpected
circuit behavior.
WARNING:Xst:643 - "SimpleCPU.v" line 127: The result of a 32x32-bit
multiplication is partially used. Only the 32 least significant bits are used.
If you are doing this on purpose, you may safely ignore this warning.
Otherwise, make sure you are not losing information, leading to unexpected
circuit behavior.
WARNING:Xst:2677 - Node <Mmult_data_toRAM_mult0002_submult_11> of sequential
type is unconnected in block <SimpleCPU>.
WARNING:Xst:1336 -  (*) More than 100% of Device resources are used
```

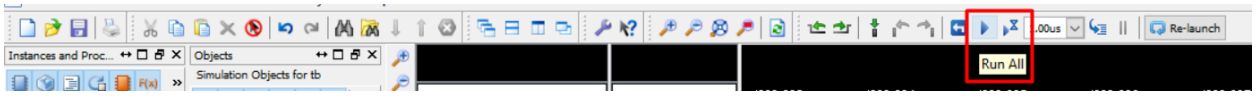
6. After modifying your design, it should be able to run the “test.asm” code given below. Let’s see if it works in the simulation.

0: CP 101 102	105: 3
1: CPi 103 5	106: 5
2: SRL 104 105	107: 35
3: SRL 106 107	108: 6
4: SRLi 108 2	109: 9
5: SRLi 109 36	110: 2
6: NAND 110 111	111: 4
7: NAND 110 110	112: 2
8: NAND 112 113	113: 6
9: NAND 112 112	114: 2
10: NANDi 114 4	115: 2
11: NAND 114 114	116: 3
12: NANDi 115 6	117: 4
13: NAND 115 115	118: 5
14: LT 116 119	119: 4
15: LT 117 119	120: 3
16: LT 118 119	121: 4
17: LTi 120 4	122: 5
18: LTi 121 4	123: 1
19: LTi 122 4	124: 4294967295
20: ADD 123 124	125: 9
21: ADDi 124 1	126: 7
22: MUL 125 126	127: 9
23: MULi 127 3	128: 0
24: BZJ 129 128	129: 26
25: CPi 130 3	130: 2
26: BZJ 132 131	131: 5
27: CPi 133 3	132: 28
28: BZJi 134 3	133: 2
29: CPi 135 3	134: 27
30: CPI 136 137	135: 2
31: CPIi 139 141	136: 4
32: BZJi 33 0	137: 138
33: 32	138: 5
101: 18	139: 140
102: 2	140: 4
103: 12	141: 5
104: 65	

7. Simulate your design by following the figure below.



8. Click on the “Run All” button at the top bar as shown in the figure below.



9. Follow the Waveform window (“Default.wcfg”) and make sure your design is working correctly. Check the console window below and make sure it says “Total Errors 0” and “Simulation Successfuly Completed !!”.
10. Show your work to the T.As.