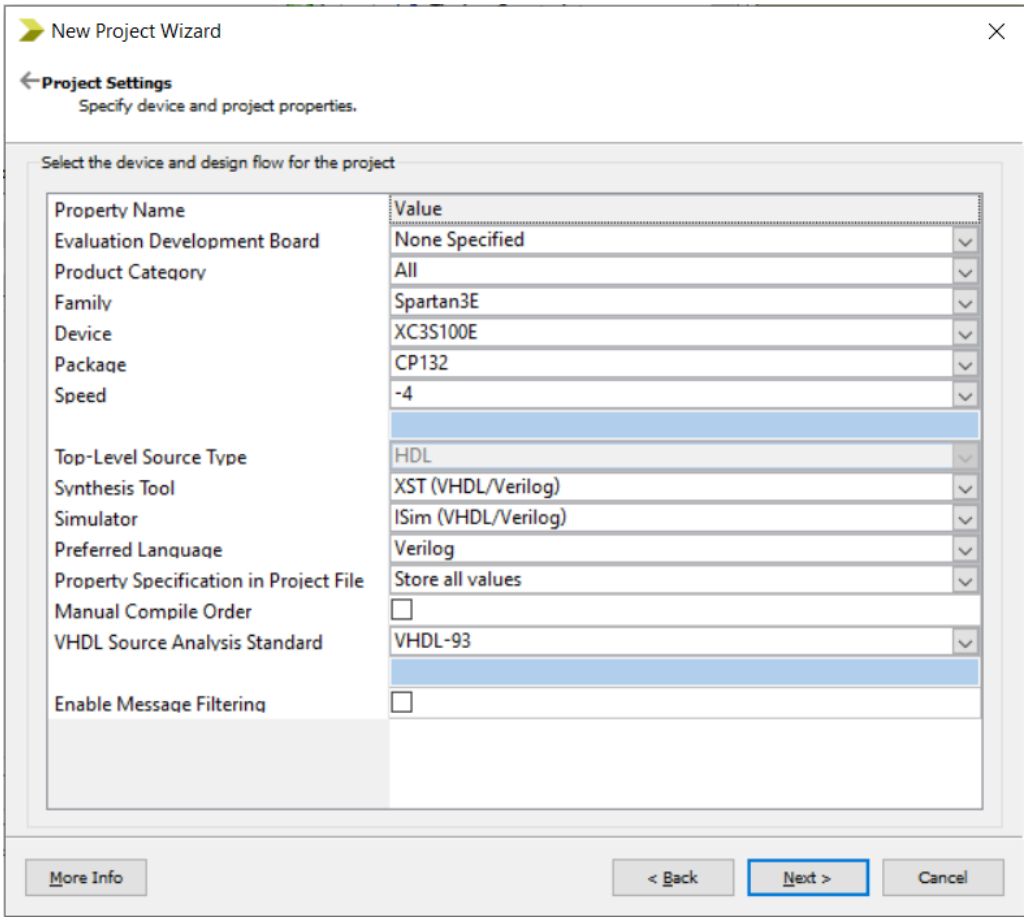
LAB 2

Part 1 – SevenSegFourDig

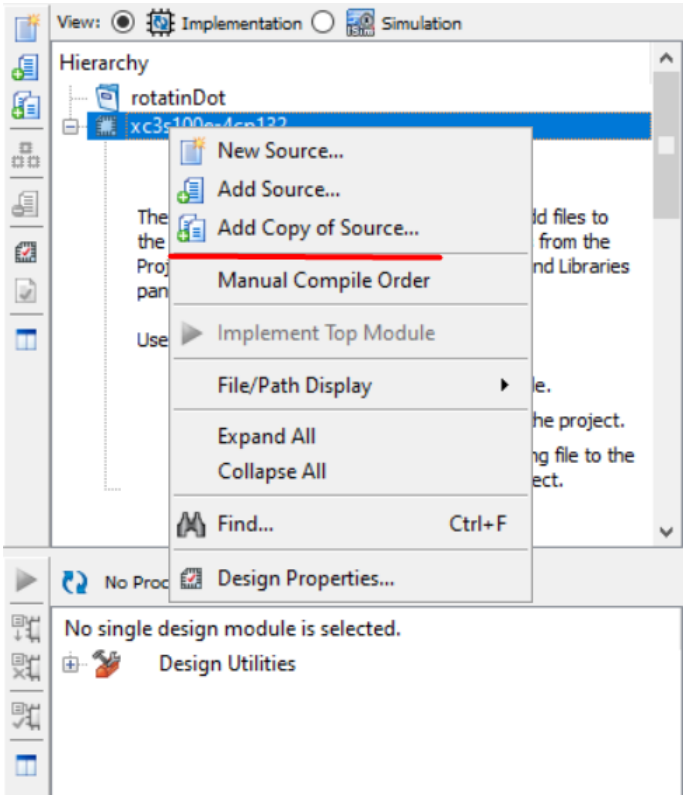
In this part you will modify the SevenSegFourDig.v file given to you so that it synthesizes on Xilinx ISE and runs on the FPGA. The FPGA should be able to display numbers from 0 to 9 and characters from A to F on all four digits. You have also been given a ucf file. DO NOT modify this file.

The SevenSegFourDig module already makes use of the SevenSegOneDig module that you have designed in your prelabs. You will be using your prelab designs in this design.

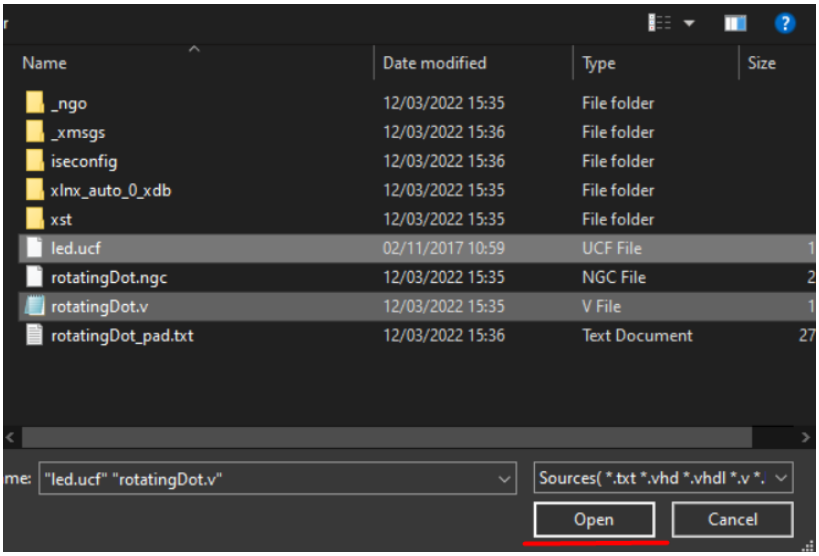
0. Open Xilinx ISE Design Suite and open a New Project. Name the Project "display2022" and choose the "C:/Xilinx/CS240" folder or your own CS240 folder.
1. Click on Next and make sure you have the same configurations chosen in the next window as the ones we have in the figure below.



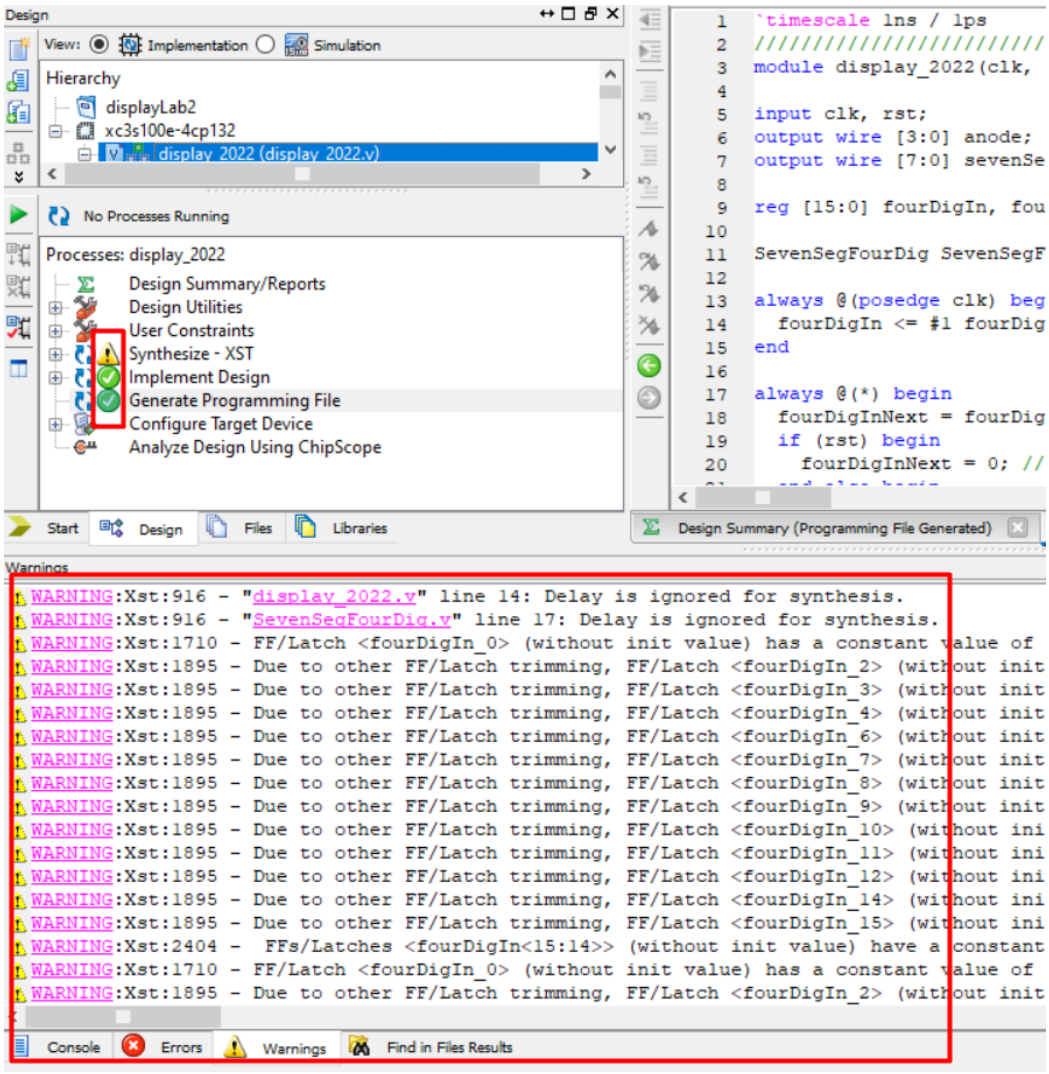
2. Click on Next, and then Next again.
3. Like in the image below, right click on "xc3s100e-4cp132" and click on "Add Copy of Source".



4. Find the display_2022.v, SevenSegFourDig.v and display_top.ucf files and choose them, and click on “Open”, like in the figure below. Note that to choose multiple files, you can press “ctrl” key and click on those files.



5. Redo step 3 and this time, find your prelab file which is SevenSegOneDig.v, and add it to your project like you did in step 4.
6. Modify SevenSegFourDig.v so that when you program your FPGA, you will be able to see digits on the Seven Segment Displays.
7. Click on “Generate Programming File” on the left bottom panel. Make sure you have the same result as is shown in the figure below.



8. Get your FPGA and upload your project to the FPGA using Digilent Adept.
9. Show us your work before you go on to the next part.

Part 2 – Display

In this part you will modify the display_top.v file given to you so that it synthesizes on Xilinx ISE and runs on the FPGA. You are going to be using SevenSegFourDig.v you completed in Part 1, SevenSegOneDig.v that you have done in your prelab, and also the display_top.ucf.

0. Open a New Project and name it “display”. Follow the same instructions as Part 1. Click on “Add Copy of Source” to add “display_top.v”, “SevenSegFourDig.v”, “SevenSegOneDig.v” and “display_top.ucf”.
1. Modify display_top.v so that the Seven Segment Displays will show numbers from 0 to 3, according to the switches. The leftmost Seven Segment should show the decimal value of sw[7:6], the second leftmost should show the decimal value of sw[5:4], and so on.
2. Click on “Generate Programming File” on the left bottom panel. Make sure you have the same result as is shown in the figure in Part 1.
3. Get your FPGA and upload your project to the FPGA using Digilent Adept.
4. Show us your work.