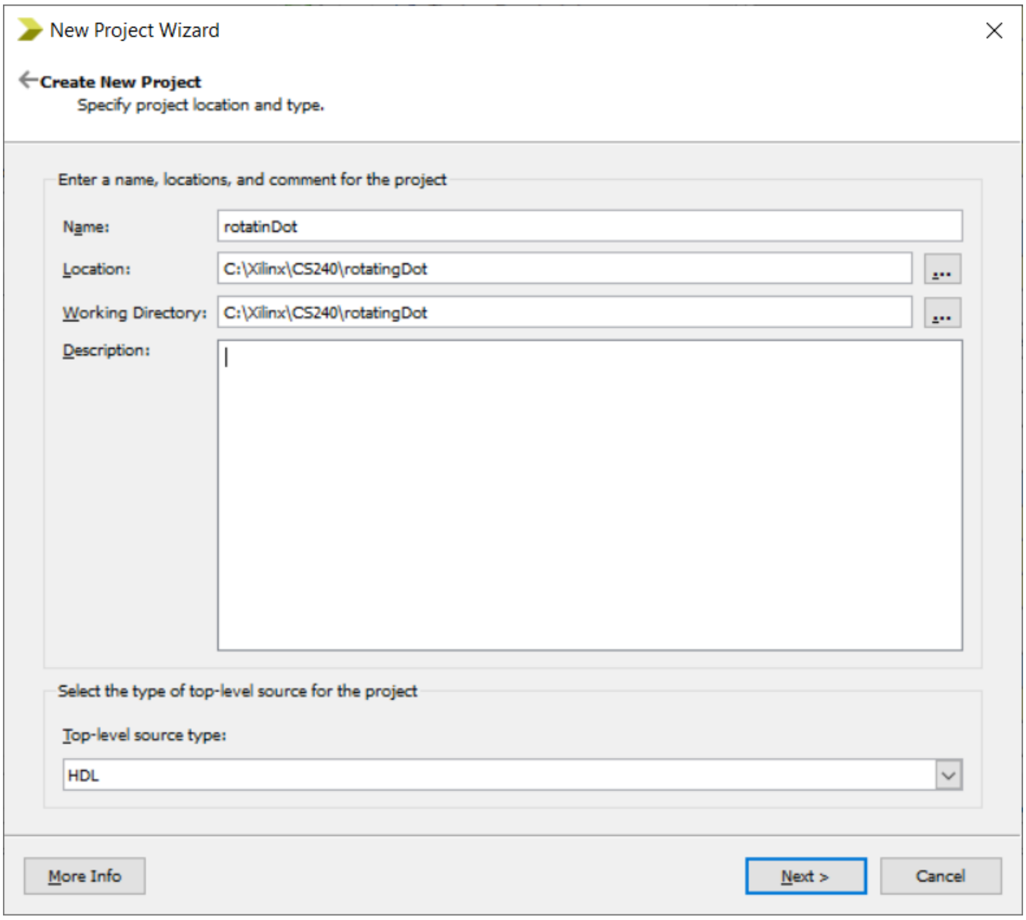
LAB 1

Part 1 – RotatingDot

In this part you will modify the rotatingDot.v file given to you so that it synthesizes on Xilinx ISE and runs on the FPGA. The FPGA should display LEDs lighting up from left to right and then looping back. You have also been given a led.ucf file. DO NOT modify this file.

0. Create a new folder in C:\Xilinx and name it CS240.
1. Open Xilinx ISE Design Suite and open a New Project. Name the Project "rotatingDot" and choose the folder you have opened in step 0, like in the figure below.


New Project Wizard
Create New Project
Specify project location and type.
Enter a name, locations, and comment for the project
Select the type of top-level source for the project
More Info
Next >
Cancel

Name: rotatinDot

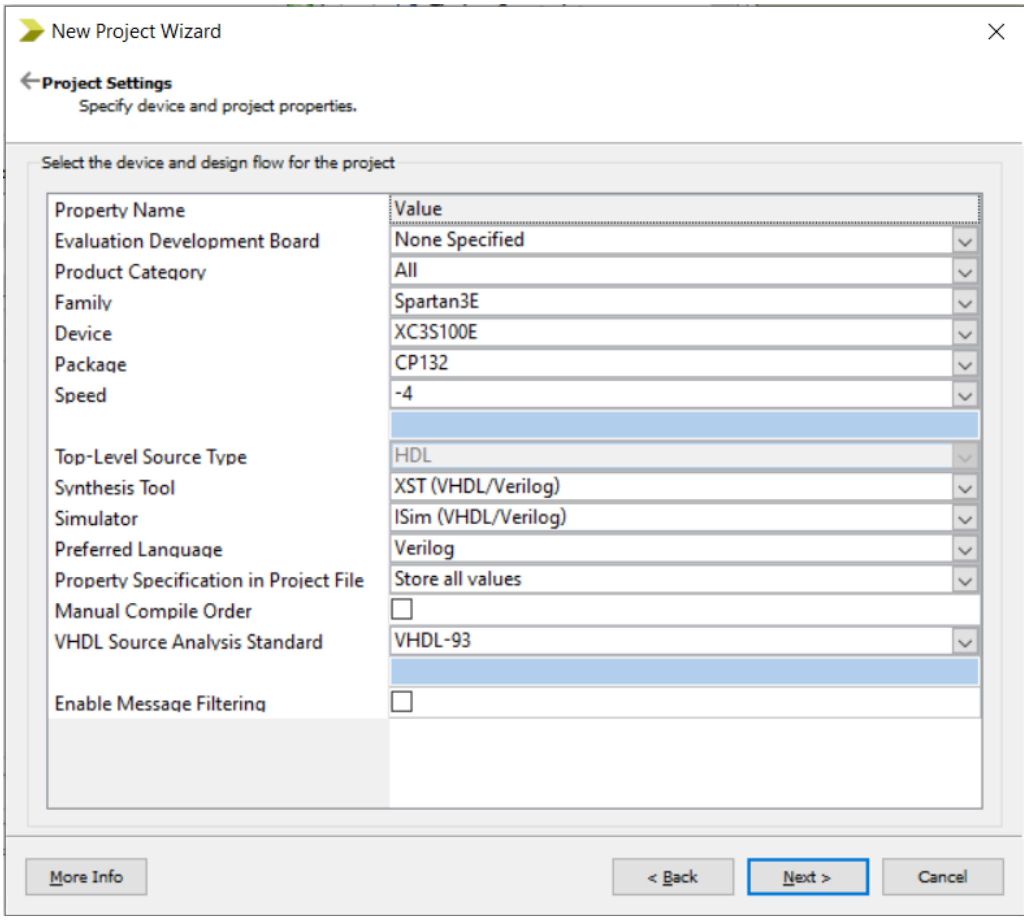
Location: C:\Xilinx\CS240\rotatingDot

Working Directory: C:\Xilinx\CS240\rotatingDot

Description:

Top-level source type: HDL

2. Click on Next and make sure you have the same configurations chosen in the next window as the ones we have in the figure below.



New Project Wizard

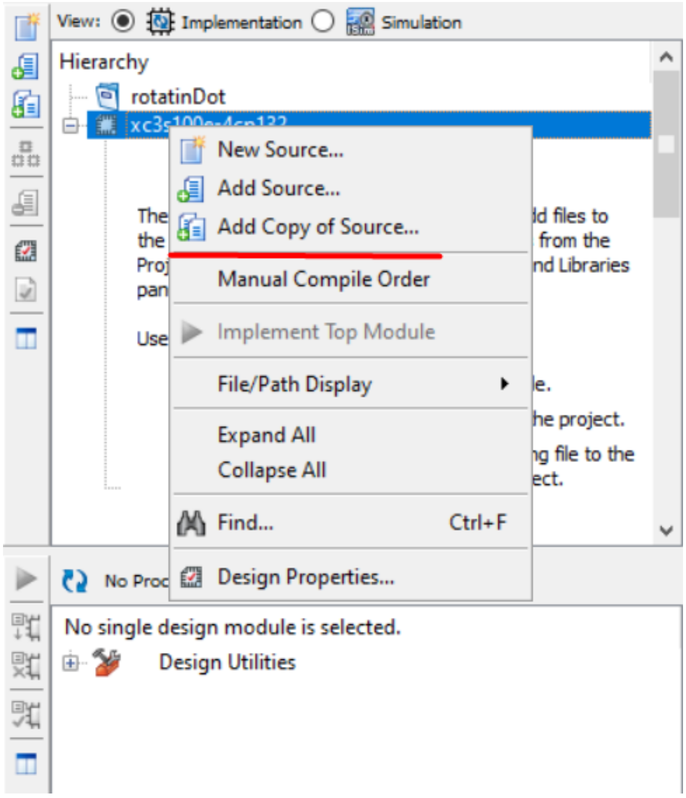
Project Settings

Specify device and project properties.

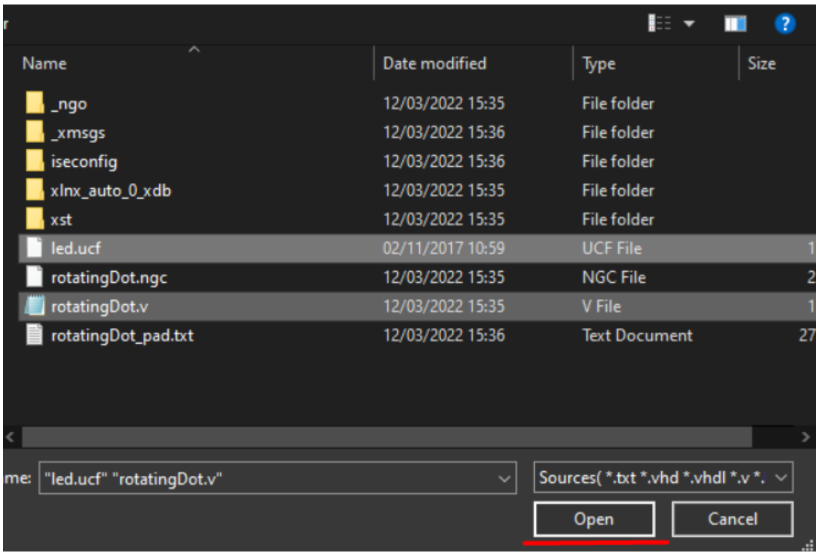
Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S100E
Package	CP132
Speed	-4
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	□
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	□

3. Click on Next, and then Next again.
4. Like in the image below, right click on “xc3s100e-4cp132” and click on “Add Copy of Source”.



5. Find the rotatingDot.v and led.ucf and choose them, and click on “Open”, like in the figure below. Note that to choose multiple files, you can press “ctrl” key and click on those files.

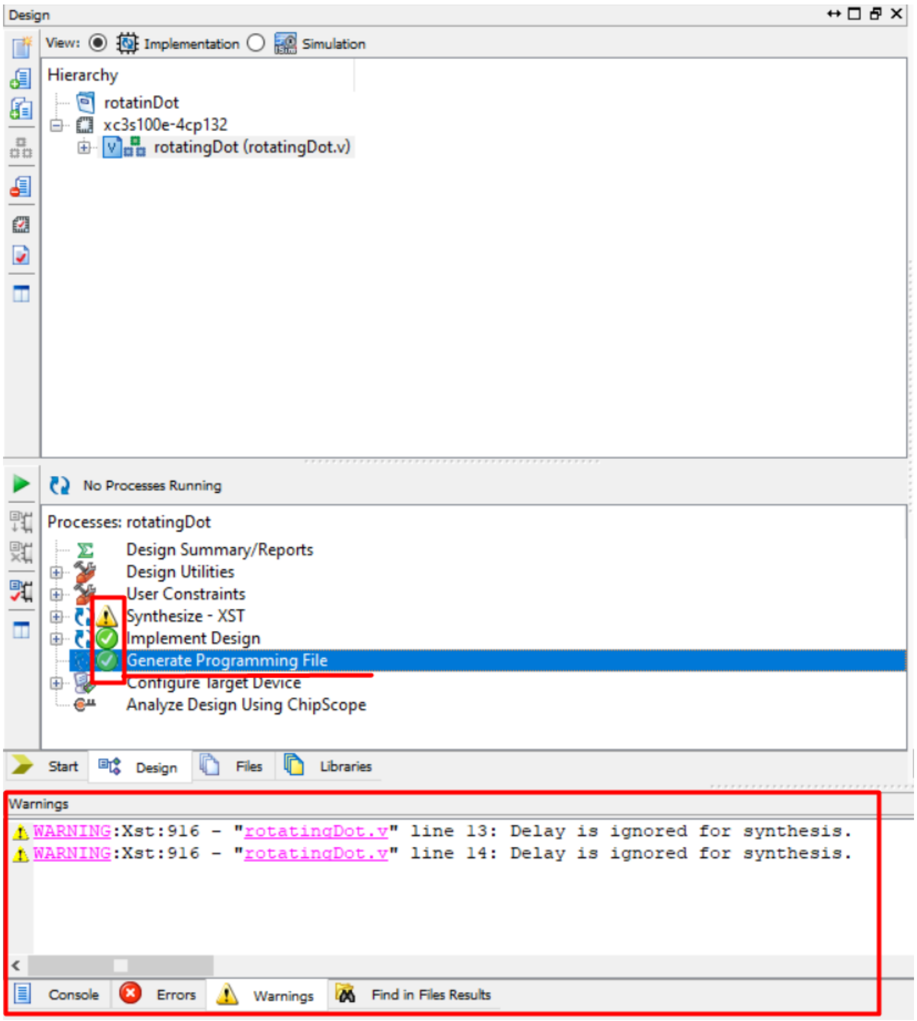


Name	Date modified	Type	Size
_ngo	12/03/2022 15:35	File folder	
_xmsgs	12/03/2022 15:36	File folder	
iseconfig	12/03/2022 15:36	File folder	
xlnx_auto_0_xdb	12/03/2022 15:35	File folder	
xst	12/03/2022 15:35	File folder	
led.ucf	02/11/2017 10:59	UCF File	1
rotatingDot.ngc	12/03/2022 15:35	NGC File	2
rotatingDot.v	12/03/2022 15:35	V File	1
rotatingDot_pad.txt	12/03/2022 15:36	Text Document	27

me: "led.ucf" "rotatingDot.v"

Sources(*.txt *.vhd *.vhdl *.v *.

6. Modify rotatingDot.v so that it displays LEDs lighting up from left to right and then goes to the leftmost one again.
7. Click on “Generate Programming File” on the left bottom panel. Make sure you have the same result as is shown in the figure below.



```
WARNING:Xst:916 - "rotatingDot.v" line 13: Delay is ignored for synthesis.
WARNING:Xst:916 - "rotatingDot.v" line 14: Delay is ignored for synthesis.
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8. Get your FPGA and upload your project to the FPGA using Digilent Adept. Have a look at CS240-Adept.pdf to learn how to do this.
9. Show us your work before you go on to the next part.

Part 2 – KnightRider

In this part you will modify the knightRider.v file given to you so that it synthesizes on Xilinx ISE and runs on the FPGA. You are going to be using the led.ucf file again.

0. Open a New Project and name it “knightRider”. Follow the same instructions as Part 1. Click on “Add Copy of Source” to add “knightRider.v” and “led.ucf”.
1. Modify knightRider.v so that it makes LEDs light up from left to right and when it reaches the rightmost one, it lights them up from right to left, and again when it reaches the leftmost one, it lights them up from left to right, and so on.
2. Click on “Generate Programming File” on the left bottom panel. Make sure you have the same result as is shown in the figure in Part 1.
3. Get your FPGA and upload your project to the FPGA using Digilent Adept.
4. Show us your work before you go on to the next part.

Part 3 – Modified KnightRider

In this part you are expected to modify knightRider.v, so that now we have two smaller knightRiders that will light up from left and right and then they will meet in the middle and then go back to their respective corners.

0. Open a New Project and name it “knightRider_modified”. Click on “Add Copy of Source” to copy “led.ucf” to the project.
1. Right click on “xc3s100e-4cp132” and click on “Add New Source”. Choose “Verilog Module” and write “knightRider_modified” as the File name. Click on Next, then Next, and then Finish.
2. Copy the contents of your knightRider.v to this file and make sure the module name is “knightRider_modified”
3. Modify your .v file as required.
4. Click on “Generate Programming File” on the left bottom panel. Make sure you have the same result as is shown in the figure in Part 1.
5. Get your FPGA and upload your project to the FPGA using Digilent Adept.
6. Show us your work before you go on to the next part.