LAB 5: Introduction to VerySimpleCPU Design

Part 1

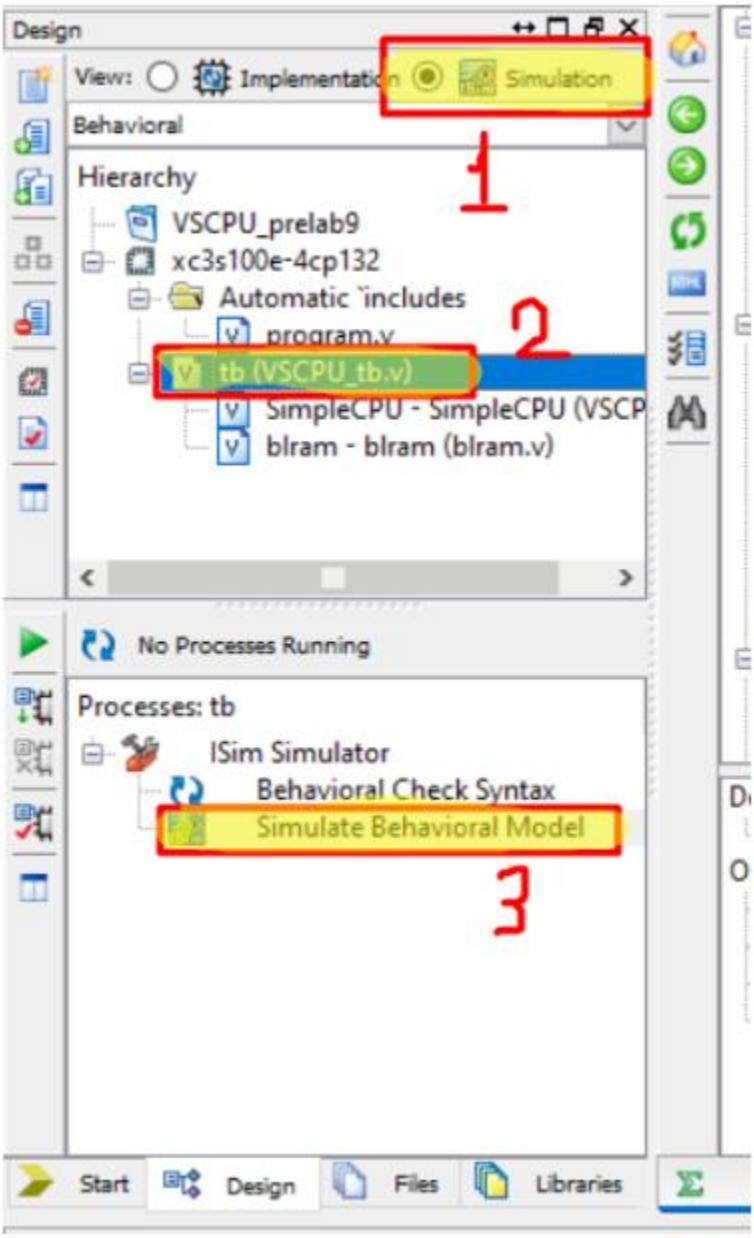
1. Download Lab5 files.
2. Create new project in Xilinx ISE Design Suite, name it "VSCPU_lab5_part1" and add the design files using "add copy of source". The files are in "VerilogTB/lab5_part1" folder. They are: VSCPU_tb.v, blram.v and program.v.
3. Add "VSCPU.v" using "add copy of source" from your "**VSCPU_prelab5**" project folder. Right-click on **"SimpleCPU (VSCPU.v)"** on the left side panel and click on **"Set as Top Module"**.
4. Modify VSCPU.v file so that the CPU can also do **CP** and **CPi** instructions.
5. Do "Synthesize – XST". Make sure you get only **trivial warnings** such as below.

```
WARNING:Xst:916 - "VSCPU.v" line 22: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 23: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 24: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 25: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 26: Delay is ignored for synthesis.
WARNING:Xst:915 - Message (916) is reported only 5 times for each module.
WARNING:Xst:646 – Signal <num2> is assigned but never used. This unconnected signal
will be trimmed during the optimization process.
WARNING:Xst:1336 - (*) More than 100% of Device resources are used
```

6. After modifying your design, it should be able to run the "lab5_part1.asm" code given below. Let's see if it works in the simulation.

```
0: ADD 12 15
1: ADDi 12 20
2: BZJ 3 5
3: 7

5: 0

7: BZJ 3 12
8: CP 40 50
9: CPi 100 20
10: BZJi 11 0
11: 10
12: 0

15: 2

20: 3

50: 100

100: 200
```

7. Simulate your design by following the figure below.



8. Follow the Waveform window (“Default.wcfg”) and make sure your design is working correctly. Check the console window below and make sure it says “Total Errors 0” and “Simulation Successfuly Completed !!”.
9. Show your work to the T.As.

Part 2

1. Create new project in Xilinx ISE Design Suite, name it "VSCPU_lab5_part2" and add the design files using "add copy of source". The files are in "VerilogTB/lab5_part2" folder. They are: VSCPU_tb.v, blram.v and program.v.
2. Add "VSCPU.v" using "add copy of source" from your "**VSCPU_lab5_part1**" project folder. Right-click on **"SimpleCPU (VSCPU.v)"** on the left side panel and click on **"Set as Top Module"**.
3. Modify VSCPU.v file so that the CPU can also do **SRL** and **SRLi** instructions.
4. Do "Synthesize – XST". Make sure you get only **trivial warnings** such as below.

```
WARNING:Xst:916 - "VSCPU.v" line 22: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 23: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 24: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 25: Delay is ignored for synthesis.
WARNING:Xst:916 - "VSCPU.v" line 26: Delay is ignored for synthesis.
WARNING:Xst:915 - Message (916) is reported only 5 times for each module.
WARNING:Xst:646 – Signal <num2> is assigned but never used. This unconnected signal
will be trimmed during the optimization process.
WARNING:Xst:1336 - (*) More than 100% of Device resources are used
```

5. After modifying your design, it should be able to run the "lab5_part2.asm" code given below. Let's see if it works in the simulation.

```
0: ADD 12 15
1: ADDi 12 20
2: BZJ 3 5
3: 7

5: 0

7: BZJ 3 12
8: CP 60 50
9: CPi 100 20
10: BZJi 11 20
11: 10
12: 0

15: 2

20: 3
```

```
30: SRL 40 41
31: SRL 42 43
32: SRLi 44 2
33: SRLi 45 36
34: BZJi 35 0
35: 34

40: 65
41: 3
42: 5
43: 35
44: 6
45: 9

50: 100

100: 200
```

6. Follow the Waveform window (“Default.wcfg”) and make sure your design is working correctly. Check the console window below and make sure it says “Total Errors 0” and “Simulation Successfuly Completed !!”.
7. Show your work to the T.As.