Readout IC for Compute-in-Memory (ROIC-CIM)

Chip Odyssey
Chipathon 2025

Introduction

The rapid development in AI (Artificial Intelligence) has piqued interest of many in semiconductor chips and and neural networks. Through this proposal we are offering the neural network enthusiasts and learners an opportunity to explore and test the neural network functionality using the analog computing.

We propose the basic concept of a dot product through analog computing and demonstrates each building blocks to the MOSbius users.

Team Odyssey Members and Fossi Ids

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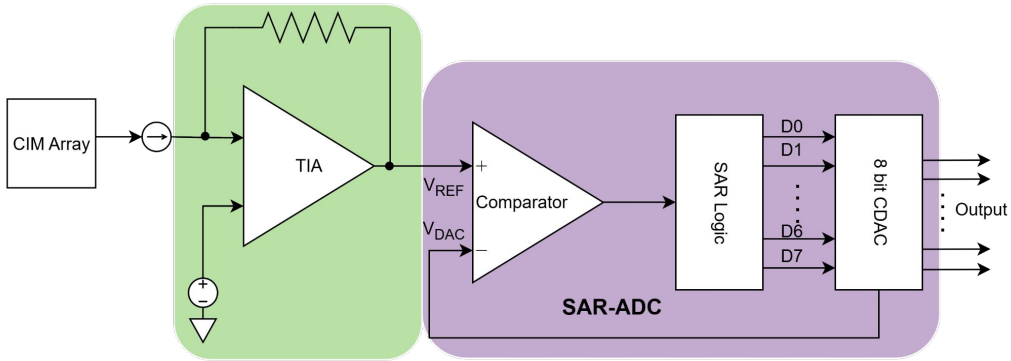
Block Diagram

The proposed system comprises an OPAMP, and a SAR-ADC containing a comparator, SAR Logic, a capacitive DAC and output buffers

SAR-ADC uses a single comparator and performs a one-bit comparison only in one internal clock, bit-by-bit

A capacitive DAC array with charge distribution generates analog reference voltage [1]



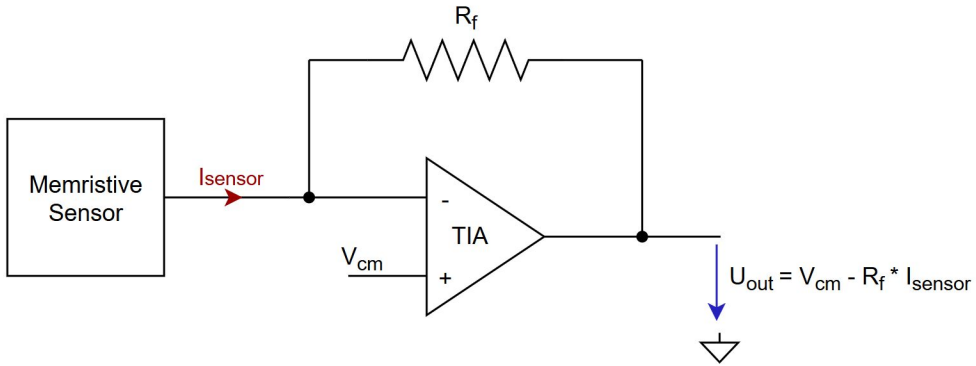
The same DAC can also be added to write memory array [2].

Specifications

Block	Parameter	Value
TIA/opAmp	DC Supply	3.3 V
	Input Driving Current	1nA- 100uA
	Linearity	To support 8 bits precision
ADC (SAR)	Resolution	6-8 bits
	Frequency	250-500 KHz
	DC supply for ADC	1.2V (will explore flavour of mos transistor)
DAC (Capacitive)	resolution	6-8 bits

OP AMP / TIA

- Input current originates from an external memristive sensor
- Common mode voltage is set by an external power supply
- Feedback resistor (Rf) is implemented internally on-chip



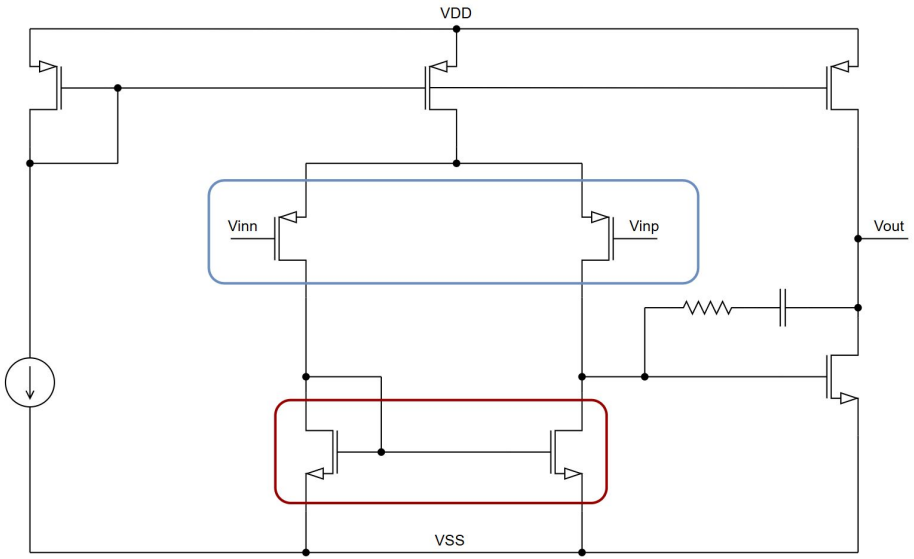
MOSBius style Amplifier

The load can be modified:

- Simple current mirror
- Cross-coupled Pair
- Cascode current mirror

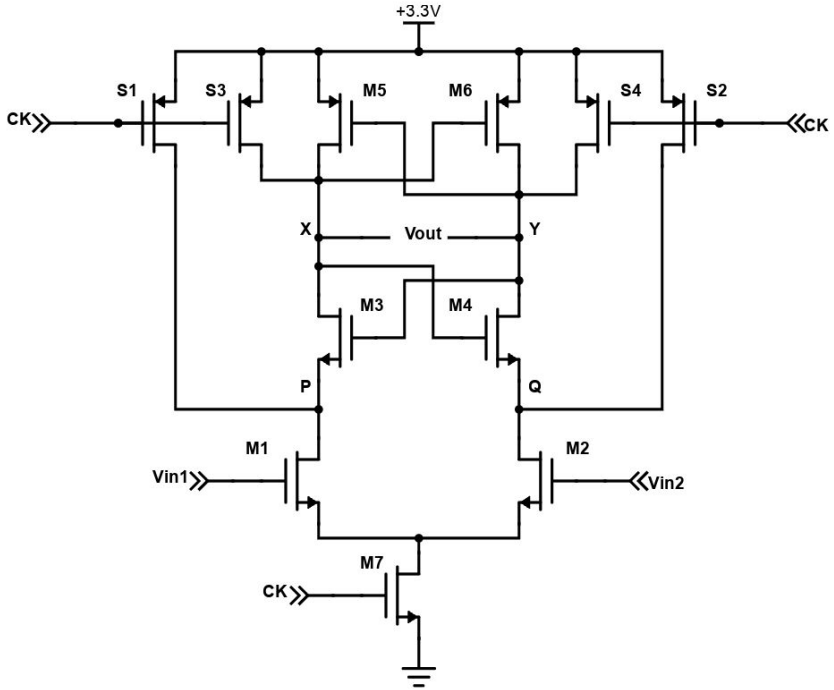
Differential pair:

- Possibility to implement cascodes
- Different inversion levels: s.i m.i w.i



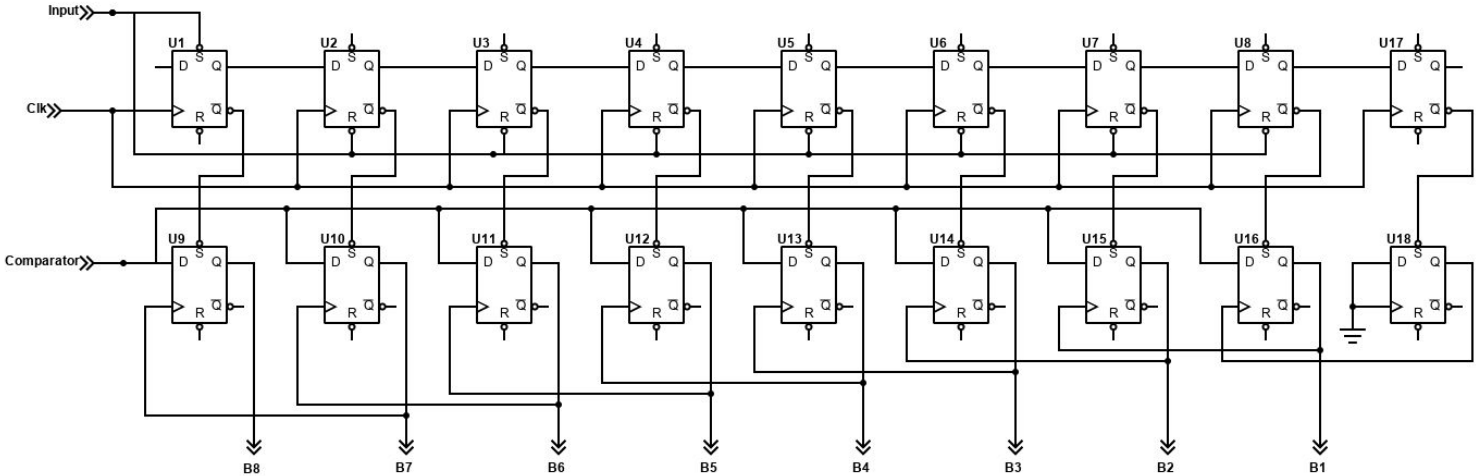
Comparator

- Standard StrongArm latch comparator design [3]
- This design will have a lot of kickback and offset noise that will need to be taken into account
  - It is still acceptable for such 8-bit medium resolution ADC
  - If issues persist, other mitigation strategies will be implemented



Input Offset	Clock Freq	Power	Kickback Noise
< 5mV	> 5 MHz	< 2mW	< 200uA

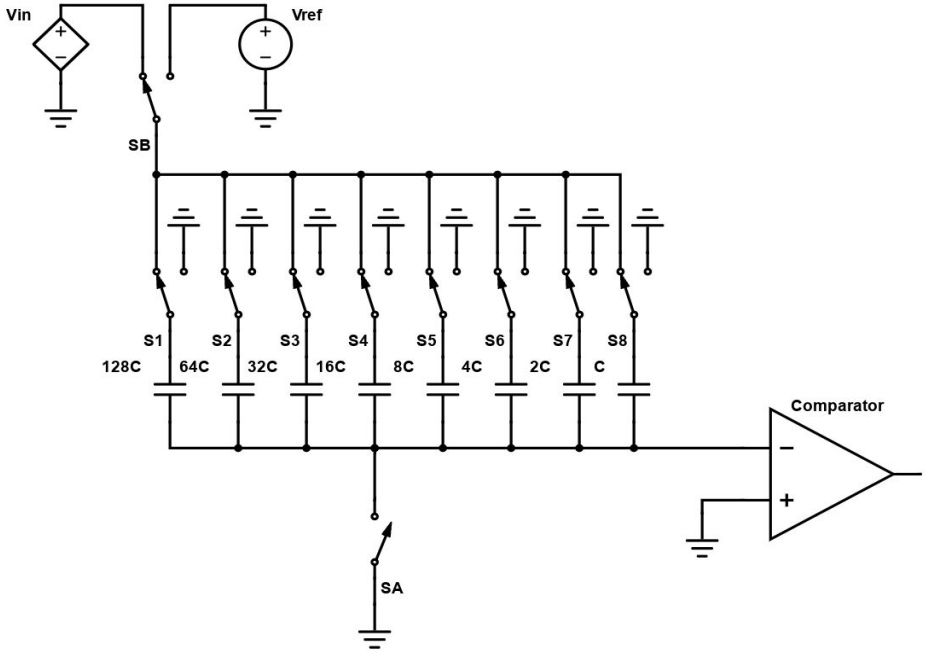
SAR Logic



- Standard 8-bit SAR logic with flip flops
- Will probably need a custom flip flop for proper clocking and set

C-DAC

- Vref=3.3 V since the supply voltage will be 3.3V
- Vin can vary between 12.9 mV to 3.3 V since it is an 8-bit DAC with max at Vref
- Use unit cell capacitors for better matching and layout
- Can use a 2-input MUX for the SPDT switches
- Can use a transmission gate for the SA sample switch



Bits	INL	DNL	Clock Frequency	Switching Efficiency
8	< 1 LSB	<1 LSB	250 kHz	> 15%

Testing the TIA

- Linearity
- Gain
- Stability
- Noise
- Offset

Testing the ADC

- Send an analog signal and route the 8-bit output to a simple R-2R ladder based DAC off chip on a PCB and measure the output
  - Verify that the signal is similar to the input (oscilloscope)
  - Measure SNR (spectrum analyzer)
  - Measure SFDR (spectrum analyzer)
  - Measure ENOB (spectrum analyzer)
  - Measure INL
  - Measure DNL
- Equipment Needed:
  - Oscilloscope
  - Signal generator
  - Low noise power supply
  - Spectrum analyzer
  - PCB with R-2R ladder DAC

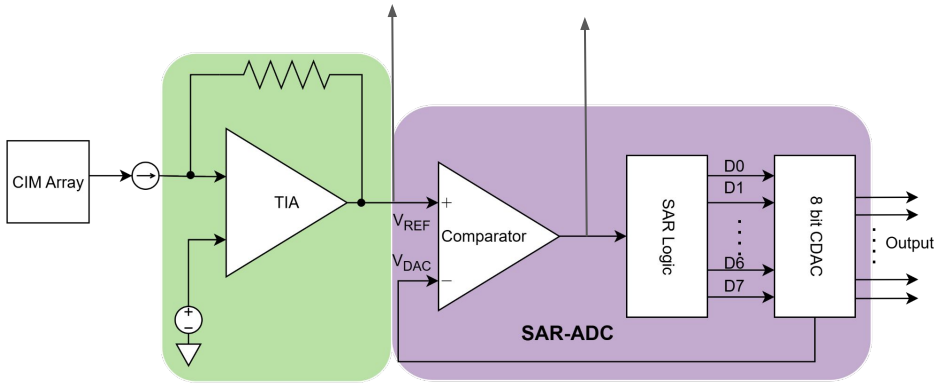
ROIC Measurement Setup

- Find some single cell diode or memristive current based sensor (can be a column of them too) as the input to the ROIC
- List of Tests:
  - TIA test and making sure all the current readouts are accurate
  - Only ADC comparator test and verifying speed and accuracy
  - Only C-DAC test and verifying speed and accuracy
  - Entire ADC
  - Entire integration test
- Equipment Needed:
  - Maybe FPGA for processing the digital output and verifying complete operation
  - PCB with R-2R ladder based DAC and measuring output changes
  - Oscilloscope
  - Signal generator
  - Low noise power supply
  - Spectrum analyzer

Pin Outs

					20	19	18	17	16										
					Memory_out	ADC_out	ADC_Vreference	ADC_Comparator_Clk	ADC_Comparator_Clk2										
1	Memory_In														ADC_reset	15
2	DAC_out														Ground_digital	14
3	TIA_bias						ROIC_CIM								1.2V_Digital	13
4	TIA_out														ADC_clk	12
5	3.3V_Analog														DAC_in	11
					1.2V_Analog	Ground_Analog	Comparator_out	TBA	TBA										
					6	7	8	9	10										

Pins: Expected about 14-20
IO pins



Team Members and Work Distribution

- TIA Current Sense - Schematic and Layout
  - Rahul, Fabian Schenzle
- 8-bit ADC - Schematic and Layout
  - C-DAC: Nitin Indukuri + Mia Kadam
  - Comparator: Kevin Oviedo + Nitin Indukuri
  - SAR Logic: Kevin Oviedo + Emmanuel Innocent
- Switch Matrix
  - Everyone
- Top integration and GDS
  - Everyone

Schedule

Week	TIA-Current Sense	ADC: C-DAC	ADC: Comparator	ADC: SAR Logic	Switch Matrix	Top Integration
27	Team formation, tool installation and internal proposal discussion					
28	Final Proposal (public) and tools hands-on					
29	Topology selection, schematic design optimization and simulation (internal)				-	-
30					-	-
31	Prepare and present schematic review (public)				-	-
32	Simulations review (public) and top schematic integration (internal)				-	Schematic
33	Top simulation review				-	Schematic

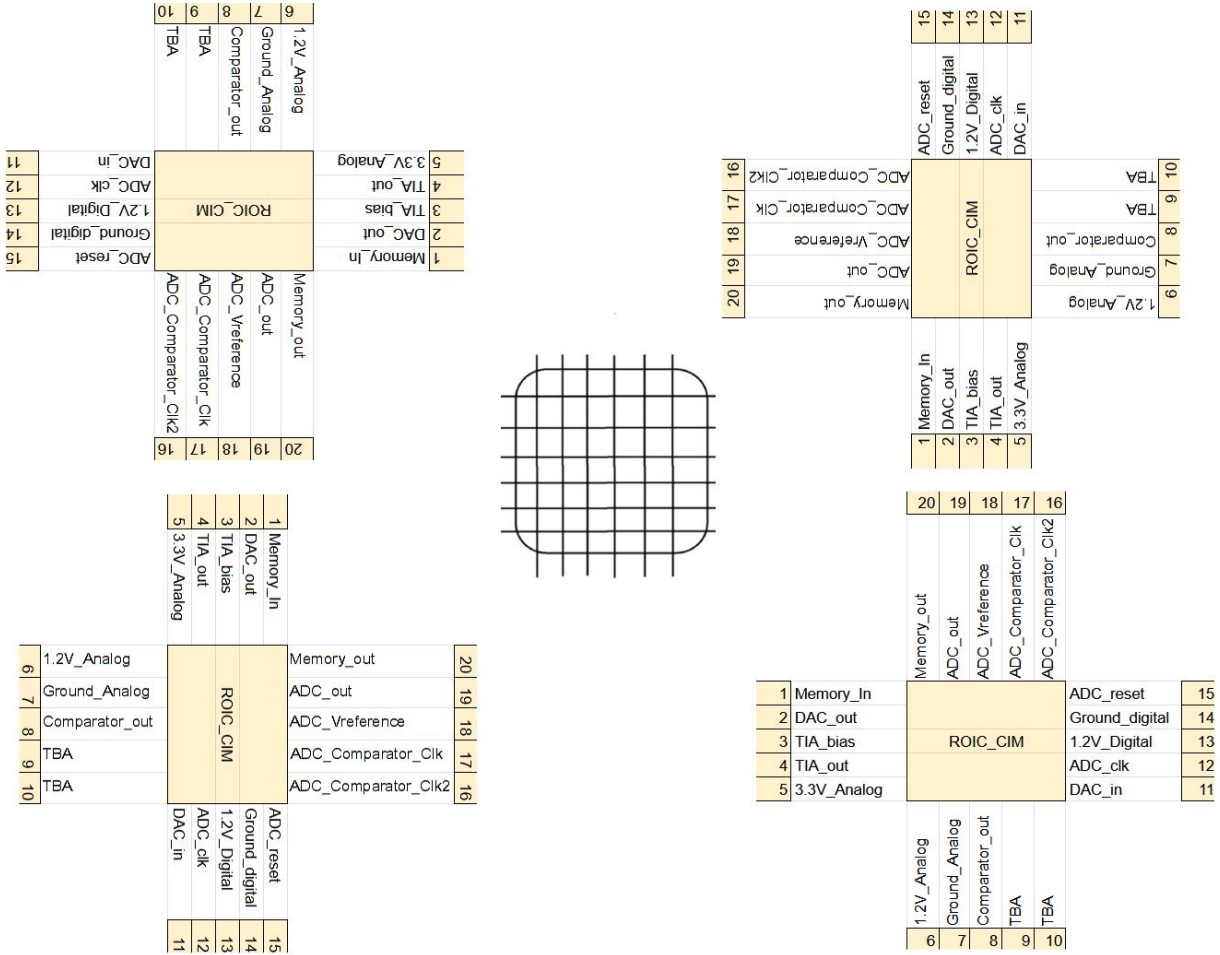
Schedule

Week	TIA-Current Sense	ADC: C-DAC	ADC: Comparator	ADC: SAR Logic	Switch Matrix	Top Integration
34	If any, final adjustments, cell layout				TBD	Floor Plan
35	Layout finalization of each cells, DRC and review (internal)				TBD	Adjustments
36	Layout review (public)				TBD	Layout
37	Top layout review (public)					
38	Post layout verification top level					
39	Final chip review (public) and GDS submission					
40	Closure					

Future work

1- Testing a single chain for read and write operation.

2- Use 4 nos. of this die to drive a 4x4 memory bar (memristor)



References

1. Jiang, H., Huang, S., Yu, S. (2025). Compute-in-Memory Architecture. In: Chattopadhyay, A. (eds) Handbook of Computer Architecture. Springer, Singapore.
2. Anugerah Firdauzi *et al*.,”Power Efficient Current-Mode SAR ADC for Memristor Readout in 28 nm CMOS”, IEEE ICECS, 2024.
3. B. Razavi, "The Design of a Comparator [The Analog Mind]," in IEEE Solid-State Circuits Magazine, vol. 12, no. 4, pp. 8-14, Fall 2020