Readout IC for Compute-in-Memory (ROIC-CIM) Schematic Review

Chip Odyssey
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Team Odyssey Members and Fossi Ids

Mia Kadam (meghanakadam)

Fabian Schenzle (fab1an)

Emmanuel (insightful_sherlock)

Kevin (kejor)

Rahul Sharma (rahul.shsr)

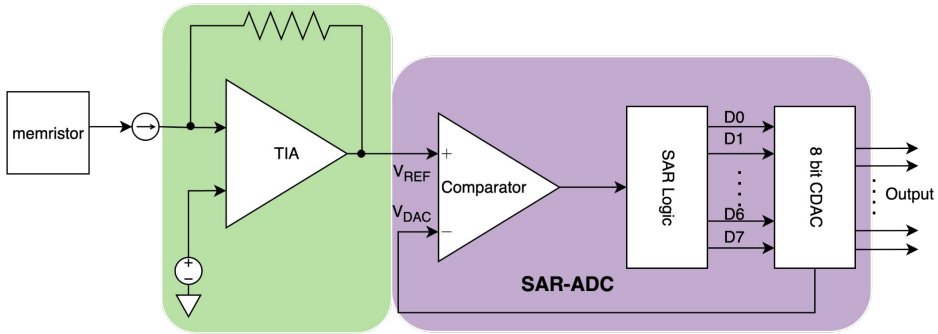
Nitin Indukuri (nindukuri)

Block Diagram

The proposed system comprises an OPAMP, and a SAR-ADC containing a comparator, SAR Logic, a capacitive DAC and output buffers

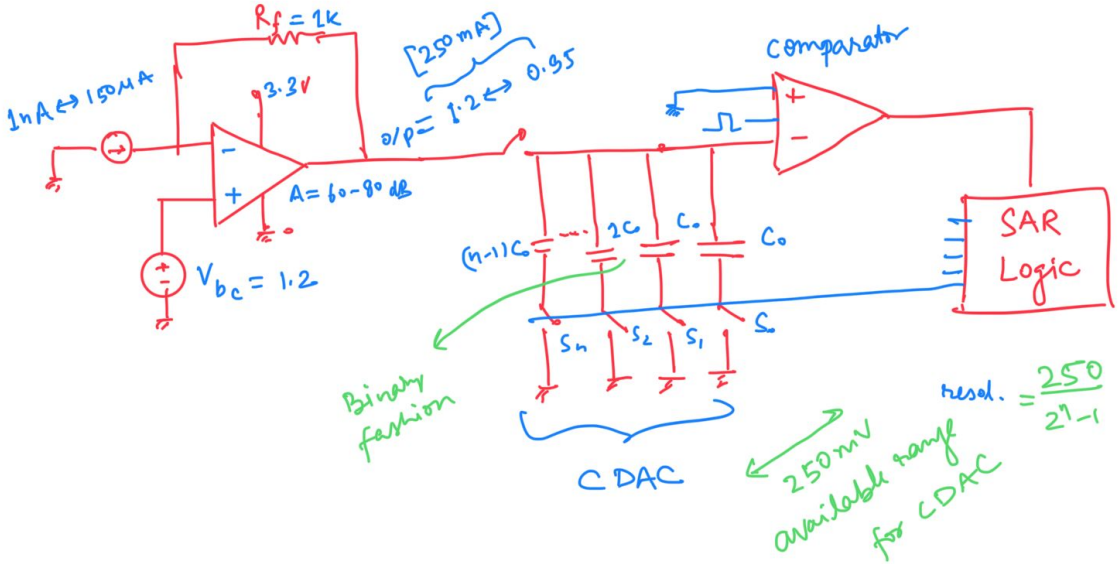
SAR-ADC uses a single comparator and performs a one-bit comparison only in one internal clock, bit-by-bit

A capacitive DAC array with charge distribution generates analog reference voltage [1]



The same DAC can also be added to write memory array [2].

Full Signal Chain and System Specs

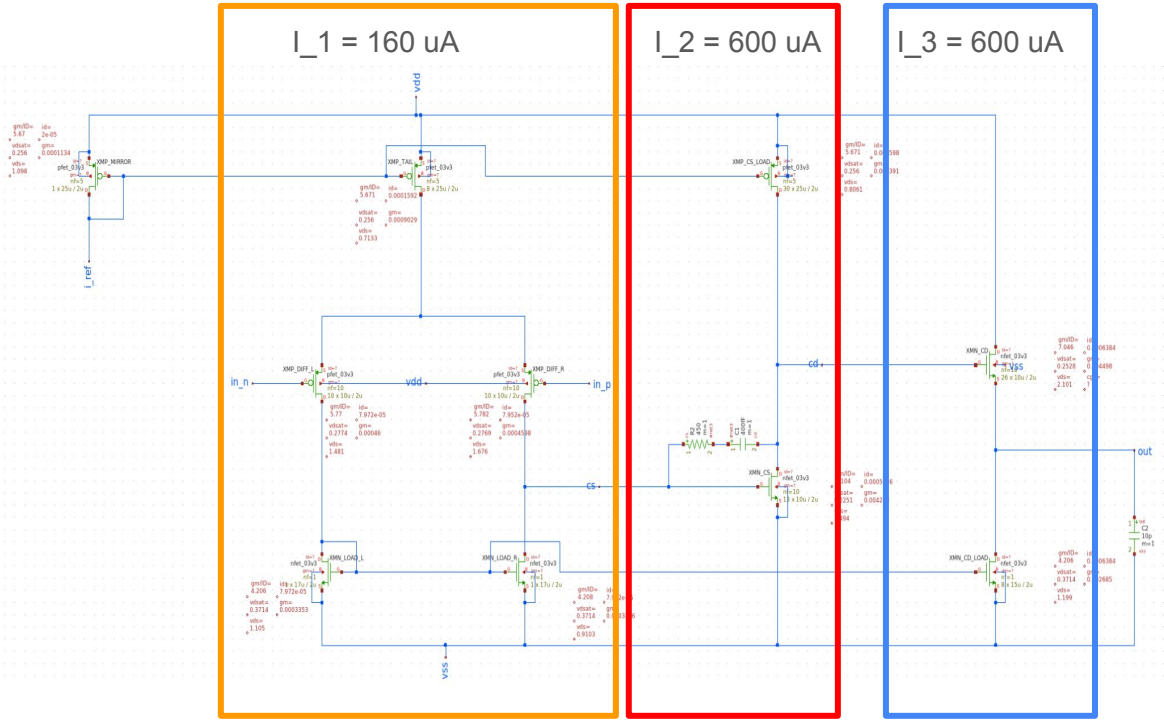


Specifications

Block	Parameter	Value
TIA/opAmp	DC Supply	3.3 V
	Input Driving Current	1 nA- 150 uA
	Linearity	To support 8 bits precision
ADC (SAR)	Resolution	6-8 bits
	Frequency	250-500 KHz
	DC supply for ADC	1.2V (will explore flavour of mos transistor)
DAC (Capacitive)	resolution	6-8 bits

TIA

- 3-stage OpAmp
- Input stage uses PMOS for more suitable common mode input range
- A common-drain output stage is used to enhance current driving capability.



TIA

Sizing:

1. Determine the current in each stage based on its current driving capability.

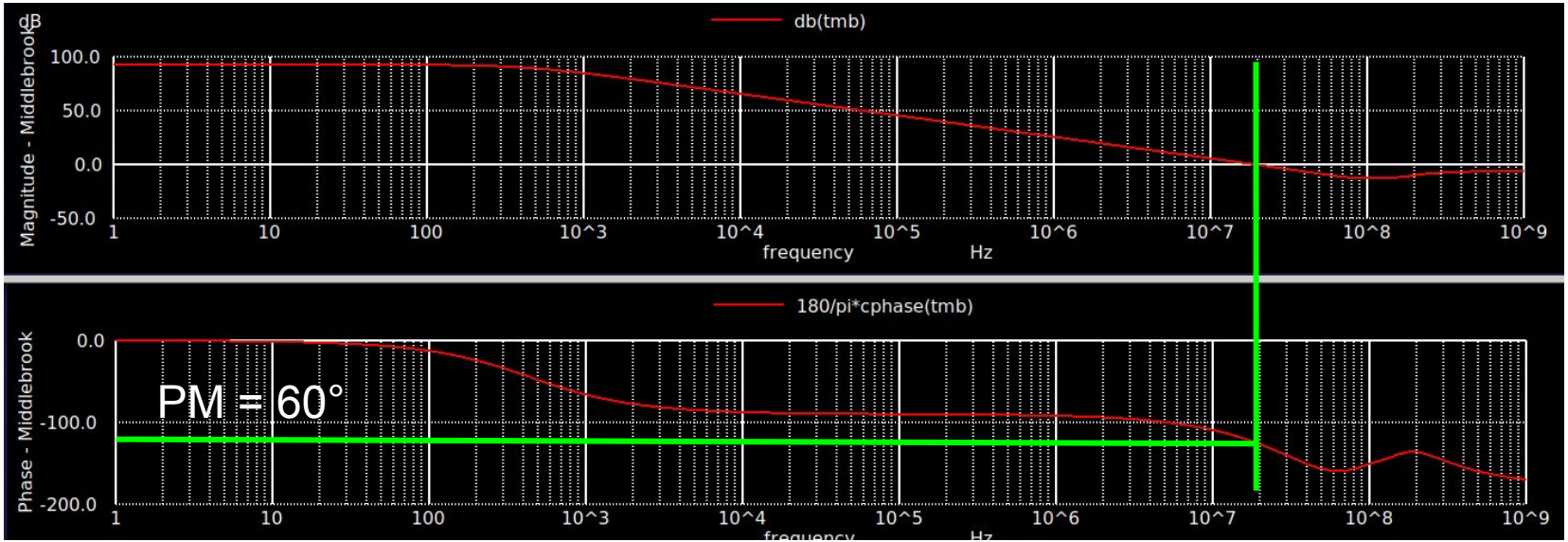
2. A custom script running in Visual Studio Code was used to automate transistor sizing based on the gm/ID design methodology.

3. Since the circuit operates at high currents, a relatively low gm/ID value (~5) was used to reduce transistor sizes.

4. All operating points are simulated within a dedicated testbench environment.

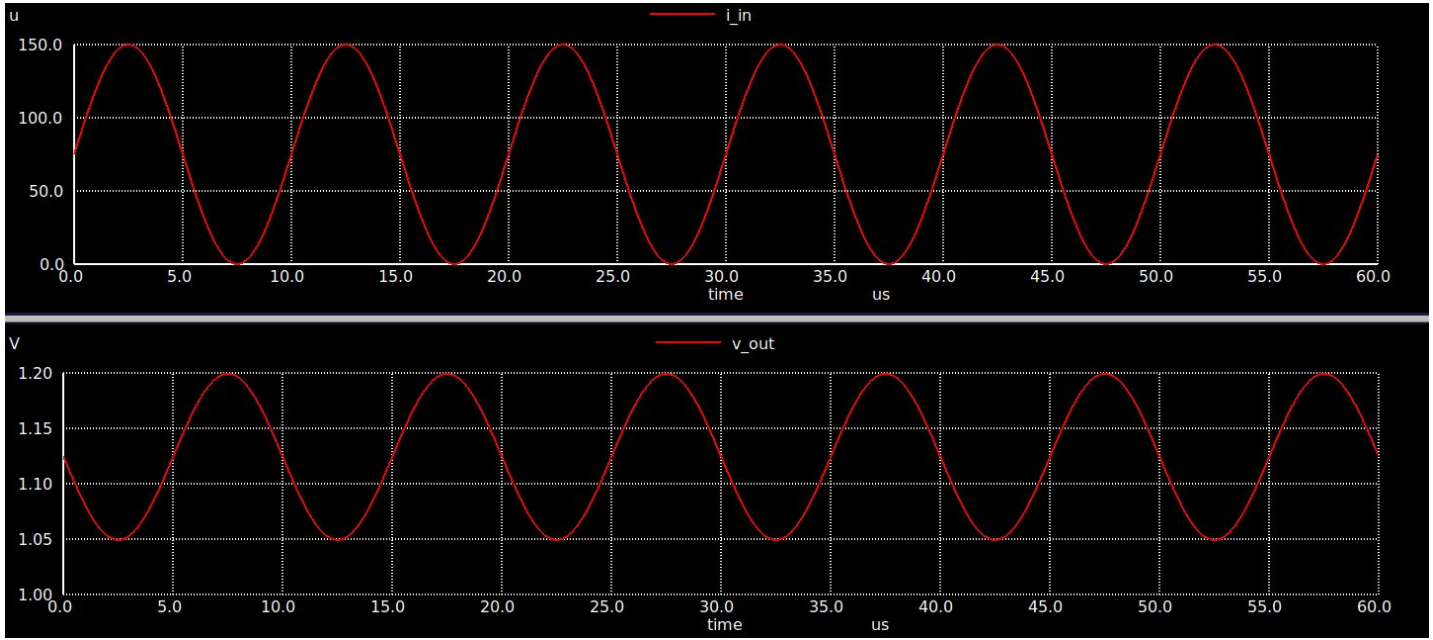
TIA: Stability Simulation

Remark: Stability simulation carried out with Middlebrook methode

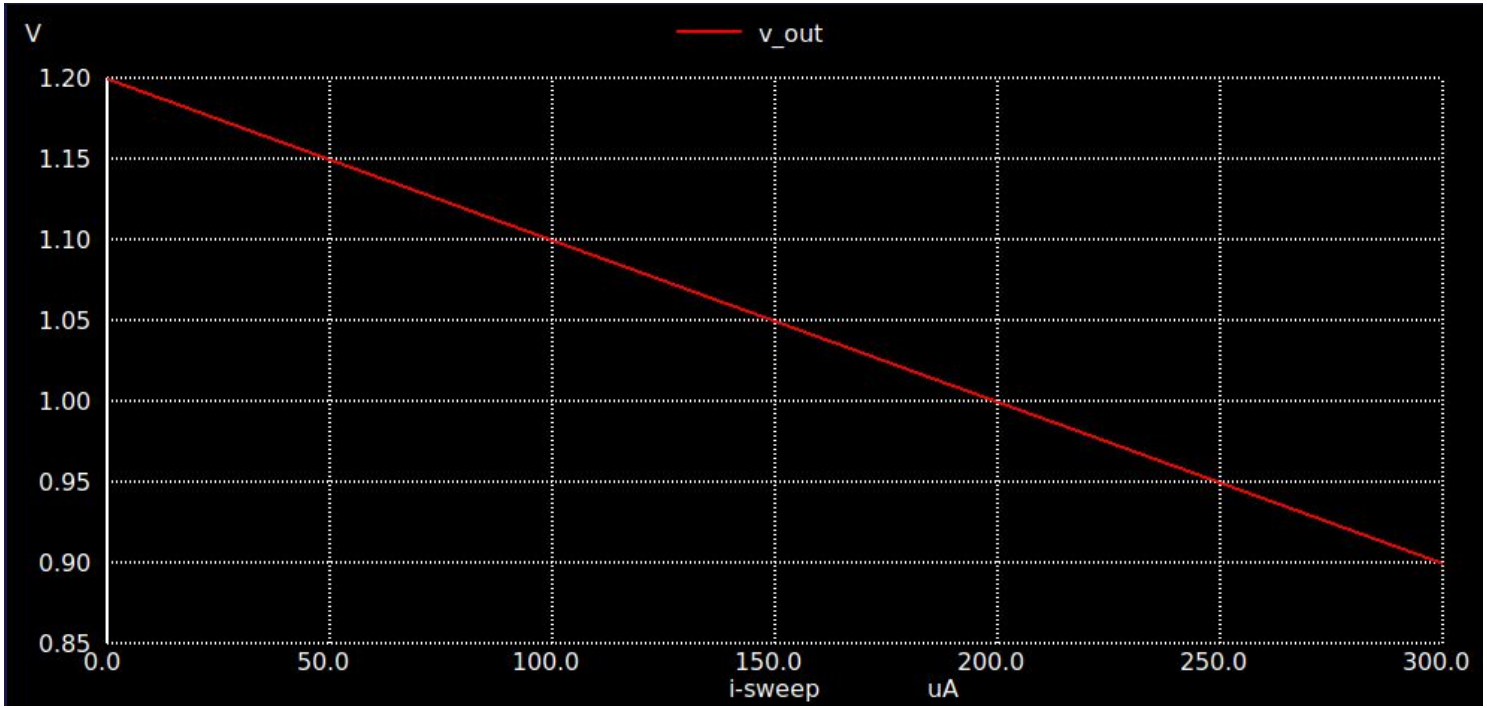


TIA: Transient Simulation

Remark: f = 100 kHz; I_range = 1 nA - 150 uA



TIA: Linearity

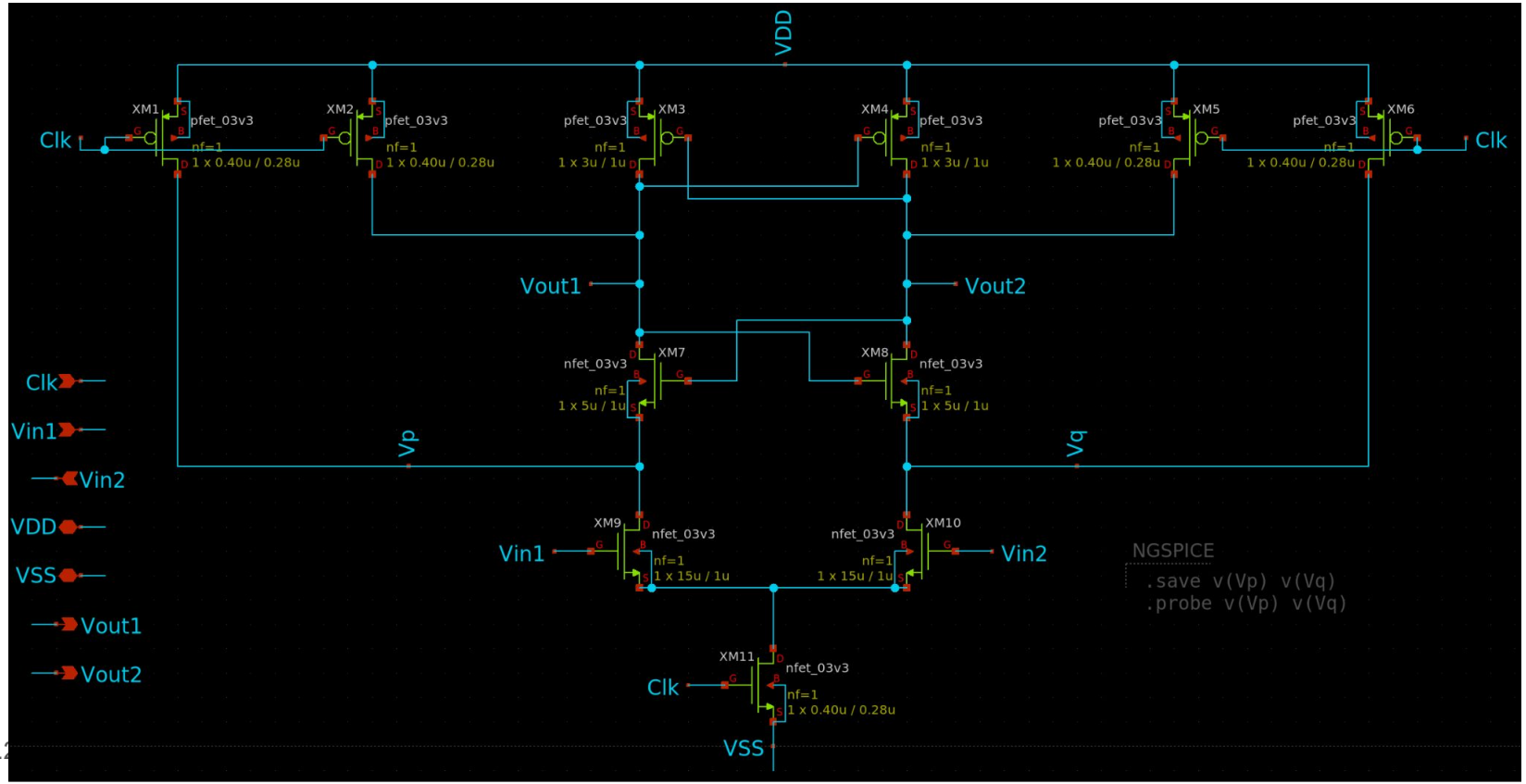


Comparator Specs

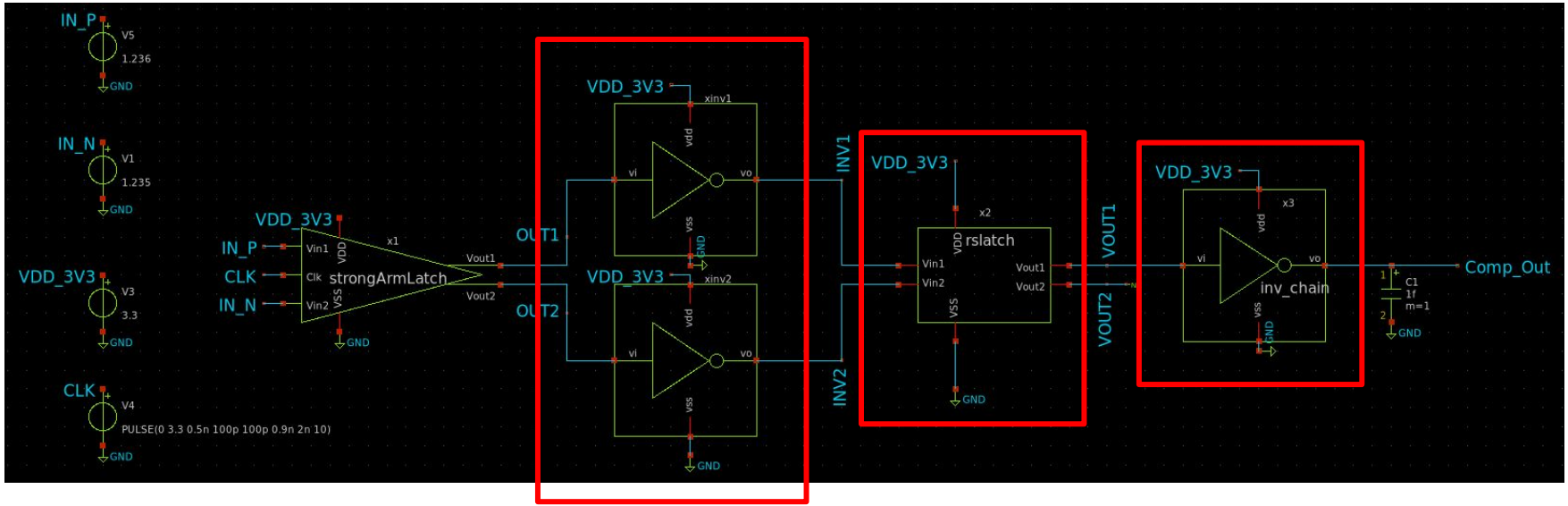
Input Offset	Clock Freq	Power	Input Referred Noise
< 2.34mV	> 1.5 MHz	< 2mW	< 1mV

- We have an input AC signal from 0.9V-1.2V so max input swing is 0.3V
  - Chose a 6-bit ADC so our LSB = 0.3 / 2^6 = 4.68mV
  - Typically want our input offset to be less than ½ of the LSB so < 2.34mV
- We chose to set our ADC sampling rate at 250kHz and for a 6-bit SAR ADC, it takes 6 cycles to determine the final value so our comparator and SAR logic have to work at a clock frequency of > 250kHz * 6 = 1.5MHz
- Ideally we want it to be somewhat low power and just set a reasonable spec of 2mW
- We don’t want too much input referred noise or it will affect our ADC ENOB and it will get too close to the LSB value

Strong Arm Latch Comparator Schematic



Comparator Basic Operation Testbench Schematic

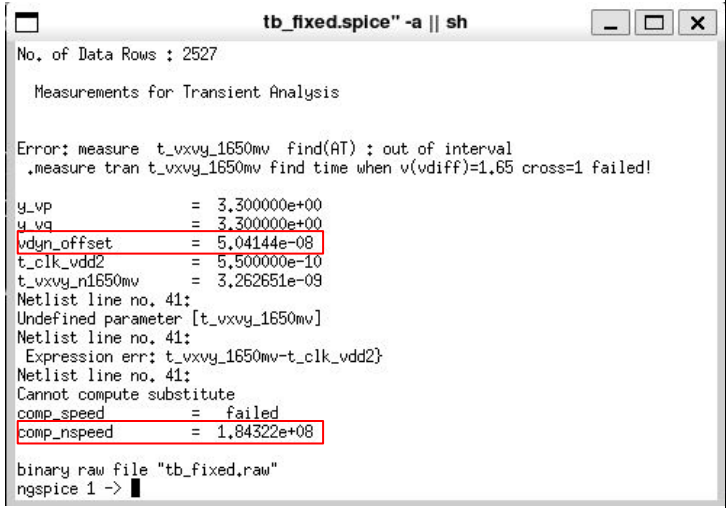


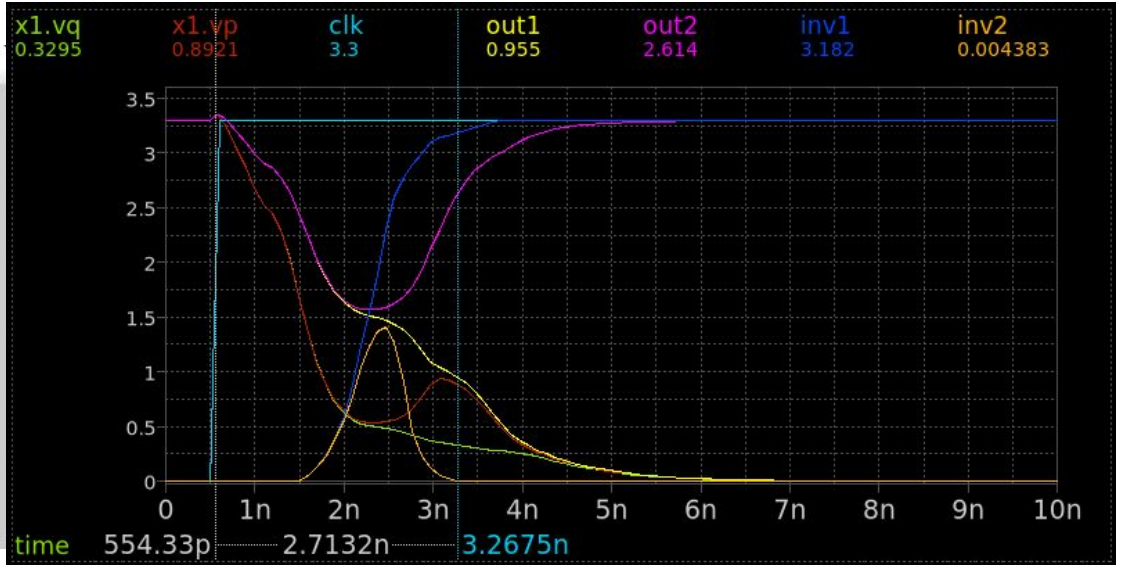
Output buffer to regenerate latch outputs

RS latch to hold output states

Inverter chain from 1x to 4x sizing to drive high impedance output capacitance

Slow Motion Operation (1mV input difference)





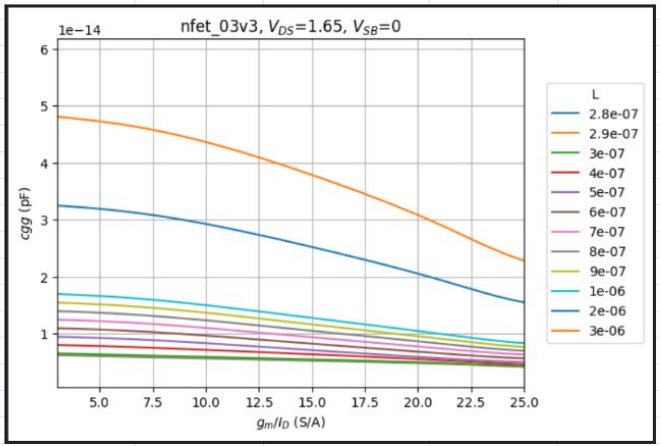
- Dynamic offset at input transistor drain nodes before next clock cycle is 50nV at 5MHz clock
- Comparator max speed assuming low output capacitance (100f) is 184MHz

Input Offset Voltage

	Units (m)	Units (um)	Pelgrom's Law
W9	1.50E-05	1.50E+01	$\Delta V_{TH1,2} = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}}$,
L9	1.00E-06	1.00E+00	
W3	3.00E-06	3.00E+00	
L3	1.00E-06	1.00E+00	
W7	5.00E-06	5.00E+00	
L7	1.00E-06	1.00E+00	

	NMOS	PMOS	
Pelgrom Coefficient (Avth in mV)	6	7	(GF180nm values)
1st Total Input Variation (mV)	1.549193338	1.807392228	
Pelgrom's Sizing Variation (mV)	2.683281573		
Input Variation from M7 M8 (mV)	1.3	(Found from simulator)	
2nd Total Input Variation (mV)	2.022374842		
Pelgrom's Sizing Variation (mV)	3.464101615		
Input Variation from M3 M4 (mV)	1.2	(Found from simulator)	
3rd Total Input Variation (mV)	2.351595203		
If we add preamp gain should be: >	1.00067881		

Input Capacitance	1.7pF	(Output Load of TIA)
LSB 4.7mV		
Want < 2.35mV		



- Chose a very large W and L for input nmos transistors to decrease input offset as much as possible without having very high input capacitance would could cause loading issues to TIA
- Added mismatch voltage sources between nodes to find input referred offset voltages

Comparator Full Test

- Used input sine wave from 0.9V to 1.2V as Vin1
- Used 1.05V as Vin2 as the center of the sine wave
- Verified that the comparator works as expected