User's Manual

Boot Operating Manual

Target Device

R9A06G037

Renesas Electronics
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   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
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2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
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3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
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   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
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Table of Contents

1. Introduction

R9A06G0037(CPX3) boots by downloading the firmware to own internal SRAM. The methods of this downloading the firmware are 2 methods below.

- Downloading from Host controller via UART (UART Boot)
- Downloading from serial flash memory connected to CPX3 (SROM Boot)

This document describes about these boot specifications and the method.

2. Firmware Format

CPX3 firmware is binary data format. This is configured by 4 fields below.

- Unique text string (12 bytes)
  This is the unique text string indicated the top of firmware.

- Checksum of Info Table (4 bytes)
  This is the inversed byte sum of Info Table field (little endian).

- Info Table
  This is the table stored the information of each segments included Firmware body field.
  Refer to section 2.1 about the details.

- Firmware body
  This is the body of firmware. This field includes some segments.
  Refer to section 2.1 about the details.

Figure 2-1 CPX3 firmware format

2.1 Structure of Info Table and Firmware Body

Figure 2-2 shows the details of firmware structure. Firmware body is configured by some segments and the information of these segments is stored in Info Table.

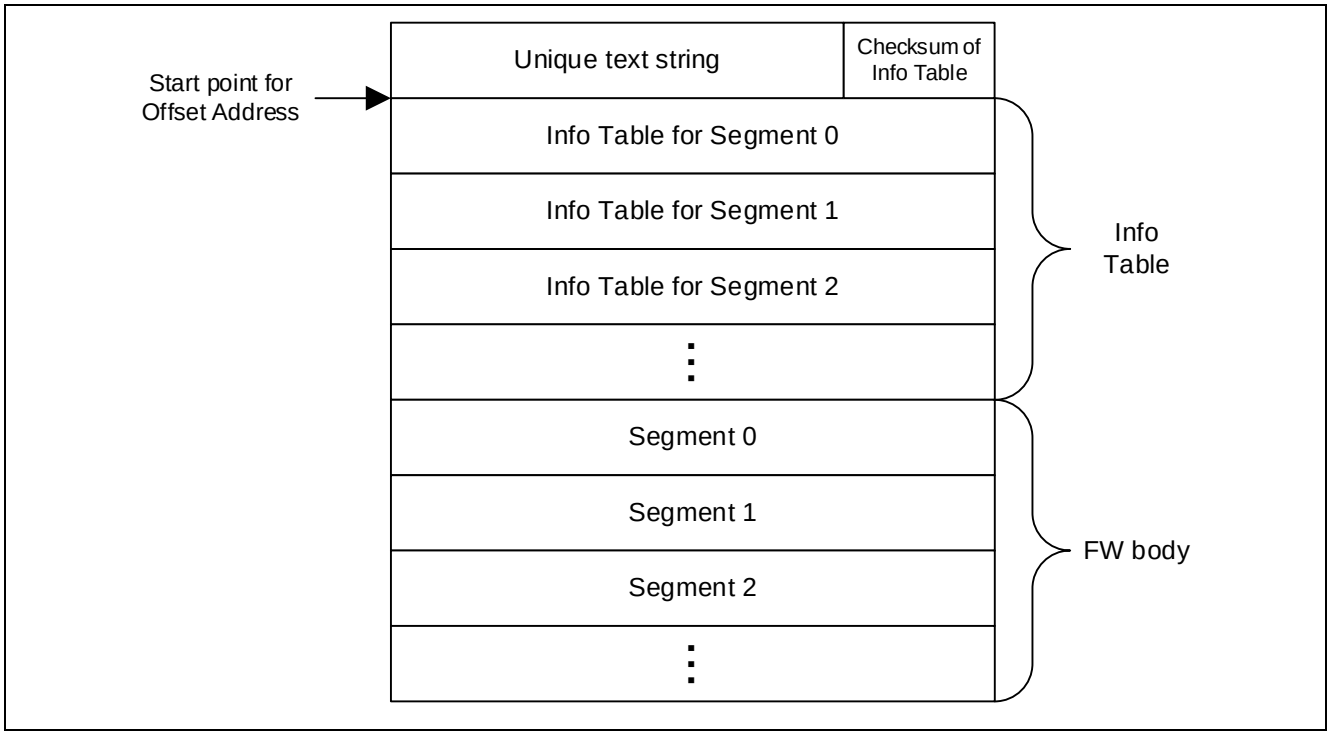

Figure 2-2 Firmware structure

The information of each segments in Info Table is configured by 4 fields below.

Each field is 4 bytes and the information of a segment is 16 bytes in total. Furthermore, the data of each fields is stored as little endian.

- Offset address of segment (4 bytes)
  This is the offset address to its segment.
  This address is the offset from the top address of Info Table.

- Destination address in CPX3 (4 bytes)
  This is the CPX3 address to store its segment.

- Segment size (4 bytes)
  This is the size of its segment.

- Checksum of segment (4 bytes)
  This is checksum of its segment.
  This value is the inversed byte sum.

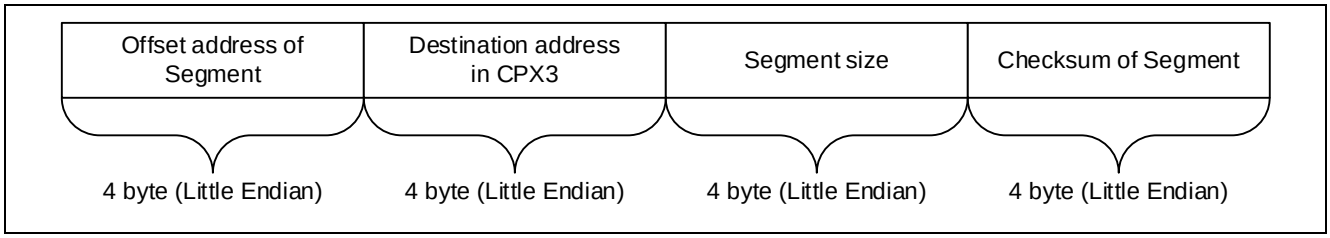

Figure 2-3 The data structure of Info Table

2.2 Example of CPX3 Firmware

Figure 2-4 shows an example of CPX3 firmware and Table 2-1 shows Info Table of its firmware.

The firmware body of CPX3 firmware is configured by 4 segments.

```
const uint8_t g_cpxprogtbl[] = {
    0x43, 0x70, 0x58, 0x73, 0x42, 0x6F, 0x4F, 0x74, 0x48, 0x65, 0x41, 0x64, 0xA0, 0xF0, 0xFF, 0xFF, /* Unique text strings and Checksum */
    0x40, 0x00, 0x00, 0x00, 0x00, 0x00, 0x07, 0x20, 0x11, 0x0D, 0x00, 0x00, 0x2F, 0x86, 0xF9, 0xFF, /* Info Table for Segment 0 */
    0x51, 0x0D, 0x00, 0x00, 0x00, 0x00, 0x02, 0x48, 0x71, 0x68, 0x01, 0x00, 0xE2, 0x92, 0x4C, 0xFF, /* Info Table for Segment 1 */
    0xC2, 0x75, 0x01, 0x00, 0x00, 0x00, 0x00, 0x48, 0x41, 0x25, 0x00, 0x00, 0x4C, 0x85, 0xED, 0xFF, /* Info Table for Segment 2 */
    0x03, 0x9B, 0x01, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0xD4, 0x01, 0x00, 0xAA, 0x14, 0x17, 0xFF, /* Info Table for Segment 3 */
    0x01, 0x45, 0xFD, ..... /* Segment 0 of Firmware body*/
    .....
    .....
    0xC1, 0x45, 0xFD, ..... /* Segment 1 of Firmware body*/
    .....
    .....
    0xB1, 0x45, 0xFD, ..... /* Segment 2 of Firmware body*/
    .....
    .....
    0xD1, 0x45, 0xFD, ..... /* Segment 3 of Firmware body*/
    .....
    .....
}
```

Figure 2-4 Example of CPX3 firmware

Table 2-1 Example of Info Table in CPX3 firmware

Segment No.	Offset address of Segment	Destination address in CPX3	Segment size	Checksum of Segment
0	0x00000040	0x20070000	0x00000D11	0xFFF9862F
1	0x00000D51	0x48020000	0x00016871	0xFF4C92E2
2	0x000175C2	0x48000000	0x00002541	0xFFED854C
3	0x00019B03	0x00000000	0x0001D401	0xFF1714AA

3. UART Boot

This chapter describes about the method of CPX3 boot by downloading the firmware from Host controller via UART (UART Boot).

Figure 3-1 shows an example of connection between CPX3 and Host controller. “BOOT0” terminal of CPX3 shall be set to High level for UART Boot.

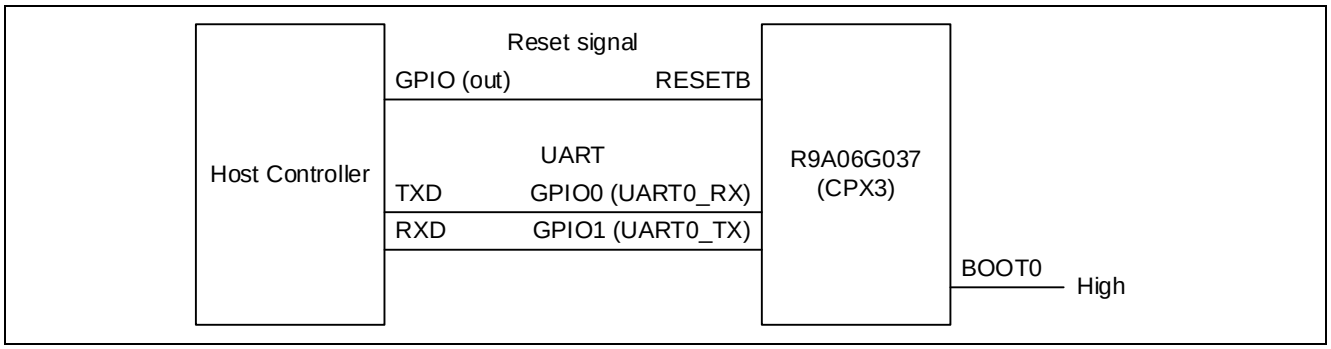

Figure 3-1 Example of connection between CPX3 and Host controller

3.1 UART Communication Spec.

CPX3 communicates with Host controller via UART by using the setting shown by Table 3-1.

Table 3-1 UART communication spec.

Item	Spec.	Note
Data unit	8 bit	-
Parity	No parity	-
Stop bit	1 bit	-
Baudrate	Segment0: 115,200bps Segment1-N: Selectable Refer to section 0 about the details.	±3% (Permissible error)
Flow control	None	-

3.2 Command Format

UART Boot sequence uses 1 byte commands.

Table 3-2 shows its command format and Table 3-3 shows its command list.

Table 3-2 Command format

bit	7	6	5	4	3	2	1	0
Field	Command ID				Parameter			

Table 3-3 Command list

Command ID	Parameter	Direction	Function	Description
0x8	0x0 – 0xF (Segment No.)	CPX -> Host	Segment transmission request	This is the command to request to transmit a segment data from CPX to Host controller. After this command was received, Host controller shall send the following data of a segment specified by the parameter (Segment No.) of this command to CPX in order. • Destination address to CPX3 in Info Table (4 bytes) • Segment size in Info Table (4 bytes) • Checksum of segment in Info Table (4 bytes) • Segment data specified by offset address of segment in Info Table (4 bytes)
0xA	0x1	CPX -> Host	Baudrate change request	This is the command to request to change baudrate from CPX to Host controller. After this command was received, Host controller shall send “Baudrate set request” command (0xC1) and the baudrate setting information (1 byte). In this sequence, if CPX cannot receive “Baudrate set request” and the baudrate setting information normally within 1 second after CPX sent this command, CPX sets the baudrate to 115,200 bps and continues the process.
0xA	0xA	Host -> CPX	Baudrate change completion	This is the command to notify of completing to change baudrate from Host controller to CPX. After this command was received, CPX starts to communicate by using the downloading baudrate specified by the baudrate setting information.
0xB	0x0	CPX -> Host	Firmware transmission completion	This is the command to notify of completing to receive all of segment data from CPX3 to Host controller. After this command was sent, CPX changes to the communicating baudrate specified by

				the baudrate setting information and boot the firmware.
0xC	0x1	Host -> CPX	Baudrate set request	This is the command to request to set the baudrate from Host controller to CPX. Host controller shall send the baudrate setting information (1 byte, 0xXY) after sending this command. The details of this information are below. X (4 bits): The downloading baudrate for Segment 1-N. Y (4 bits): The communicating baudrate after the firmware is booted. Refer to Table 3-4 about the set value for X and Y. The recommended value of the downloading baudrate is 1,000,000 bps. And refer to the specifications of each firmware about the recommended value of the communicating baudrate.
0xC	0xF	CPX -> Host	Baudrate set accept	This is the command to notify of completing to receive “Baudrate set request” command and the baudrate setting information. After this command was received, Host controller shall change the baudrate to the downloading baudrate set by “Baudrate set request” command and shall send “Baudrate change completion” command (0xAA) to CPX.

Table 3-4 The baudrate set value

Set value	Baudrate (bps)	Practical baudrate (bps)	Error rate (%)
0x0	9600	9588.66	-0.12
0x1	19200	19166.67	-0.17
0x2	38400	38333.33	-0.17
0x3	57600	57500.00	-0.17
0x4	115200	115000.00	-0.17
0x5	230400	230000.00	-0.17
0x6	300000	302631.58	0.88
0x7	375000	375000.00	0.00
0x8	460800	453947.37	-1.49
0x9	500000	507352.94	1.47
0xA	750000	750000.00	0.00
0xB	937500	958333.33	2.22
0xC	1000000	1014705.88	1.47

3.3 UART Boot Sequence

Figure 3-3 shows UART Boot sequence by using the commands.

The control signals in this figure are described as shown in Figure 3-2.

Refer the specifications of each firmware for the behavior of the firmware after booting.

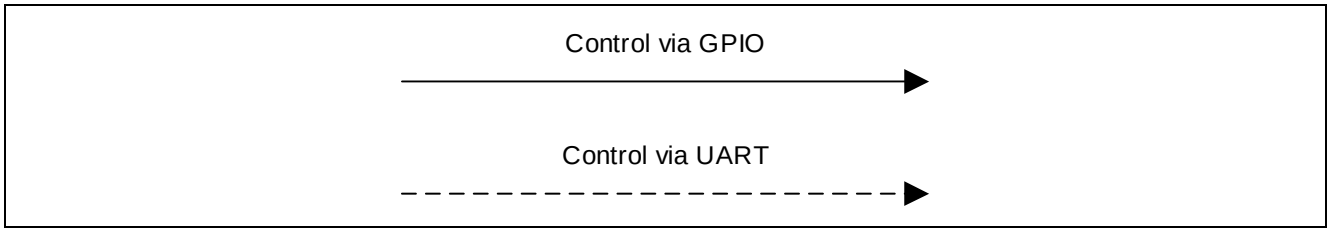

Figure 3-2 Notation of the control signal in the sequence flow

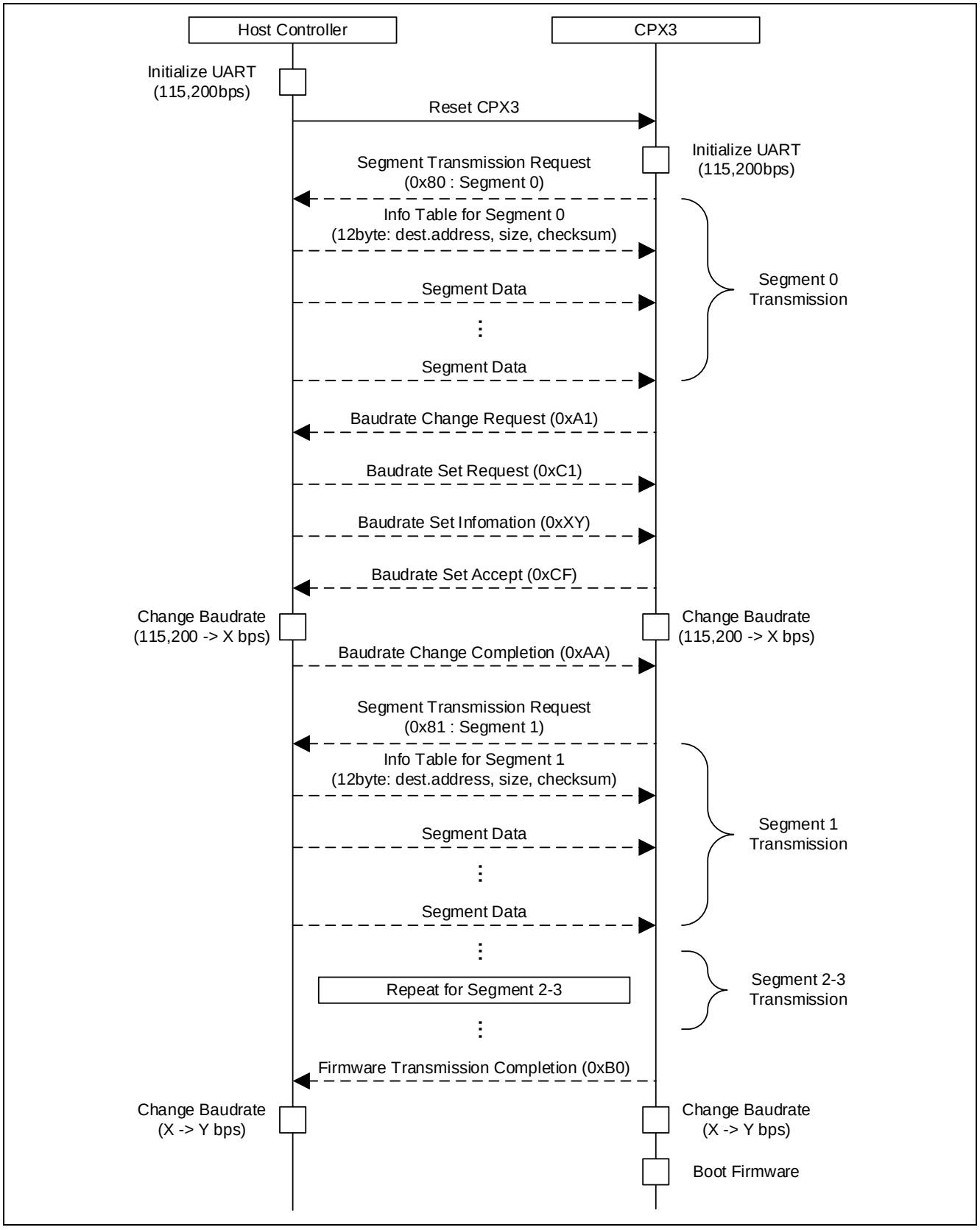

Figure 3-3 UART Boot sequence

3.4 Error Causes

Table 3-5 shows the possible errors in UART Boot sequence and their recommended process to recovery.

Table 3-5 The error causes in UART Boot sequence

No.	Error cause	Detector	When this error should be detected.	The recommended process to recovery
1	Timeout	Host controller	When Host controller cannot receive the response within 2 seconds after sending any commands to CPX.	Host controller shall reset CPX.
2	Checksum error	CPX	When CPX checks the checksum after receiving the segment data from Host controller.	CPX will send “Segment transmission request” of a segment detected checksum error again when checksum error is detected. Host controller shall send the segment data requested again.
3	CRC error	CPX	When CPX checks the CRC32 after receiving the segment data from Host controller.	CPX will send “Segment transmission request” of a segment detected CRC32 error again when CRC32 error is detected. Host controller shall send the segment data requested again.

4. SROM Boot

This chapter describes about the method of CPX3 boot by downloading the firmware stored in serial flash memory connected to CPX3 (SROM Boot).

Figure 4-1 shows an example of connection between CPX3 and serial flash memory. “BOOT0” terminal of CPX3 shall be set to Low level for SROM Boot.

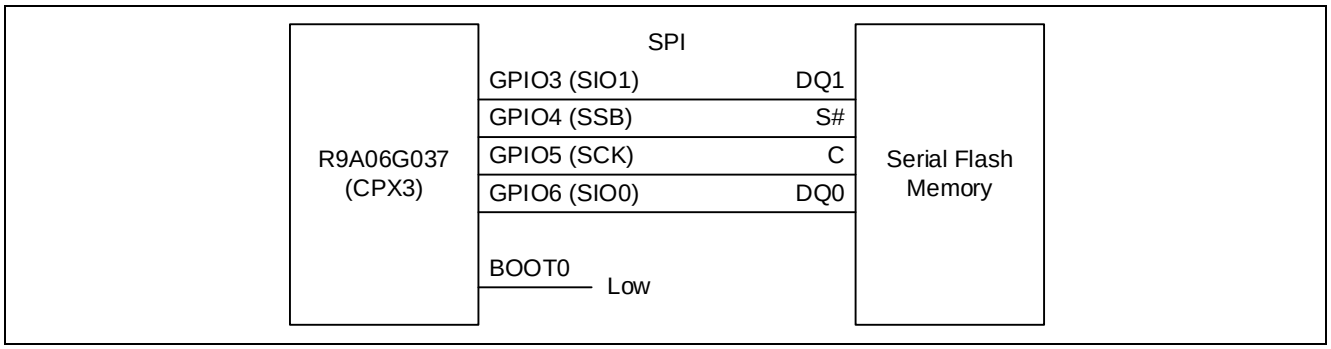

Figure 4-1 Example of connection between CPX3 and serial flash memory

4.1 Mapping of Serial Flash Memory

Figure 4-2 and Figure 4-3 show examples of mapping of serial flash memory.

CPX3 maps serial flash memory to internal address 0x10000000 in CPX3. Therefore, this example is explained that the start address of serial flash memory is 0x10000000.

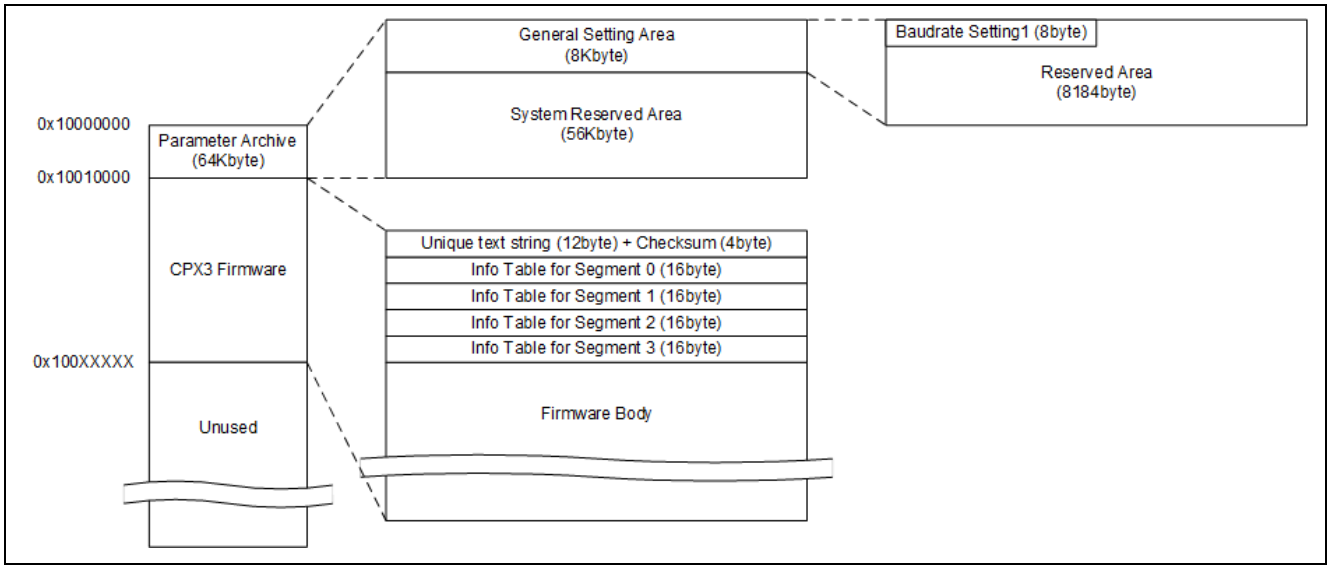

Figure 4-2 Example1 of mapping of serial flash memory

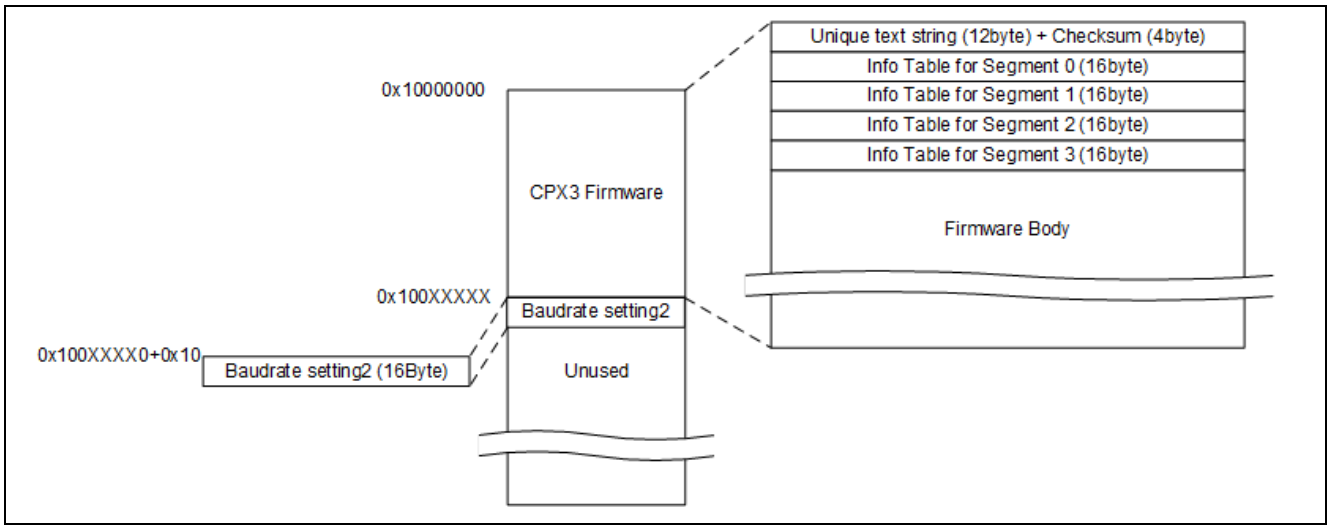

Figure 4-3 Example2 of mapping of serial flash memory

When booting firmware from serial flash memory, it is necessary to arrange the firmware from the 64 Kbyte aligned address. Firmware is arranged from 0x10010000 in the example of Figure 4-2 and 0x10000000 in the example of Figure 4-3. When specifying the baud rate setting for communicating with the host controller via the firmware boot, it is necessary to write to the beginning of serial flash (baudrate setting1, 8bytes) or the 16-byte aligned address of immediately after the final address of CPX3 firmware (baudrate setting2, 16bytes).

Ex.) When the final address of the firmware is 0x1036FE8, the start address of baudrate setting2 is 0x1036FF0.

If the baud rate setting is not written in the serial flash, the baud rate is set to 115200 bps.

Details of baud rate setting1 field and setting values are shown in Figure 4-4 and Table 4-1.

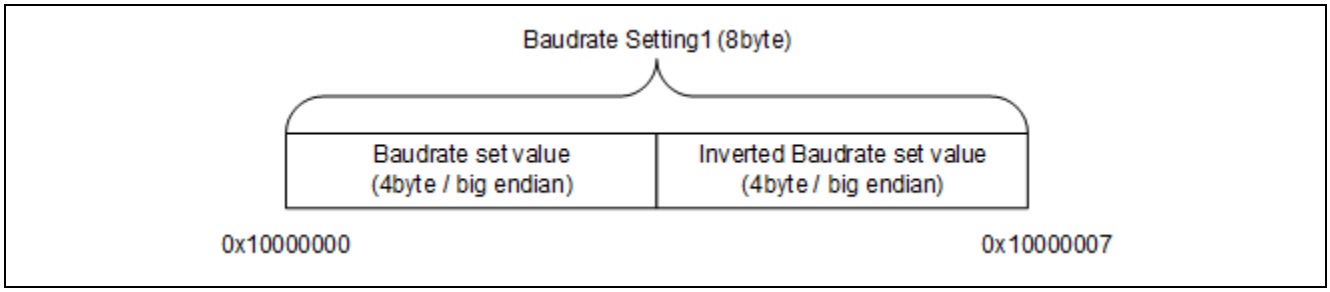

Figure 4-4 Detail of Baudrate Setting1 filed

The beginning of 4 bytes in this field shall be stored the baudrate set value and the next 4 bytes shall be stored the inverted value of the beginning of 4 bytes.

Table 4-1 Set value of Baudrate Setting1 field

Baudrate (bps)	Practical baudrate (bps)	Set value
9600	9588.66	0x00000000FFFFFFFF
19200	19166.67	0x00000001FFFFFFFE
38400	38333.33	0x00000002FFFFFFFD
57600	57500.00	0x00000003FFFFFFFC
115200	115000.00	0x00000004FFFFFFFB
230400	230000.00	0x00000005FFFFFFFA
300000	302631.58	0x00000006FFFFFFF9
375000	375000.00	0x00000007FFFFFFF8
460800	453947.37	0x00000008FFFFFFF7
500000	507352.94	0x00000009FFFFFFF6
750000	750000.00	0x0000000AFFFFFFF5
937500	958333.33	0x0000000BFFFFFFF4
1000000	1014705.88	0x0000000CFFFFFFF3

Details of baud rate setting1 field and setting values are shown in Figure 4-5and Figure 4-3.

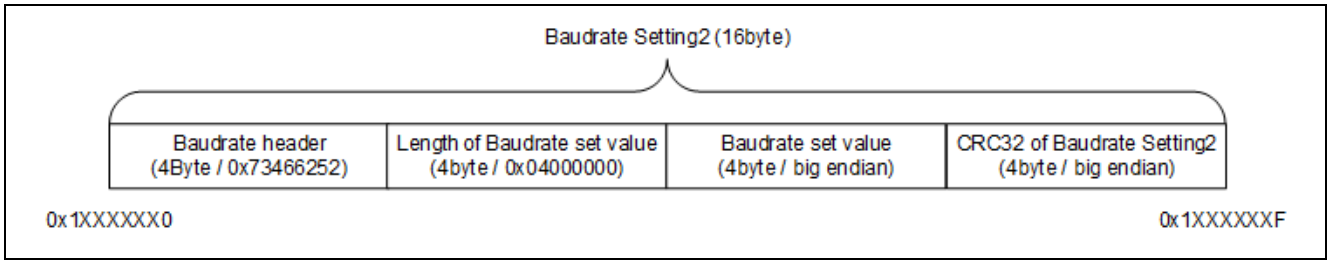

Figure 4-5 Detail of Baudrate Setting2 filed

In the baud rate setting2 field, set the header (fixed value, 0x73466252) to the first 4 bytes, the length of the setting value of the baud rate to the next 4 bytes in little endian (fixed value, 0x04000000), set the baud rate value to the next 4 bytes and write CRC32 of baud rate setting2 to the next 4 bytes. For the calculation parameters of CRC 32, see Table 4-2.

Table 4-2 CRC parameters

Item	Description
Name	CRC32
Polynomial	0x4C11DB7
Shift direction	Left
Initial value	0
Output XOR	0x00000000
Finalization	Not bit inversion

Table 4-3 Set value of Baudrate Setting2 field

Baudrate (bps)	Practical baudrate (bps)	Set value
9600	9588.66	0x73466252040000000000000FB1DC209
19200	19166.67	0x73466252040000000000001FFDCDFBE
38400	38333.33	0x73466252040000000000002F29FF967
57600	57500.00	0x73466252040000000000003F65EE4D0
115200	115000.00	0x73466252040000000000004E819B4D5
230400	230000.00	0x73466252040000000000005ECD8A962
300000	302631.58	0x73466252040000000000006E19B8FBB
375000	375000.00	0x73466252040000000000007E55A920C
460800	453947.37	0x73466252040000000000008DD152FB1
500000	507352.94	0x73466252040000000000009D9D43206
750000	750000.00	0x7346625204000000000000AD49714DF
937500	958333.33	0x7346625204000000000000BD0560968
1000000	1014705.88	0x7346625204000000000000CCE11596D

When there is a valid baud rate setting1 and baud rate setting2 in the serial flash, the baud rate setting2 is preferentially set.

4.2 SROM Boot Sequence

Figure 4-6 shows the internal processing sequence when CPX3 is booted from serial flash memory.

At first, CPX3 searches “Unique text string” in the firmware from the address aligned on 64Kbytes boundary after CPX3 is reset. In the case that “Unique text string” is not found, CPX3 gives up SROM Boot and starts the sequence of UART Boot. In the case that “Unique text string” is found, CPX3 starts to download the firmware. If CRC32 of downloaded firmware is invalid, it will give up SROM boot and starts the sequence of UART Boot.

After the firmware download is completed, CPX3 reads and verifies “Baudrate setting” stored in the top of serial flash memory. If the read value is not correct, CPX3 continues the process as baudrate is 115,200bps.

Refer the specifications of each firmware for the behavior of the firmware after booting.

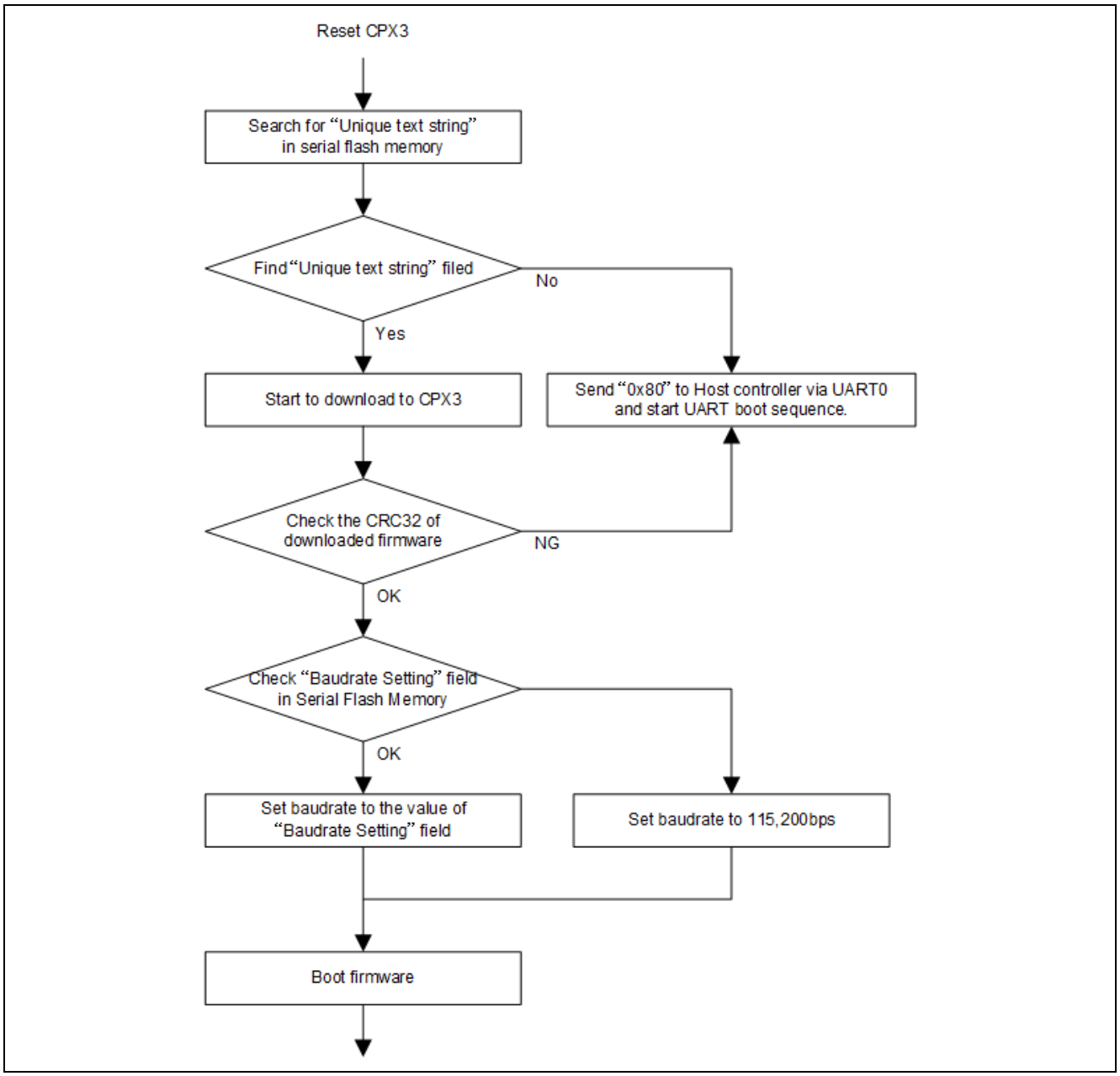

Figure 4-6 CPX3 internal processing sequence for SROM Boot

4.3 Serial Flash Memory that operation has been confirmed

Table 4-4 shows Serial Flash Memory that operation has been confirmed.

Table 4-4 List of Serial Flash Memory that operation has been confirmed

Model number	Manufacturer
M25PX16-VMN6TP	Micron Technology, Inc.
N25Q032A13ESC40	Micron Technology, Inc.
S25FL116K0XMFI041	Cypress Semiconductor Corp.
AT25SF321-SSHD	Adesto Technologies Corporation, Inc

5. Revision History

Date	Revision	Section	Substance
May 19, 2017	1.00	-	First edition.
Apr. 25, 2018	1.01	3.4	Table 3-5 CRC error added to error cause
		4.1	Since serial flash memory mapping has been extended, a baud rate setting method is added.
		4.2	Changed the flow chart as CRC32 check added
May 08, 2018	1.02	4.3	Added serial flash memory whose operation has been confirmed.

Boot Operating Manual

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Colophon 4.1

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