

# GameBoy Opcode Summary

The GameBoy has instructions & registers similiar to the 8080, 8085, & Z80 microprocessors. The internal 8-bit registers are A, B, C, D, E, F, H, & L. Theses registers may be used in pairs for 16-bit operations as AF, BC, DE, & HL. The two remaining 16-bit registers are the program counter (PC) and the stack pointer (SP).

The F register holds the cpu flags. The operation of these flags is identical to their Z80 relative. The lower four bits of this register always read zero even if written with a one.

Flag Register							
7	6	5	4	3	2	1	0
Z	N	H	C	0	0	0	0

The GameBoy CPU is based on a subset of the Z80 microprocessor. A summary of these commands is given below.

Mnemonic	Symbolic Operation	Comments	CPU Clocks	Flags - Z,N,H,C
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## 8-Bit Loads

LD r,s	$r \leftarrow s$	$s=r,n,(HL)$	$r=4, n=8, (HL)=8$
LD d,r	$d \leftarrow r$	$d=r,(HL)$	$r=4, (HL)=8$
LD d,n	$d \leftarrow n$		$r=8, (HL)=12$
LD A,(ss)	$A \leftarrow (ss)$	$ss=BC,DE,HL,nn$	$[BC,DE,HL]=8, nn=16$
LD (dd),A	$(dd) \leftarrow A$	$dd=BC,DE,HL,nn$	
LD A,(C)	$A \leftarrow (\$FF00+C)$	-	8
LD (C),A	$(\$FF00+C) \leftarrow A$		8
LDD A,(HL)	$A \leftarrow (HL), HL \leftarrow HL - 1$		8
LDD (HL),A	$(HL) \leftarrow A, HL \leftarrow HL - 1$		8
LDI A,(HL)	$A \leftarrow (HL), HL \leftarrow HL + 1$		8
LDI (HL),A	$(HL) \leftarrow A, HL \leftarrow HL + 1$		8
LDH (n),A	$(\$FF00+n) \leftarrow A$		12
LDH A,(n)	$A \leftarrow (\$FF00+n)$		12

## 16-Bit Loads

[illegible]

LD dd,nn	dd ← nn	dd=BC,DE,HL,SP	12				
LD (nn),SP	(nn) ← SP	-	20	-	-	-	-
LD SP,HL	SP ← HL		8				
LD HL,(SP+e)	HL ← (SP+e)		12	0	0	*	*
PUSH ss	(SP-1) ← ssh, (SP-2) ← ssl, SP ← SP-2	ss=BC,DE,HL,AF	16				
POP dd	ddl ← (SP), ddh ← (SP+1), SP ← SP+2	dd=BC,DE,HL,AF	12	-	-	-	-

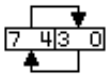
## 8-Bit ALU

ADD A,s	A ← A + s	CY is the carry flag. s=r,n,(HL)	r=4, n=8, (HL)=8	*	0	*	*
ADC A,s	A ← A + s + CY						
SUB s	A ← A - s			*	1	*	*
SBC A,s	A ← A - s - CY			*	0	1	0
AND s	A ← A ∧ s			*	0	0	0
OR s	A ← A ∨ s			*	0	0	0
XOR s	A ← A ⊕ s			*	1	*	*
CP s	A - s	s=r,(HL)	r=4, (HL)=12	*	0	*	-
INC s	s ← s + 1			*	1	*	-
DEC s	s ← s - 1						

## 16-Bit Arithmetic

ADD HL,ss	HL ← HL + ss	ss=BC,DE,HL,SP	8	-	0	*	*
ADD SP,e	SP ← SP + e		16	0	0	*	*
INC ss	ss ← ss + 1		8				
DEC ss	ss ← ss - 1		8	-	-	-	-

## Miscellaneous

SWAP s		Swap nibbles. s=r,(HL)	r=8, (HL)=16	*	0	0	0
DAA	Converts A into packed BCD.	-	4	*	-	0	*
CPL	A ← /A		4	-	1	1	-
CCF	CY ← /CY	CY is the carry flag.	4	-	0	0	*
SCF	CY ← 1		4	-	0	0	1

NOP	No operation.					4				
HALT	Halt CPU until an interrupt occurs.					4				
STOP	Halt CPU.			-		4	-	-	-	-
DI	Disable Interrupts.					4				
EI	Enable Interrupts.					4				

## Rotates & Shifts

RLCA									
RLA			4		0	0	0	*	
RRCA									
RRA									
RLC s									
RL s									
RRC s		s=A,r,(HL)	r=8,(HL)=16						
RR s					*	0	0	*	
SLA s									
SRA s		s=r,(HL)	r=8, (HL)=16						
SRL s									

## Bit Opcodes

BIT b,s	$Z \leftarrow \text{sb}$		r=8, (HL)=12	*	0	1	-
SET b,s	$\text{sb} \leftarrow 1$	Z is zero flag. s=r,(HL)	r=8, (HL)=16	-	-	-	-
RES b,s	$\text{sb} \leftarrow 0$						

## Jumps

JP nn	$\text{PC} \leftarrow \text{nn}$		16
JP cc,nn	If cc is true, $\text{PC} \leftarrow \text{nn}$ , else continue.		If cc is true, 16 else 12.
JP (HL)	$\text{PC} \leftarrow \text{HL}$	-	4
JR e	$\text{PC} \leftarrow \text{PC} + e$		12
JR cc,e	if cc is true, $\text{PC} \leftarrow \text{PC} + e$ , else continue.		If cc is true, 12 else 8.

## Calls

CALL nn	(SP-1) ← PCh, (SP-2) ← PCl, PC ← nn, SP ← SP-2	-	24
CALL cc,nn	If condition cc is false continue, else same as CALL nn.	-	If cc is true, 24 else 12.

## Restarts

RST f	(SP-1) ← PCh, (SP-2) ← PCl, PCh ← 0, PCl ← f, SP ← SP-2	-	16
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## Returns

RET	pcl ← (SP), pch ← (SP+1), SP ← SP+2	-	16
RET cc	If cc is true, RET else continue.	-	If cc is true, 20 else 8.
RETI	Return then enable interrupts.	-	16

## Terminology

-	Flag is not affected by this operation.
*	Flag is affected according to result of operation.
b	A bit number in any 8-bit register or memory location.
C	Carry flag.
cc	Flag condition code: C,NC,NZ,Z
d	Any 8-bit destination register or memory location.
dd	Any 16-bit destination register or memory location.
e	8-bit signed 2's complement displacement.
f	8 special call locations in page zero.
H	Half-carry flag.
N	Subtraction flag.
NC	Not carry flag
NZ	Not zero flag.
n	Any 8-bit binary number.
nn	Any 16-bit binary number.
r	Any 8-bit register. (A,B,C,D,E,H, or L)
s	Any 8-bit source register or memory location.
sb	A bit in a specific 8-bit register or memory location.

ss	Any 16-bit source register or memory location.
Z	Zero Flag.