CSE 341

Assignment

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Sec - 06

Ans to the Que No-1

Given,

frequency = 11.5 MHz

= 11.5×10^6 Hz

Duty cycle = 40% $\therefore \frac{T_{ON}}{T_{ON} + T_{off}} = 0.4$

(a) Time for 1 clock pulse, $T = \frac{1}{11.5 \times 10^6}$ sec

= 86.96 nsec (Ans)

(b) Time for 1 bus cycle = (86.96×4) ns

= 347.84 ns.

(Ans)

(c) We know,

$T_{ON} + T_{OFF} = 1$ clock state

$$\therefore \frac{T_{ON}}{T_{ON} + T_{OFF}} = 0.4$$

$$\Rightarrow T_{ON} = 0.4 \times (T_{ON} + T_{OFF})$$

$$= (0.4 \times 86.96)\ ns$$

$$= 34.784\ ns$$

$$\therefore T_{OFF} = (86.96 - 34.784)\ ns$$

$$= 52.176\ ns$$

Ans

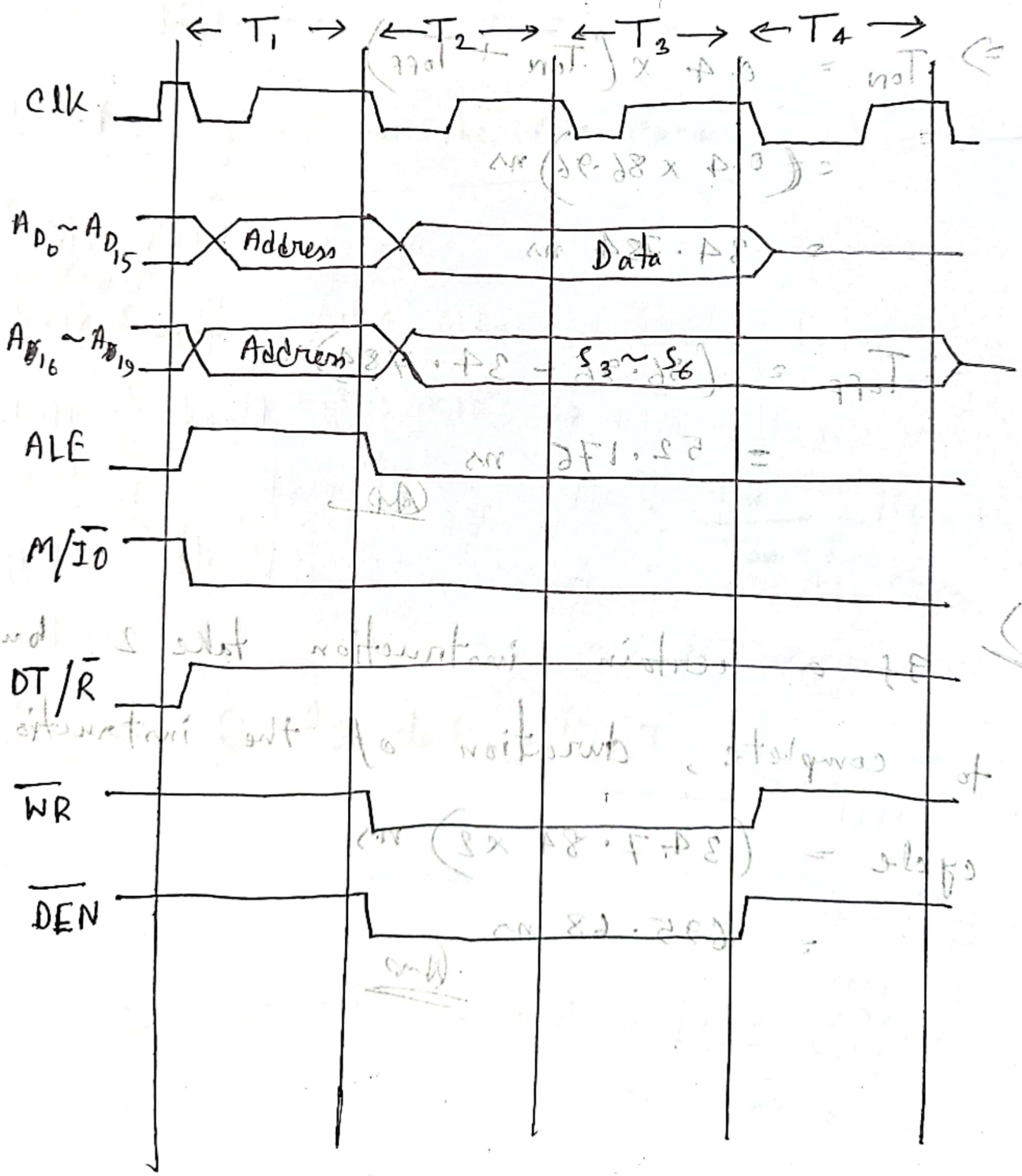
(d) If a certain instruction take 2 bus cycle to complete, duration of the instruction cycle $= (347.84 \times 2)\ ns$

$$= 695.68\ ns$$

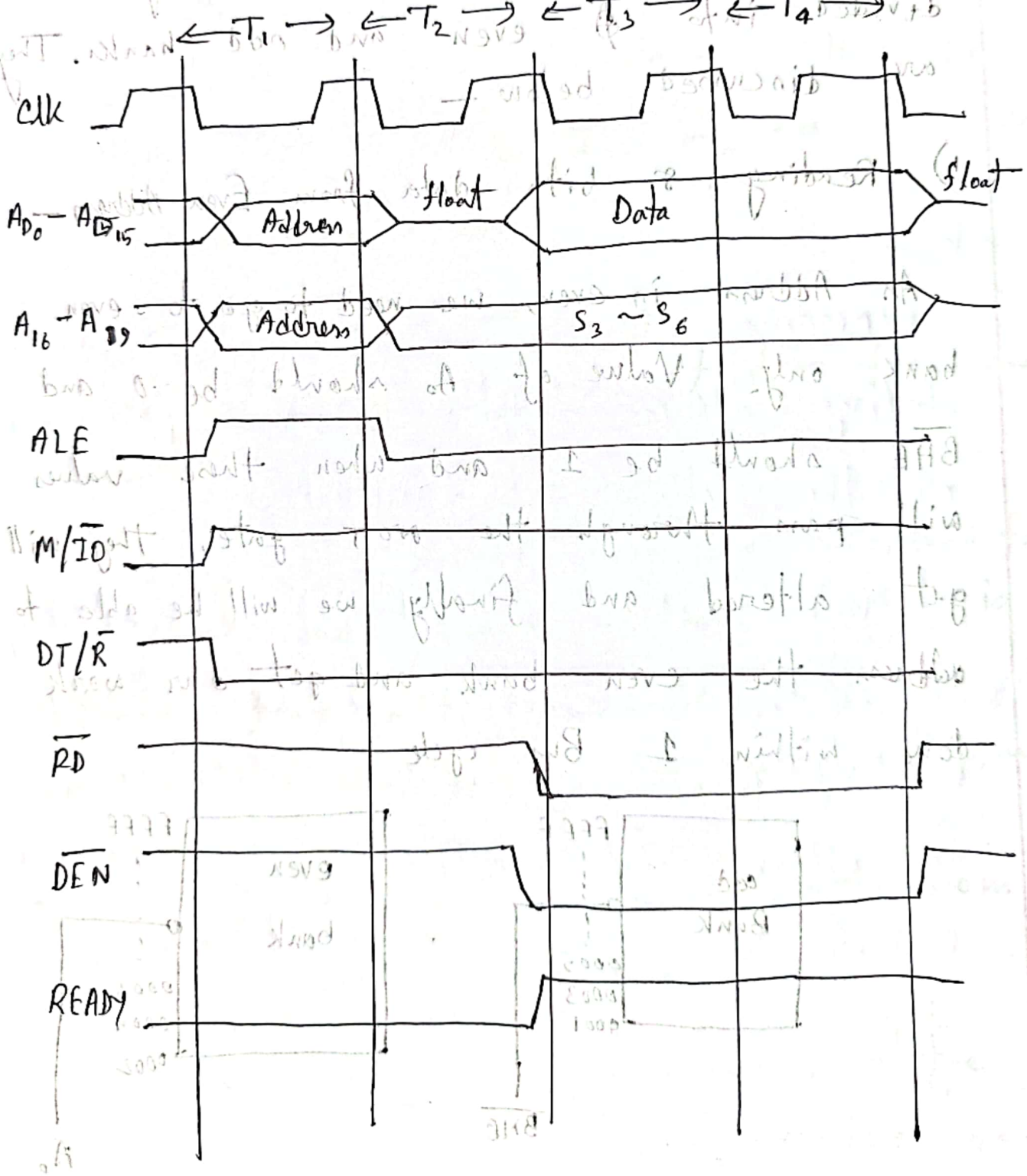
Ans

Ans to the Que No-2

(a) write cycle of an intel 8086 that is trying to write data to an external I/O →



(b) Read cycle of an intel 8086 that is trying to read data to memory ⇒

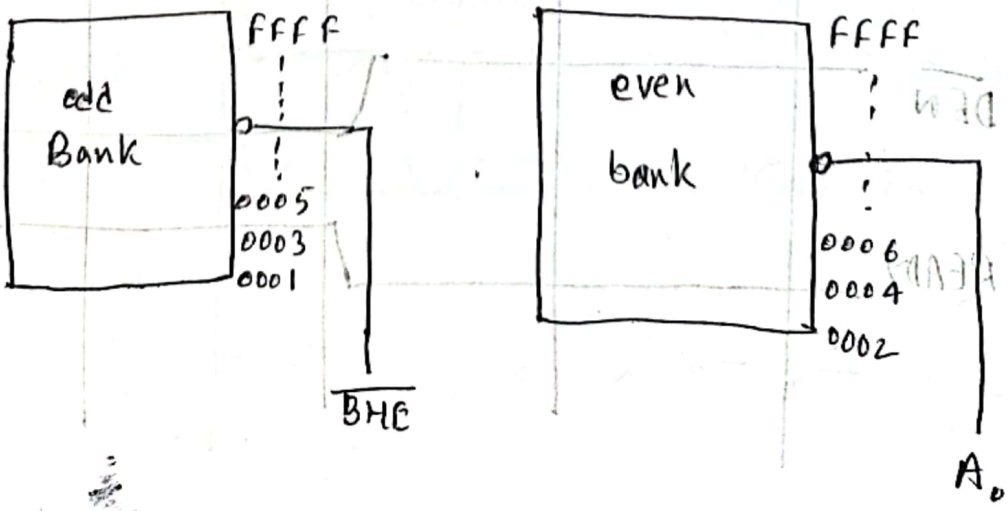


Ans to the Que No - 3

Data can be accessed from the memory in four different ways, given the memory is divided into 2 even and odd banks. They are discussed below —

1) Reading 8 bits data from Even Address —

As Address is even, we need to go to even bank only. Value of A_0 should be 0 and $\overline{BHE}$ should be 1 and when these values will pass through the NOT gate, they will get altered and finally we will be able to address the even bank and get our work done within 1 Bus cycle.



(2) Reading / Writing 8 bits of data from an odd address :—

They only bank that needs to be visited to complete this operation is odd bank as we are dealing with 8 bits of data only. Here, $\overline{BHE}$ will be 0 and A_0 will be 1. 1 bus cycle is needed the previous one.

(3) Reading / Writing 16 bits of data from even address :—

Here first 8 bits of data is retrieved from even bank and second 8 bits of data is retrieved from odd bank. So $\overline{BHE}$ and A_0 both will be 0. Only 1 bus cycle is required.

(4) Reading / Writing 16 bits of data from odd bank address :—

Here two bus cycle are required, in the first one, we enter odd bank and in the second

one, we enter even bank and get 8 bits of high byte.

1st bus cycle: $\overline{BHE} = 0$ & $A_0 = 1$

2nd bus cycle: $\overline{BHE} = 1$ & $A_0 = 0$

(b)

Accessing 16 bit data with an odd starting address require 2 bus cycle because of the allignment of data.

If we try to access a 16 bit data item starting at an odd address, the data is not alligned properly. Memory systems are often optimized for alligned accesses, that means accessing a 16 bit item from an even address is more efficient as it can be fetched in a single cycle. But, if we start at an odd

address, the memory controller may need to perform two separate accesses. One retrieve 1st byte from the odd addres and the other one retrieve the 2nd byte from even address. Thus, it requires two bus cycle instead of one.

Ans to the Que No-4

Given,

Interrupt ~~Type~~ : TYPE 123

$(123 \times 4) = (492)_d = (1EC)_h$ value

∴ location of low byte of IP is 0001ECh
∴ location of high byte of IP is 001EDh
} 16 bits IP

∴ location of low byte of CS is 001EEh
∴ location of high byte of CS is 001EFh
} 16 bits CS