SET B

CSE 341: Microprocessors
Department of Computer Science and Engineering
Brac University

Examination: Final
Duration: 1 Hour 45 Minutes

Semester: Summer 23
Full Marks: 35

Name:	ID:	Section:

1. CO2 Suppose an **8086** wants to **read 2 bytes** of **data** from an **odd memory location**. Now the memory is working at a **slower rate** than the 8086. Hence when reading the **1st byte of data**, the 8086 has to **wait** for an **additional 2 clock pulses**. But the **2nd byte** was read **without any delay**. Now assuming the 8086 is working at a **frequency** of **10MHz calculate** the following: **7**

a. The value of the **Instruction Cycle (in nanoseconds). [3]**

b. The values of A_0 and **BHE'** pins while transferring the **2 bytes** of data. **[2]**

c. The value of T_{ON} and T_{OFF} assuming the 8086 is running at a **duty cycle** of **40%. [2]**

2. CO3 Assume you have a **different version** of the **8259A Programmable Interrupt Controller (PIC)** known as **PICx** to control the numerous hardware interrupts. The **PICx** can take **14 interrupt requests** using the pins IR_0 - IR_{13}. The Interrupt Service Register (ISR) size is **X bits** and the **Interrupt Mask Register** (IMR) is **Y bits**. The IR_3 pin is **masked by default**. There are **priority levels** assigned to **each request pin**. Now suppose PICx is receiving **multiple** interrupt **requests** in the following order:

At **T= 0ns**, an interrupt request occurred at IR_{12} that will take **35ns** to be served.
At **T= 10ns**, IR_{10} and IR_3 receive requests **each** of which takes **40ns** to be served.
At **T= 25ns**, IR_0 and IR_2 receive requests **each** of which takes **50ns** to be served.

a. **Deduce** the values of **X** and **Y** [1]

b. **Explain** the role of the **Priority Resolver** in **PICx**. [1]

c. **Explain** in detail how the values of the **ISR** and **IMR** registers will change according to the above requests. [3]

d. Calculate the value of **T (time)** when all the **interrupt requests** have been **served**. [2]

3. CO3

a. **Illustrate a block diagram** showing how **multiple 8237 DMAC** can be connected in the **first-level cascading scheme. Show** only the pins relevant to the **request** and **acknowledgment.** [3] 7

b. **Analyze two** differences between **Programmed IO** and **Interrupt Driven IO.** [2]

c. Assume you have an 8237 DMAC in which the **$DREQ_0$** and **$DACK_1$** pins are **disabled.** Then **deduce** the **maximum** number of **peripheral** devices accommodated in a **first-level cascading scheme.** Also, would this number change if only the **$DREQ_2$** and **$DACK_2$** pins were disabled? Justify your answer. [2]

4. CO3 7

Address	000D4h	000D5h	000D6h	000D7h	751EBh	751ECh	751EDh	751EEh
Data	9Ch	A0h	15h	6Bh	F0h	89h	5Bh	6Eh

a. **Explain** if the interrupt caused by the **INT 53** instruction is **maskable or not.** Provide your **reasoning.** [1]

b. If the Intel 8086 encounters the **INT 53** instruction, then **calculate** the starting address of the corresponding **ISR.** Also, what will be the first 2-byte hex instruction that will be fetched to the **instruction queue** from the ISR? [2+1]

c. **Explain** in detail all the steps on how an 8086 **responds** to a signal received on the **INTR pin.** [3]

5. CO4 7

a. **Assess** the differences between the **Real Address Mode** and the **Protected Virtual Address Mode** of the **80286.** (provide 3 differences) [3]

b. Assume the **hex** value of the **access rights** of an 80286 system **descriptor** is **B2h**. Now, based on this, **evaluate** with **reasoning** which of the statements are **true/false:** [4]

i. The corresponding segment is not mapped to the physical memory.
ii. The segment will allow to ignore the DPL.
iii. The Segment is a Stack Segment that is readable.
iv. A task with a privilege level of 10 should be able to access the segment.