CSE341

Final - exam

Fall '23

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Section : 01

Set :

Ans to the Q No - 2

(A)

(i) instnaetion cyele = 160 ns

(ii) In this senanio 16 bit's and unaligned wond. So that in this case we need 2 cyele to complete this;

1 Bus cycle = $\frac{4}{2} \times 160 = 320$

(iii)

$$f = \frac{1}{160\,ns}$$

$$= \frac{1}{160 \times 10^{6} \times 10^{-9}}$$

$$= 6.25\ MHz$$

(iv) duty cycle = 20%

$$\text{duty cycle} = \frac{T_{ON}}{T_{ON} + T_{off}} \times 100$$

$$\Rightarrow \text{~~duty cycle~~ } 20 = \frac{T_{ON}}{T_{ON} + T_{off}} \times 100$$

$$\therefore T_{ON} + T_{off} = 20\,T_{ON} \times 100$$

(iv) duty cycte = 20 %.

$$0.2 = \frac{T_{ON}}{T_{ON} + T_{OW}}$$

$$\therefore \quad 0.2\,T_{OW} + 0.2\,T_{OFF} = T_{ON}$$

$$T_{ON} - 0.2\,T_{ON} = 0.2\,T_{OFF}$$

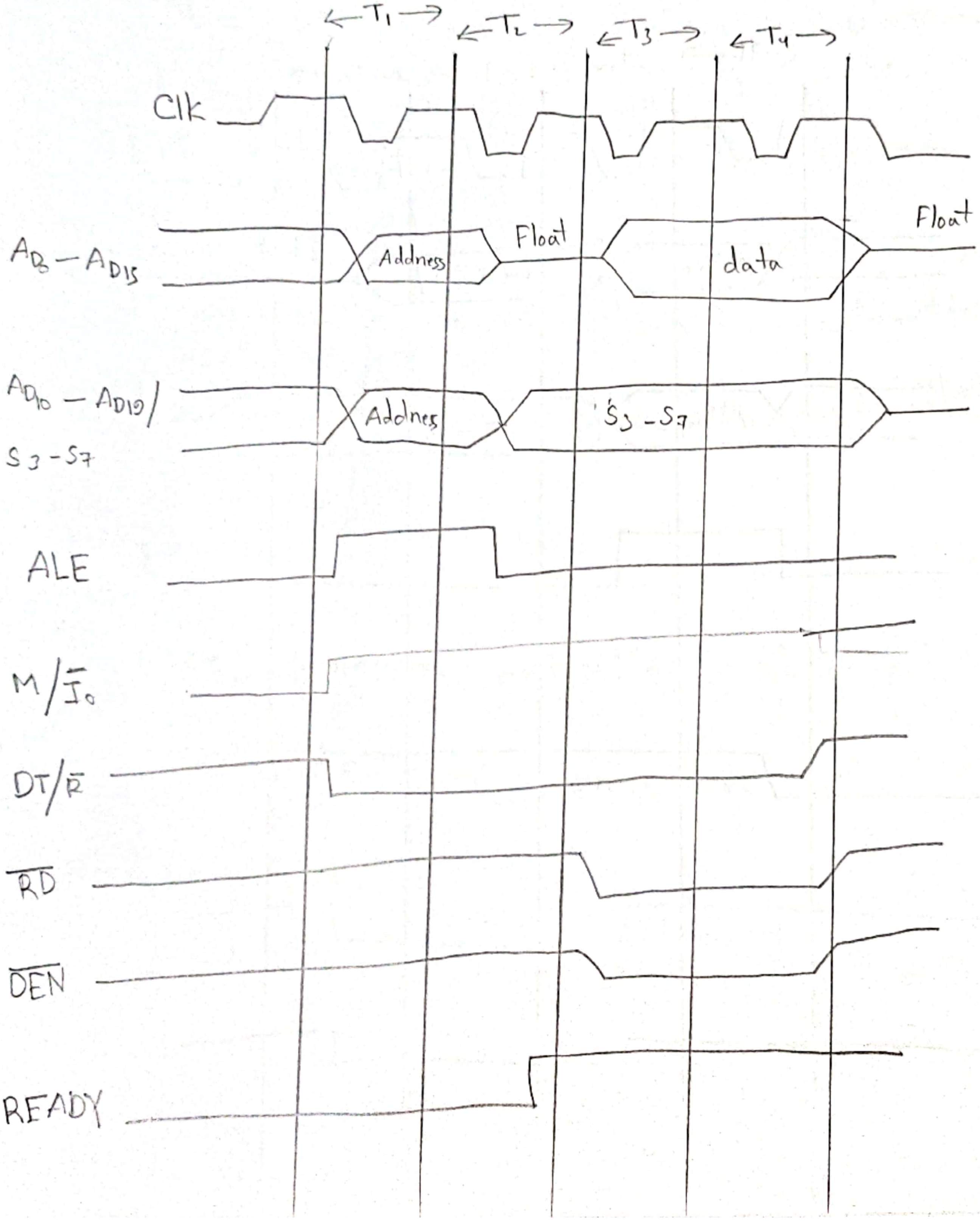
$$\Rightarrow \quad 0.8\,T_{ON} = 0.2\,T_{OFF}$$

$$\therefore \quad T_{ON} = \frac{0.2}{0.8}\,T_{OFF}$$

$$= \frac{1}{4}\,T_{OFF}$$

(B)

This is a nead and memony use here



(c)

80286 micno pnocesson EM and MP

EM = PRocesson execution emulaton.

MP = Moniton pnocesson enecution -

mp ane allow to wait instnaction to genanate a pnocesson entention

and

EM= pnocesson entention absence the emalaate of pnocesson extention by cpu.

Ans to the Q No — 4

(A)

T = ~~30~~40 ns → IRG → 50 ns

T = 17 ns → IRS → 20 ns

T = 27 ns → IR7

↳ IR0] ⟶ 37 ns

T_1 = 10

IRR = IRG = 7

∴ ISR = IRG = 1

∴ 10 + 7 = 17

∴ IRG = 30 − 7 = 43 ns

$T_1 = 10$

IRR = IR6 = 7

ISR = IR6 = 7

10 + 7 = 17

time left of IR6 = 50 − 7 = 43 ns

$T_1 =$ 17 ns

∴ IR5 > IR6 ∴ ISR will ~~s~~nesened

17 + 10 = 27 | IR5 = 20 − 10 = 10ns

again IR7 and IR0 annived

IR0 > IR5 ∴ IR0 will be sened

$T_2 =$ 27 + 37 = 64 ns

IR5 > IR7

IR5 will Seneed

$T_2 = 64 + 6 = 74$

IR6 > IR 7

$\therefore T_2 = 74 + 37 = 111$ ns

Aften 111 ns IR6 will conplotity served.

(b)

IRR :

	1					1	1
IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0

ISR :

						1	1
Ir	Ir	Ir5	Ir4	Ir3	Ir2	Ir1	Ir0

IMR :

I4	Ie4	Ir3	Ir	Ir	Ir	IR	IR0

when a intenup anmied at 8259 A DIe it ult neele thnough the IR Pin. The pnionity of the pin ane IR0 most pnionity the othen and the ~~alat~~ lost pnionity will be IR_7.

IR6, IRo will senea fret

IRO) IR6

IRR = IRO =1

IRR = IR6 =1

again ISR = ISRO = 1

after serving the intennupt anive though pin IRo, IRo will sene,

ISR = ISR6 =1

50 internupt .

IR_0 — 8

IR_1 — 8

IR_2 — 8

IR_3 — 8

IR_4 — 8

IR_5 — 8

I_6

I_7

1 master + 6 slave

= 7 total PICs .

Ans to the Q No-3

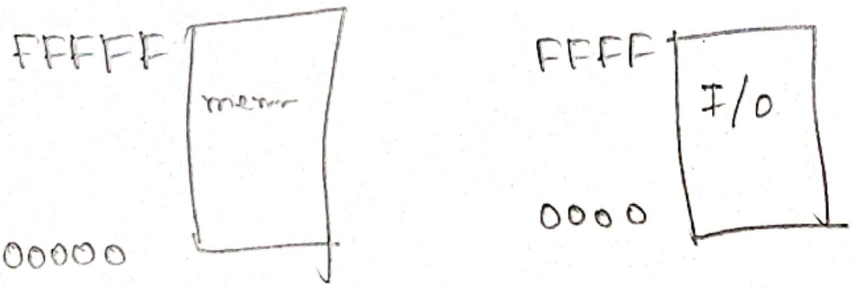
(a)

① OUT 1234 h, Ax this are invalied.

For this will 1234 h is not ~~an~~ a memory address. That's why this is invalid

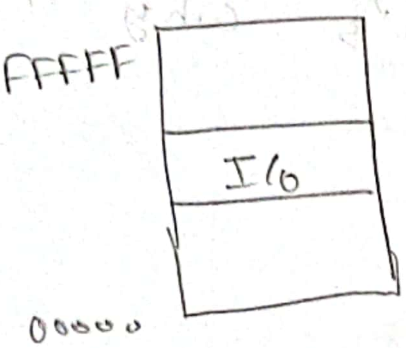
(B)

In ~~ii)~~ ii) out Dx, Ax this is a addressing maping (Isolated I/O). In this case use different memory for the I/O.



For this we use 4 ~~ins~~ ~~bit~~ byte

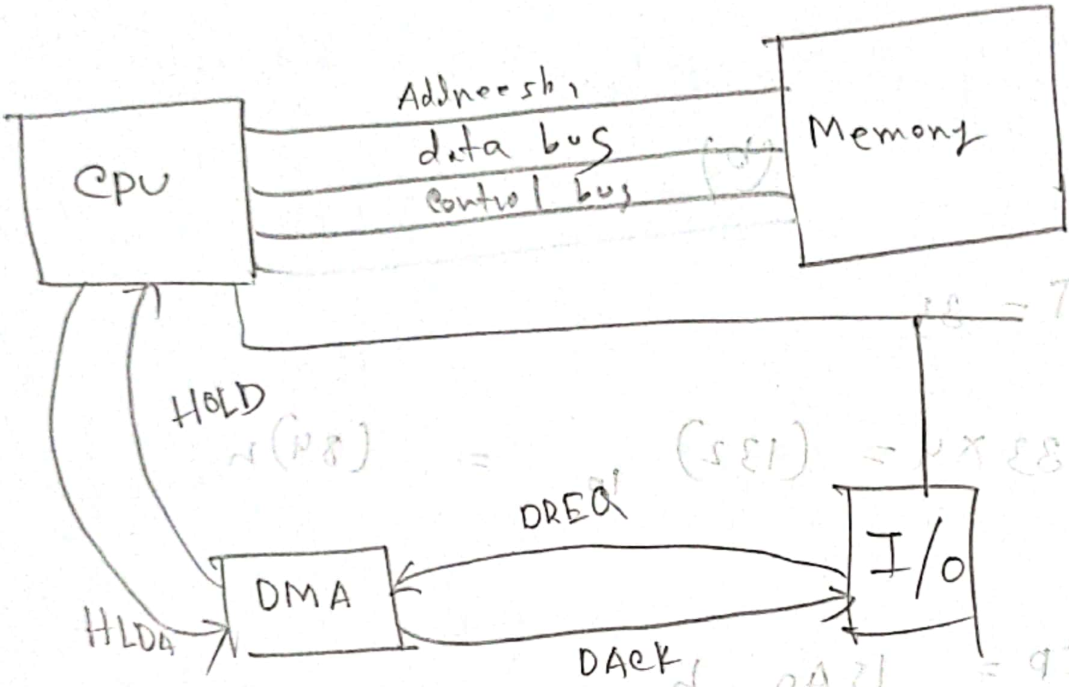
In the iii] mov [1234h], AX in this instraction we use memory mapped I/O .



In this case we use a memory ~~to~~ for I/O. For this reason we can access it from mov instruction.

(c)

Dineeft memony aceecs



Ans to the Q No- I

(a)

1 kb of menony on 00000h 003FF h

(b)

INT = 33

$33 \times 4 = (132)_{10} = (84)_h$

IP = 15A0 h

CS = 1A02 h

P.A = CS × 10 + IP

= 1B5C0 h

1B5C0 data= 5Bh

1B5C1 " = 6Fh

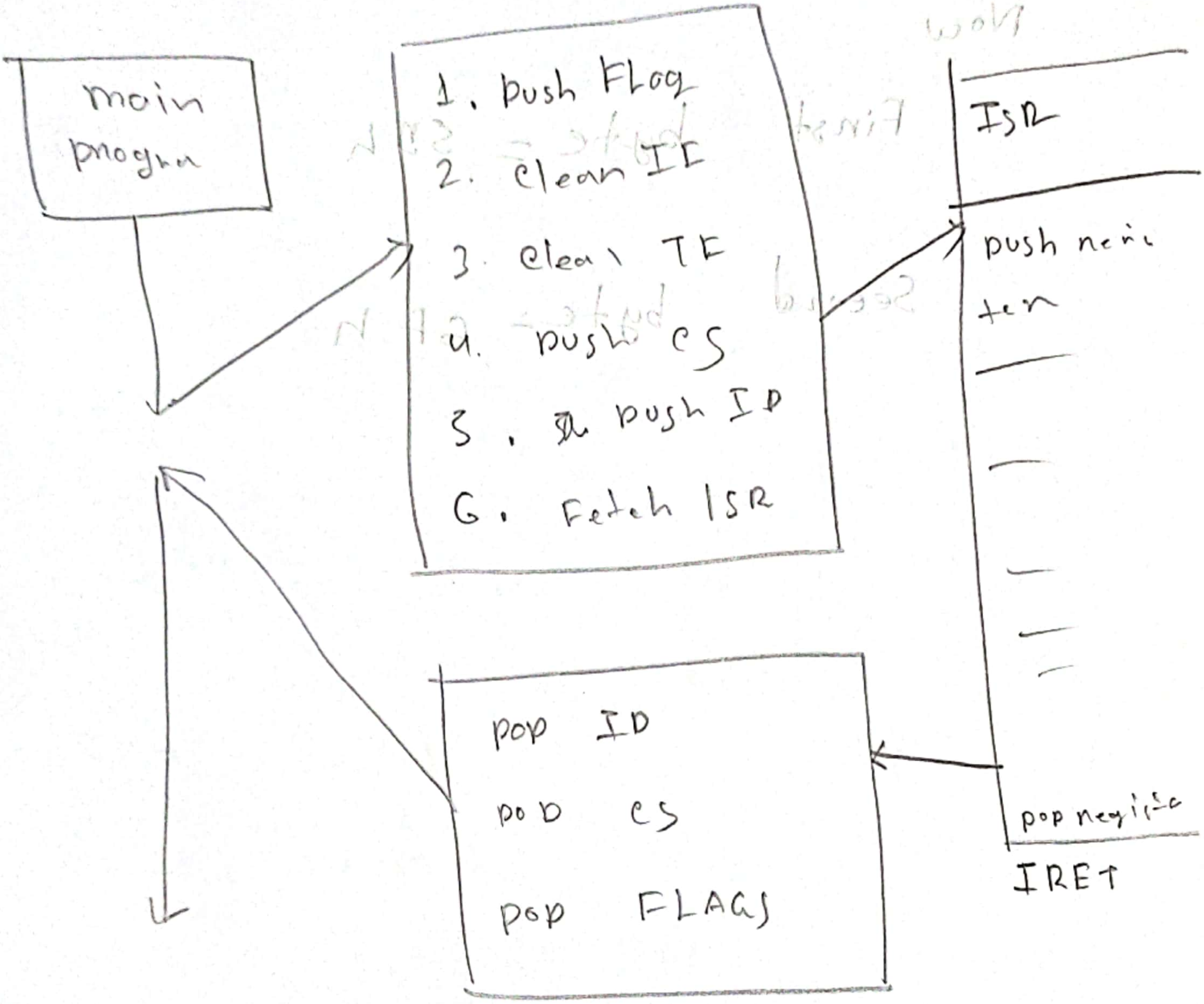
Now

First byte = 5Bh

Second byte = 6Fh

(c)

Interrupt in 8086 pin.



This is the diagram how interrupt in 8086 works.