CSE 341: Microprocessors
Department of Computer Science and Engineering
Brac University

Examination: Final | Semester: Fall 23
Duration: 1 Hour 30 Minutes | Full Marks: 30

1. CO3 **8**

Addr.	84h	85h	86h	87h	17401h	17402h	132h	133h	134h	135h
Data	A0h	15h	02h	1Ah	5Bh	6Eh	11h	23h	ACh	54h

A. **Deduce** the size of the **Interrupt Vector Table** (IVT) of the Intel 8086. [1]

B. **Calculate** the **interrupt vector** of the **ISR** corresponding to the interrupt caused by **INT 33**. Also, deduce the first **2-byte** hex instruction that will be fetched to the instruction queue from the ISR. [3+1 = 4]

C. **Explain** in detail the **actions** taken by **8086** when responding to an **interrupt** request in the **INTR** pin. [3]

2. CO2 CO4 **10**

A. **Suppose** you have an **8086** microprocessor that takes **160ns** to **fetch**, **decode**, and **execute** an instruction that asks to take in **16 bits** of **data** from an **unaligned** word and store it inside the **DX** register. Now **deduce** the following based on the given information (show all necessary calculations):

i. Length of **1 instruction cycle** for the aforementioned instruction. [1]
ii. Time for **1 Bus cycle** for the 8086. [1]
iii. **Frequency** at which the 8086 operates. [2]
iv. Time for $\mathbf{T_{ON}}$ and $\mathbf{T_{OFF}}$ (duty cycle = 20%). [1]

B. **Illustrate** the timing diagram for the aforementioned operation (in question A) showcasing the $\mathbf{AD_0}$ **-** $\mathbf{AD_{15}}$, **ALE**, **RD'/WR', Ready** (use either read or write), and **M/IO'** (use either memory or I/O) pins. [3]

C. **Explain** what it would mean for an **80286** microprocessor to have both **EM** and **MP** bits set to **1**. [2]

3. CO3 **(i) OUT 1234h, AX** **(ii) OUT DX, AX where DX = 1234h** **(iii) MOV [1234h], AX** **9**

Assuming **1234h** represents an address that points to a peripheral, answer questions A and B

A. **Deduce** if any of these instructions are **invalid** or **not**. Provide your **reasons**. [2]

B. **Explain** in detail how the **I/O addressing** technique showcased in the **2nd** instruction is different from the one showcased in the **3rd** instruction. [3]

C. Suppose, you are running an **Intel 8086** with an **8237 DMA controller**. Now assume a scenario where an **I/O** device **requests** the DMA to initiate a **transfer of data** with the **memory**. The DMA controller understands that a **DMA read operation** will take place. **Explain** how this operation will take between the **DMA**, **I/O**, **memory**, and the **8086**. Also **elaborate** on the **values** of the **HRQ**, **HLDA**, **DREQ**, **DACK**, **IOR'**, **IOW'**, **MEMR'**, and **MEMW'** pins at **each stage** of the process. [4]

4. CO3 In a **real-time** control system utilizing a **microcontroller** with the **8259A Programmable Interrupt Controller** (PIC), a critical situation arises where **four devices** simultaneously trigger **interrupts**. The 8259A is currently in **fixed priority** mode. Now answer questions A, B, and C. **8**

A. At **T = 10ns**, **IR6** receives an **interrupt**. The CPU will take **50ns** to serve that interrupt. However, at **T = 17ns**, an interrupt occurs at **IR5** which requires **20ns** to get served. At **T = 27ns**, **two** interrupt requests occur at **IR7** and **IR0** respectively. **Each** of the interrupts will require **37ns** to get served. **Deduce** the value of **T** when the interrupt at **IR6** is served **completely**. [3]

B. **Explain** how a particular interrupt gets served when a **high signal** is received at any of the **IR** pins of the **8259A PIC**. [4]

C. **Estimate** the **minimum** number of PICs (master + slave) required to get **50** interrupt requests at a **time**. [1]