Preliminary

MY9221

12-Channel LED Driver With Grayscale Adaptive Pulse Density Modulation Control

General Description

The MY9221, 12-channels (R/G/B x 4) constant current APDM (Adaptive Pulse Density Modulation) LED driver, operates over a 3V ~ 5.5V input voltage range. The device provides 12 open-drain constant current sinking outputs that are rated to 17V and delivers up to 60mA of high accuracy current to each string of LED. The current at each output is programmable by means of three external current setting resistors. MY9221 features a 10MHz EMI reduction data clock input. MY9221 also offers a 2-wire serial interface to send the grayscale data, control command including 16/14/12/8-bit grayscale selection, grayscale clock frequency division selection, output polarity selection for high power LED driving, output Tr/Tf timing selection, current output waveform selection, and to realize the internal-latch function. MY9221 provides adaptive pulse density modulation method to increase the visual refresh rate up to 1000 Hz @ 16-bit grayscale and reduce the flickers, and it also provides output current bilateral processing for EMI reduction. Moreover MY9221 utilizes clock duty recovery technique and pulse re-timing to help long distance and multiple cascading applications. MY9221 provides typical ±1% channel-to-channel LED current accuracy. Additional features include a ±0.1% regulated output current capability and fast output transient response. MY9221 is available in a 20-pin QFN or 24-pin SSOP/TSSOP package and specified over the -40°C to +85°C ambient temperature range.

Features

- 3 ~ 5.5V Operating supply voltage
- R/G/B x4 Output Channels
- 3~60mA@5V Constant current output range
- 3~35mA@3.3V Constant current output range
- Current setting by 3 external resistors
- 17V Rated output channels for long LED strings
- ±1%(typ.) LED Current accuracy between channels
- ±2%(typ.) LED Current accuracy between chips
- 10MHz(max.) ~ 70 KHz(min.) clock frequency for EMI reduction data transfer [patent pending] (compatible with traditional 20MHz(max.))
- 16 / 14 / 12 / 8 bit grayscale selection
- Built-in internal grayscale clock supports refresh rate >1000Hz@16-bit grayscale, >256KHz@8-bit grayscale
- Grayscale clock frequency selection for High Power LED driving application (min. 33.6KHz)
- Grayscale clock source selection (SSOP & TSSOP only): internal or external
- PWM or APDM control selection [patent pending]
- Clock duty recovery for cascading application
- Schmitt trigger input
- Output Current Tr / Tf programmable
- Output Current Bilateral Processing for EMI reduction
- -40°C to +85°C Ambient temperature range

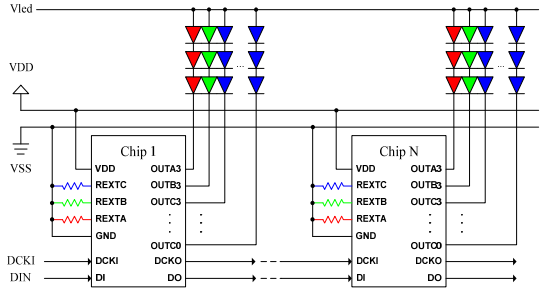
Applications

- Indoor and Outdoor LED Video Displays
- Full Color Mesh Display
- Full Color Dot Matrix Module
- Architectural and Decorative Lighting
- LCD Display Backlighting

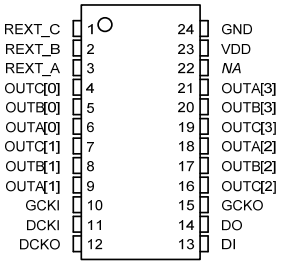
Order information

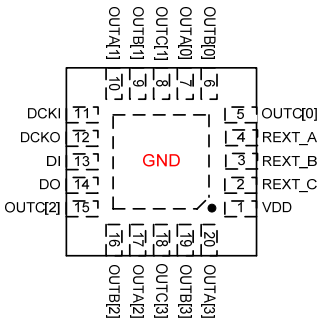
Part	Package Information	
MY9221SS	SSOP24-150mil-0.635mm	2500 pcs/Reel
MY9221QD	QFN20-4mmx4mm-0.5mm	3000 pcs/Reel
MY9221TE	TSSOP24-173mil-0.65mm (Exposed Pad)	2500 pcs/Reel

Typical Operating Circuits



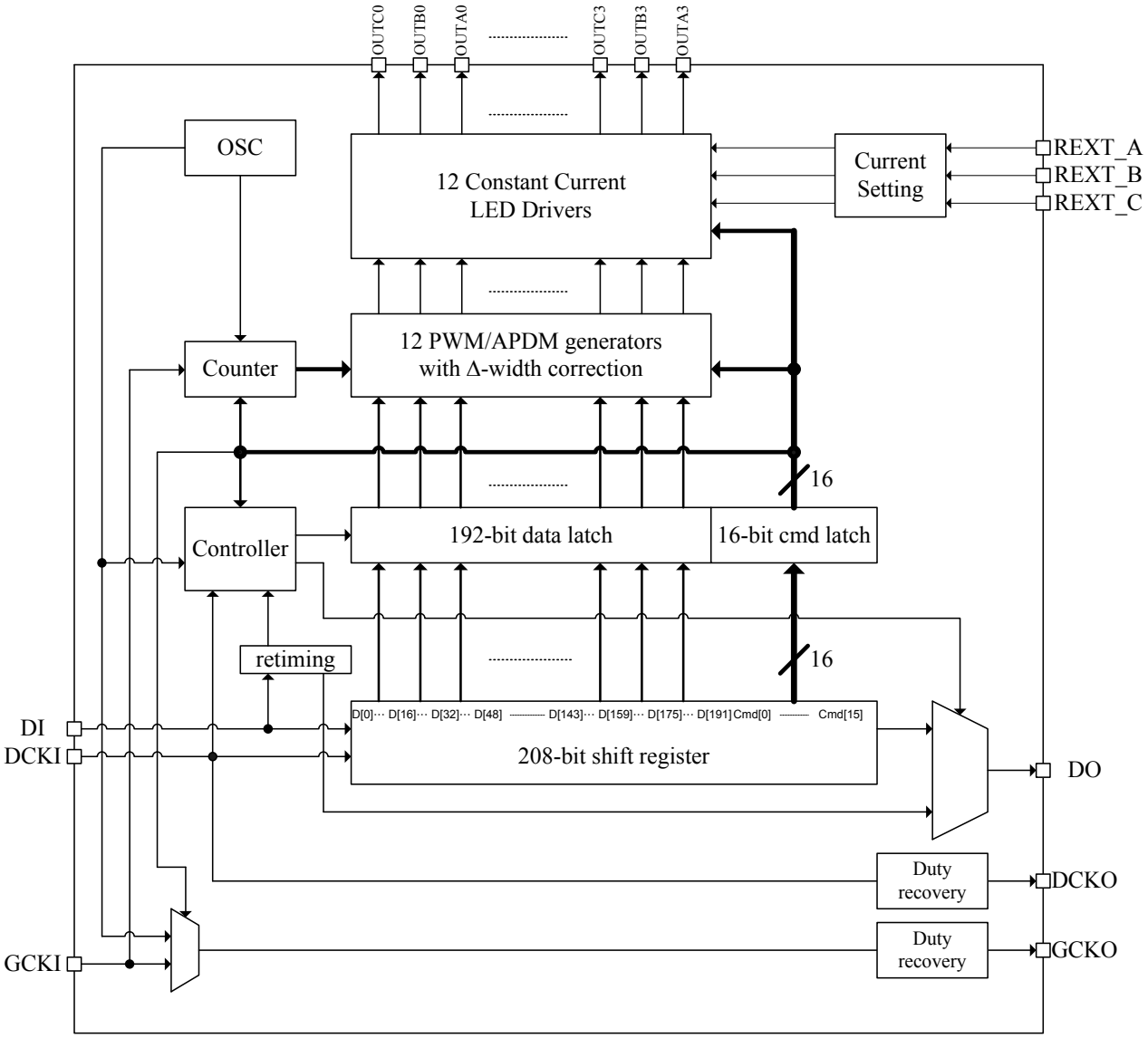
Pin Configuration





For pricing, delivery, and ordering information, please contact MY-Semi Inc. at +886-3-658-5656, or email to INFO@MY-Semi.com.tw or visit MY-Semi's website at www.MY-Semi.com or www.MY-Semi.com.tw

Block Diagram

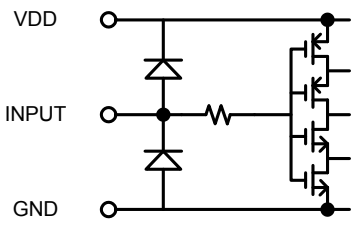


Pin Description

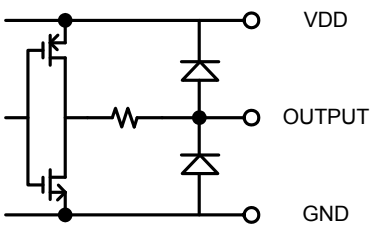
PIN No.		PIN NAME	FUNCTION
SSOP24 TSSOP24	QFN20		
1,2,3	2,3,4	REXT_C,B,A	External resistors connected between REXT and GND for individual output current value setting.
19,16,7,4	18,15,8,5	OUTC[3:0]	Constant current outputs.
20,17,8,5	19,16,9,6	OUTB[3:0]	
21,18,9,6	20,17,10,7	OUTA[3:0]	
10	---	GCKI	External grayscale clock input for PWM/APDM operation.
11	11	DCKI	Clock input terminal for serial data transfer. Data is sampled at both rising edge and falling edge of DCKI.
12	12	DCKO	Clock output terminal for serial data transfer.
13	13	DI	Serial data input terminal.
14	14	DO	Serial data output terminal.
15	---	GCKO	Grayscale clock output When command data “osc” = ‘L’, GCKO comes from internal osc When command data “osc” = ‘H’, GCKO comes from GCKI
23	1	VDD	Supply voltage terminal.
24	Thermal pad	GND	Ground terminal.
22	---	NA	Not used

Equivalent Circuit of Inputs and Outputs

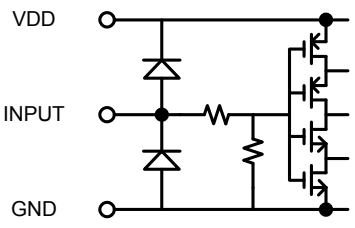
1. DI, DCKI terminals



2. DO, DCKO, GCKO terminals



3. GCKI terminal



Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	VDD	-0.3 ~ 7.0	V
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Output Current	IOUT	60	mA
Output Voltage	VOUT	-0.3 ~ 17	V
Input Clock Frequency	FDCK	0.07 ~ 10	MHz
GND Terminal Current	IGND	750	mA
Thermal Resistance (4 Layer PCB)	Rth(j-a)	70.5 (SSOP24-150mil-0.635mm) 43 (QFN20-4mmx4mm) 31 (TSSOP24-173mil-0.65mm (EP))	°C/W
Operating Supply Voltage	VDD	3.0 ~ 5.5	V
Operating Ambient Temperature	Top	-40 ~ 85	°C
Storage Temperature	Tstg	-55 ~ 150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other condition beyond those specified is not supported.

(2) All voltage values are with respect to ground terminal.

Electrical Characteristics (VDD = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 4.8 mA	—	—	0.4	V
	VOH	IOH= 5.3 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 2340 Ω	—	±1	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±2	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 19.5 KΩ	—	±1	±3	%
Output Current Skew (Chip-to-Chip)*2	dIOUT4		—	±2	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 2340 Ω VOUT = 1 V ~ 3 V	—	±.0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 2340 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	2.40	—	mA
	$I_{DD2(off)}$	input signal is static Rrext = 2340 Ω all outputs turn off	—	5.73	—	
	$I_{DD3(on)}$	input signal is static Rrext = 2340 Ω all outputs turn on	—	5.85	—	
	$I_{DD4(off)}$	input signal is static Rrext = 19.5 KΩ all outputs turn off	—	2.84	—	
	$I_{DD5(on)}$	input signal is static Rrext = 19.5 KΩ all outputs turn on	—	2.84	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_3)}{4}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\left(\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_3)}{4} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right) \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Electrical Characteristics (VDD = 3.3 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	VIH	CMOS logic level	0.7VDD	—	VDD	V
Input Voltage "L" Level	VIL	CMOS logic level	GND	—	0.3VDD	
Output Leakage Current	ILK	VOUT = 17 V	—	—	0.1	uA
Output Voltage (DO)	VOL	IOL = 3.9 mA	—	—	0.4	V
	VOH	IOH= 3.8 mA	VDD-0.4	—	—	
Output Current Skew (Channel-to-Channel) *1	dIOUT1	VOUT = 1.0 V Rrext = 2340 Ω	—	±1	±3	%
Output Current Skew (Chip-to-Chip) *2	dIOUT2		—	±2	±6	%
Output Current Skew (Channel-to-Channel)*1	dIOUT3	VOUT = 1.0 V Rrext = 19.5 KΩ	—	±1	±3	%
Output Current Skew (Channel-to-Channel)*2	dIOUT4			±2	±6	%
Output Voltage Regulation*3	% / VOUT	Rrext = 2340 Ω VOUT = 1 V ~ 3 V	—	±0.1	—	% / V
Supply Voltage Regulation*4	% / VDD	Rrext = 2340 Ω VDD = 3 V ~ 5.5 V	—	±0.6	±1	
Supply Current *5	$I_{DD1(off)}$	all pins are open unless VDD and GND	—	1.97	—	mA
	$I_{DD2(off)}$	input signal is static Rrext = 2340 Ω all outputs turn off	—	5.22	—	
	$I_{DD3(on)}$	input signal is static Rrext = 2340 Ω all outputs turn on	—	5.22	—	
	$I_{DD4(off)}$	input signal is static Rrext = 19.5 KΩ all outputs turn off	—	2.74	—	
	$I_{DD5(on)}$	input signal is static Rrext = 19.5 KΩ all outputs turn on	—	2.79	—	

*1 Channel-to-channel skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{Iout_n}{\frac{(Iout_0 + Iout_1 + \ldots + Iout_3)}{4}} - 1 \right] * 100\%$$

*2 Chip-to-Chip skew is defined by the formula below:

$$\Delta(\%) = \left[\frac{\frac{(Iout_0 + Iout_1 + \ldots + Iout_3)}{4} - (Ideal\ \ Output\ \ Current)}{(Ideal\ \ Output\ \ Current)} \right] * 100\%$$

*3 Output voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@Vout_n = 3V) - Iout_n(@Vout_n = 1V)}{Iout_n(@Vout_n = 3V)} \right] * \frac{100\%}{3V - 1V}$$

*4 Supply voltage regulation is defined by the formula below:

$$\Delta(\%/V) = \left[\frac{Iout_n(@V_{DD} = 5.5V) - Iout_n(@V_{DD} = 3V)}{Iout_n(@Vcc = 3V)} \right] * \frac{100\%}{5.5V - 3V}$$

*5 IO excluded.

Switching Characteristics (VDD = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	DCKI-to-DO	tpLH1	VIH = VDD VIL = GND Rrext = 2340 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	29	39	ns
	DCKI-to-DCKO	tpLH2		—	6.3	19	
	GCKI-to-GCKO	tpLH3		—	10.5	19	
	DI-to-DO @ Internal-latch control cycle	tpLH4		—	12	—	
Propagation Delay ('H' to 'L')	DCKI-to-DO	tpHL1		—	39	59	
	DCKI-to-DCKO	tpHL2		—	6.3	19	
	GCKI-to-GCKO	tpHL3		—	9	19	
Pulse Duration	DCKI	$tw_{(DCK)}$		50	—	7200	
	GCKI	$tw_{(GCK)}$		50	—	—	
	DI @ Internal-latch control cycle	$twH_{(DI)}$		70	—	—	
	DI @ Internal-latch control cycle	$twL_{(DI)}$		230	—	—	
Setup Time	DI	$tsu_{(D)}$		10	—	—	
Hold Time	DI	$th_{(D)}$		10	—	—	
DO/DCKO/GCKO Rise Time		$tr_{(DO)}$		—	5	—	
DO/DCKO/GCKO Fall Time		$tf_{(DO)}$		—	5	—	
Output Current Rise Time (fast)		Tor_f		—	10	—	
Output Current Fall Time (fast)		Tof_f		—	4	—	
Output Current Rise Time (slow)		Tor_s		—	90	—	
Output Current Fall Time (slow)		Tof_s		—	66	—	
DI Retiming @ Internal-latch control cycle		Tw_re		70	90	110	
Internal-latch Start Time		Tstart		12	—	—	us
Internal-latch Stop Time*		Tstop		200	—	—	ns
DCKI Freq.		F(DCKI)		0.07	—	10	MHz
Internal OSC Freq.		F(OSC)		6.9	8.6	10.3	MHz
GCKI Freq.		F(GCKI)		—	—	10	MHz

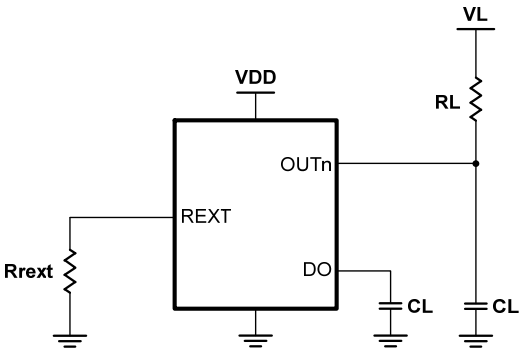
* Tstop (min.) for cascade application must > "200ns + N*10ns" (N is the cascade number of drivers)

Switching Characteristics (VDD = 3.3V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay ('L to 'H')	DCKI-to-DO	tpLH1	VIH = VDD VIL = GND Rrext = 2340 Ω VL =5.0 V RL = 150 Ω CL = 13 pF	—	34	39	ns
	DCKI-to-DCKO	tpLH2		—	7.9	19	
	GCKI-to-GCKO	tpLH3		—	12	19	
	DI-to-DO @ Internal-latch control cycle	tpLH4		—	18	—	
Propagation Delay ('H' to 'L')	DCKI-to-DO	tpHL1		—	40	59	
	DCKI-to-DCKO	tpHL2		—	8.2	19	
	GCKI-to-GCKO	tpHL3		—	10.5	19	
Pulse Duration	DCKI	$tw_{(DCK)}$		50	—	7200	
	GCKI	$tw_{(GCK)}$		50	—	—	
	DI @ Internal-latch control cycle	$twH_{(DI)}$		70	—	—	
	DI @ Internal-latch control cycle	$twL_{(DI)}$		230	—	—	
Setup Time	DI	$tsu_{(D)}$		10	—	—	
Hold Time	DI	$th_{(D)}$		10	—	—	
DO/DCKO/GCKO Rise Time		$tr_{(DO)}$		—	8.5	—	
DO/DCKO/GCKO Fall Time		$tf_{(DO)}$		—	8.5	—	
Output Current Rise Time (fast)		Tor_f		—	13.4	—	
Output Current Fall Time (fast)		Tof_f		—	7.5	—	
Output Current Rise Time (slow)		Tor_s		—	153	—	
Output Current Fall Time (slow)		Tof_s		—	77	—	
DI Retiming @ Internal-latch control cycle		Tw_re		90	110	130	
Internal-latch Start Time		Tstart		12	—	—	us
Internal-latch Stop Time*		Tstop		200	—	—	ns
DCKI Freq.		F(DCKI)		0.07	—	10	MHz
Internal OSC Freq.		F(OSC)		6.7	8.4	10.1	MHz
GCKI Freq.		F(GCKI)		—	—	10	MHz

* Tstop (min.) for cascade application must > "200ns + N*10ns" (N is the cascade number of drivers)

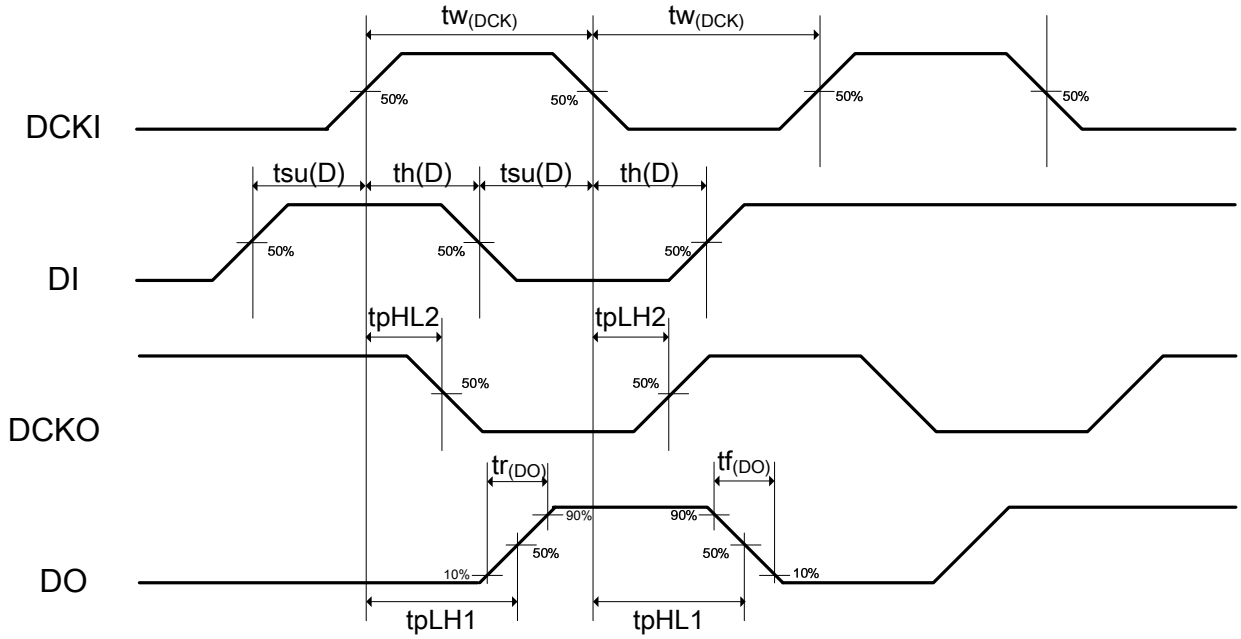
Switching Characteristics Test Circuit



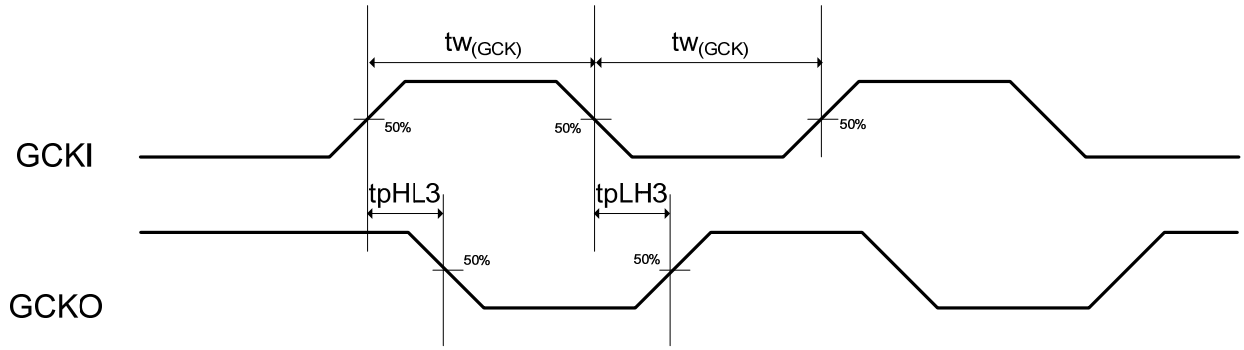
Switching Characteristics Test Circuit

Timing Diagram

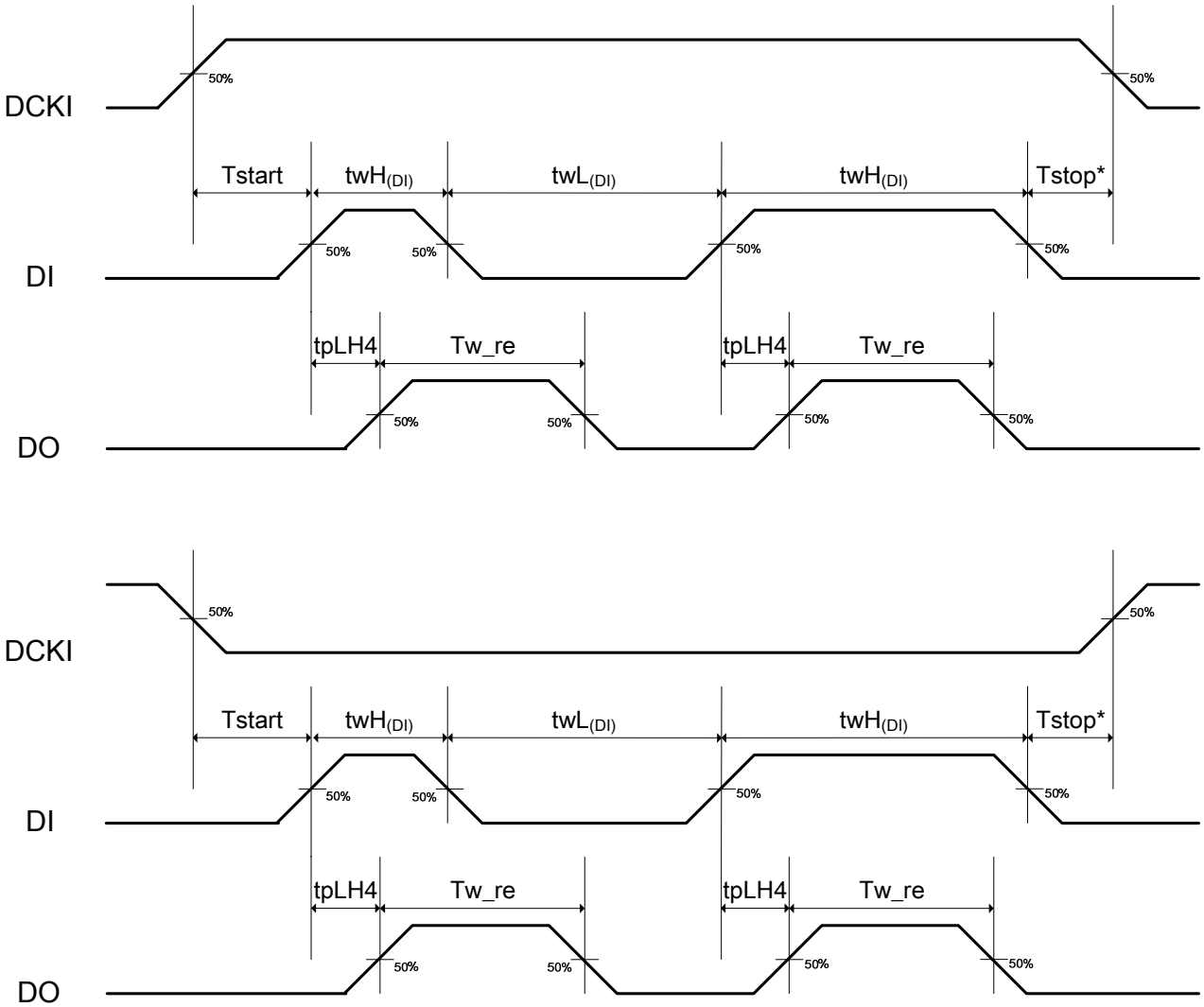
1. DCKI, DCKO - DI, DO



2. GCKI-GCKO



3. DCKI-DI & DI-DO @ Internal-latch control cycle



* Tstop (min.) for cascade application must > “200ns + N*10ns” (N is the cascade number of drivers)

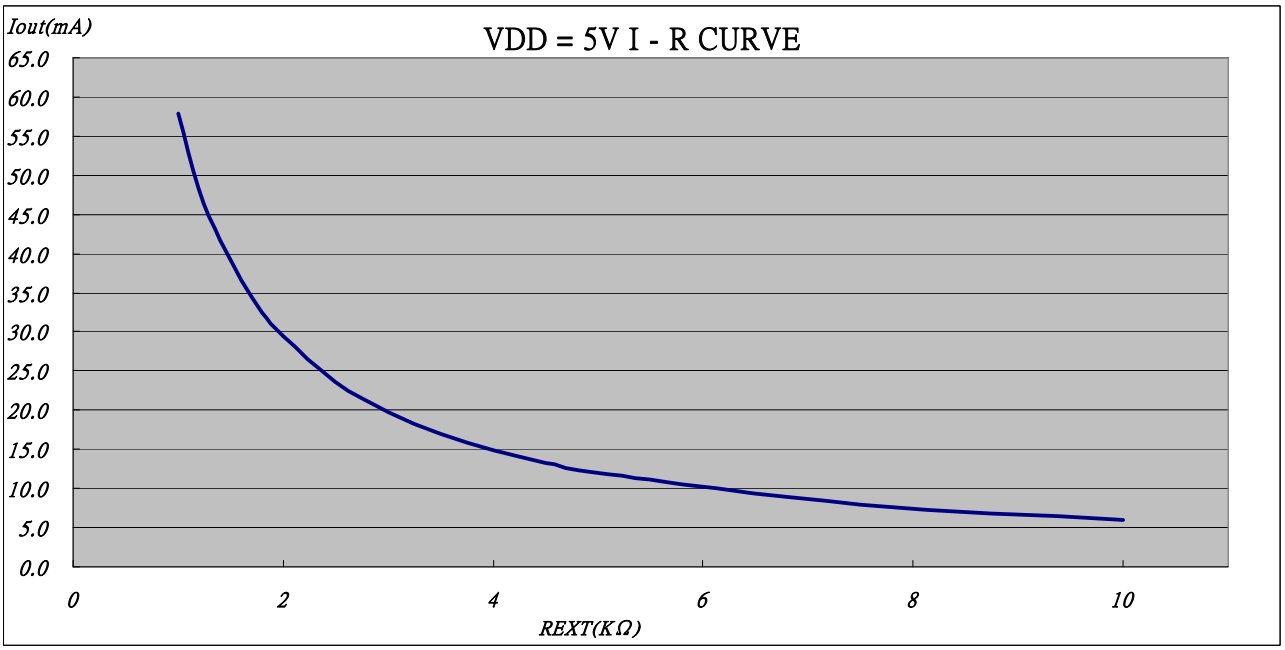
Reference Resistor

The constant current values are determined by an external resistor placed between REXT pin and GND pin. The following formula is utilized to calculate the current value:

$$Iout(mA) = \frac{1.28 * 45.5}{Rrext \quad (K\Omega)}$$

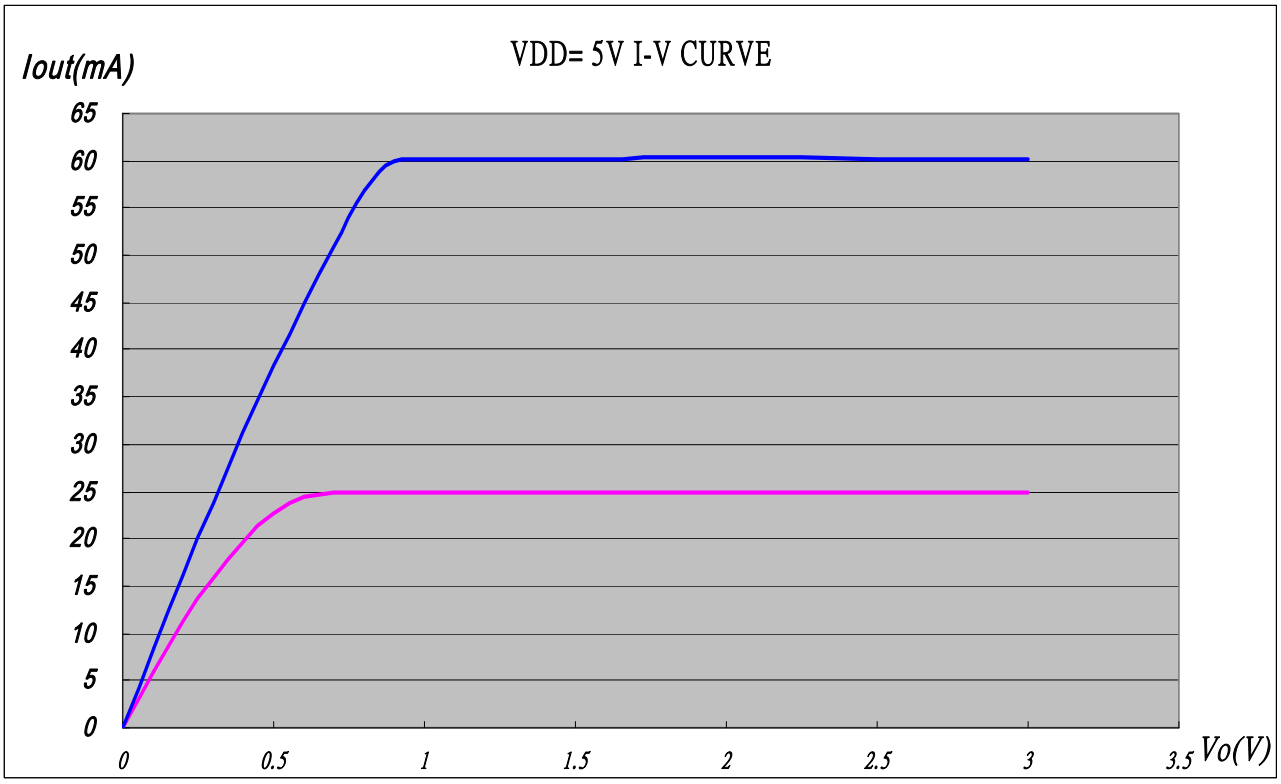
Where Rrext is a resistor placed between REXT and GND

For example, Iout is 25mA when Rrext=2340Ω and Iout is 3mA when Rrext=19.5 KΩ



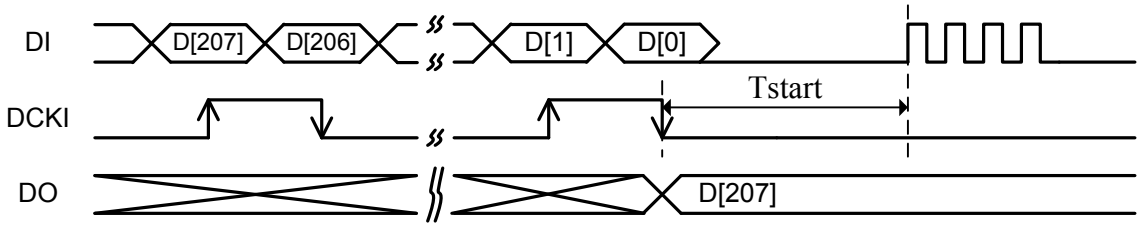
Constant-Current Output

The current characteristics could maintain invariable in the influence of loading voltage. Therefore, the MY9221 could minimize the interference of different LED forward voltages and produce the constant current. The following figures illustrate the suitable output voltage should be determined in order to keep an excellent performance.



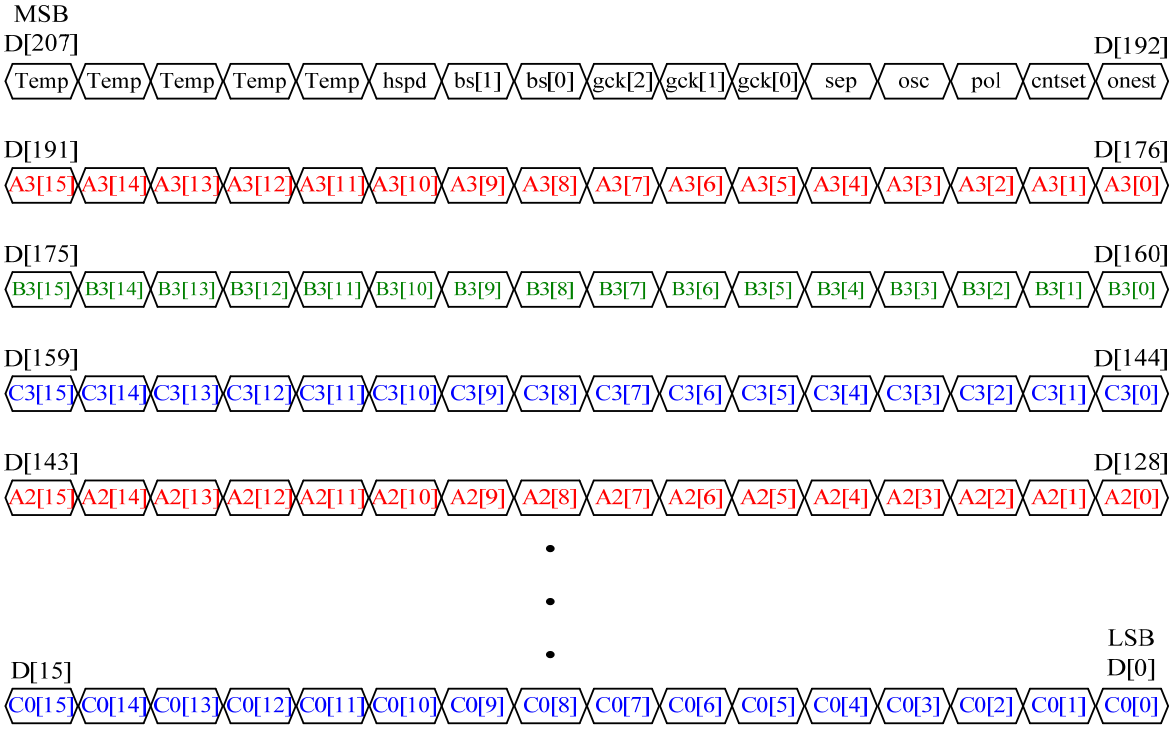
Serial Data Interface

The MY9221 transmits data from the DI pin on both rising and falling edge of the data clock (DCKI). After whole given serial data are shifted into 208-bit shift register, then the data can be loaded into the latch register by internal-latch function. The serial data will be shifted out from the DO pin on the synchronization of the rising and falling edge of DCKI.



Data Format

16-bit command data and 12x16-bit PWM data. (Total: 208-bit)



16-bit Command Data Description (CMD[15:0]) = D[207:192])

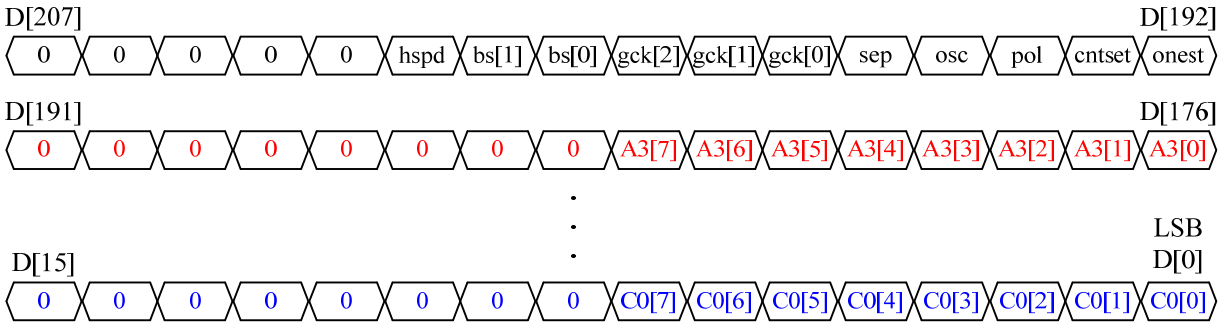
BIT No.	Name	DESCRIPTION	FUNCTION
CMD[15:11]	Temp	Not used	Please filled with all “0”
CMD[10]	hspd	Iout Tr/Tf select	0 : Iout slow mode 1 : Iout fast mode
CMD[9:8]	bs[1:0]	Grayscale resolution select	00 : 8-bit grayscale application 01 : 12-bit grayscale application 10 : 14-bit grayscale application 11 : 16-bit grayscale application
CMD[7:5]	gck[2:0]	Grayscale clock freq. select	000 : original freq. 001 : original freq/2 010 : original freq/4 011 : original freq/8 100 : original freq/16 101 : original freq64 110 : original freq/128 111 : original freq/256
CMD[4]	sep	Output waveform select	0 : MY-PWM output waveform (similar to traditional waveform) 1 : APDM output waveform
CMD[3]	osc	Grayscale clock source select	0 : internal oscillator (8.6MHz) (internal GCK source) 1 : external clock from GCKI pin (external GCK source)
CMD[2]	pol	Output polarity select	0 : work as LED driver 1 : work as MY-PWM/APDM generator
CMD[1]	cntset	Counter reset select	0 : free running mode 1 : counter reset mode (Only usable when osc = “1”)
CMD[0]	onest	One-shot select	0 : frame cycle repeat mode 1 : frame cycle One-shot mode (Only usable when cntset = “1”)

Grayscale data format

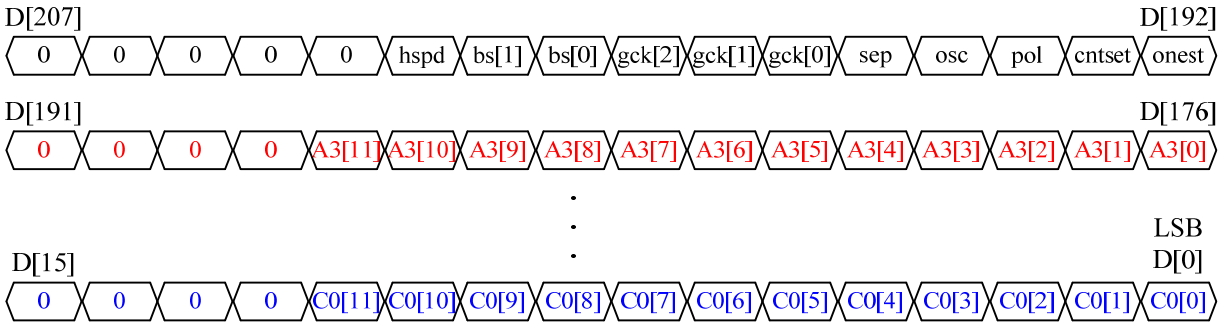
16-bit grayscale data for per channel (D[191:176], D[175:160], D[159:144], D[143:128]…D[15:0])

bs[1:0]	DESCRIPTION	PWM DATA FORMAT
00	8-bit grayscale mode	Fill the eight most significant bits with "0", Fill the eight least significant bits with 8-bit grayscale data.
01	12-bit grayscale mode	Fill the four most significant bits with "0", Fill the twelve least significant bits with 12-bit grayscale data.
10	14-bit grayscale mode	Fill the two most significant bits with "0", Fill the fourteen least significant bits with 14-bit grayscale data.
11	16-bit grayscale mode	Filled 16-bit grayscale data directly.

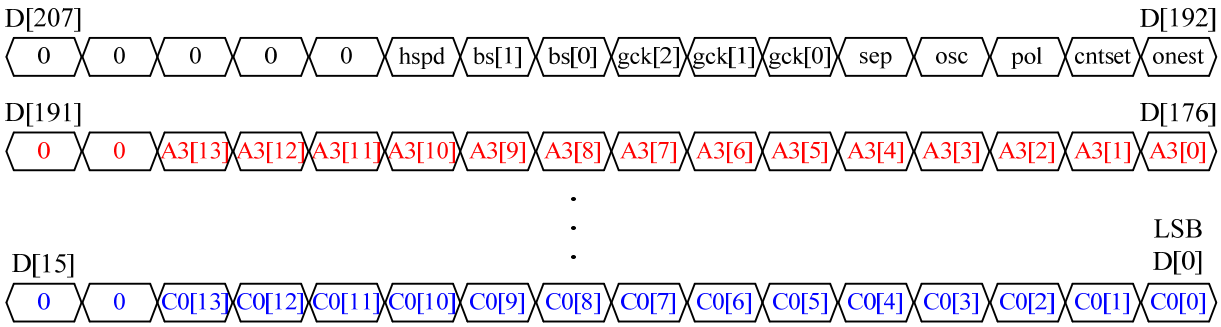
Data Format of 8-bit grayscale mode (bs[1:0]=00)



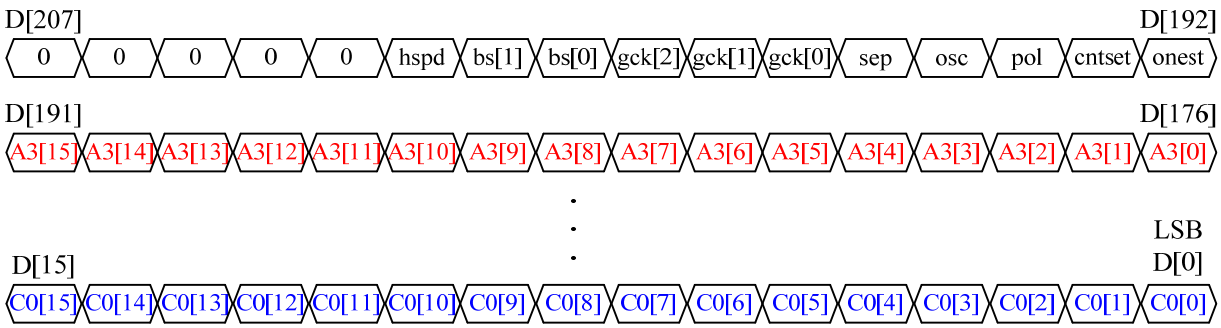
Data Format of 12-bit grayscale mode (bs[1:0]=01)



Data Format of 14-bit grayscale mode (bs[1:0]=10)



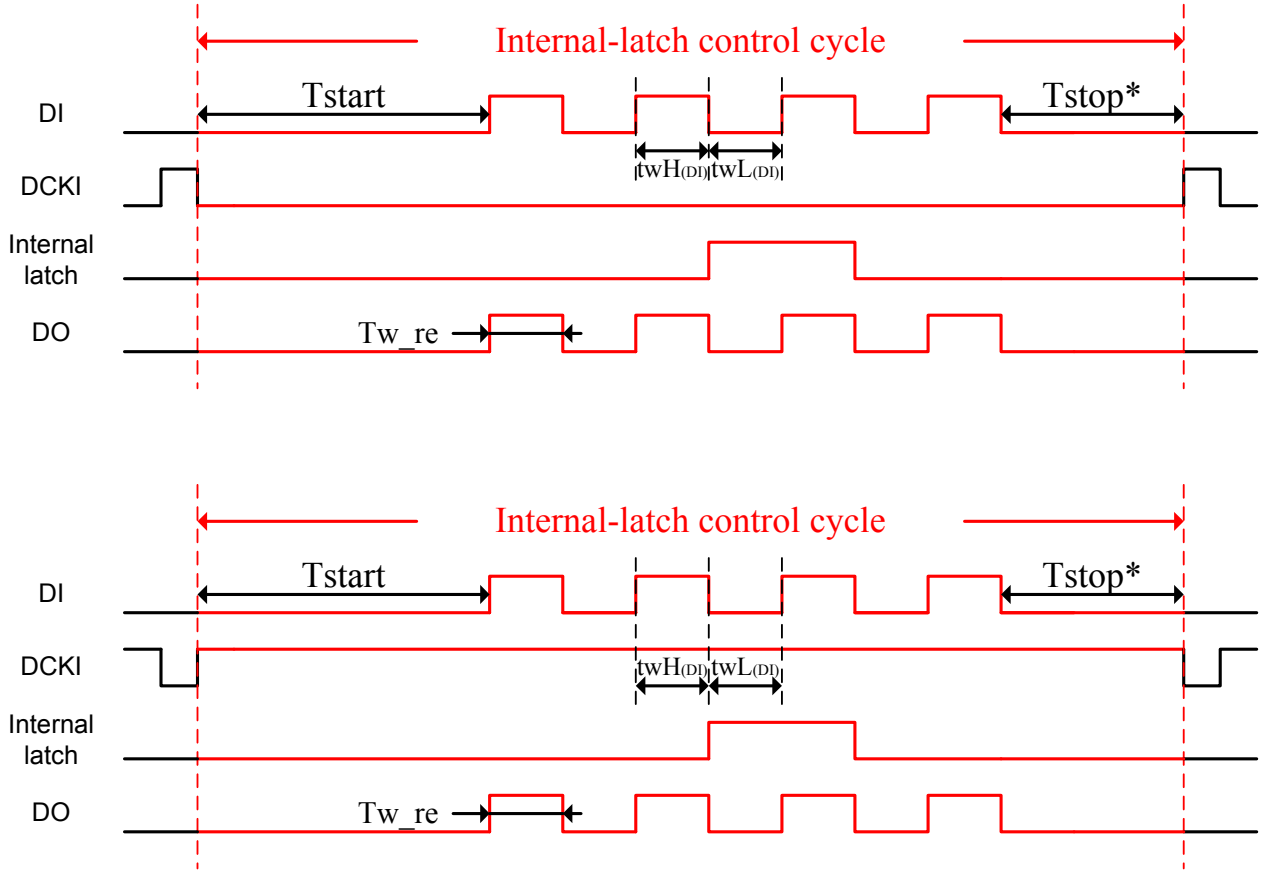
Data Format of 16-bit grayscale mode (bs[1:0]=11)



Internal-latch control cycle timing diagram

The steps to trigger internal-latch function are shown below:

1. After whole given serial data are shifted into shift register, keeping DCKI at a fixed level (no matter "high" or "low") for more than 12us. (Tstart > 12us)
2. Send 4 DI pulses ($twH_{(DI)}$>70ns, $twL_{(DI)}$> 230ns, Tstop*)
3. Data is loaded into the latch register at 2nd falling edge of DI pulse



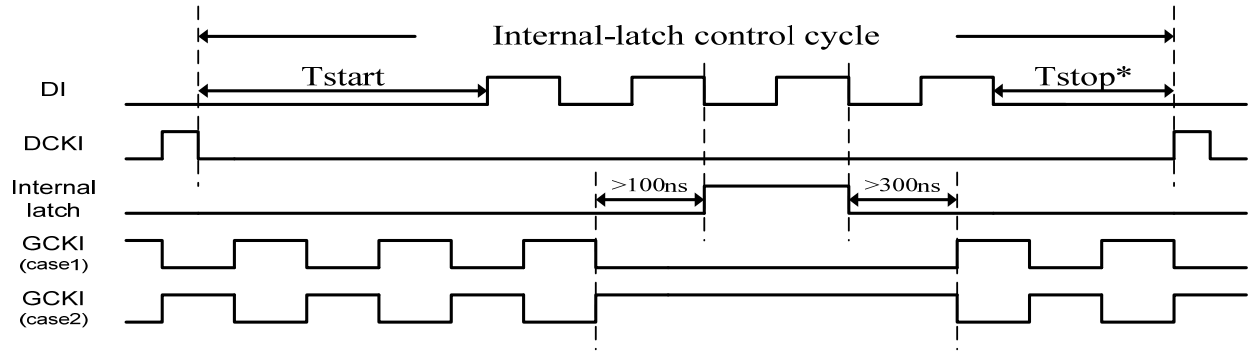
***Tstop (min.) for cascade application must > "200ns + N*10ns"**
(N is the cascade number of drivers)

Pulse retiming at Internal-latch control cycle

MY9221 provides DO signal retiming function which is fixed at Tw_re = 90ns@VDD=5V under internal-latch control cycle to prevent variation of the duty ratio caused by long cascading

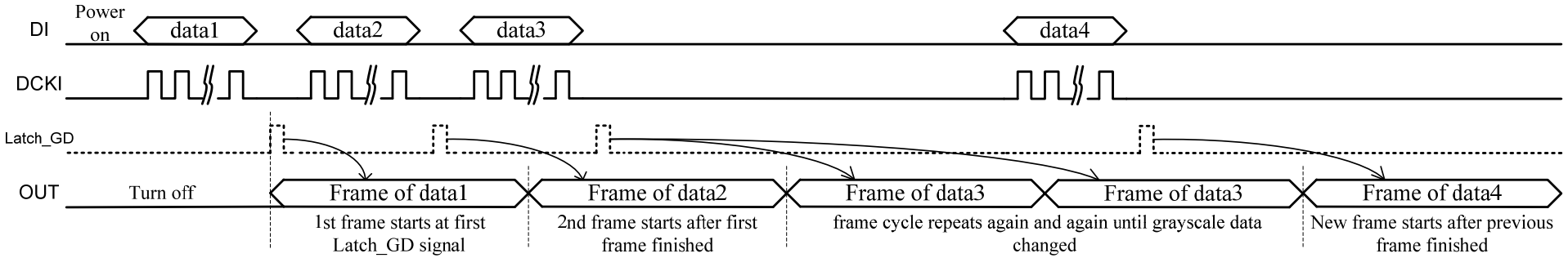
External Grayscale Clock Mode (osc = “1”)

When osc=”1”, users can use the external grayscale clock function. The grayscale clock is controlled by GCKI pin. Both the rising and falling edge of GCKI pulse can increase the grayscale counter by one. The MY9221 compare the grayscale data of each output with grayscale counter value. If the grayscale data is larger than grayscale counter value, the OUT will switch on. Some timing constrains must be obeyed, which are shown below:



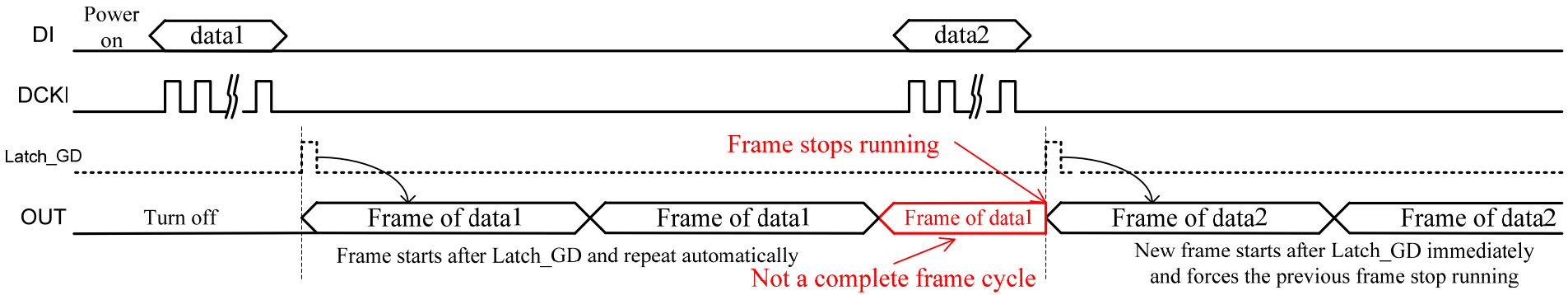
Free Running Mode

The first frame cycle after power-on will synchronize with the first Latch_GD signal (Latch_GD is the latch signal for grayscale data.). A new frame cycle for new grayscale data will start after the previous frame cycle completely finished. If the grayscale data doesn’t change, the frame cycle will repeat again and again automatically. This mode ensures every frame cycle to be performed completely.



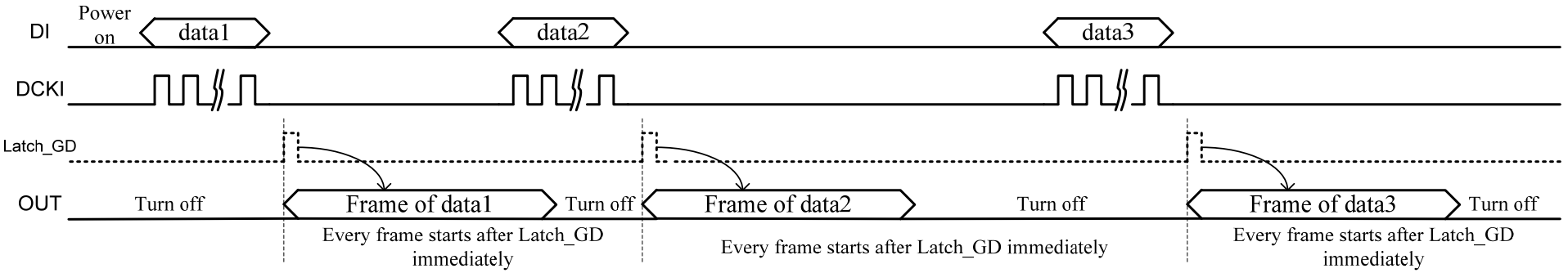
Grayscale Counter Reset Mode (Only usable when osc = ”1” : external grayscale clock mode)

Every new frame cycle of new grayscale data will synchronize with the Latch_GD signal. Frame cycles of the same grayscale data will repeat again and again automatically until the next grayscale data is loaded. When the next grayscale data is loaded, it will force the previous frame stop running. This means that the previous frame cycle may not perform completely.



One-shot Mode (Only usable when cntset = “1” : grayscale counter reset mode)

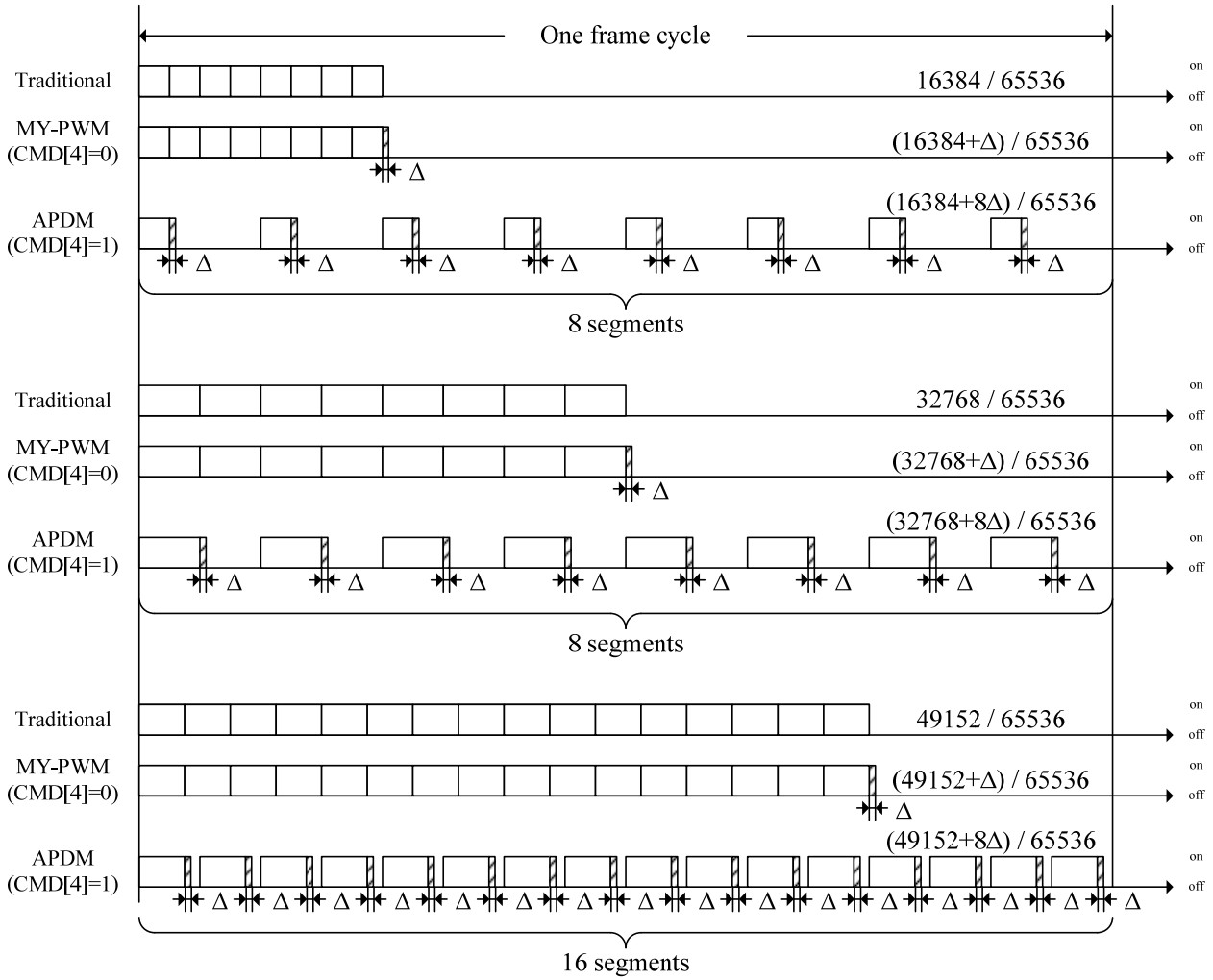
Every new frame cycle of new grayscale data will synchronize with the Latch_GD signal. And one grayscale data will just perform only one complete frame cycle. After one complete cycle, the output current will turn off until next grayscale data is loaded.



Adaptive Pulse Density Modulation with Δ-Width Correction

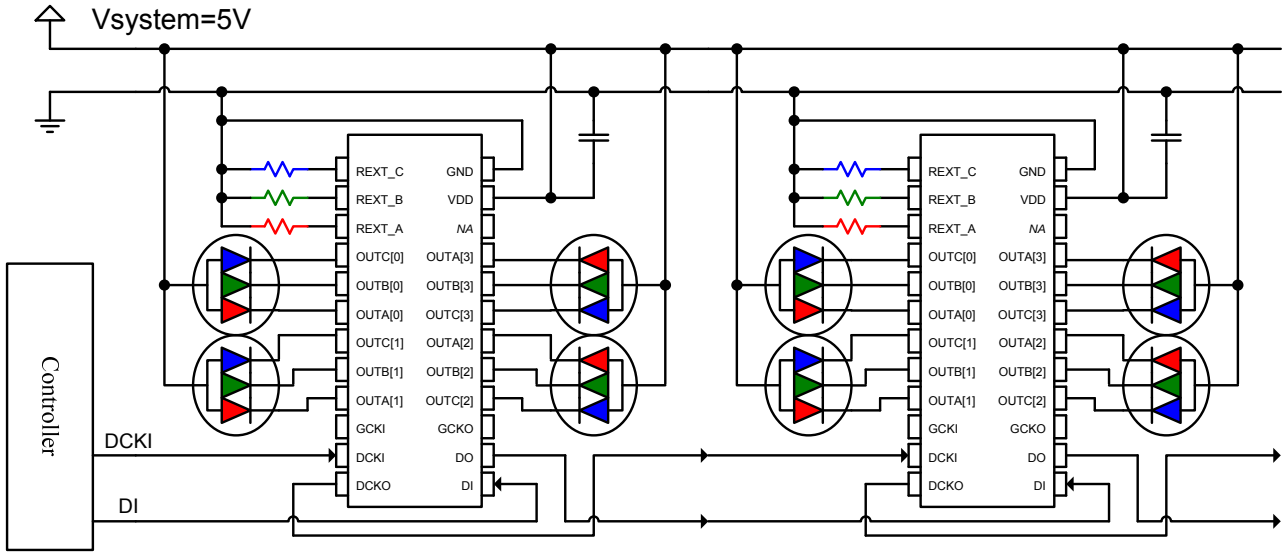
Adaptive Pulse Density Modulation (APDM) with Δ-Width Correction is a technique to improve output current waveform distortion and increase visual refresh rate. The adaptive output waveform is controlled by the grayscale value automatically. When all outputs operate at high grayscale resolution (grayscale resolution ≧ 75%), the output waveform is divided into more segments to increase visual refresh rate. Otherwise the output waveform is divided into less segments at low grayscale resolution to improve output current linearity. (grayscale resolution < 75%). And the Δ-Width Correction (Δ ≠ 0) is used to compensate the non-ideal output current transient response.

(e.g. 16-bit grayscale application, Δ ≠ 0)

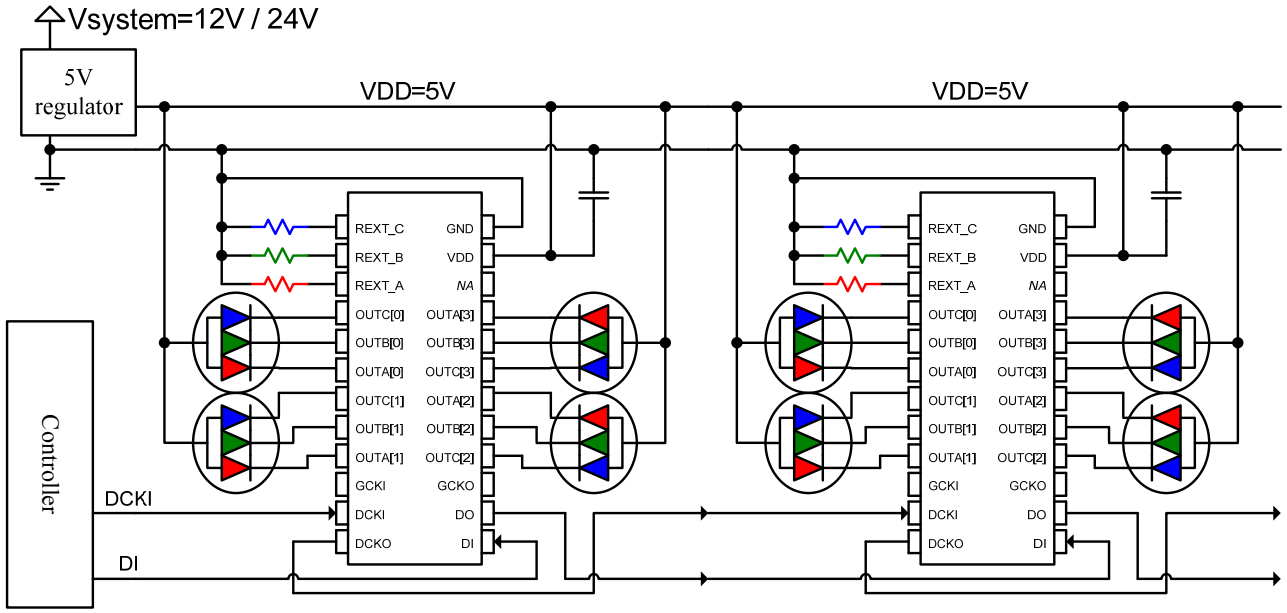


Application Diagram

1. Work as LED driver with system supply voltage = 5V (Set CMD[2] = “L”)
   Use internal grayscale clock & Internal-latch function



2. Work as LED driver with system supply voltage = 12V/24V (Set CMD[2] = “L”)
   Use internal grayscale clock & Internal-latch function



Power Dissipation

When the 12 output channels are turned on, the practical power dissipation is determined by the following equation:

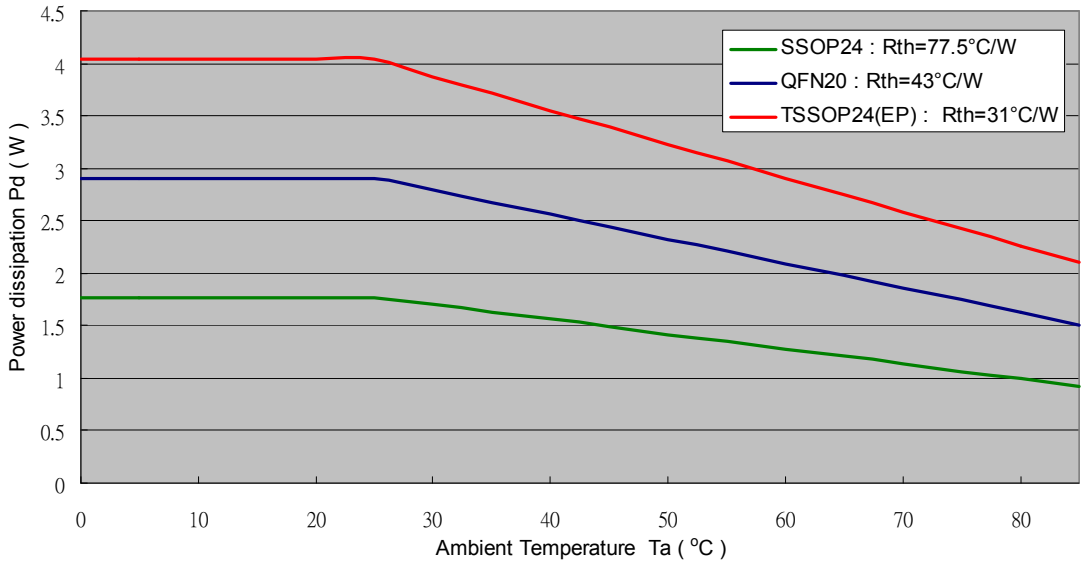
$$PD\ (practical) = V_{DD} \times I_{DD} + VoutA3 \times IoutA3 \times DutyA3 + \ldots + VoutC0 \times IoutC0 \times DutyC0$$

In secure operating conditions, the power consumption of an integrated chip should be less than the maximum permissible power dissipation which is determined by the package types and ambient temperature. The formula for maximum power dissipation is described as follows:

$$PD\ (max) = \frac{Tj(max)(℃) - Ta(℃)}{Rth(j\text{-}a)(℃/Watt)}$$

The PD(max) declines as the ambient temperature rises. Therefore, suitable operating conditions should be designed with caution according to the chosen package and the ambient temperature. The following figure illustrates the relation between the maximum power dissipation and the ambient temperature in the three different packages.

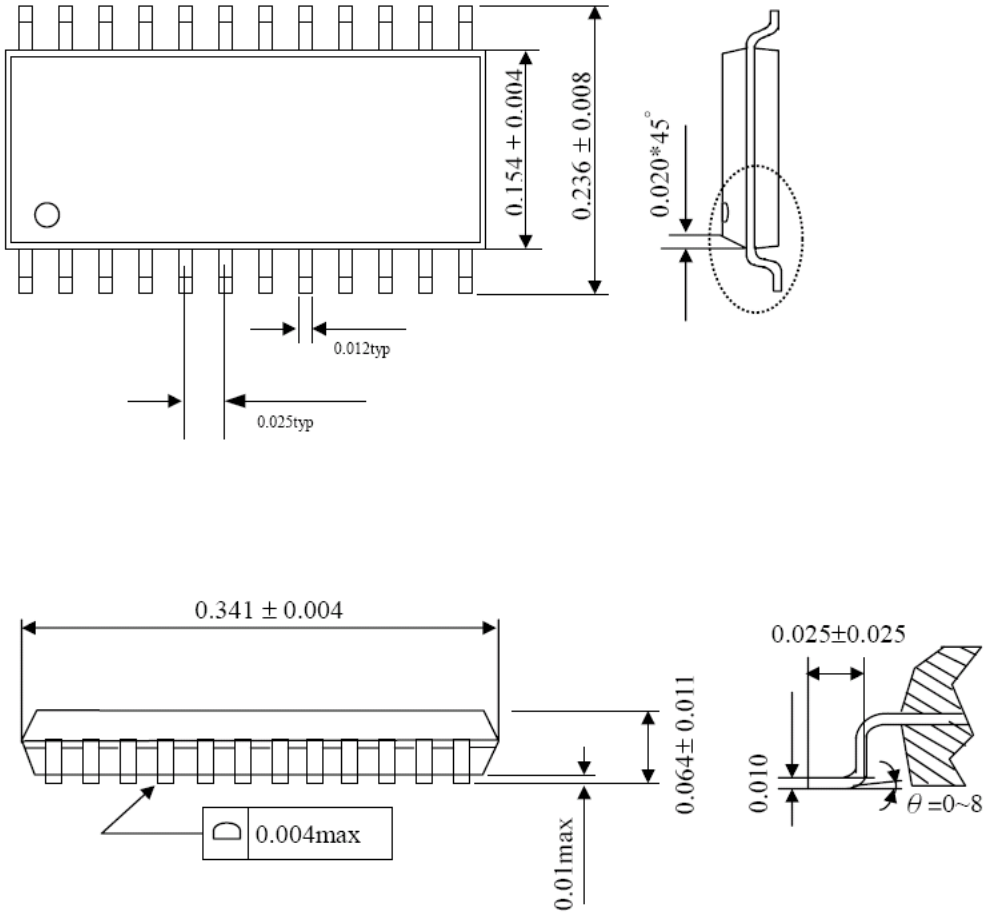
Maximum Power Dissipation v.s. Ambient Temperature



Package Outline Dimension

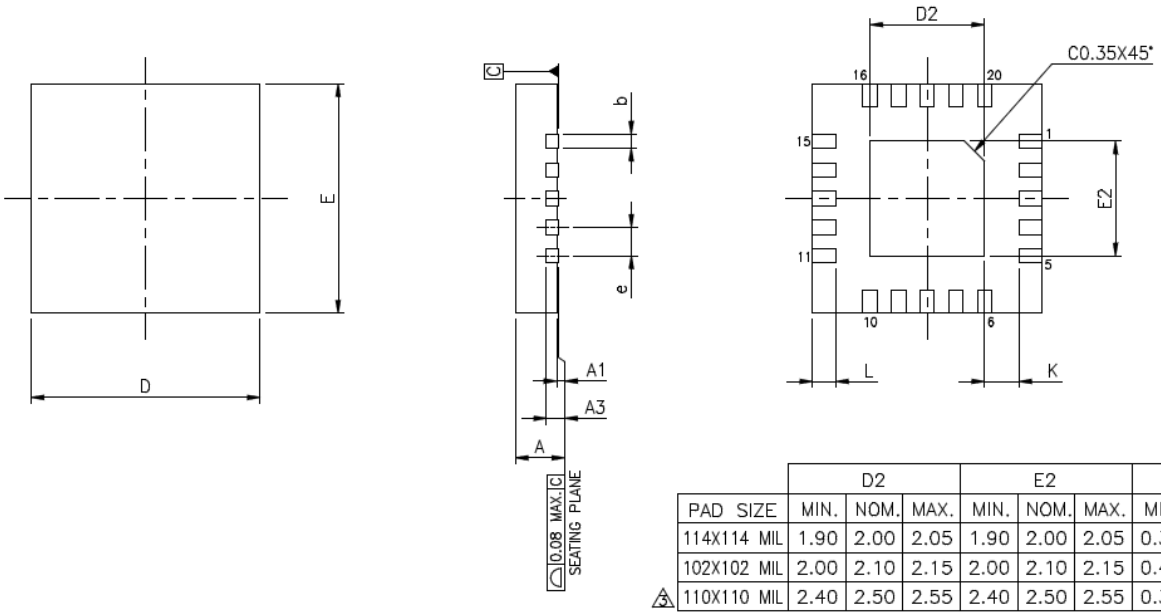
SSOP24-150mil-0.635mm

Unit: inch



Package Outline Dimension

QFN20-4mmx4mm



PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
114X114 MIL	1.90	2.00	2.05	1.90	2.00	2.05	0.30	0.40	0.50
102X102 MIL	2.00	2.10	2.15	2.00	2.10	2.15	0.45	0.55	0.65
3 110X110 MIL	2.40	2.50	2.55	2.40	2.50	2.55	0.35	0.45	0.55

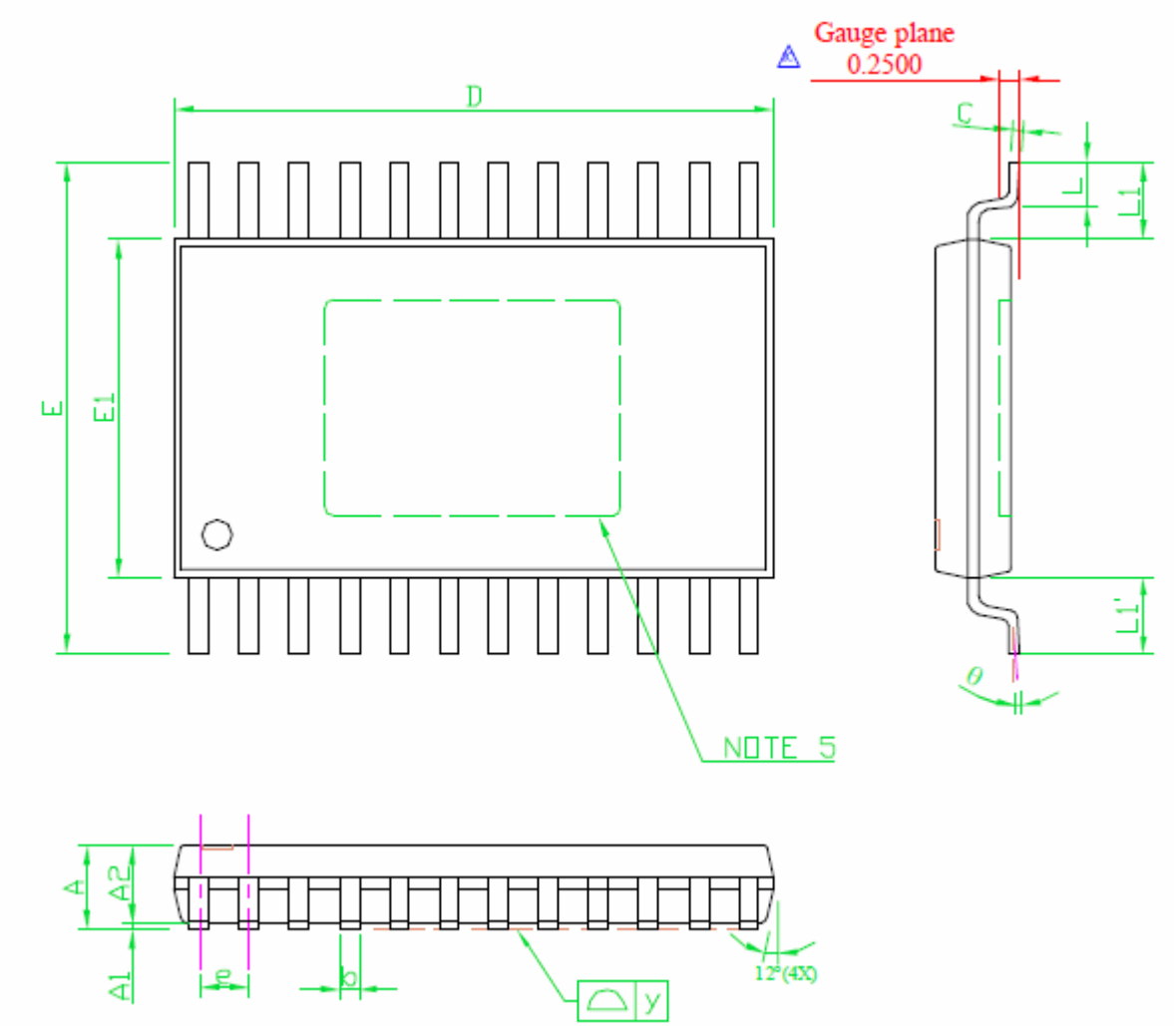
UNIT : mm

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.20	0.25	0.30
D		4.00 BSC	
E		4.00 BSC	
e		0.50 BSC.	
K	0.20	—	—

UNIT : mm

Package Outline Dimension

TSSOP24-173mil-0.65mm (EP)



SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.15	---	---	0.045
A1	0.00	---	0.10	0.000	---	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	---	0.30	0.007	---	0.012
C	0.09	---	0.20	0.004	---	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	---	0.65	---	---	0.026	---
L	0.45	0.60	0.75	0.018	0.024	0.030
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°
|L1-L1'|	---	---	0.12	---	---	0.005
L1	1.00REF			0.039REF		

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.
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