CDT204 – Computer Architecture

> Date: Jun. 8th 2023
>
> Time: 8:30 – 12:30
>
> Help: Small calculator is allowed in the exam

The exam has 37 points and 2 Bonus points. The grades will be awarded as follows:

- 3 : 19 Points
- 4 : 25 Points
- 5 : 32 Points

Important Notes:

- Give as full an answer as possible to obtain full marks. All calculations, approximations, assumptions and justifications must be reported for full credit unless stated otherwise. Please use figures and examples to clarify.
- If you do not understand a question clearly, you are allowed to call the teacher and ask.
- Write the question and part number on each page clearly.
- Answer each question on a separate page.
- In case you might have forgotten:

  $1GB = 2^{10}MB = 2^{20}KB = 2^{30}B$

  $1\ sec = 10^{3}\ ms = 10^{6}\ \mu s = 10^{9}\ ns = 10^{12}\ ps$

Live long and prosper

Task 1 – General (5p)

The following C code calculates the absolute value of a signed integer '**x**'. The '**>>**' operator is the arithmetic right shift operator and the '**^**' operator is the XOR operator in C language.

```
int sign = x>>31;
x = (x^sign)-sign;
```

A. Explain the logic behind the algorithm used in the above code. How does this code achieve its goal of calculating the absolute value? (3p)
B. Rewrite the code in order to calculate the absolute value of a single byte (8 bit value). (1p)
C. Using drawing and schematics show the behavior of the code that you wrote for part B in calculating the absolute value of -56 stored in a single byte. (1p)

Task 2 – Performance (8p + BONUS 2p)

The table below shows the number of instructions per processor core on a multicore processor as well as the average CPI for executing the program on 1, 2, 4, or 8 cores.

Processors	No. Instructions per Processor	CPI
1	1.00E+10	1.2
2	5.00E+09	1.4
4	2.50E+09	1.8
8	1.25E+09	2.6

A. Assuming a 3 GHz clock frequency, what is the execution time of the program using 1, 2, 4, or 8 cores? (2p)
B. If using a single core, find the required CPI for this core to get an execution time equal to the time obtained by using the number of cores in the table above. Note that the number of instructions should be the aggregate number of instructions executed across all the cores. (3p)
C. Assume that the power consumption of a processor core can be described by the following equation:

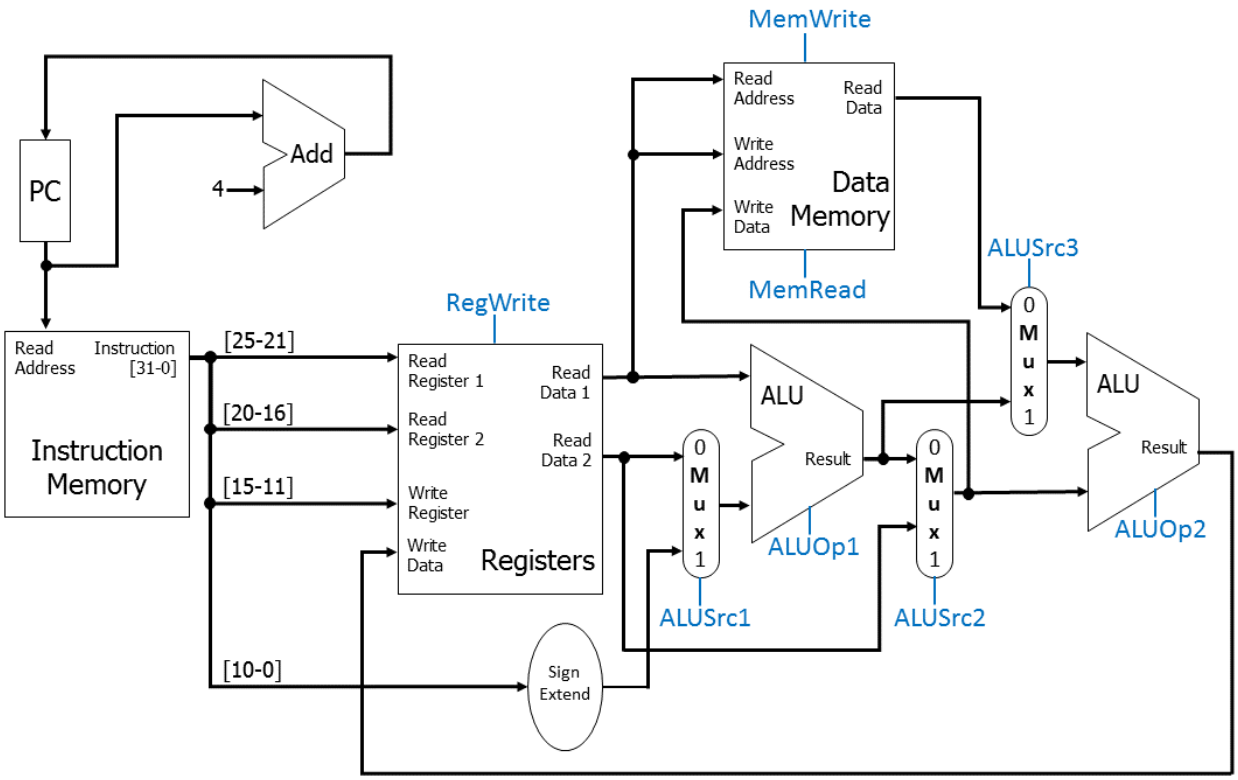
$$Power = CfV^2$$

where ***f*** is the frequency and ***C*** is a constant which in this case it is equal to 5mA/MHz (the core needs 5 milliamps per MHz of frequency). ***V*** is the operation voltage of the processor and can be described by the following equation:

$$Voltage = \frac{1}{5} frequecy + 0.4$$

with the frequency measured in GHz. So, for example, at 5 GHz, the voltage would be 1.4 V. Find the power consumption of the program executing on 1, 2, 4, and 8 cores assuming that each core is operating at a 3 GHz clock frequency. Likewise, find the power consumption of the program executing on 1, 2, 4, or 8 cores assuming that each core is operating at 500 MHz. (3p)
D. **BONUS**: Discuss the results from part C. What can you conclude from the data? (2p)

Task 3 – Datapath (8p)



The datapath above supports the following instructions:

- **`lw_add rd, (rs), rt`** (fused load and add): Register **`rd`** will be set to the summation of memory value addressed by register **`rs`** and the value stored in register **`rt`**. `R[rd] = Mem[R[rs]]+R[rt]`
- **`addi_st (rs), rs, imm`** (fused immediate add and store): The memory addressed by register **`rs`** will be set to summation of register **`rs`** and constant value **`imm`**. `Mem[R[rs]]=R[rs]+imm`
- **`sll_add rd, rs, rt, imm`** (fused immediate left shift and sum): Value of register **`rs`** is shifted left by constant value **`imm`** then added to register **`rt`** and stored in register **`rd`**. `R[rd]=(R[rs]<<imm)+R[rt]`

All instructions use the same format (shown below). Not all instructions use all the fields below.

op (bits 31-26)	rs (bits 25-21)	rt (bits 20-16)	rd (bits 15-11)	imm (bits 10-0)

For each of the above instructions, specify how the control signals should be set for correct operation. Use **`X`** for don't care. **`ALUOp`** can be **`ADD`**, **`SUB`**, **`SLL`**, **`PASS_A`**, or **`PASS_B`** (i.e., **`PASS_A`** means pass the top operand through without changing it).

You can find an empty table for this task on the last page of the exam sheet, which you can use to write your answer in. Detach it from the exam sheet and put it in your answers folder.

Task 4 – Pipelining (5p)

Consider the following MIPS program:

```
.global __start

.data
x: .word 256

.text
__start:
        addi $s0, $zero, 0
        addi $s1, $zero, 1
        lw   $s2, x
loop:
        beq  $s2, $s1, end
        div  $s2, $s2, 2
        addi $s0, $s0, 1
        j    loop
end:
        ...
```

a. What will the value of $s0 register be when the program reaches point "end"? (The 'DIV' instruction performs integer division). Motivate your answer. (3p)
b. Write the equivalent C code for the above MIPS code. (2p)

Task 5 – Cache Performance (6p)

Suppose physical addresses are 32 bits wide. Suppose there is a cache containing 256K words of data (not including tag bits), and each cache block contains 4 words. For each of the following cache configurations:

a. Direct mapped
b. 2-way set associative
c. 4-way set associative
d. Fully associative

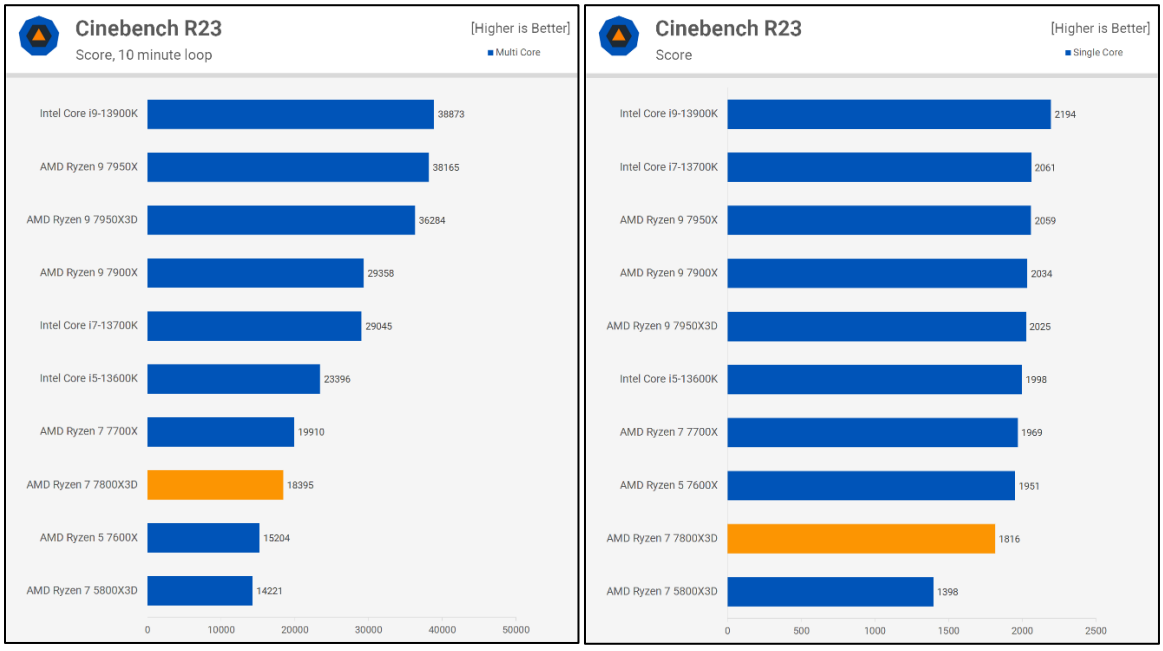
Specify how the 32-bit address would be partitioned.

Task 6 – Multiprocessing (5p)

The specs for two of current high-end CPUs in the market are given below. Namely the AMD Ryzen 7 7800X3D and Intel Core I9-13900k.

	AMD Ryzen 7 7800X3D	Intel Core i9-13900K
No. of Cores	8	24
No. of Threads	16	32
Base Clock	4.20 GHz	3.00 GHz
Boost Clock	5.00 GHz	5.80 GHz
Max. Memory Speed	6000 MHz	7200 MHz
L1 Cache	512 KB	1024 KB
L2 Cache	8 MB	32 MB
L3 Cache	96 MB	36 MB
TDP	120 Watts	250 Watts
Launch Price	$449	$599

The following benchmarks show the performance of the CPUs in different scenarios[1].

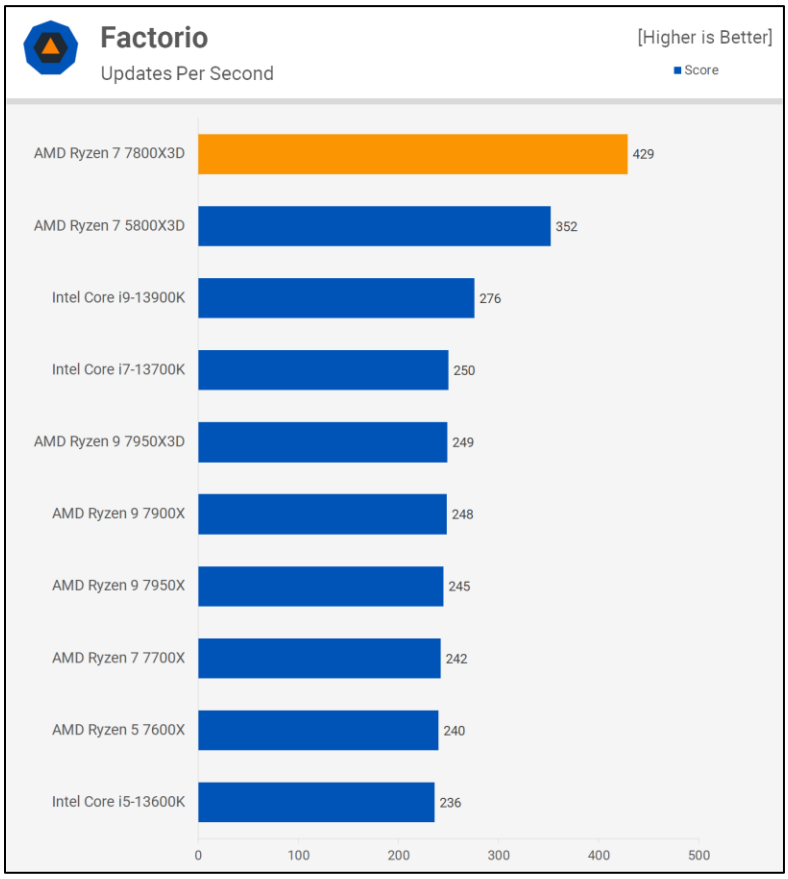


The chart on the left shows the multi-core performance of these CPUs (and some others) and the chart on the right shows the single-core performance.

A. Why does the intel CPU perform much better (more than double) than AMD in the Multi-core test? (1p)
B. Why does such a performance gap cannot be seen in the single core test? (1p) Where does the extra single core performance of the intel CPU come from? (1p)

[1] Benchmarks are taken from www.techspot.com

When it comes to gaming the charts look different, for example the chart for Factorio is presented below.



C. What can be reason for AMD's CPU performing being much better than the Intel CPU in this test? (1p)

D. The first table in this task provides the price of the CPUs and also their power consumption. Given these values which one do you think would be a better choice in the long term? (2p)

Answer Sheet for Task 3

Inst.	ALUSrc1	ALUSrc2	ALUSrc3	ALUOp1	ALUOp2	MemRead	MemWrite	RegWrite
lw_add								
addi_st								
sll_add								