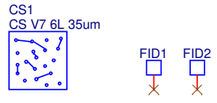
Revision	Date	Author	Description
1	11/02/2021	M.Gregis	First Draft
2	18/06/2021	G.Boschini	- Uploaded symbol from library - Changed R25 to not mounted - Changed J2, J3, J4 to 4UCON supplier
3	26/07/2021	M. Cossali	- Uploaded symbol from library - Changed J2 MPN to 4UCON 00820 and J3 MPN to 4UCON 00815 - Changed the MCU U6 MPN to STM32L4R5ZIY6
4	13/09/2021	G.Boschini	- Swapped J2 pin2 with pin3
5	15/09/2021	G.Boschini	- Added pullup resistor on I2C1 nets
6	04/02/2022	M.Gregis	- Added QWIIC connector - Changed J5 to 7x2 header to support STLINK V3 standard.
7	17/02/2022	M.Gregis	- Updated PCB - Added new Castellated PAD for CS signal (PAD65) - BOOT signal made available on Castellated PAD (PAD51) - added PAD66/67/68/69 (NC) - Changed J6 supply to +VIO



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Project	**SWAN**	Page name	
Board	**SWAN-F**		**00 - REVISION**
Designer	**M. Gregis**	Approved	**G.Boschini**
Project Code	**2021-0248**	Customer	**Blues**
Internal Code	-	Code	**-**

Data	Rev.	Rev. changes	Sheet
Tuesday, April 26, 2022	**7**	See Revision Page	**1 / 5**

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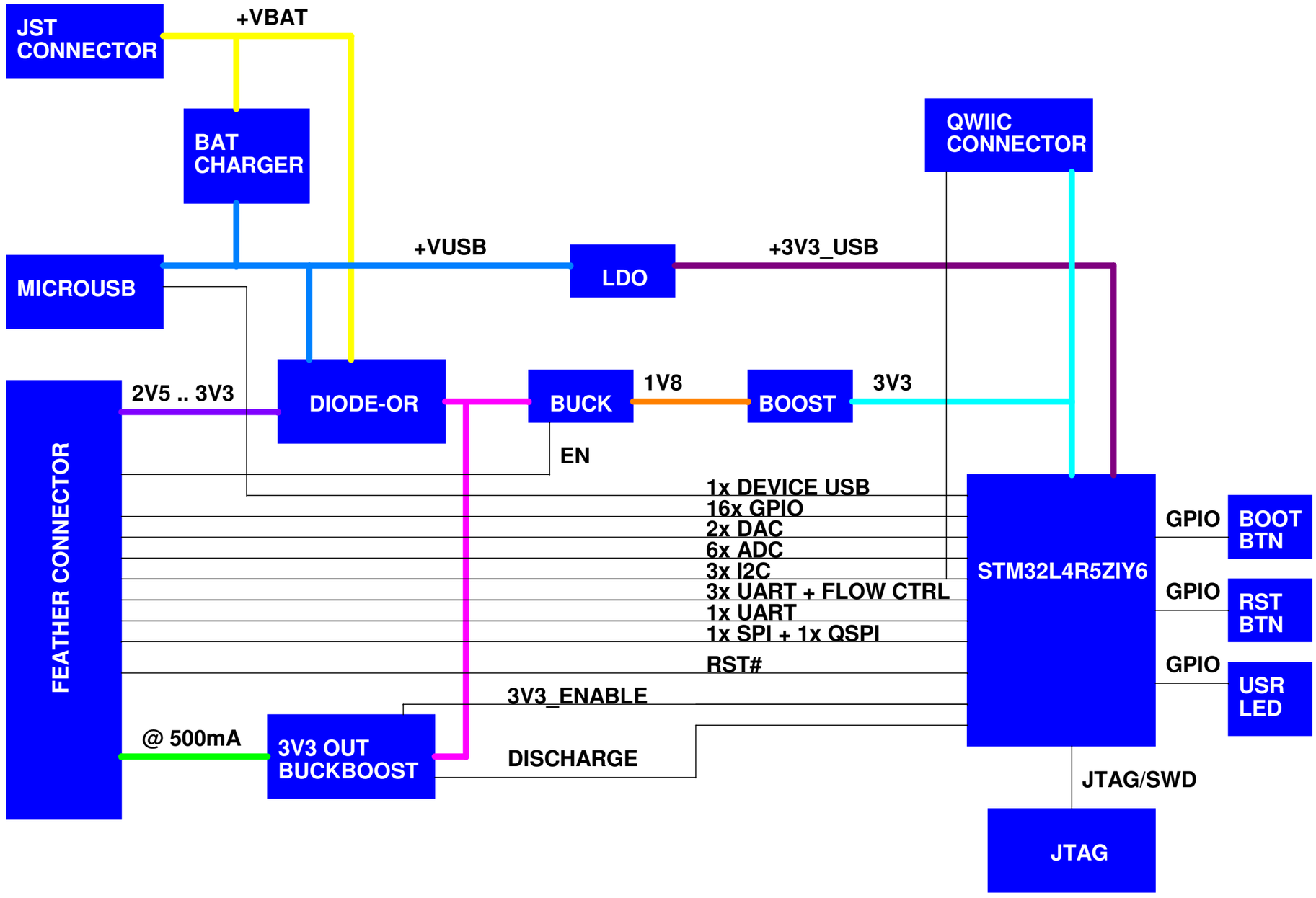

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Project	SWAN	Page name	
Board	SWAN-F		01 - BLOCK DIAGRAM
Designer	M. Gregis	Approved	G.Boschini
Project Code	2021-0248	Customer	Blues
Internal Code	-	Code	-

Data	Rev.	Rev. changes	Sheet
Tuesday, April 26, 2022	7	See Revision Page	2 / 5

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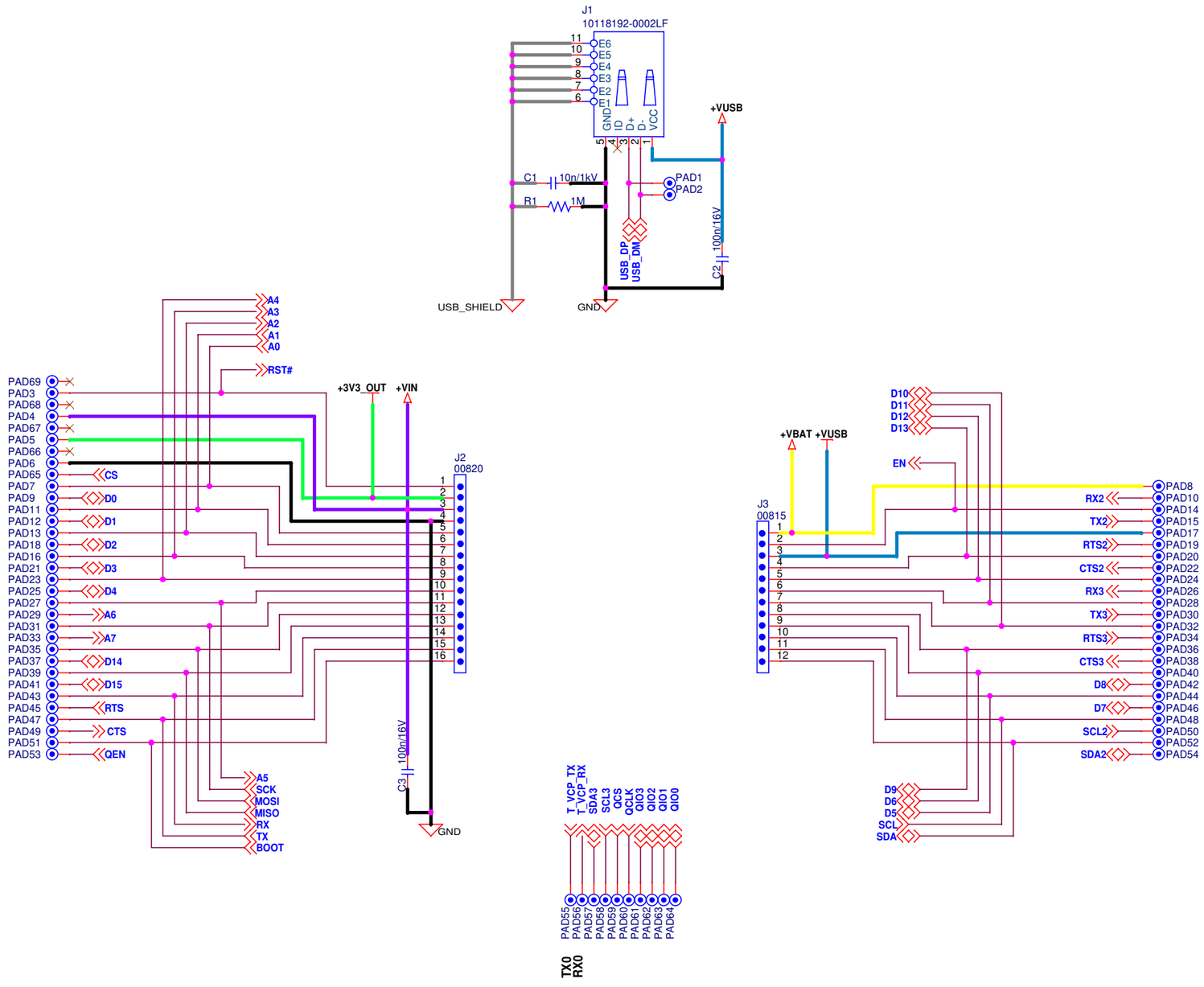

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	Project **SWAN**	Page name	
	Board **SWAN-F**	**02 - FEATHER CONNECTORS**	
	Designer **M. Gregis**	Approved **G.Boschini**	
	Project Code **2021-0248**	Customer **Blues**	
	Internal Code -	Code **-**	
Data: Tuesday, April 26, 2022	Rev. **7**	Rev. changes: See Revision Page	Sheet **3 / 5**

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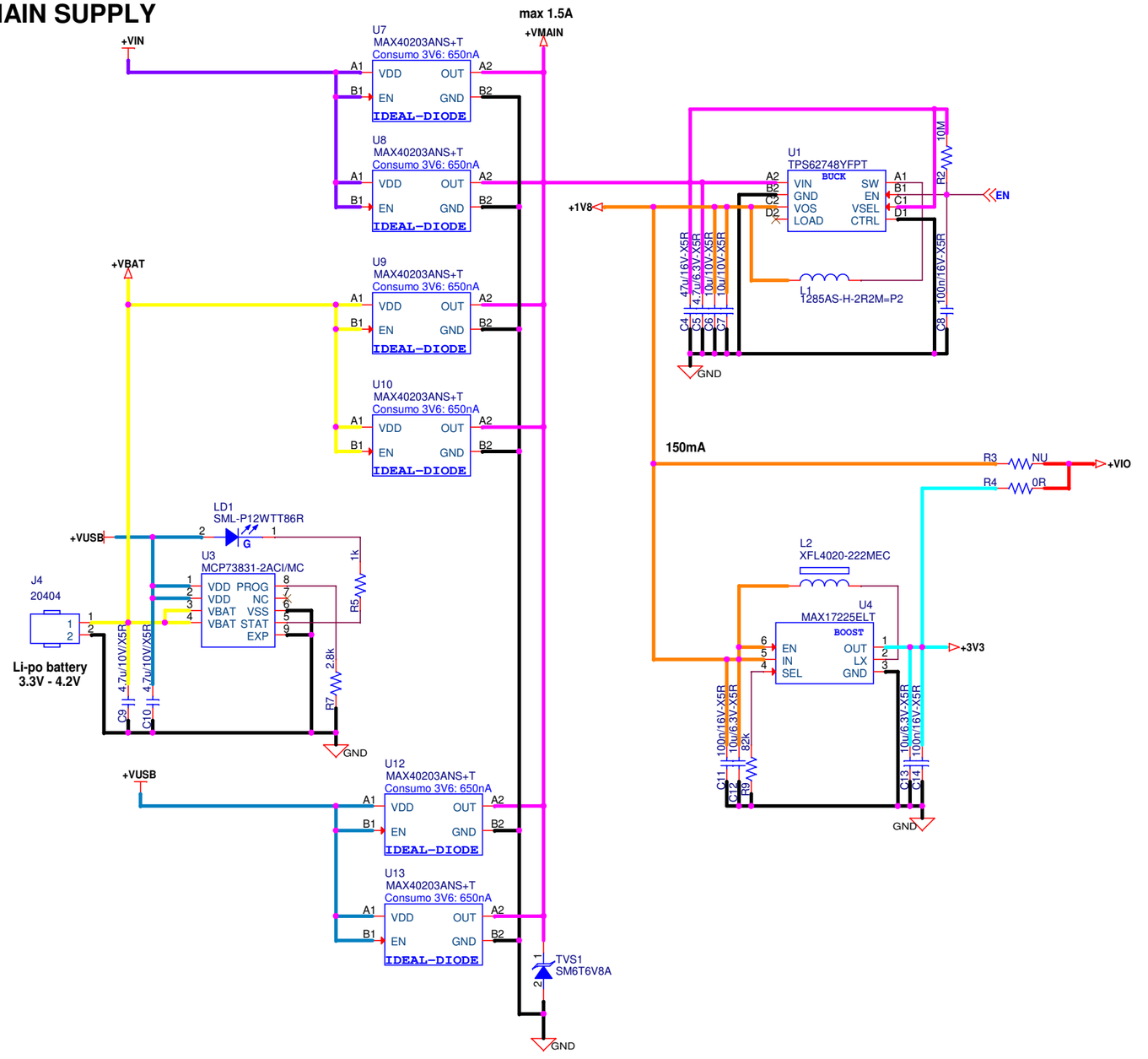
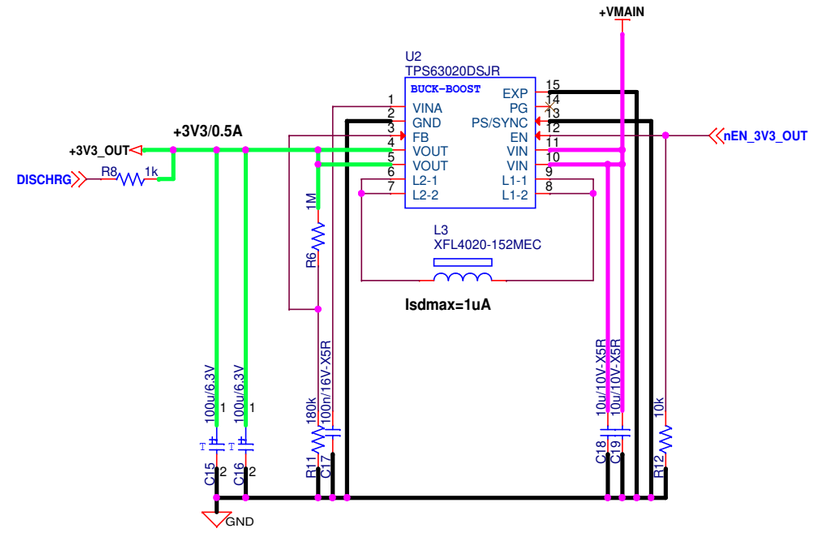
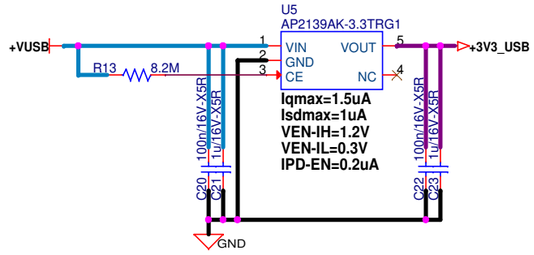
MAIN SUPPLY



3V3 OUTPUT SUPPLY



USB LDO



FAE TECHNOLOGY via C. Battisti 136, 24025, Gazzaniga (Bg), Italy Mail: info@fae.technology Tel: +39 035738130	Project **SWAN**	Page name	
	Board **SWAN-F**	**03 - POWER**	
	Designer **M. Gregis**	Approved **G.Boschini**	
	Project Code **2021-0248**	Customer **Blues**	
	Internal Code **-**	Code **-**	
Data Tuesday, April 26, 2022	Rev. **7**	Rev. changes See Revision Page	Sheet **4 / 5**

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MCU

U6
STM32L4R5ZIY6
Consumo 3V3: 17mA

VDD=+1V7 - +3V6

VDDUSB=+3V - +3V6

DO NOT CONNECT
PB2 TO VDD

USB DETECT
5V TOLERANT PIN

SET DISCHRG PIN
AS OPEN-DRAIN
WITHOUT PU/PD

VERSION BITS
PG[0..3]

USER LED

LD2
SML-P12U2TT86R

Q1
DMN62D0UW-7

QWIIC CONNECTOR

J6
BM04B-SRSS-TBT

PB1
PB-SKRPADE010

PB2
PB-SKRPABE010

PB3
PB-SKRPADE010

Y1
ABS06-107-32.768KHZ-T

J5
21691

Project	SWAN	Page name	04 - CPU
Board	SWAN-F		
Designer	M. Gregis	Approved	G.Boschini
Project Code	2021-0248	Customer	Blues
Internal Code	-	Code	-
Data	Tuesday, April 26, 2022	Rev.	7
Rev. changes	See Revision Page	Sheet	5 / 5

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