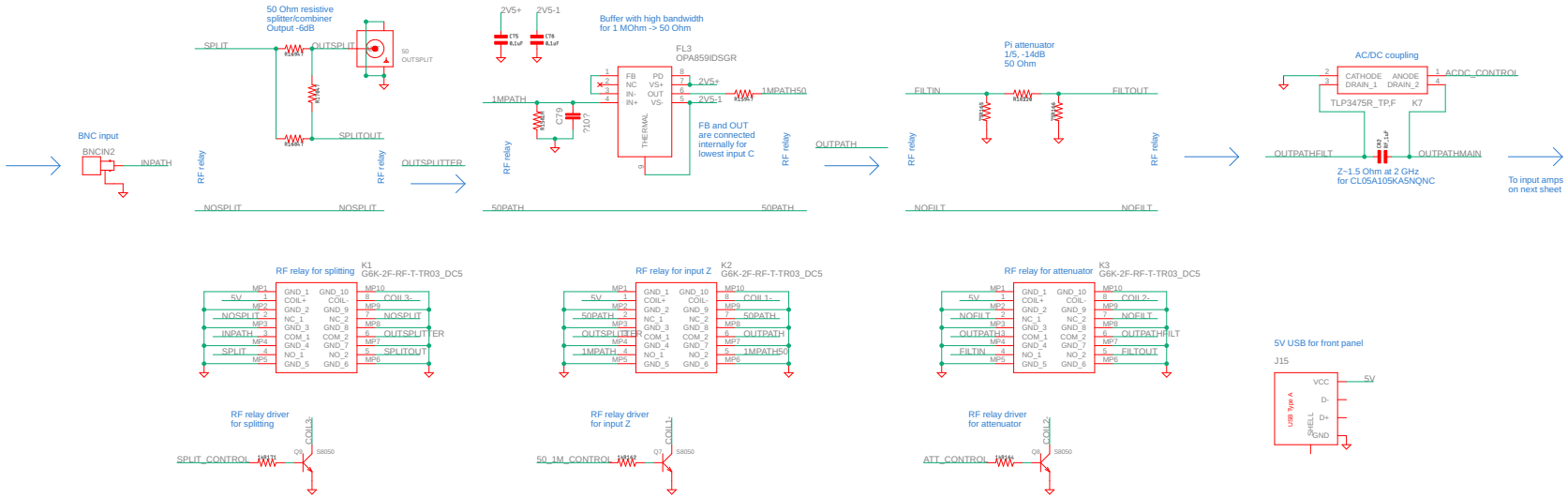
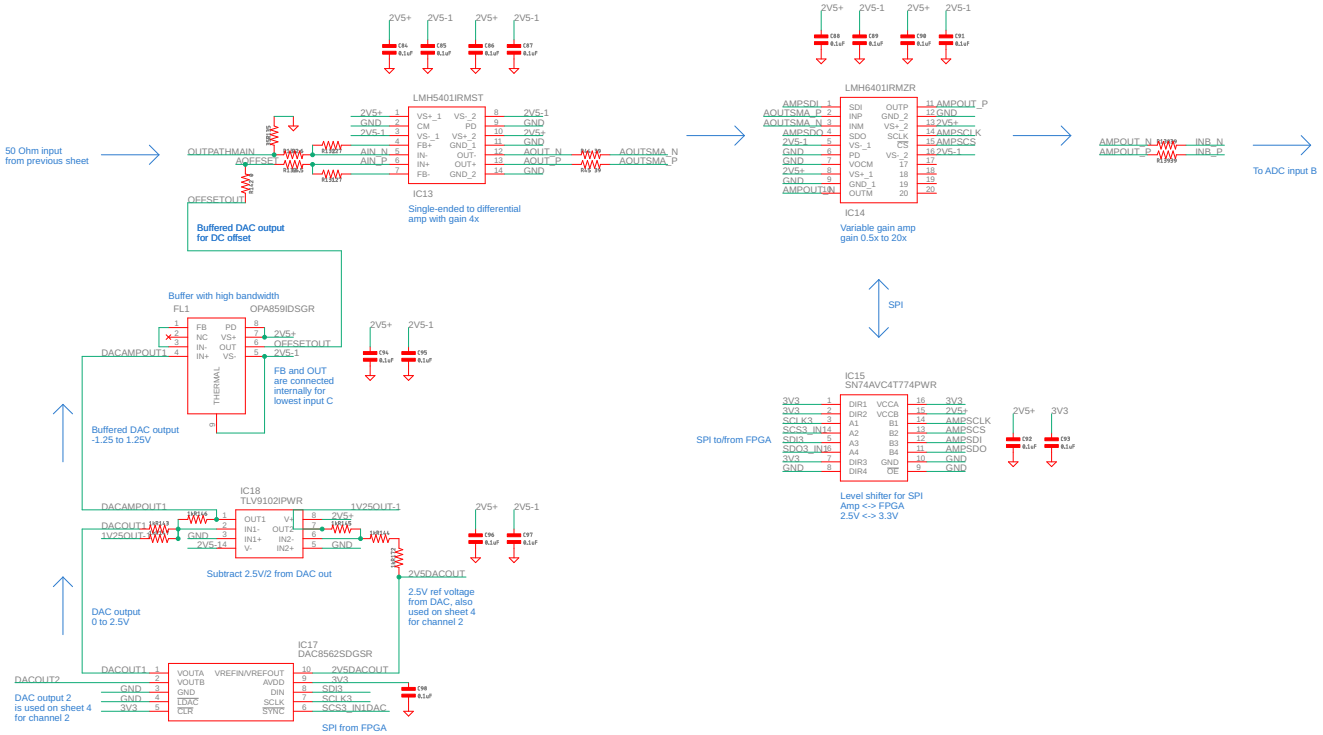
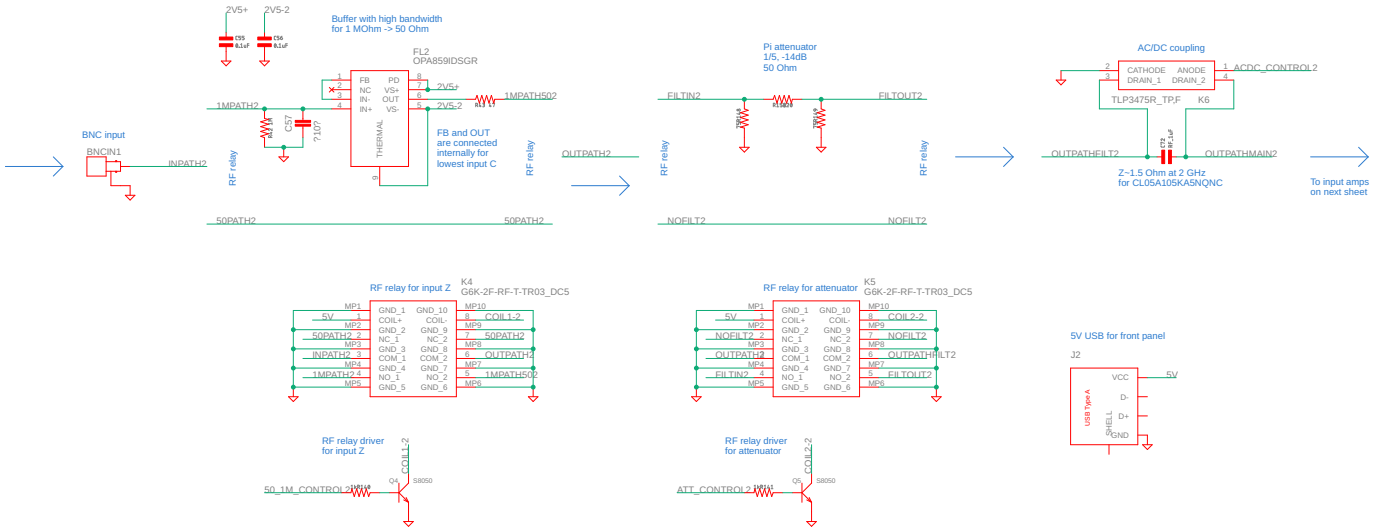
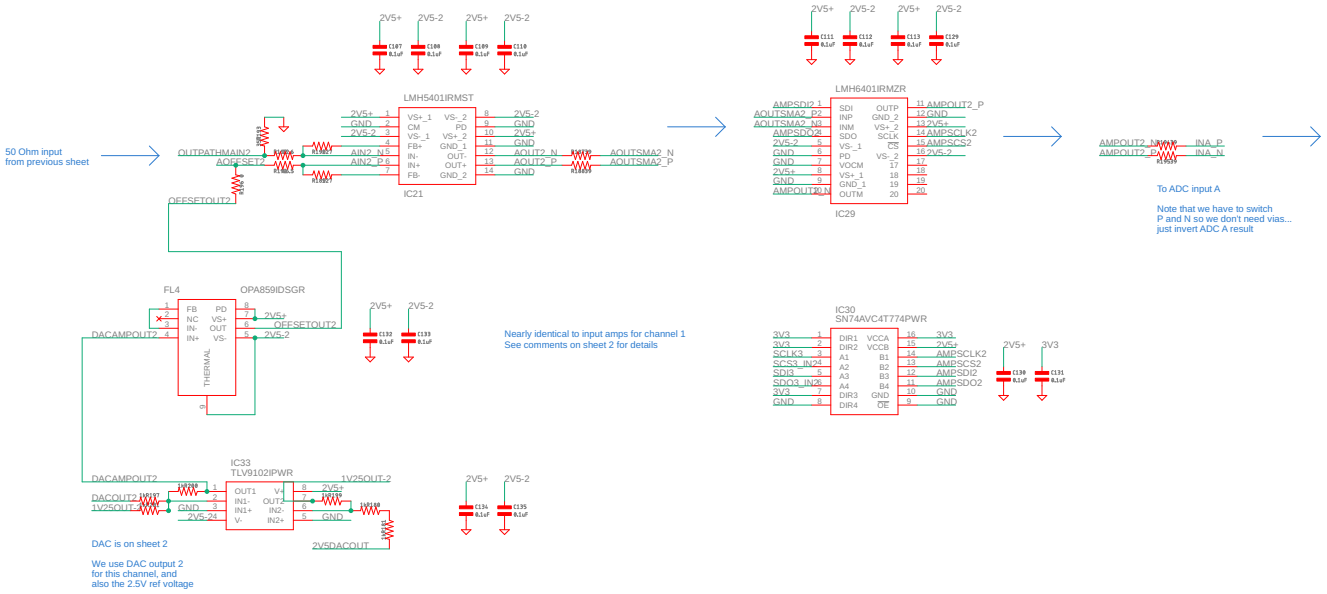
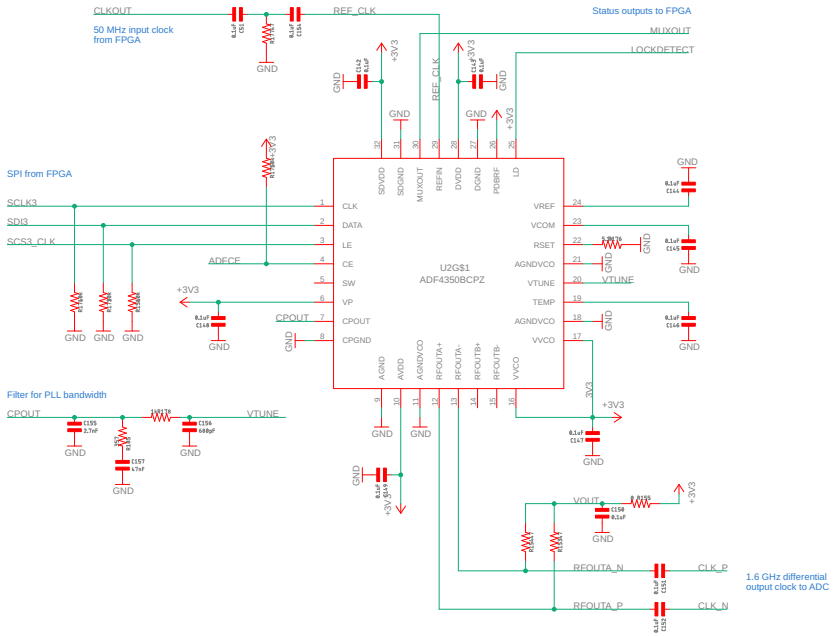
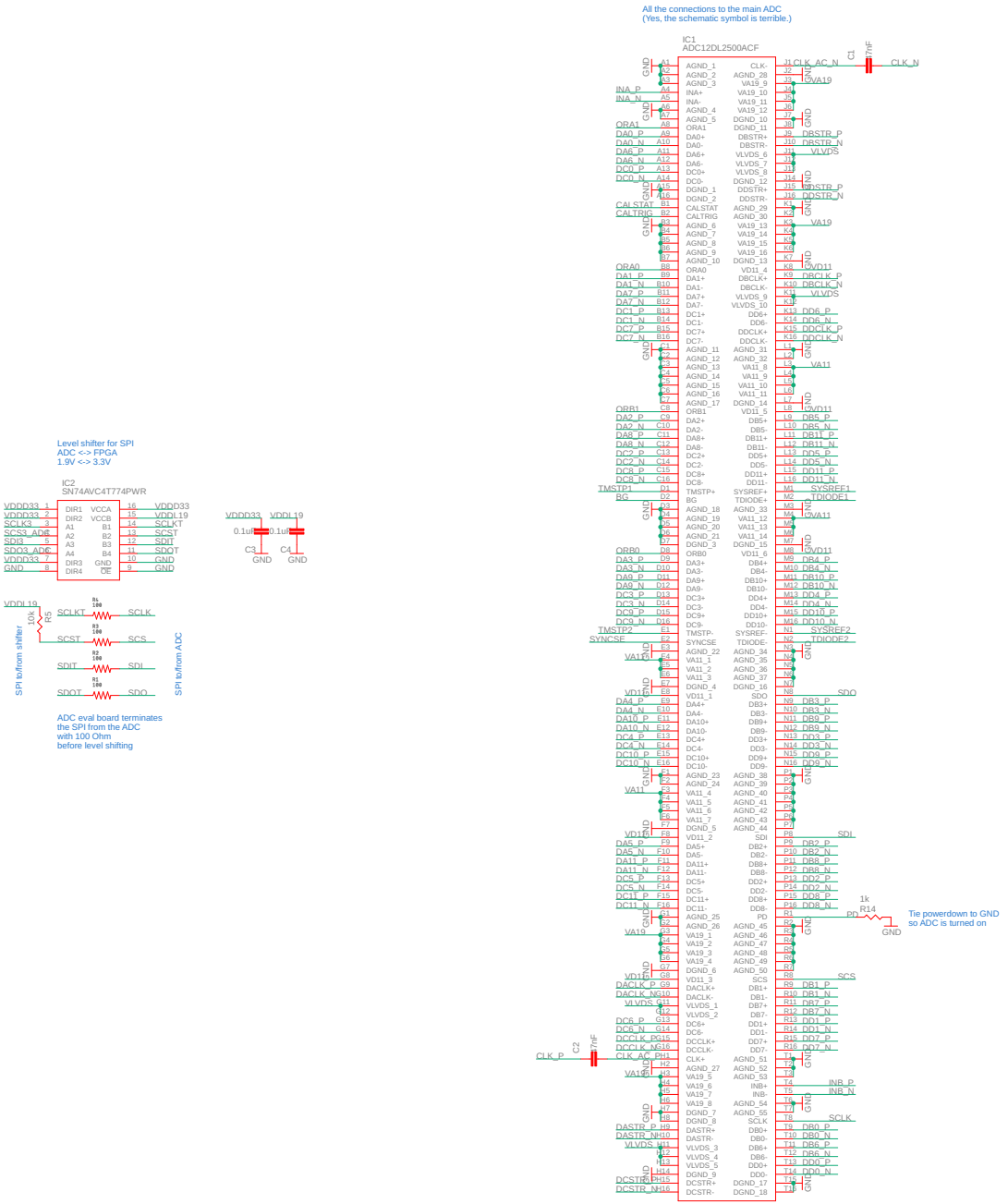

BNC input
BNCIN2
INPATH
RF relay
50 Ohm resistive splitter/combiner Output -6dB
SPLIT
OUTSPLIT
SPLITOUT
NOSPLIT
OUTSPLITTER
Buffer with high bandwidth for 1 MOhm -> 50 Ohm
2V5+
2V5-1
FL3
OPA859IDSGR
1MPATH
1MPATH50
FB and OUT are connected internally for lowest input C
50PATH
OUTPATH
Pi attenuator 1/5, -14dB 50 Ohm
FILTIN
FILTOUT
NOFILT
AC/DC coupling
ACDC_CONTROL
TLP3475R_TP,F
K7
OUTPATHFILT
OUTPATHMAIN
Z~1.5 Ohm at 2 GHz for CL05A105KA5NQNC
To input amps on next sheet
RF relay for splitting
K1
G6K-2F-RF-T-TR03_DC5
RF relay for input Z
K2
G6K-2F-RF-T-TR03_DC5
RF relay for attenuator
K3
G6K-2F-RF-T-TR03_DC5
RF relay driver for splitting
SPLIT_CONTROL
RF relay driver for input Z
50_1M_CONTROL
RF relay driver for attenuator
ATT_CONTROL
S8050
5V USB for front panel
J15
USB Type A
VCC
D-
D+
GND
SHELL
5V

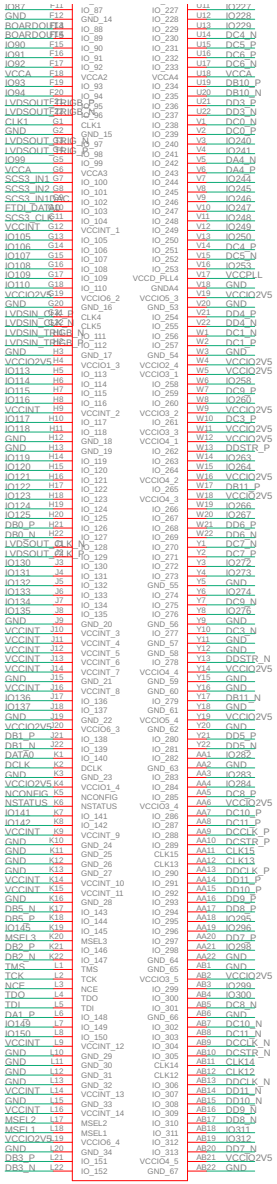

50 Ohm input
from previous sheet
OUTPATHMAIN
AOFFSET
OFFSETOUT
LMH5401IRMST
IC13
Single-ended to differential
amp with gain 4x
AIN_N
AIN_P
AOUTSMA_N
AOUTSMA_P
Buffered DAC output
for DC offset
Buffer with high bandwidth
FL1
OPA859IDSGR
DACAMPOUT1
FB and OUT
are connected
internally for
lowest input C
Buffered DAC output
-1.25 to 1.25V
IC18
TLV9102IPWR
1V25OUT-1
Subtract 2.5V/2 from DAC out
2V5DACOUT
2.5V ref voltage
from DAC, also
used on sheet 4
for channel 2
DAC output
0 to 2.5V
IC17
DAC8562SDGSR
DACOUT1
DACOUT2
DAC output 2
is used on sheet 4
for channel 2
SPI from FPGA
LMH6401IRMZR
IC14
Variable gain amp
gain 0.5x to 20x
AMPOUT_N
AMPOUT_P
INB_N
INB_P
To ADC input B
SPI
IC15
SN74AVC4T774PWR
SPI to/from FPGA
Level shifter for SPI
Amp <-> FPGA
2.5V <-> 3.3V


BNC input
BNCIN1
INPATH2
RF relay
1MPATH2
Buffer with high bandwidth
for 1 MOhm -> 50 Ohm
FL2
OPA859IDSGR
2V5+
2V5-2
1MPATH502
FB and OUT
are connected
internally for
lowest input C
50PATH2
OUTPATH2
Pi attenuator
1/5, -14dB
50 Ohm
FILTIN2
FILTOUT2
NOFILT2
AC/DC coupling
ACDC_CONTROL2
TLP3475R_TP.F
K6
OUTPATHFILT2
OUTPATHMAIN2
Z~1.5 Ohm at 2 GHz
for CL05A105KA5NQNC
To input amps
on next sheet
RF relay for input Z
K4
G6K-2F-RF-T-TR03_DC5
RF relay for attenuator
K5
RF relay driver
for input Z
RF relay driver
for attenuator
50_1M_CONTROL2
ATT_CONTROL2
5V USB for front panel
J2
5V


50 Ohm input
from previous sheet
OUTPATHMAIN2
AOFFSET2
OFFSETOUT2
LMH5401IRMST
IC21
AOUTSMA2_N
AOUTSMA2_P
LMH6401IRMZR
IC29
AMPOUT2_P
AMPOUT2_N
INA_P
INA_N
To ADC input A
Note that we have to switch
P and N so we don't need vias...
just invert ADC A result
FL4
OPA859IDSGR
DACAMPOUT2
Nearly identical to input amps for channel 1
See comments on sheet 2 for details
IC30
SN74AVC4T774PWR
IC33
TLV9102IPWR
1V25OUT-2
2V5DACOUT
DAC is on sheet 2
We use DAC output 2
for this channel, and
also the 2.5V ref voltage

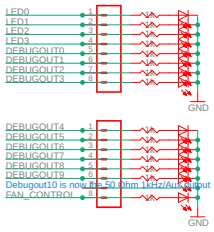

CLKOUT
50 MHz input clock from FPGA
REF_CLK
Status outputs to FPGA
MUXOUT
LOCKDETECT
SPI from FPGA
SCLK3
SDI3
SCS3_CLK
ADFCE
U2G$1
ADF4350BCPZ
CLK
DATA
LE
CE
SW
VP
CPOUT
CPGND
SDVDD
SDGND
MUXOUT
REFIN
DVDD
DGND
PDBRF
LD
VREF
VCOM
RSET
AGNDVCO
VTUNE
TEMP
AGNDVCO
VVCO
AGND
AVDD
AGNDVCO
RFOUTA+
RFOUTA-
RFOUTB+
RFOUTB-
VVCO
Filter for PLL bandwidth
CPOUT
VTUNE
VOUT
REFOUTA_N
REFOUTA_P
CLK_P
CLK_N
1.6 GHz differential output clock to ADC
GND
+3V3


All the connections to the main ADC
(Yes, the schematic symbol is terrible.)
IC1
ADC12DL2500ACF
Level shifter for SPI
ADC <-> FPGA
1.9V <-> 3.3V
IC2
SN74AVC4T774PWR
SPI to/from shifter
SPI to/from ADC
ADC eval board terminates
the SPI from the ADC
with 100 Ohm
before level shifting
Tie powerdown to GND
so ADC is turned on

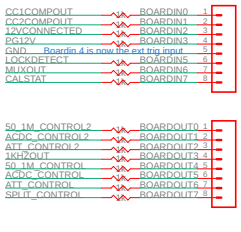


2.5V outputs from
the FPGA for debugging, etc.

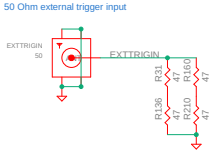
These go to LEDs for monitoring



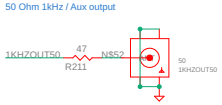
2.5V inputs and outputs to/from
the FPGA for status monitoring
and control of things, etc.



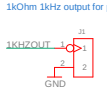
50 Ohm external trigger input



50 Ohm 1kHz / Aux output

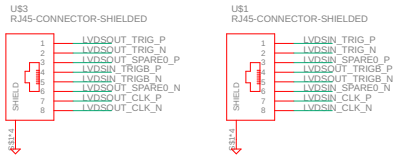


1kOhm 1kHz output for probe compensation



Extra clock input and output

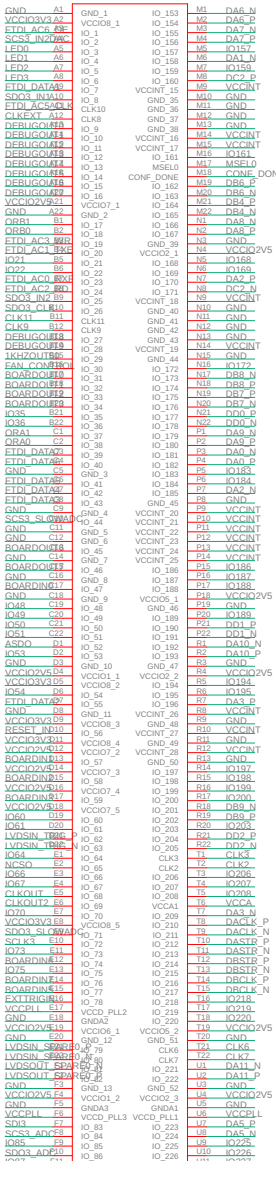
LVDS outputs and inputs for sync between boards

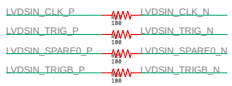


Cyclone IV E left and right I/O banks support
true LVDS transmitters, so use them for LVDS outputs

50 MHz clock for FPGA

All the inputs and outputs for the FPGA
(Yes, this schematic symbol is even terribler.)

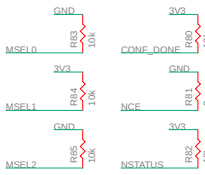




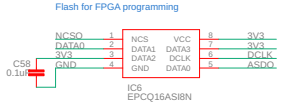
LVDS receivers require an external 100 Ohm termination resistor
between the two signals at the input buffer

We use 0201 resistors that fit on the bottom of the board and connect
the vias under the FPGA for each LVDS input pair

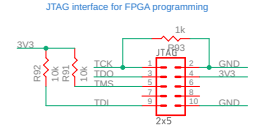
For FPGA programming



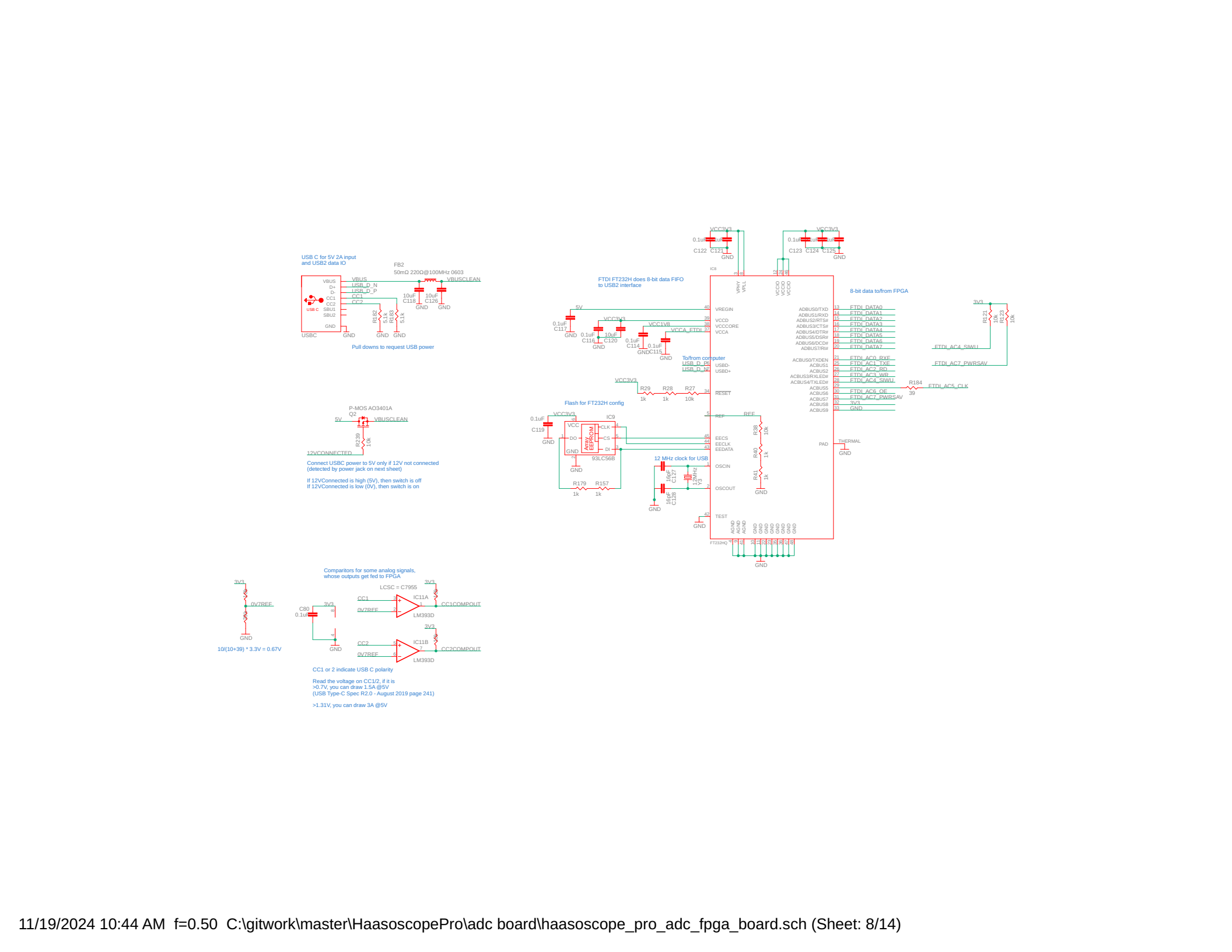
Flash for FPGA programming

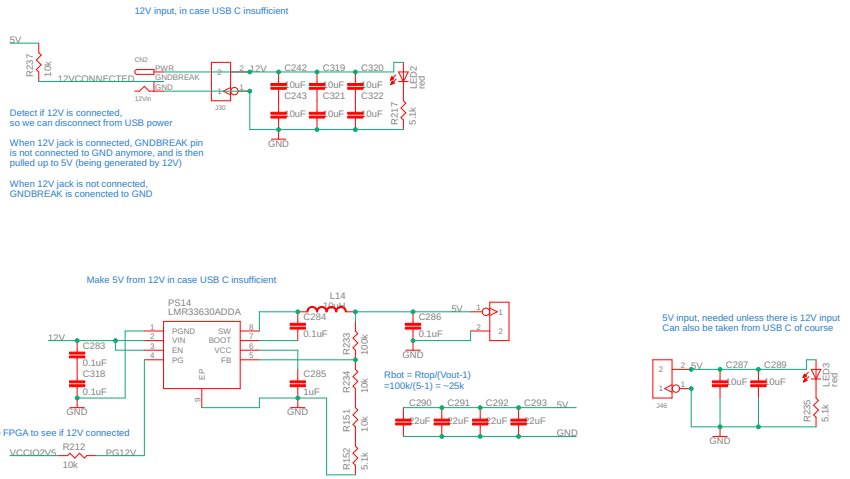


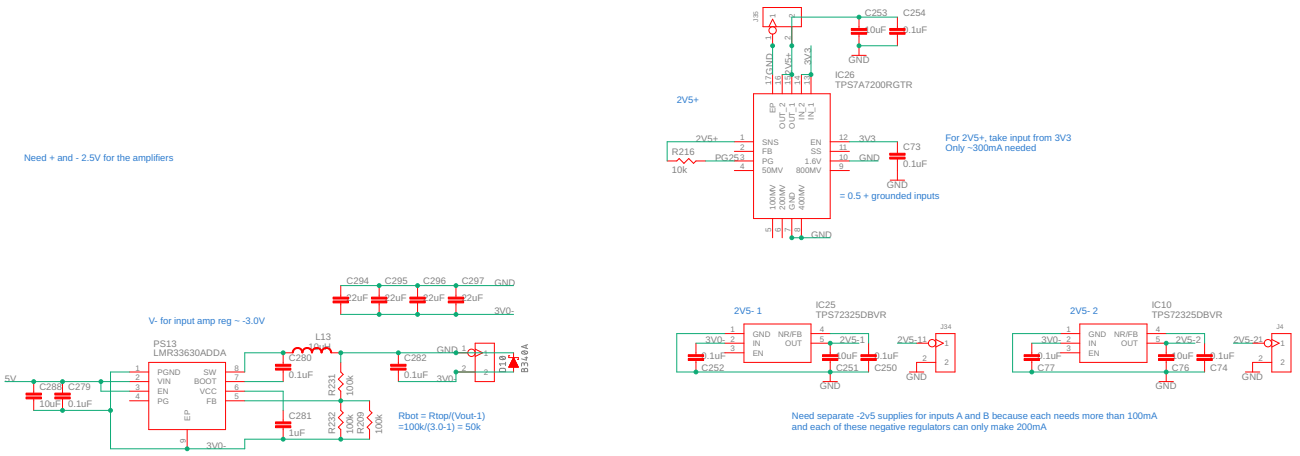
JTAG interface for FPGA programming

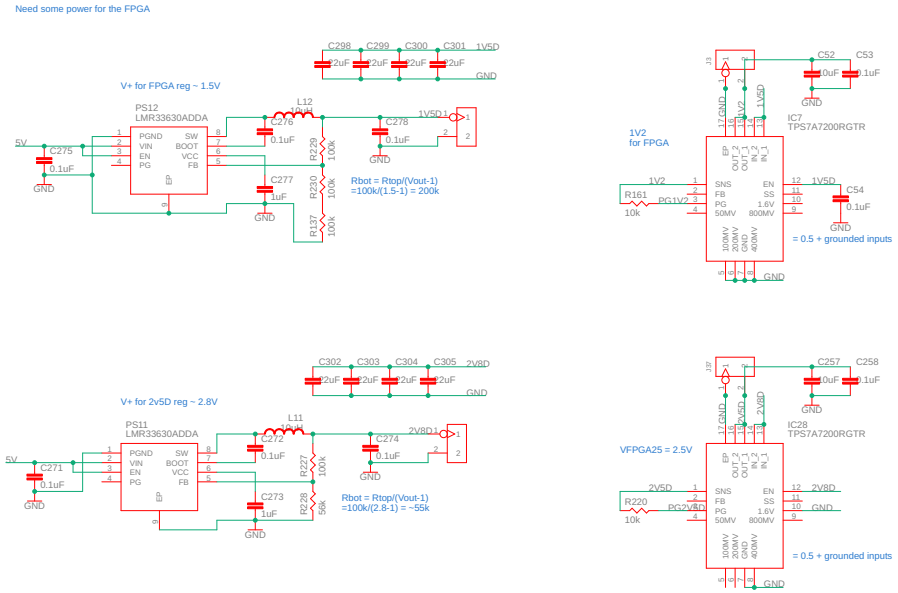


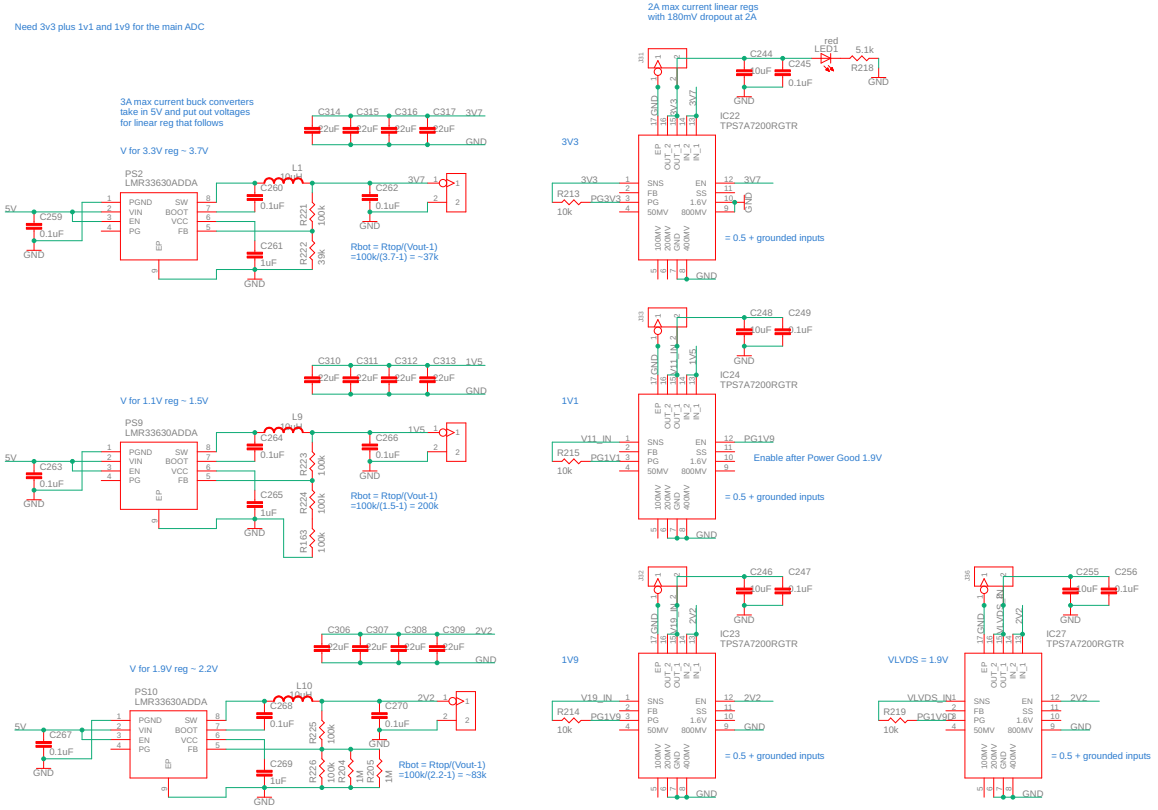
Hard reset (reload firmware) and soft reset (send reset signal to firmware) buttons

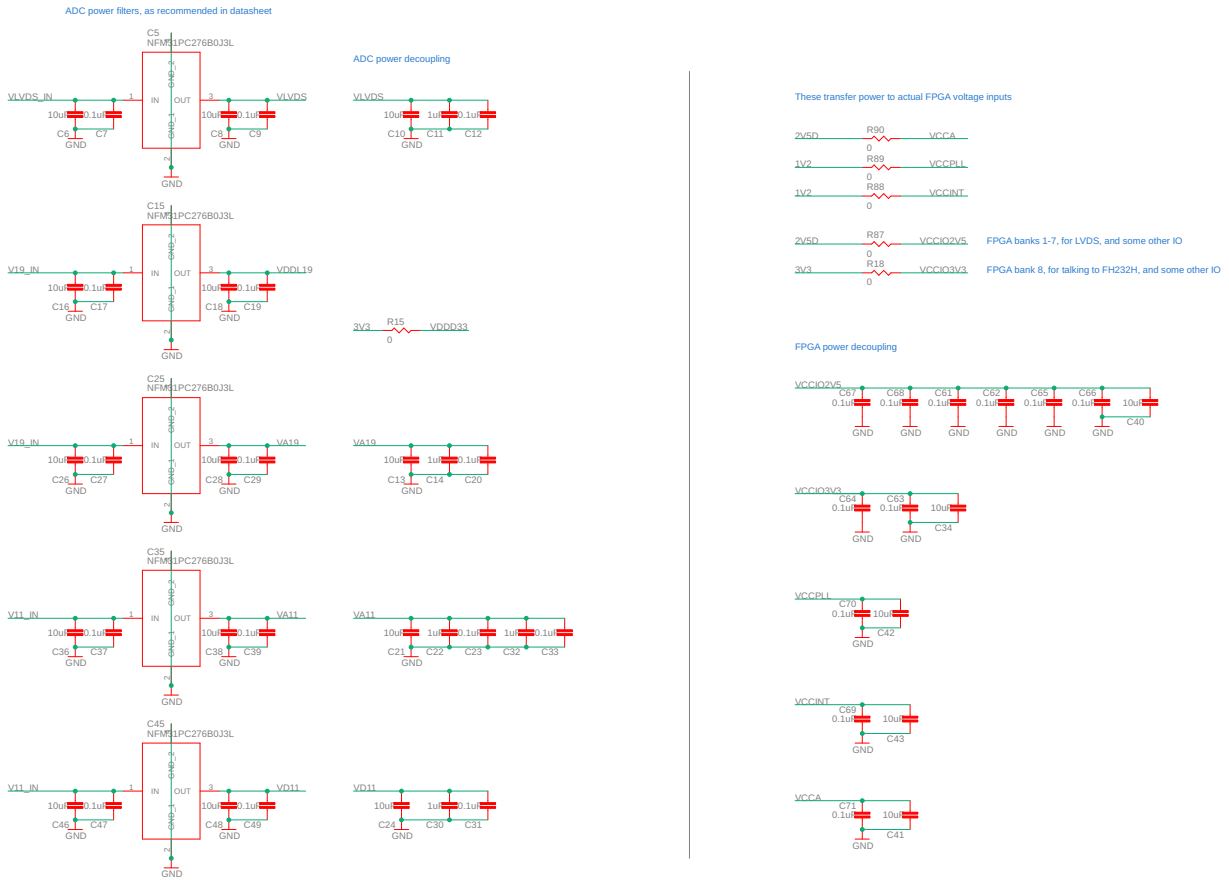

USB C for 5V 2A input
and USB2 data IO
FB2
50mΩ 220Ω@100MHz 0603
VBUSCLEAN
Pull downs to request USB power
P-MOS AO3401A
Q2
12VCONNECTED
Connect USBC power to 5V only if 12V not connected
(detected by power jack on next sheet)
If 12VConnected is high (5V), then switch is off
If 12VConnected is low (0V), then switch is on
Comparitors for some analog signals,
whose outputs get fed to FPGA
LCSC = C7955
LM393D
10/(10+39) * 3.3V = 0.67V
CC1 or 2 indicate USB C polarity
Read the voltage on CC1/2, if it is
>0.7V, you can draw 1.5A @5V
(USB Type-C Spec R2.0 - August 2019 page 241)
>1.31V, you can draw 3A @5V
FTDI FT232H does 8-bit data FIFO
to USB2 interface
8-bit data to/from FPGA
To/from computer
Flash for FT232H config
93LC56B
12 MHz clock for USB
FT232HQ

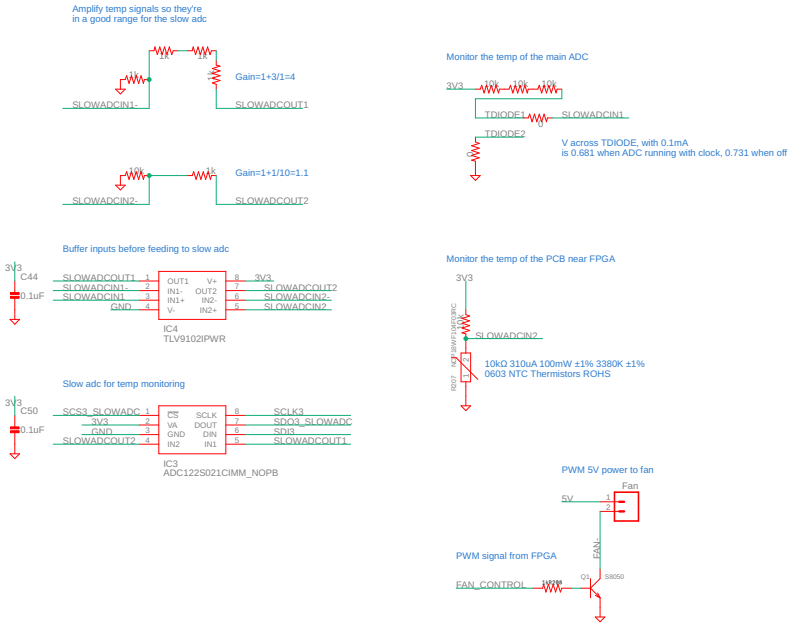

12V input, in case USB C insufficient
5V
R237
10k
12VCONNECTED
CN2
PWR
GNDBREAK
GND
12Vin
J30
12V
C242
C319
C320
C243
C321
C322
0uF
LED2
red
R217
5.1k
GND
Detect if 12V is connected,
so we can disconnect from USB power
When 12V jack is connected, GNDBREAK pin
is not connected to GND anymore, and is then
pulled up to 5V (being generated by 12V)
When 12V jack is not connected,
GNDBREAK is conencted to GND
Make 5V from 12V in case USB C insufficient
PS14
LMR33630ADDA
PGND
VIN
EN
PG
SW
BOOT
VCC
FB
EP
L14
10uH
C284
0.1uF
C283
0.1uF
C318
0.1uF
C285
1uF
R233
100k
R234
10k
R151
10k
R152
5.1k
C286
0.1uF
5V
Rbot = Rtop/(Vout-1)
=100k/(5-1) = ~25k
C290
C291
C292
C293
2uF
To FPGA to see if 12V connected
VCCIO2V5
R212
10k
PG12V
5V input, needed unless there is 12V input
Can also be taken from USB C of course
J46
C287
C289
LED3
red
R235
5.1k


Need + and - 2.5V for the amplifiers
V- for input amp reg ~ -3.0V
PS13
LMR33630ADDA
L13
10
C280
0.1uF
C282
0.1uF
C294
C295
C296
C297
2uF
GND
3V0-
5V
C278
10uF
C279
0.1uF
C281
1uF
R231
100k
R232
100k
R233
100k
Rbot = Rtop/(Vout-1)
=100k/(3.0-1) = 50k
IC26
TPS7A7200RGTR
C253
C254
0.1uF
3V3
2V5+
R216
10k
PG
C73
0.1uF
For 2V5+, take input from 3V3
Only ~300mA needed
= 0.5 + grounded inputs
2V5- 1
IC25
TPS72325DBVR
C252
C251
C250
2V5-1
2V5-11
J34
2V5- 2
IC10
C77
C76
C74
2V5-2
2V5-21
J4
Need separate -2v5 supplies for inputs A and B because each needs more than 100mA
and each of these negative regulators can only make 200mA


Need some power for the FPGA
V+ for FPGA reg ~ 1.5V
PS12
LMR33630ADDA
L12
1.5uH
C298
C299
C300
C301
2uF
1V5D
GND
5V
C275
0.1uF
C276
0.1uF
C277
1uF
R229
100k
R230
100k
R137
100k
C278
0.1uF
1V5D1
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
1V2
for FPGA
IC7
TPS7A7200RGTR
C52
C53
10uF
0.1uF
R161
10k
PG1V2
C54
0.1uF
= 0.5 + grounded inputs
V+ for 2v5D reg ~ 2.8V
PS11
LMR33630ADDA
L11
1.5uH
C302
C303
C304
C305
2V8D
C271
0.1uF
C272
0.1uF
C273
1uF
R227
100k
R228
56k
C274
0.1uF
2V8D1
Rbot = Rtop/(Vout-1)
=100k/(2.8-1) = ~55k
VFPGA25 = 2.5V
IC28
TPS7A7200RGTR
C257
C258
10uF
0.1uF
2V5D
R220
10k
PG2V8D
= 0.5 + grounded inputs


Need 3v3 plus 1v1 and 1v9 for the main ADC
3A max current buck converters take in 5V and put out voltages for linear reg that follows
V for 3.3V reg ~ 3.7V
PS2
LMR33630ADDA
L1
10uH
C259
C260
C261
C262
R221
100k
R222
39k
Rbot = Rtop/(Vout-1)
=100k/(3.7-1) = ~37k
V for 1.1V reg ~ 1.5V
PS9
LMR33630ADDA
L9
10uH
C263
C264
C265
C266
R223
100k
R224
100k
R163
100k
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
V for 1.9V reg ~ 2.2V
PS10
LMR33630ADDA
L10
10uH
C267
C268
C269
C270
R225
100k
R226
100k
R204
1M
R205
1M
Rbot = Rtop/(Vout-1)
=100k/(2.2-1) = ~83k
2A max current linear regs with 180mV dropout at 2A
3V3
IC22
TPS7A7200RGTR
C244
C245
LED1
R218
5.1k
R213
10k
= 0.5 + grounded inputs
1V1
IC24
TPS7A7200RGTR
C248
C249
R215
10k
Enable after Power Good 1.9V
= 0.5 + grounded inputs
1V9
IC23
TPS7A7200RGTR
C246
C247
R214
10k
= 0.5 + grounded inputs
VLVDS = 1.9V
IC27
TPS7A7200RGTR
C255
C256
R219
10k
= 0.5 + grounded inputs


ADC power filters, as recommended in datasheet
C5
NFM31PC276B0J3L
VLVDS_IN
VLVDS
10uf
0.1uf
C6
C7
C8
C9
GND
IN
OUT
GND
C15
NFM31PC276B0J3L
V19_IN
VDDL19
C16
C17
C18
C19
C25
NFM31PC276B0J3L
V19_IN
VA19
C26
C27
C28
C29
C35
NFM31PC276B0J3L
V11_IN
VA11
C36
C37
C38
C39
C45
NFM31PC276B0J3L
V11_IN
VD11
C46
C47
C48
C49
ADC power decoupling
VLVDS
1uf
C10
C11
C12
3V3
R15
0
VDDD33
VA19
C13
C14
C20
VA11
C21
C22
C23
C32
C33
VD11
C24
C30
C31
These transfer power to actual FPGA voltage inputs
2V5D
R90
VCCA
1V2
R89
VCCPLL
R88
VCCINT
R87
VCCIO2V5
FPGA banks 1-7, for LVDS, and some other IO
3V3
R18
VCCIO3V3
FPGA bank 8, for talking to FH232H, and some other IO
FPGA power decoupling
VCCIO2V5
C67
C68
C61
C62
C65
C66
C40
VCCIO3V3
C64
C63
C34
VCCPLL
C70
C42
VCCINT
C69
C43
VCCA
C71
C41


Amplify temp signals so they're
in a good range for the slow adc
1k
1k
1k
Gain=1+3/1=4
SLOWADCIN1-
SLOWADCOUT1
10k
1k
Gain=1+1/10=1.1
SLOWADCIN2-
SLOWADCOUT2
Buffer inputs before feeding to slow adc
3V3
C44
0.1uF
SLOWADCOUT1
SLOWADCIN1-
SLOWADCIN1
GND
OUT1
IN1-
IN1+
V-
V+
OUT2
IN2-
IN2+
3V3
SLOWADCOUT2
SLOWADCIN2-
SLOWADCIN2
IC4
TLV9102IPWR
Slow adc for temp monitoring
3V3
C50
0.1uF
SCS3_SLOWADC
3V3
GND
SLOWADCOUT2
CS
VA
GND
IN2
SCLK
DOUT
DIN
IN1
SCLK3
SDO3_SLOWADC
SDI3
SLOWADCOUT1
IC3
ADC122S021CIMM_NOPB
Monitor the temp of the main ADC
3V3
10k
10k
10k
TDIODE1
SLOWADCIN1
TDIODE2
V across TDIODE, with 0.1mA
is 0.681 when ADC running with clock, 0.731 when off
Monitor the temp of the PCB near FPGA
3V3
SLOWADCIN2
10kΩ 310uA 100mW ±1% 3380K ±1%
0603 NTC Thermistors ROHS
PWM 5V power to fan
Fan
5V
FAN
PWM signal from FPGA
FAN_CONTROL
10k
Q1
S8050