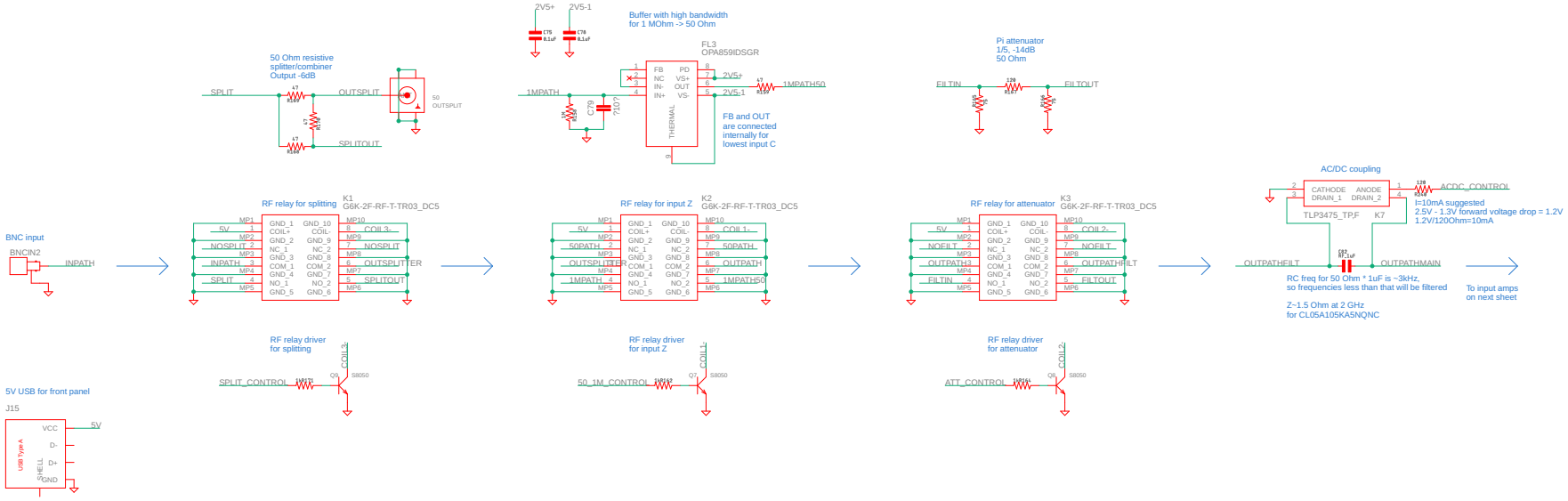
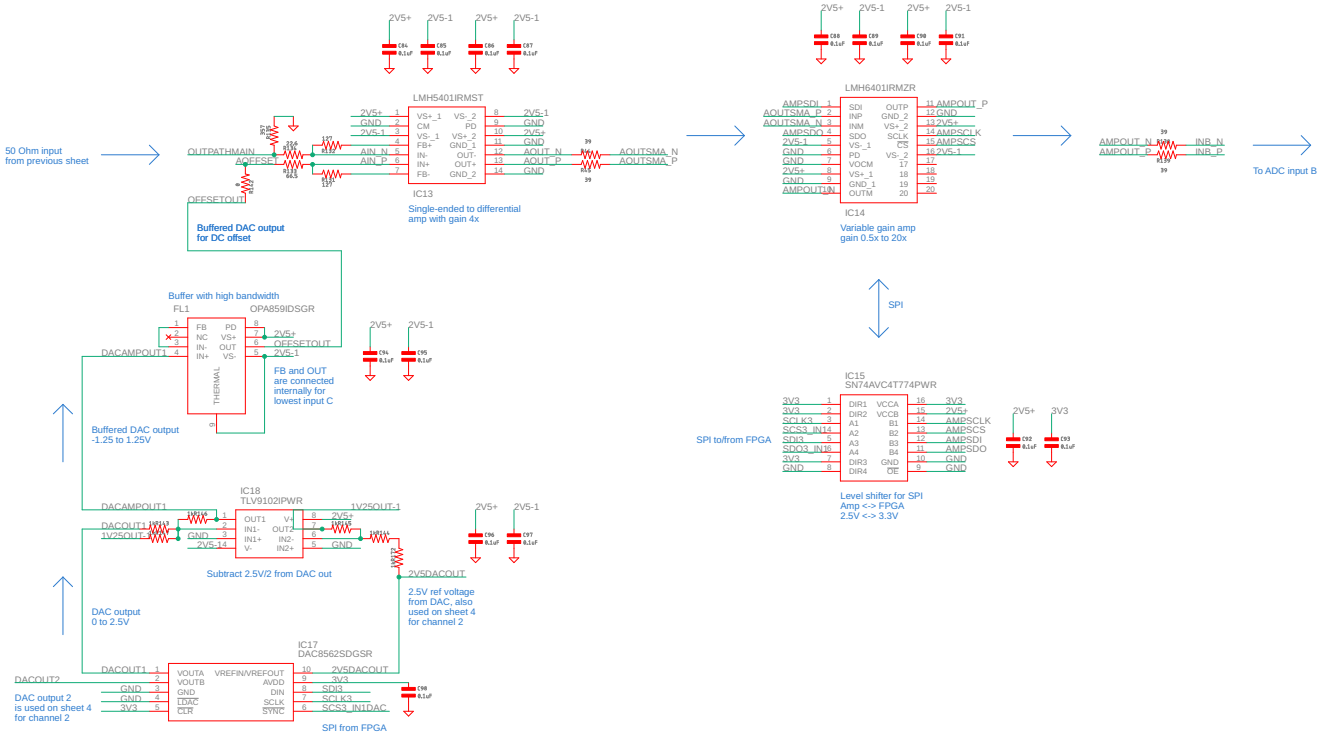
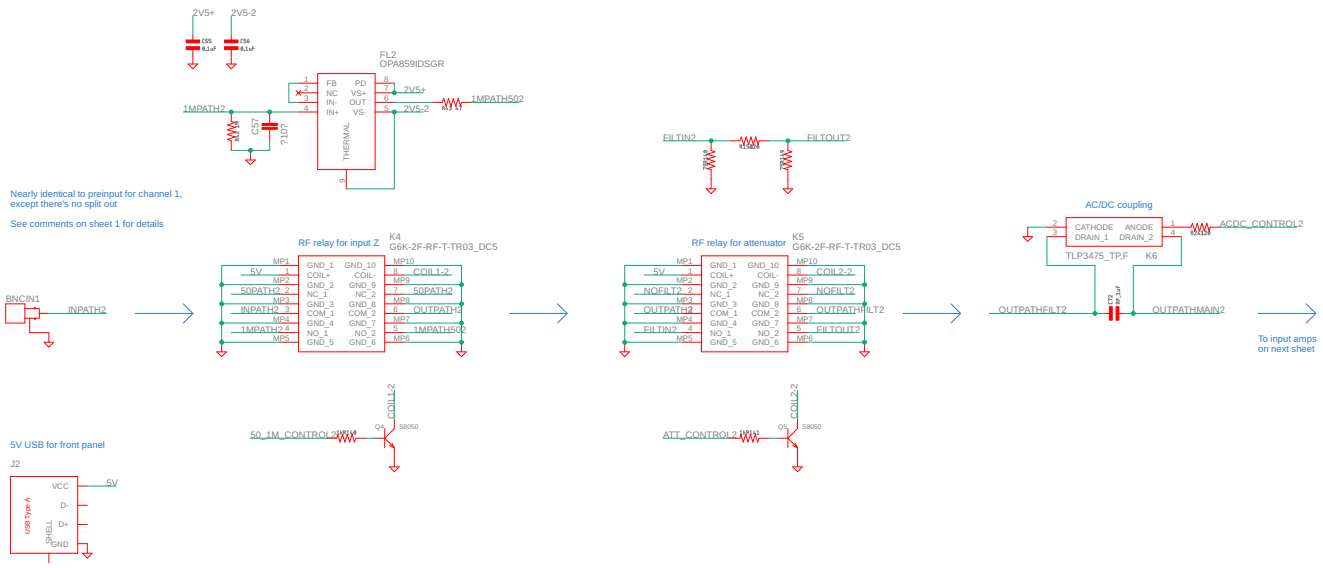
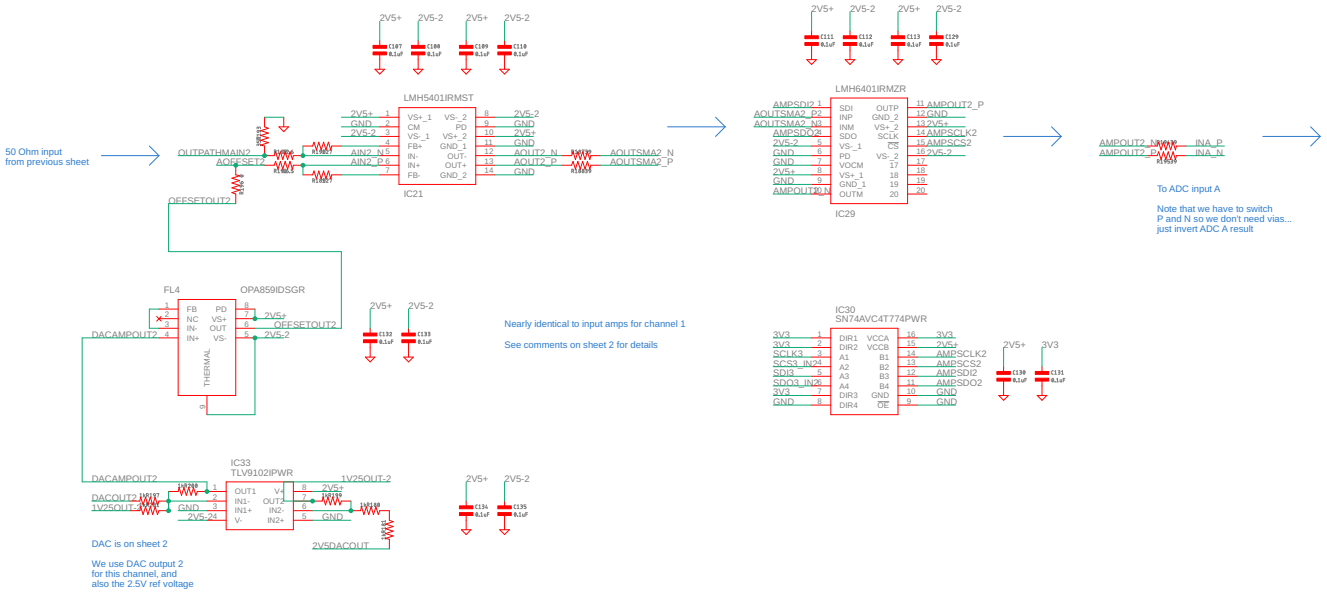
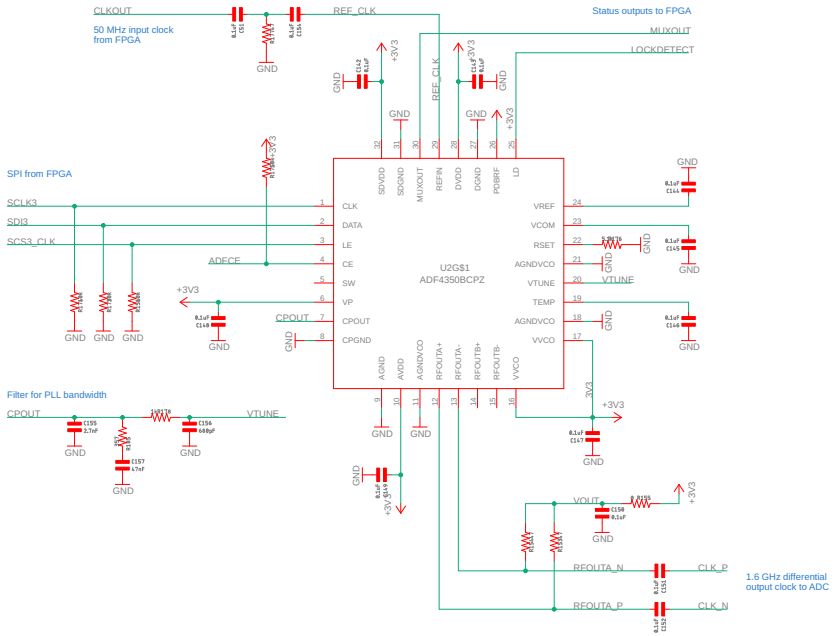
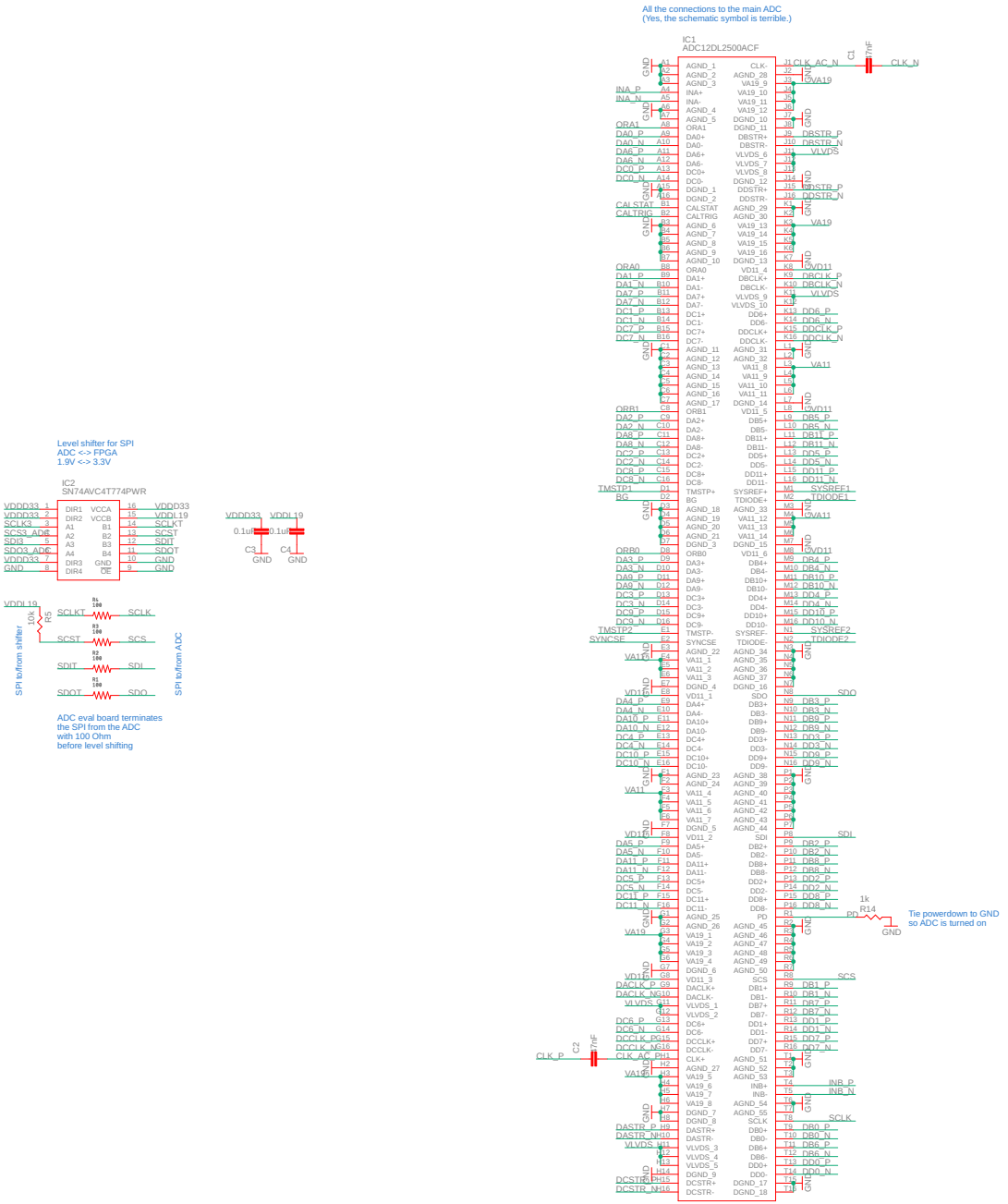

BNC input
BNCIN2
INPATH
RF relay for splitting
K1
G6K-2F-RF-T-TR03_DC5
50 Ohm resistive
splitter/combiner
Output -6dB
SPLIT
OUTSPLIT
SPLITOUT
RF relay driver
for splitting
SPLIT_CONTROL
COIL3-
5V USB for front panel
J15
VCC
D-
D+
GND
SHELL
USB TypeA
5V
2V5+
2V5-1
Buffer with high bandwidth
for 1 MOhm -> 50 Ohm
FL3
OPA859IDSGR
1MPATH
1MPATH50
FB and OUT
are connected
internally for
lowest input C
RF relay for input Z
K2
G6K-2F-RF-T-TR03_DC5
50PATH
OUTSPLITTER
OUTPATH
1MPATH50
RF relay driver
for input Z
50_1M_CONTROL
COIL1-
Pi attenuator
1/5, -14dB
50 Ohm
FILTIN
FILTOUT
RF relay for attenuator
K3
G6K-2F-RF-T-TR03_DC5
NOFILT
OUTPATHFILT
FILTIN
FILTOUT
RF relay driver
for attenuator
ATT_CONTROL
COIL2-
AC/DC coupling
CATHODE
ANODE
DRAIN_1
DRAIN_2
TLP3475_TP,F
K7
ACDC_CONTROL
I=10mA suggested
2.5V - 1.3V forward voltage drop = 1.2V
1.2V/120Ohm=10mA
OUTPATHFILT
OUTPATHMAIN
RC freq for 50 Ohm * 1uF is ~3kHz,
so frequencies less than that will be filtered
Z~1.5 Ohm at 2 GHz
for CL05A105KA5NQNC
To input amps
on next sheet

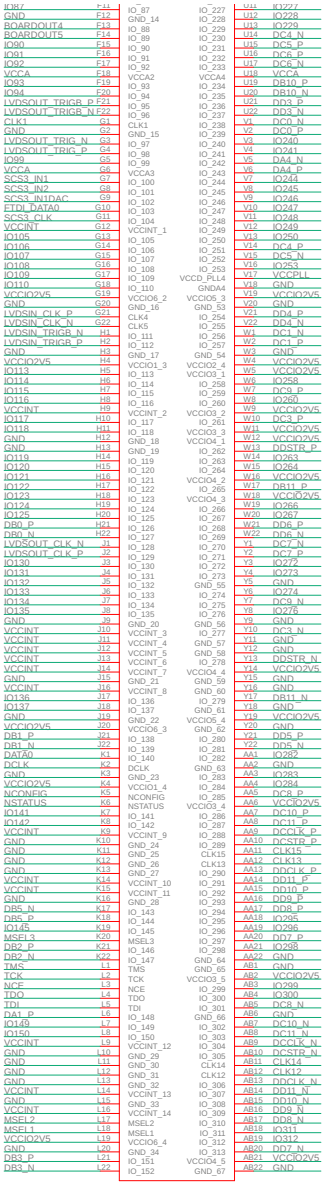

50 Ohm input
from previous sheet
OUTPATHMAIN
AOFFSET
OFFSETOUT
LMH5401IRMST
IC13
Single-ended to differential
amp with gain 4x
AOUTSMA_N
AOUTSMA_P
Buffered DAC output
for DC offset
LMH6401IRMZR
IC14
Variable gain amp
gain 0.5x to 20x
AMPOUT_N
AMPOUT_P
INB_N
INB_P
To ADC input B
Buffer with high bandwidth
FL1
OPA859IDSGR
DACAMPOUT1
FB and OUT
are connected
internally for
lowest input C
Buffered DAC output
-1.25 to 1.25V
SPI
IC15
SN74AVC4T774PWR
SPI to/from FPGA
Level shifter for SPI
Amp <-> FPGA
2.5V <-> 3.3V
IC18
TLV9102IPWR
1V25OUT-1
Subtract 2.5V/2 from DAC out
2V5DACOUT
2.5V ref voltage
from DAC, also
used on sheet 4
for channel 2
DAC output
0 to 2.5V
IC17
DAC8562SDGSR
DACOUT1
DACOUT2
DAC output 2
is used on sheet 4
for channel 2
SPI from FPGA


2V5+
2V5-2
C55
0.1uF
C56
0.1uF
FL2
OPA859IDSGR
FB
NC
IN-
IN+
PD
VS+
OUT
VS-
THERMAL
2V5+
2V5-2
1MPATH2
C57
?107
1MPATH502
FILTIN2
FILTOUT2
Nearly identical to preinput for channel 1, except there's no split out
See comments on sheet 1 for details
RF relay for input Z
K4
G6K-2F-RF-T-TR03_DC5
BNCIN1
INPATH2
5V
50PATH2
INPATH2
1MPATH2
COIL1-2
50PATH2
OUTPATH2
1MPATH502
50_1M_CONTROL2
COIL1-2
Q4
S8050
RF relay for attenuator
K5
G6K-2F-RF-T-TR03_DC5
NOFILT2
OUTPATH2
FILTIN2
COIL2-2
NOFILT2
OUTPATHFILT2
FILTOUT2
ATT_CONTROL2
COIL2-2
Q5
S8050
AC/DC coupling
CATHODE
ANODE
DRAIN_1
DRAIN_2
TLP3475_TP,F
K6
ACDC_CONTROL2
C75
0.1uF
OUTPATHFILT2
OUTPATHMAIN2
To input amps on next sheet
5V USB for front panel
J2
USB Type A
VCC
D-
D+
GND
SHELL
5V


50 Ohm input
from previous sheet
OUTPATHMAIN2
AOFFSET2
OFFSETOUT2
LMH5401IRMST
IC21
AOUTSMA2_N
AOUTSMA2_P
LMH6401IRMZR
IC29
AMPOUT2_N
AMPOUT2_P
INA_P
INA_N
To ADC input A
Note that we have to switch
P and N so we don't need vias...
just invert ADC A result
FL4
OPA859IDSGR
DACAMPOUT2
Nearly identical to input amps for channel 1
See comments on sheet 2 for details
IC30
SN74AVC4T774PWR
IC33
TLV9102IPWR
1V25OUT-2
2V5DACOUT
DAC is on sheet 2
We use DAC output 2
for this channel, and
also the 2.5V ref voltage

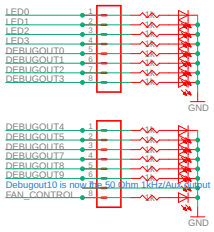

CLKOUT
50 MHz input clock from FPGA
REF_CLK
Status outputs to FPGA
MUXOUT
LOCKDETECT
SPI from FPGA
SCLK3
SDI3
SCS3_CLK
ADFCE
U2G$1
ADF4350BCPZ
CLK
DATA
LE
CE
SW
VP
CPOUT
CPGND
SDVDD
SDGND
MUXOUT
REFIN
DVDD
DGND
PDBRF
LD
VREF
VCOM
RSET
AGNDVCO
VTUNE
TEMP
AGNDVCO
VVCO
AGND
AVDD
AGNDVCO
RFOUTA+
RFOUTA-
RFOUTB+
RFOUTB-
VVCO
Filter for PLL bandwidth
CPOUT
VTUNE
VOUT
REFOUTA_N
REFOUTA_P
CLK_P
CLK_N
1.6 GHz differential output clock to ADC
GND
+3V3


All the connections to the main ADC
(Yes, the schematic symbol is terrible.)
IC1
ADC12DL2500ACF
Level shifter for SPI
ADC <-> FPGA
1.9V <-> 3.3V
IC2
SN74AVC4T774PWR
SPI to/from shifter
SPI to/from ADC
ADC eval board terminates
the SPI from the ADC
with 100 Ohm
before level shifting
Tie powerdown to GND
so ADC is turned on

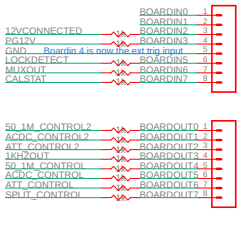

IO87 F11
GND F12
BOARDOUT4 F13
BOARDOUT5 F14
IO90 F15
IO91 F16
IO92 F17
VCCA F18
IO93 F19
IO94 F20
LVDSOUT_TRIGB_P F21
LVDSOUT_TRIGB_N F22
CLK1 G1
GND G2
LVDSOUT_TRIG_N G3
LVDSOUT_TRIG_P G4
IO99 G5
VCCA G6
SCS3_IN1 G7
SCS3_IN2 G8
SCS3_IN1DAC G9
FTDI_DATA0 G10
SCS3_CLK G11
VCCINT G12
IO105 G13
IO106 G14
IO107 G15
IO108 G16
IO109 G17
IO110 G18
VCCIO2V5 G19
GND G20
LVDSIN_CLK_P G21
LVDSIN_CLK_N G22
LVDSIN_TRIGB_N H1
LVDSIN_TRIGB_P H2
GND H3
VCCIO2V5 H4
IO113 H5
IO114 H6
IO115 H7
IO116 H8
VCCINT H9
IO117 H10
IO118 H11
GND H12
GND H13
IO119 H14
IO120 H15
IO121 H16
IO122 H17
IO123 H18
IO124 H19
IO125 H20
DB0_P H21
DB0_N H22
LVDSOUT_CLK_N J1
LVDSOUT_CLK_P J2
IO130 J3
IO131 J4
IO132 J5
IO133 J6
IO134 J7
IO135 J8
GND J9
VCCINT J10
VCCINT J11
VCCINT J12
VCCINT J13
VCCINT J14
GND J15
VCCINT J16
IO136 J17
IO137 J18
GND J19
VCCIO2V5 J20
DB1_P J21
DB1_N J22
DATA0 K1
DCLK K2
GND K3
VCCIO2V5 K4
NCONFIG K5
NSTATUS K6
IO141 K7
IO142 K8
VCCINT K9
GND K10
GND K11
GND K12
GND K13
VCCINT K14
VCCINT K15
GND K16
DB5_N K17
DB5_P K18
IO145 K19
MSEL3 K20
DB2_P K21
DB2_N K22
TMS L1
TCK L2
NCE L3
TDO L4
TDI L5
DA1_P L6
IO149 L7
IO150 L8
VCCINT L9
GND L10
GND L11
GND L12
GND L13
VCCINT L14
GND L15
VCCINT L16
MSEL2 L17
MSEL1 L18
VCCIO2V5 L19
GND L20
DB3_P L21
DB3_N L22
IO_87
GND_14
IO_88
IO_89
IO_90
IO_91
IO_92
VCCA2
IO_93
IO_94
IO_95
IO_96
CLK1
GND_15
IO_97
IO_98
IO_99
VCCA3
IO_100
IO_101
IO_102
IO_103
IO_104
VCCINT_1
IO_105
IO_106
IO_107
IO_108
IO_109
IO_110
VCCIO6_2
GND_16
CLK4
CLK5
IO_111
IO_112
GND_17
VCCIO1_3
IO_113
IO_114
IO_115
IO_116
VCCINT_2
IO_117
IO_118
GND_18
GND_19
IO_119
IO_120
IO_121
IO_122
IO_123
IO_124
IO_125
IO_126
IO_127
IO_128
IO_129
IO_130
IO_131
IO_132
IO_133
IO_134
IO_135
GND_20
VCCINT_3
VCCINT_4
VCCINT_5
VCCINT_6
VCCINT_7
GND_21
VCCINT_8
IO_136
IO_137
GND_22
VCCIO6_3
IO_138
IO_139
IO_140
DCLK
GND_23
VCCIO1_4
NCONFIG
NSTATUS
IO_141
IO_142
VCCINT_9
GND_24
GND_25
GND_26
GND_27
VCCINT_10
VCCINT_11
GND_28
IO_143
IO_144
IO_145
MSEL3
IO_146
IO_147
TMS
TCK
NCE
TDO
TDI
IO_148
IO_149
IO_150
VCCINT_12
GND_29
GND_30
GND_31
GND_32
VCCINT_13
GND_33
VCCINT_14
MSEL2
MSEL1
VCCIO6_4
GND_34
IO_151
IO_152
IO_227
IO_228
IO_229
IO_230
IO_231
IO_232
IO_233
VCCA4
IO_234
IO_235
IO_236
IO_237
IO_238
IO_239
IO_240
IO_241
IO_242
IO_243
IO_244
IO_245
IO_246
IO_247
IO_248
IO_249
IO_250
IO_251
IO_252
IO_253
VCCD_PLL4
GNDA4
VCCIO5_3
GND_53
IO_254
IO_255
IO_256
IO_257
GND_54
VCCIO2_4
VCCIO3_1
IO_258
IO_259
IO_260
VCCIO3_2
IO_261
VCCIO3_3
VCCIO4_1
IO_262
IO_263
IO_264
VCCIO4_2
IO_265
VCCIO4_3
IO_266
IO_267
IO_268
IO_269
IO_270
IO_271
IO_272
IO_273
GND_55
IO_274
IO_275
IO_276
GND_56
IO_277
GND_57
GND_58
IO_278
VCCIO4_4
GND_59
GND_60
IO_279
GND_61
VCCIO5_4
GND_62
IO_280
IO_281
IO_282
GND_63
IO_283
IO_284
IO_285
VCCIO3_4
IO_286
IO_287
IO_288
IO_289
CLK15
CLK13
IO_290
IO_291
IO_292
IO_293
IO_294
IO_295
IO_296
IO_297
IO_298
GND_64
GND_65
VCCIO3_5
IO_299
IO_300
IO_301
GND_66
IO_302
IO_303
IO_304
IO_305
CLK14
CLK12
IO_306
IO_307
IO_308
IO_309
IO_310
IO_311
VCCIO4_5
GND_67
U11 IO227
U12 IO228
U13 IO229
U14 DC4_N
U15 DC5_P
U16 DC5_P
U17 DC6_N
U18 VCCA
U19 DB10_P
U20 DB10_N
U21 DD3_P
U22 DD3_N
V1 DC0_N
V2 DC0_P
V3 IO240
V4 IO241
V5 DA4_N
V6 DA4_P
V7 IO244
V8 IO245
V9 IO246
V10 IO247
V11 IO248
V12 IO249
V13 IO250
V14 DC4_P
V15 DC5_N
V16 IO253
V17 VCCPLL
V18 GND
V19 VCCIO2V5
V20 GND
V21 DD4_P
V22 DD4_N
W1 DC1_N
W2 DC1_P
W3 GND
W4 VCCIO2V5
W5 VCCIO2V5
W6 IO258
W7 DC9_P
W8 IO260
W9 VCCIO2V5
W10 DC3_P
W11 VCCIO2V5
W12 VCCIO2V5
W13 DDSTR_P
W14 IO263
W15 IO264
W16 VCCIO2V5
W17 DB11_P
W18 VCCIO2V5
W19 IO266
W20 IO267
W21 DD6_P
W22 DD6_N
Y1 DC7_N
Y2 DC7_P
Y3 IO272
Y4 IO273
Y5 GND
Y6 IO274
Y7 DC9_N
Y8 IO276
Y9 GND
Y10 DC3_N
Y11 GND
Y12 GND
Y13 DDSTR_N
Y14 VCCIO2V5
Y15 GND
Y16 GND
Y17 DB11_N
Y18 GND
Y19 VCCIO2V5
Y20 GND
Y21 DD5_P
Y22 DD5_N
AA1 IO282
AA2 GND
AA3 IO283
AA4 IO284
AA5 DC8_P
AA6 VCCIO2V5
AA7 DC10_P
AA8 DC11_P
AA9 DCCLK_P
AA10 DCSTR_P
AA11 CLK15
AA12 CLK13
AA13 DDCLK_P
AA14 DD11_P
AA15 DD10_P
AA16 DD9_P
AA17 DD8_P
AA18 IO295
AA19 IO296
AA20 DD7_P
AA21 IO298
AA22 GND
AB1 GND
AB2 VCCIO2V5
AB3 IO299
AB4 IO300
AB5 DC8_N
AB6 GND
AB7 DC10_N
AB8 DC11_N
AB9 DCCLK_N
AB10 DCSTR_N
AB11 CLK14
AB12 CLK12
AB13 DDCLK_N
AB14 DD11_N
AB15 DD10_N
AB16 DD9_N
AB17 DD8_N
AB18 IO311
AB19 IO312
AB20 DD7_N
AB21 VCCIO2V5
AB22 GND

2.5V outputs from
the FPGA for debugging, etc.

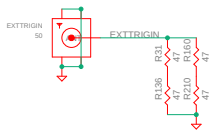
These go to LEDs for monitoring



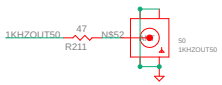
2.5V inputs and outputs to/from
the FPGA for status monitoring
and control of things, etc.



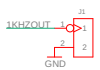
50 Ohm external trigger input



50 Ohm 1kHz / Aux output

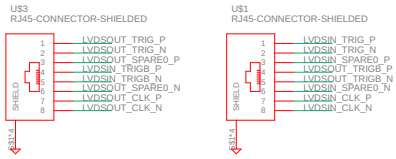


1kOhm 1kHz output for probe compensation



Extra clock input and output

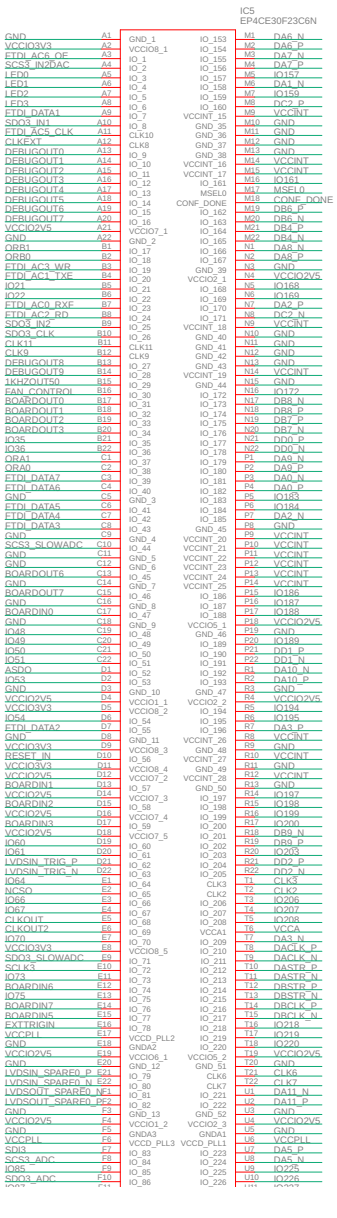
LVDS outputs and inputs for sync between boards

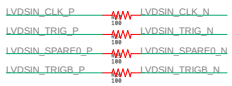


Cyclone IV E left and right I/O banks support
true LVDS transmitters, so use them for LVDS outputs

50 MHz clock for FPGA

All the inputs and outputs for the FPGA
(Yes, this schematic symbol is even terribler.)

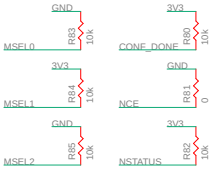




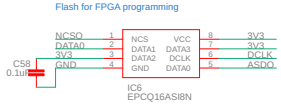
LVDS receivers require an external 100 Ohm termination resistor
between the two signals at the input buffer

We use 0201 resistors that fit on the bottom of the board and connect
the vias under the FPGA for each LVDS input pair

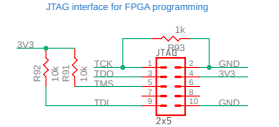
For FPGA programming



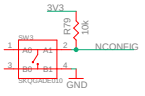
Flash for FPGA programming

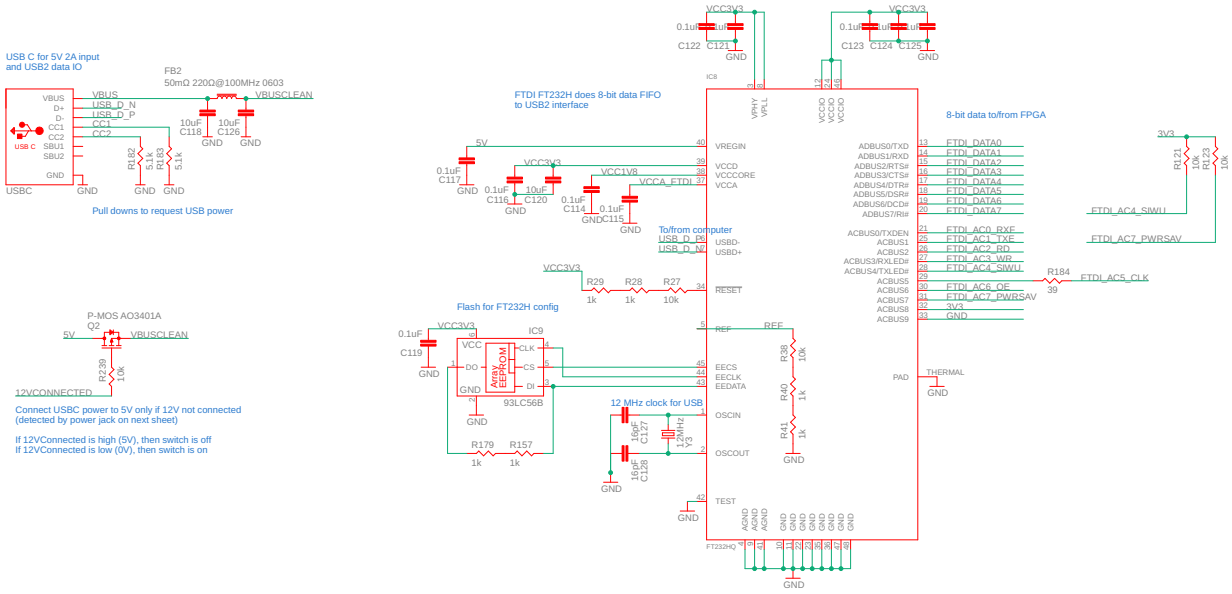


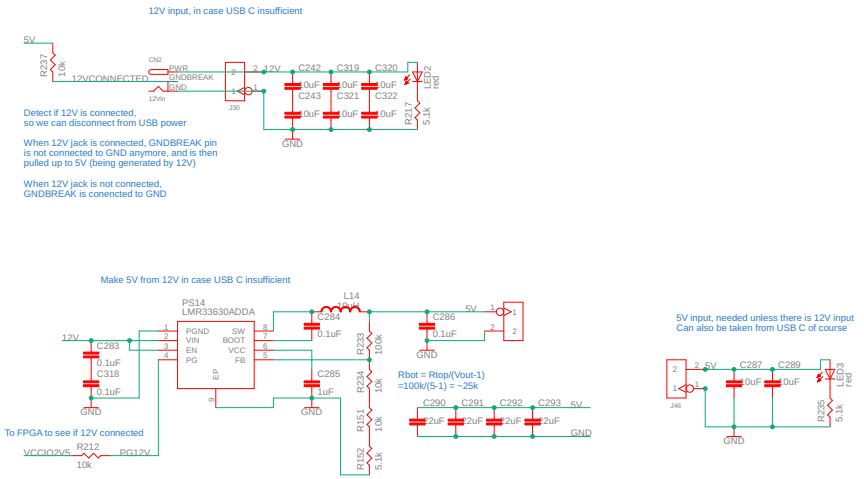
JTAG interface for FPGA programming

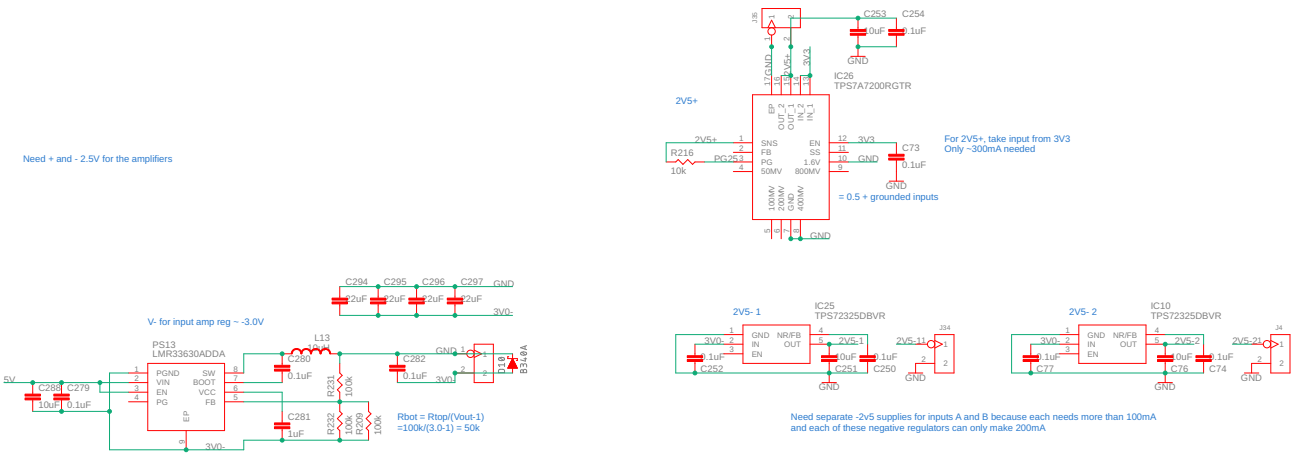


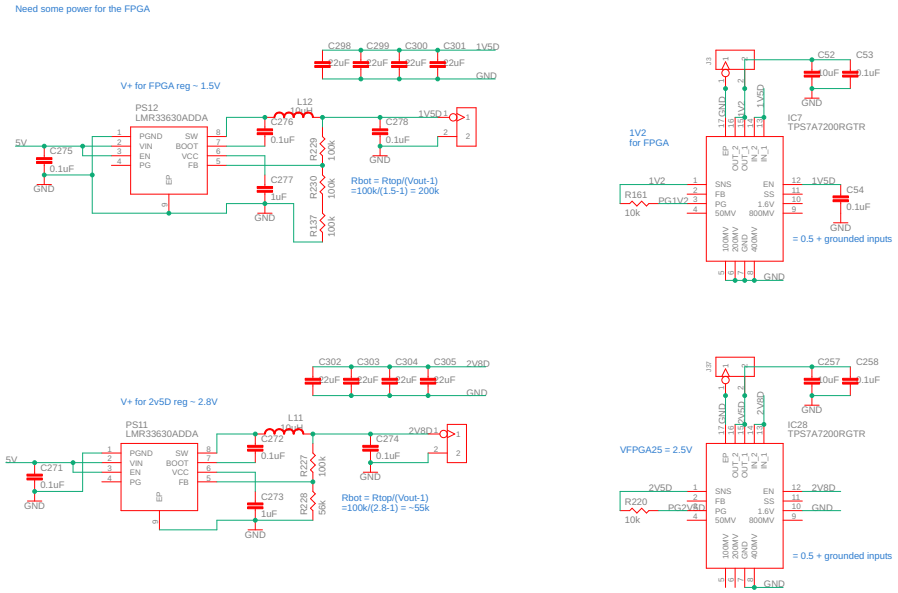
Hard reset (reload firmware) and soft reset (send reset signal to firmware) buttons

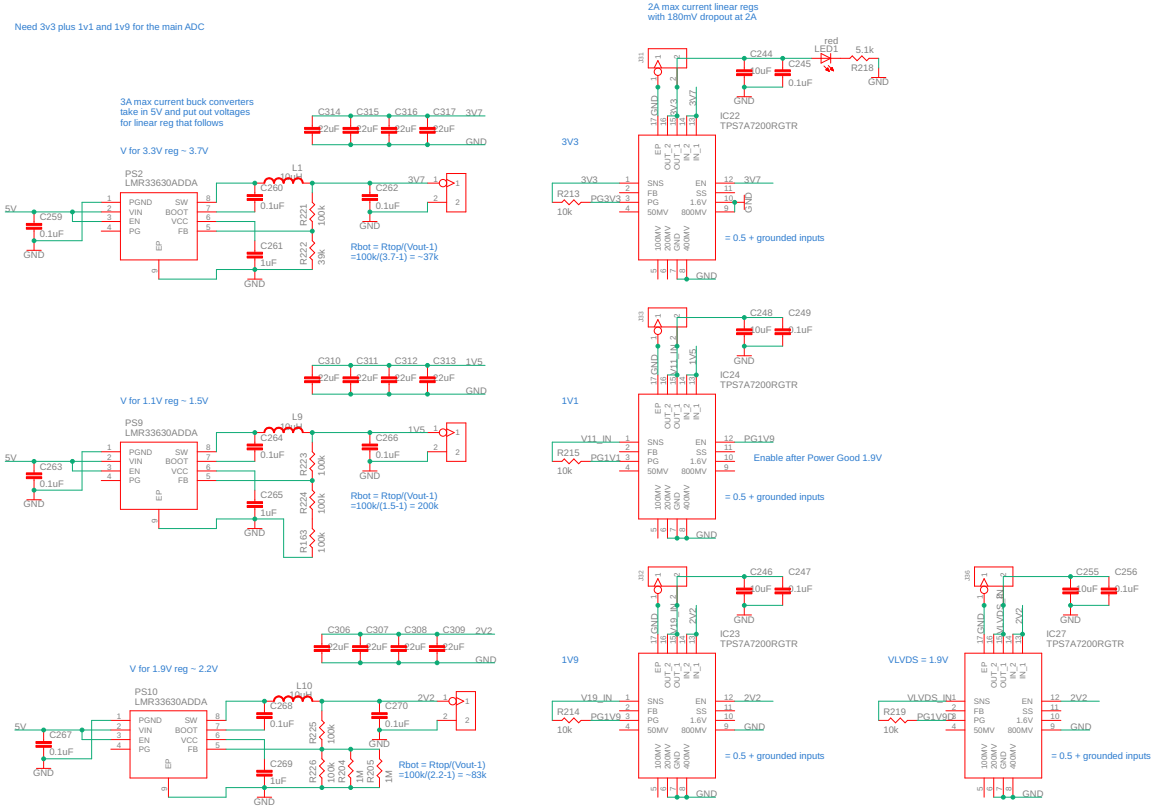


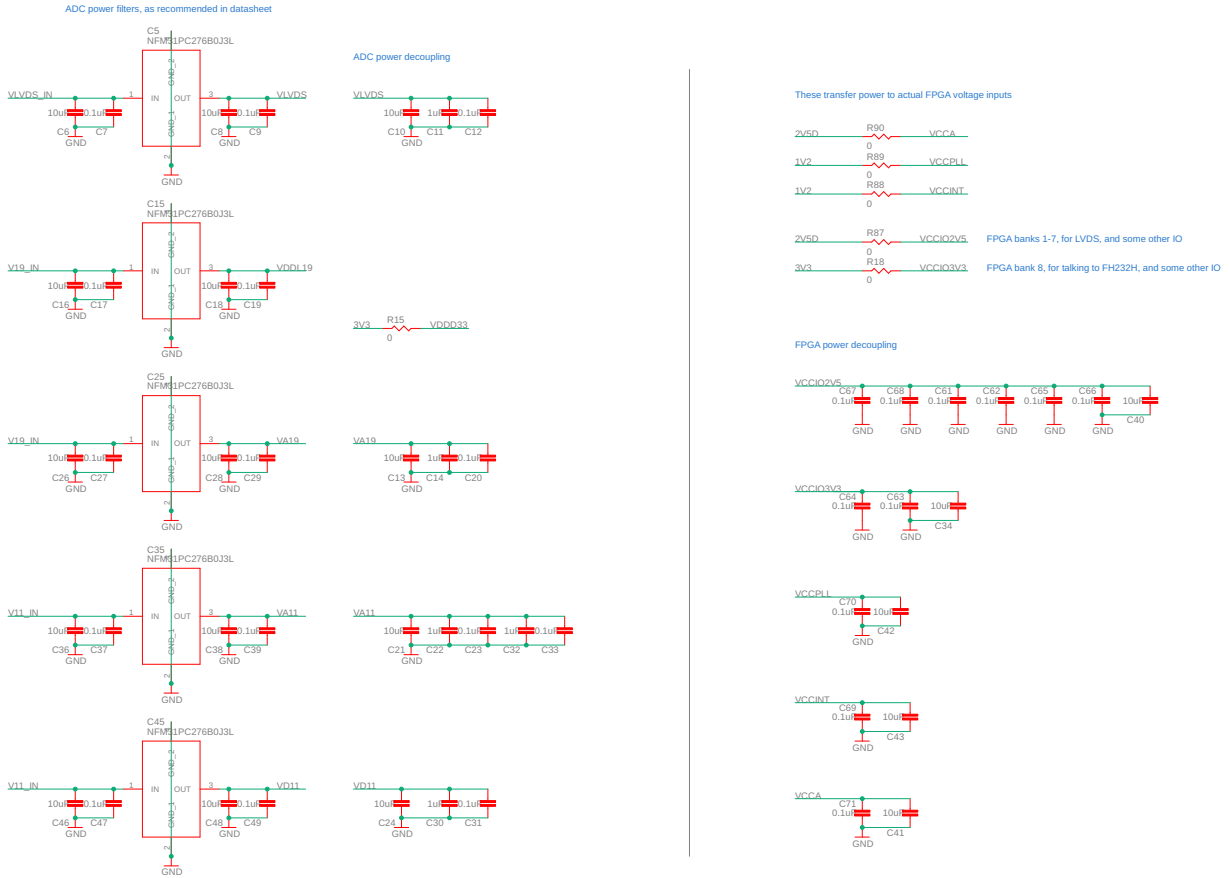

USB C for 5V 2A input
and USB2 data IO
FB2
50mΩ 220Ω@100MHz 0603
VBUS
USB_D_N
USB_D_P
CC1
CC2
VBUSCLEAN
10uF C118
10uF C126
R182 5.1k
R183 5.1k
USBC
GND
Pull downs to request USB power
P-MOS AO3401A
Q2
5V
VBUSCLEAN
R239 10k
12VCONNECTED
Connect USBC power to 5V only if 12V not connected
(detected by power jack on next sheet)
If 12VConnected is high (5V), then switch is off
If 12VConnected is low (0V), then switch is on
VCC3V3
0.1uF C122
1uF C121
0.1uF C123
1uF C124
1uF C125
IC8
FTDI FT232H does 8-bit data FIFO
to USB2 interface
VREGIN
VCCD
VCCCORE
VCCA
VCC1V8
VCCA_FTDI
0.1uF C117
0.1uF C116
10uF C120
0.1uF C114
0.1uF C115
USBD-
USBD+
To/from computer
USB_D_P6
USB_D_N6
RESET
R29 1k
R28 1k
R27 10k
Flash for FT232H config
IC9
0.1uF C119
93LC56B
Array EEPROM
CLK
CS
DI
DO
R179 1k
R157 1k
REF
R38 10k
R40 1k
R41 1k
EECS
EECLK
EEDATA
12 MHz clock for USB
16pF C127
16pF C126
12MHz Y3
OSCIN
OSCOUT
TEST
PAD
THERMAL
8-bit data to/from FPGA
ADBUS0/TXD
ADBUS1/RXD
ADBUS2/RTS#
ADBUS3/CTS#
ADBUS4/DTR#
ADBUS5/DSR#
ADBUS6/DCD#
ADBUS7/RI#
ACBUS0/TXDEN
ACBUS1
ACBUS2
ACBUS3/RXLED#
ACBUS4/TXLED#
ACBUS5
ACBUS6
ACBUS7
ACBUS8
ACBUS9
FTDI_DATA0
FTDI_DATA1
FTDI_DATA2
FTDI_DATA3
FTDI_DATA4
FTDI_DATA5
FTDI_DATA6
FTDI_DATA7
FTDI_AC0_RXF
FTDI_AC1_TXE
FTDI_AC2_RD
FTDI_AC3_WR
FTDI_AC4_SIWU
FTDI_AC6_OE
FTDI_AC7_PWRSAV
3V3
GND
3V3
R121 10k
R123 10k
FTDI_AC4_SIWU
FTDI_AC7_PWRSAV
R184 39
FTDI_AC5_CLK
FT232HQ

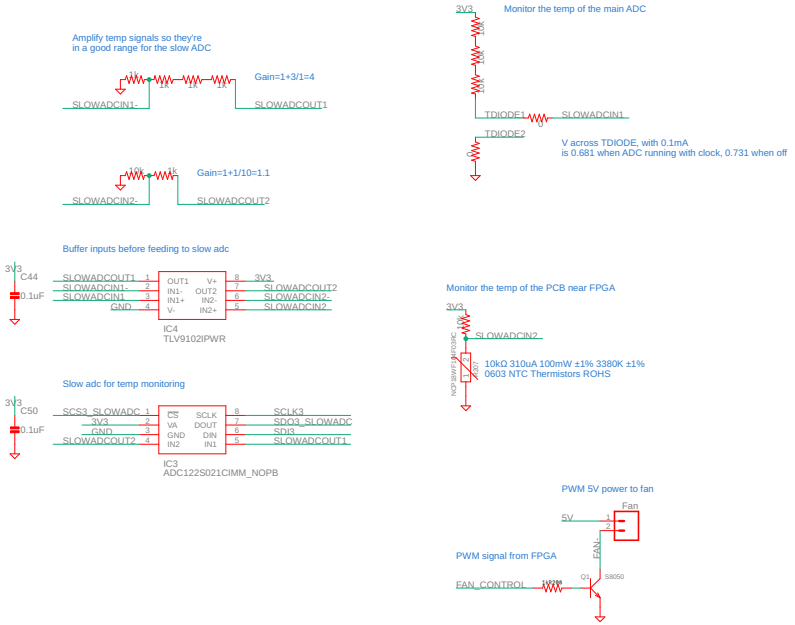

12V input, in case USB C insufficient
5V
R237
10k
12VCONNECTED
CN2
PWR
GNDBREAK
GND
12Vin
J30
12V
C242
C319
C320
C243
C321
C322
0uF
LED2
red
R217
5.1k
GND
Detect if 12V is connected,
so we can disconnect from USB power
When 12V jack is connected, GNDBREAK pin
is not connected to GND anymore, and is then
pulled up to 5V (being generated by 12V)
When 12V jack is not connected,
GNDBREAK is conencted to GND
Make 5V from 12V in case USB C insufficient
PS14
LMR33630ADDA
PGND
VIN
EN
PG
SW
BOOT
VCC
FB
L14
10uH
C284
0.1uF
C286
5V
C283
C318
R233
100k
R234
10k
C285
1uF
R151
10k
R152
5.1k
Rbot = Rtop/(Vout-1)
=100k/(5-1) = ~25k
C290
C291
C292
C293
2uF
To FPGA to see if 12V connected
VCCIO2V5
R212
10k
PG12V
5V input, needed unless there is 12V input
Can also be taken from USB C of course
J46
C287
C289
LED3
R235


Need + and - 2.5V for the amplifiers
V- for input amp reg ~ -3.0V
PS13
LMR33630ADDA
L13
Rbot = Rtop/(Vout-1)
=100k/(3.0-1) = 50k
IC26
TPS7A7200RGTR
2V5+
For 2V5+, take input from 3V3
Only ~300mA needed
= 0.5 + grounded inputs
2V5- 1
IC25
TPS72325DBVR
2V5- 2
IC10
TPS72325DBVR
Need separate -2v5 supplies for inputs A and B because each needs more than 100mA
and each of these negative regulators can only make 200mA


Need some power for the FPGA
V+ for FPGA reg ~ 1.5V
PS12
LMR33630ADDA
L12
1V5D
C298
C299
C300
C301
2uF
GND
5V
C275
0.1uF
C276
0.1uF
C277
1uF
R229
100k
R230
100k
R137
100k
C278
0.1uF
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
1V2
for FPGA
IC7
TPS7A7200RGTR
C52
C53
10uF
0.1uF
R161
10k
C54
0.1uF
= 0.5 + grounded inputs
V+ for 2v5D reg ~ 2.8V
PS11
LMR33630ADDA
L11
2V8D
C302
C303
C304
C305
C271
C272
C273
C274
R227
100k
R228
56k
Rbot = Rtop/(Vout-1)
=100k/(2.8-1) = ~55k
VFPGA25 = 2.5V
IC28
TPS7A7200RGTR
C257
C258
R220
10k
2V5D
2V8D


Need 3v3 plus 1v1 and 1v9 for the main ADC
3A max current buck converters take in 5V and put out voltages for linear reg that follows
V for 3.3V reg ~ 3.7V
PS2
LMR33630ADDA
L1
10uH
C260
0.1uF
C262
0.1uF
C259
0.1uF
C261
1uF
R221
100k
R222
39k
Rbot = Rtop/(Vout-1)
=100k/(3.7-1) = ~37k
C314 C315 C316 C317 3V7
2uF
GND
5V
3V7
V for 1.1V reg ~ 1.5V
PS9
LMR33630ADDA
L9
10uH
C264
0.1uF
C266
0.1uF
C263
0.1uF
C265
1uF
R223
100k
R224
100k
R163
100k
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
C310 C311 C312 C313 1V5
1V5
V for 1.9V reg ~ 2.2V
PS10
LMR33630ADDA
L10
10uH
C268
0.1uF
C270
0.1uF
C267
0.1uF
C269
1uF
R225
100k
R226
100k
R204
1M
R205
1M
Rbot = Rtop/(Vout-1)
=100k/(2.2-1) = ~83k
C306 C307 C308 C309 2V2
2V2
2A max current linear regs with 180mV dropout at 2A
3V3
IC22
TPS7A7200RGTR
C244
10uF
C245
0.1uF
LED1
red
5.1k
R218
R213
10k
PG3V3
= 0.5 + grounded inputs
1V1
IC24
TPS7A7200RGTR
C248
10uF
C249
0.1uF
V11_IN
R215
10k
PG1V1
PG1V9
Enable after Power Good 1.9V
= 0.5 + grounded inputs
1V9
IC23
TPS7A7200RGTR
C246
10uF
C247
0.1uF
V19_IN
R214
10k
PG1V9
= 0.5 + grounded inputs
VLVDS = 1.9V
IC27
TPS7A7200RGTR
C255
10uF
C256
0.1uF
VLVDS_IN1
R219
10k
PG1V9
= 0.5 + grounded inputs


ADC power filters, as recommended in datasheet
C5
NFM31PC276B0J3L
VLVDS_IN
VLVDS
C6 C7 C8 C9
GND
C15
NFM31PC276B0J3L
V19_IN
VDDL19
C16 C17 C18 C19
C25
NFM31PC276B0J3L
V19_IN
VA19
C26 C27 C28 C29
C35
NFM31PC276B0J3L
V11_IN
VA11
C36 C37 C38 C39
C45
NFM31PC276B0J3L
V11_IN
VD11
C46 C47 C48 C49
ADC power decoupling
VLVDS
C10 C11 C12
VA19
C13 C14 C20
VA11
C21 C22 C23 C32 C33
VD11
C24 C30 C31
3V3
R15
0
VDDD33
These transfer power to actual FPGA voltage inputs
2V5D
R90
0
VCCA
1V2
R89
0
VCCPLL
1V2
R88
0
VCCINT
2V5D
R87
0
VCCIO2V5
FPGA banks 1-7, for LVDS, and some other IO
3V3
R18
0
VCCIO3V3
FPGA bank 8, for talking to FH232H, and some other IO
FPGA power decoupling
VCCIO2V5
C67 C68 C61 C62 C65 C66 C40
VCCIO3V3
C64 C63 C34
VCCPLL
C70 C42
VCCINT
C69 C43
VCCA
C71 C41


Amplify temp signals so they're
in a good range for the slow ADC
1k
1k
1k
1k
Gain=1+3/1=4
SLOWADCIN1-
SLOWADCOUT1
10k
1k
Gain=1+1/10=1.1
SLOWADCIN2-
SLOWADCOUT2
Buffer inputs before feeding to slow adc
3V3
C44
0.1uF
SLOWADCOUT1
SLOWADCIN1-
SLOWADCIN1
GND
OUT1
IN1-
IN1+
V-
V+
OUT2
IN2-
IN2+
3V3
SLOWADCOUT2
SLOWADCIN2-
SLOWADCIN2
IC4
TLV9102IPWR
Slow adc for temp monitoring
3V3
C50
0.1uF
SCS3_SLOWADC
3V3
GND
SLOWADCOUT2
CS
VA
GND
IN2
SCLK
DOUT
DIN
IN1
SCLK3
SDO3_SLOWADC
SDI3
SLOWADCOUT1
IC3
ADC122S021CIMM_NOPB
Monitor the temp of the main ADC
3V3
TDIODE1
SLOWADCIN1
TDIODE2
V across TDIODE, with 0.1mA
is 0.681 when ADC running with clock, 0.731 when off
Monitor the temp of the PCB near FPGA
3V3
SLOWADCIN2
10kΩ 310uA 100mW ±1% 3380K ±1%
0603 NTC Thermistors ROHS
PWM 5V power to fan
Fan
5V
FAN
PWM signal from FPGA
FAN_CONTROL
Q1
S8050