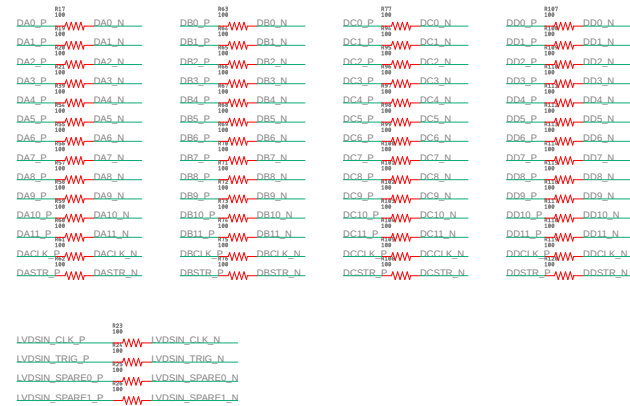
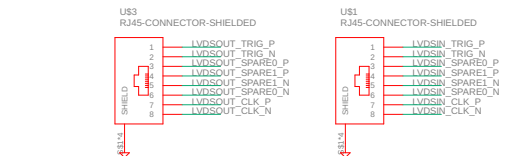
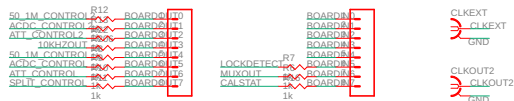






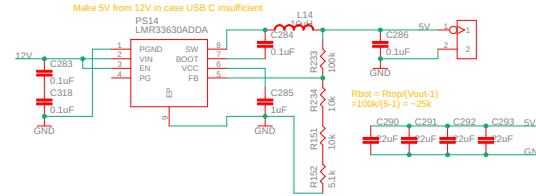
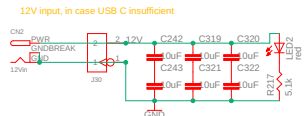
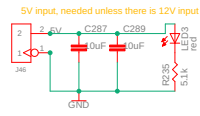
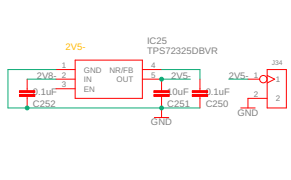
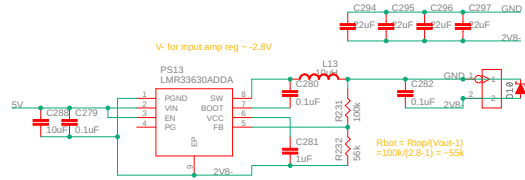
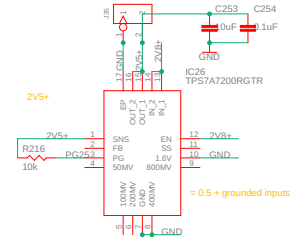
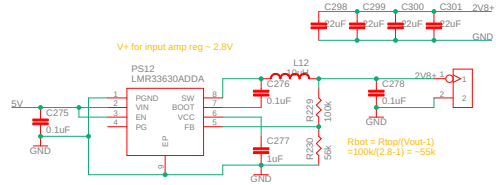
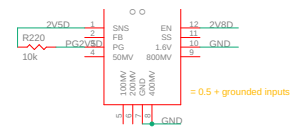
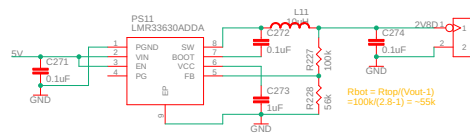
BOARDIO17A	IO_88	U13	IO229	
BOARDIO18A	IO_89	U14	DC4_N	
IO90	F18	IO_231	U15	DC5_P
IO91	F19	IO_232	U16	DC6_P
IO92	F17	IO_233	U17	DC8_N
VCCA_F18	VCCA2	VCCA4	U18	VCCA
IO93	F19	IO_234	U19	DB10_P
IO94	F20	IO_235	U20	DB10_N
LVDSIN_SE0B0	IO_95	IO_236	U21	DD3_P
LVDSIN_SE0B1	IO_96	IO_237	U22	DD3_N
CLK1_G1	CLK1	IO_238	V1	DC0_N
GND_G1	GND_15	IO_239	V2	DC0_P
LVDSOUT_0B0	IO_97	IO_240	V3	IO240
LVDSOUT_0B1	IO_98	IO_241	V4	IO241
IO99	G5	IO_242	V5	DA4_N
VCCA_G5	VCCA3	IO_243	V6	DA4_P
SCSS_INT1_G1	IO_100	IO_244	V7	IO244
SCSS_INT2_G5	IO_101	IO_245	V8	IO245
SCSS_INT0B0	IO_102	IO_246	V9	IO246
ETDI_DATA0	IO_103	IO_247	V10	IO247
SCSS_CLK1_G1	IO_104	IO_248	V11	IO248
VCCINT_G14	VCCINT_1	IO_249	V12	IO249
IO105	IO_105	IO_250	V13	IO250
IO106	G14	IO_251	V14	DC4_P
IO107	G15	IO_252	V15	DC5_N
IO108	G16	IO_253	V16	IO253
IO109	G17	IO_254	V17	VCCPLL
IO110	G18	GND44	V18	GND
VCCIO2V5_H1	VCCIO2_2	VCCIO5_3	V19	VCCIO2V5
GND_G20	GND_16	GND_53	V20	GND
LVDSIN_0B0_P	CLK4	IO_254	V21	DD4_P
LVDSIN_0B0_N	CLK5	IO_255	V22	DD4_N
LVDSOUT_SE0B0	IO_256	IO_256	W1	DC1_N
LVDSOUT_SE0B1	IO_257	IO_257	W2	DC1_P
GND_H1	GND_17	GND_54	W3	GND
VCCIO2V5_H1	VCCIO3_3	VCCIO2_4	W4	VCCIO2V5
IO113	H5	IO_113	W5	VCCIO2V5
IO114	H6	IO_114	W6	IO258
IO115	H7	IO_115	W7	DC3_P
IO116	H8	IO_116	W8	IO260
VCCINT_H9	VCCINT_2	VCCIO3_2	W9	VCCIO2V5
IO117	H10	IO_117	W10	DC3_P
IO118	H11	IO_118	W11	VCCIO2V5
GND_H13	GND_18	VCCIO4_1	W13	DDSTR_P
IO119	H14	IO_119	W14	IO263
IO120	H15	IO_120	W15	IO264
IO121	H16	IO_121	W16	VCCIO2V5
IO122	H17	IO_122	W17	DB11_P
IO123	H18	IO_123	W18	VCCIO2V5
IO124	H19	IO_124	W19	IO266
IO125	H20	IO_125	W20	IO267
DB0_P_H21	IO_126	IO_268	W21	DD6_P
DB0_N_H22	IO_127	IO_269	W22	DD6_N
LVDSOUT_0L0	IO_128	IO_270	V1	DC7_N
IO130	J1	IO_129	V2	DC7_P
IO131	J2	IO_130	V3	IO272
IO132	J3	IO_131	V4	IO273
IO133	J4	IO_132	Y5	GND
IO134	J5	IO_133	Y6	IO274
IO135	J6	IO_134	Y7	DC9_N
GND_J9	GND_20	IO_135	Y8	IO275
VCCINT_J10	VCCINT_3	GND_58	V9	GND
VCCINT_J11	VCCINT_4	IO_277	V10	DC3_N
VCCINT_J12	VCCINT_5	GND_57	V11	GND
VCCINT_J13	VCCINT_6	GND_58	V12	GND
VCCINT_J14	VCCINT_7	IO_278	V13	DDSTR_N
GND_J15	GND_21	VCCIO4_4	V14	VCCIO2V5
VCCINT_J16	VCCINT_8	GND_59	V15	GND
IO136	J17	GND_60	V16	GND
IO137	J18	IO_136	V17	DB11_N
GND_J19	GND_22	GND_61	V18	GND
VCCIO2V5_H1	VCCIO5_4	VCCIO5_4	V19	VCCIO2V5
DB1_P_K20	VCCIO6_3	GND_62	V20	GND
DB1_N_K21	IO_138	IO_280	V21	DD5_P
DATA0_K1	IO_139	IO_281	V22	DD5_N
CLK_K2	IO_140	IO_282	AA1	IO282
VCCIO2V5_K4	CLK_K2	GND_63	AA2	GND
NCONF0_K5	GND_23	IO_283	AA3	IO283
NCONF1_K6	VCCIO4_4	IO_284	AA4	IO284
NSTATUS_K7	NCONF0	IO_285	AA5	DC8_P
IO141	NSTATUS	VCCIO4_4	AA6	VCCIO2V5
IO142	K9	IO_286	AA7	DC10_P
VCCINT_K9	IO_142	IO_287	AA8	DC11_P
GND_K10	GND_24	IO_288	AA9	DCSTR_P
GND_K11	GND_25	IO_289	AA10	DCSTR_N
GND_K12	GND_26	CLK15	AA11	CLK15
VCCINT_K14	GND_27	CLK13	AA12	CLK13
VCCINT_K15	VCCINT_10	IO_290	AA13	DD11_P
GND_K16	VCCINT_11	IO_291	AA14	DD10_P
DB5_P_K17	GND_28	IO_292	AA15	DD10_N
IO145	K19	IO_293	AA16	DD9_P
MSEL3_K20	IO_143	IO_294	AA17	DD8_P
DB2_P_K21	IO_144	IO_295	AA18	IO295
DB2_N_K22	MSEL3	IO_296	AA19	IO296
TMS_L3	DB2_P_K21	IO_297	AA20	DD7_P
TPK_L5	IO_145	IO_298	AA21	IO298
NCE_L1	IO_146	GND_64	AA22	GND
TD0_L4	TMS	GND_65	AB1	GND
TD1_L6	TPK	VCCIO5_5	AB2	VCCIO2V5
IO149	NCE	IO_299	AB3	IO299
IO150	TD0	IO_300	AB4	IO300
VCCINT_L3	TD1	IO_301	AB5	DC8_N
GND_L10	IO_148	GND_66	AB6	GND
GND_L11	IO_149	IO_302	AB7	DC10_N
VCCINT_L12	IO_150	IO_303	AB8	DC11_N
GND_L13	VCCINT_12	IO_304	AB9	DCCLK_N
GND_L14	GND_29	IO_305	AB10	DCSTR_N
GND_L15	GND_30	CLK14	AB11	CLK14
VCCINT_L16	GND_31	CLK12	AB12	CLK12
GND_L17	GND_32	IO_306	AB13	DDCLK_N
VCCINT_L18	VCCINT_13	IO_307	AB14	DD11_N
GND_L19	GND_33	IO_308	AB15	DD10_N
VCCINT_L20	VCCINT_14	IO_309	AB16	DD9_P
MSEL1_L21	MSEL1	IO_310	AB17	DD8_N
VCCIO2V5_L22	MSEL1	IO_311	AB18	IO311
GND_L23	VCCIO4_4	IO_312	AB19	IO312
DB3_P_L24	GND_34	IO_313	AB20	DD7_N
DB3_N_L25	IO_151	VCCIO4_5	AB21	VCCIO2V5
	IO_152	GND_67	AB22	GND

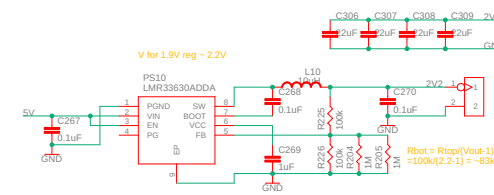
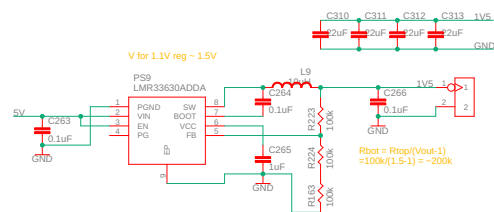
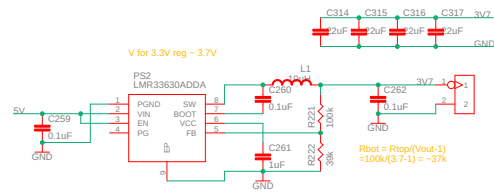


The LVDS receiver requires an external 100 Ohm termination resistor between the two signals at the input buffer.









V+ for 2v5D reg ~ 2.8V

