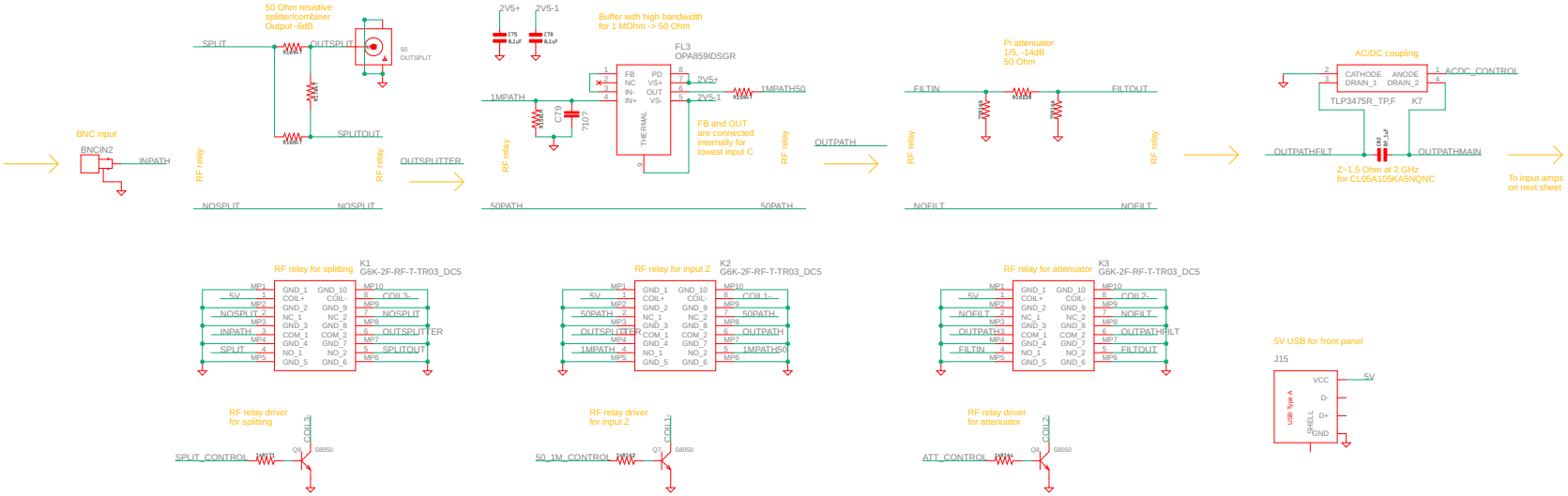
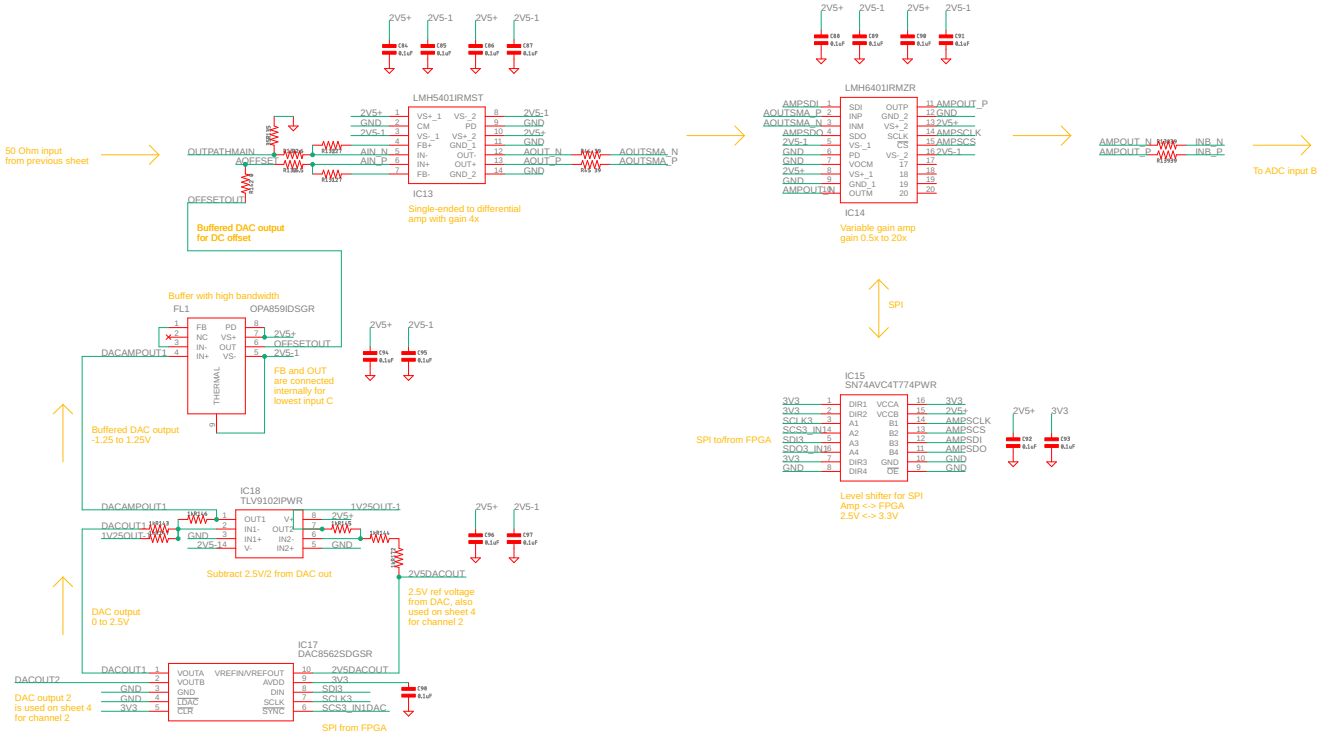
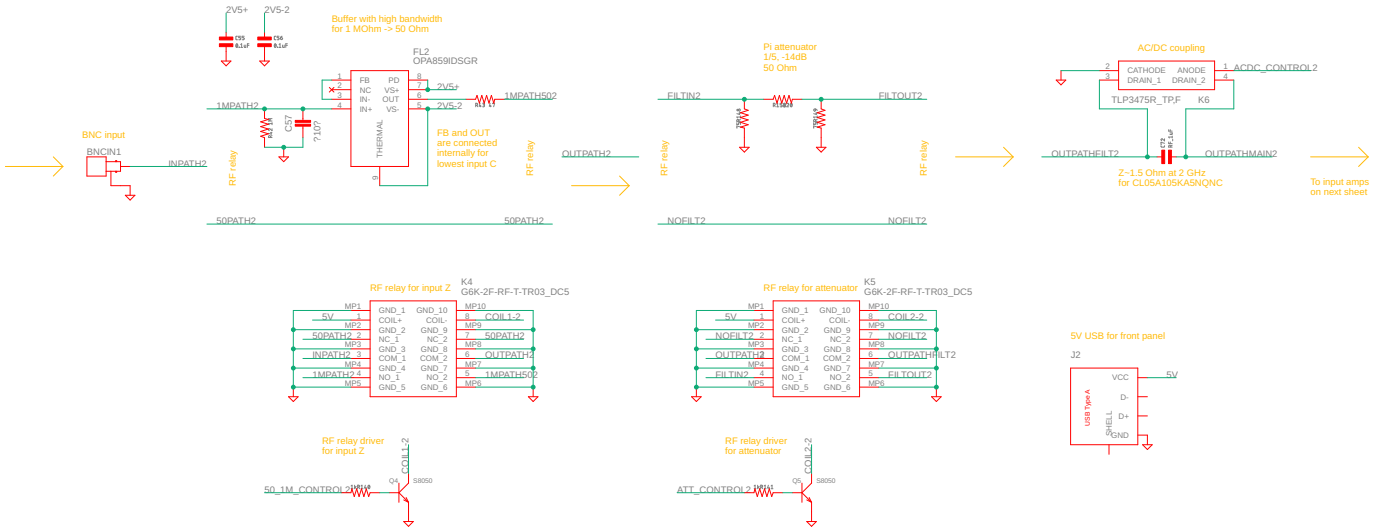
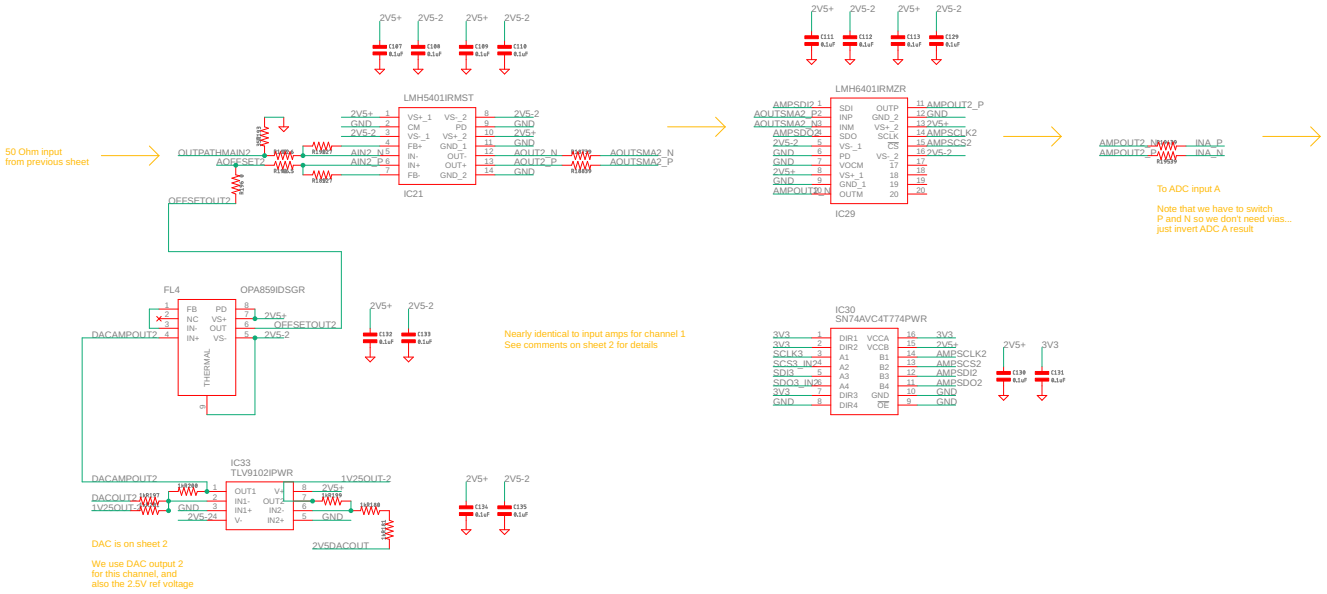
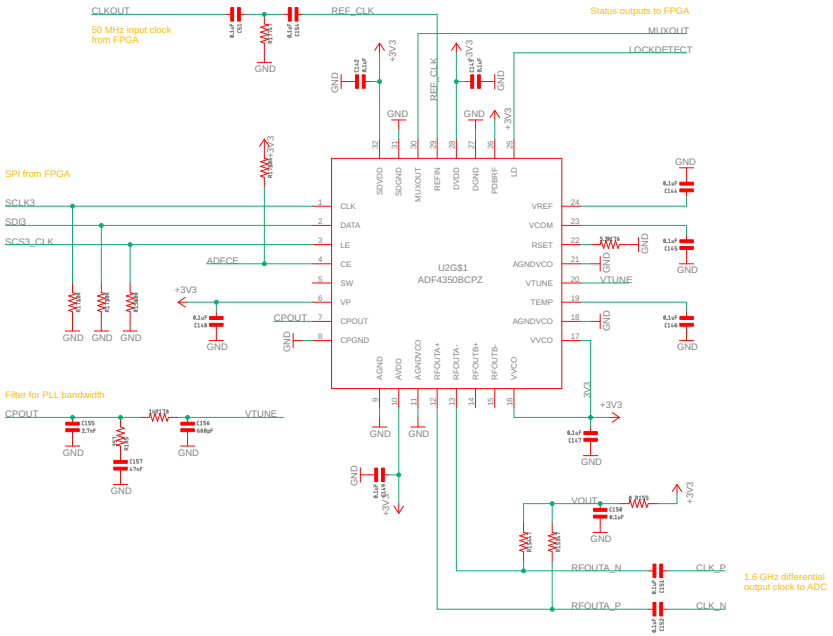
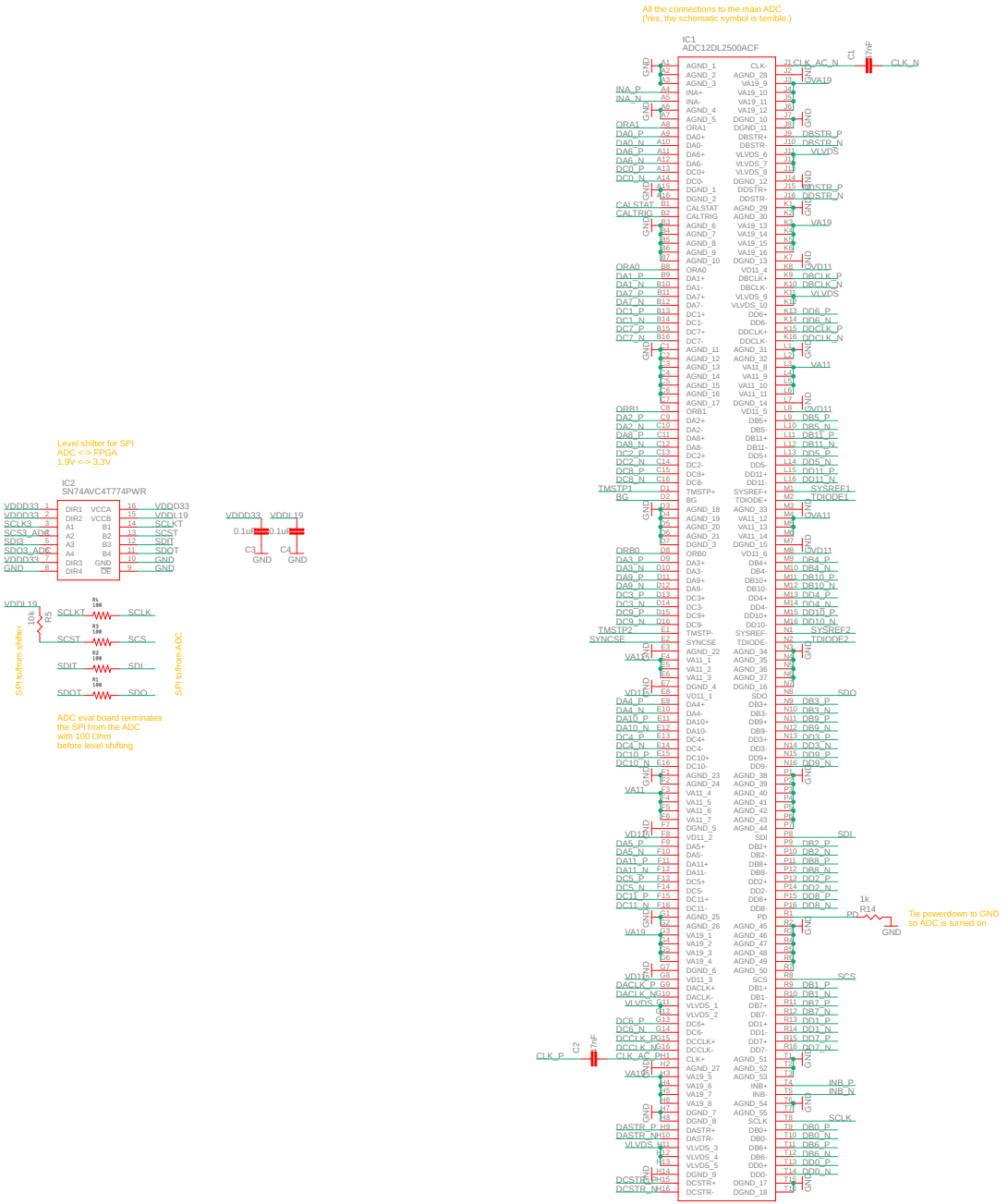

BNC input
BNCIN2
INPATH
RF relay
50 Ohm resistive splitter/combiner Output -6dB
SPLIT
OUTSPLIT
50 OUTSPLIT
SPLITOUT
NOSPLIT
OUTSPLITTER
2V5+
2V5-1
Buffer with high bandwidth for 1 MOhm -> 50 Ohm
FL3
OPA859IDSGR
1MPATH
1MPATH50
FB and OUT are connected internally for lowest input C
50PATH
OUTPATH
Pi attenuator 1/5, -14dB 50 Ohm
FILTIN
FILTOUT
NOFILT
AC/DC coupling
ACDC_CONTROL
TLP3475R_TP,F
K7
OUTPATHFILT
OUTPATHMAIN
Z~1.5 Ohm at 2 GHz for CL05A105KA5NQNC
To input amps on next sheet
RF relay for splitting
K1
G6K-2F-RF-T-TR03_DC5
RF relay for input Z
K2
G6K-2F-RF-T-TR03_DC5
RF relay for attenuator
K3
G6K-2F-RF-T-TR03_DC5
RF relay driver for splitting
SPLIT_CONTROL
RF relay driver for input Z
50_1M_CONTROL
RF relay driver for attenuator
ATT_CONTROL
S8050
5V USB for front panel
J15
USB Type A
VCC
D-
D+
GND
SHELL
5V


50 Ohm input
from previous sheet
OUTPATHMAIN
AOFFSET
OFFSETOUT
LMH5401IRMST
IC13
Single-ended to differential
amp with gain 4x
AOUTSMA_N
AOUTSMA_P
LMH6401IRMZR
IC14
Variable gain amp
gain 0.5x to 20x
AMPOUT_N
AMPOUT_P
INB_N
INB_P
To ADC input B
Buffered DAC output
for DC offset
Buffer with high bandwidth
FL1
OPA859IDSGR
DACAMPOUT1
FB and OUT
are connected
internally for
lowest input C
Buffered DAC output
-1.25 to 1.25V
SPI
IC15
SN74AVC4T774PWR
SPI to/from FPGA
Level shifter for SPI
Amp <-> FPGA
2.5V <-> 3.3V
IC18
TLV9102IPWR
1V25OUT-1
Subtract 2.5V/2 from DAC out
2V5DACOUT
2.5V ref voltage
from DAC, also
used on sheet 4
for channel 2
DAC output
0 to 2.5V
IC17
DAC8562SDGSR
DACOUT1
DACOUT2
DAC output 2
is used on sheet 4
for channel 2
SPI from FPGA


2V5+
2V5-2
C55 0.1uF
C56 0.1uF
Buffer with high bandwidth
for 1 MOhm -> 50 Ohm
FL2
OPA859IDSGR
FB
NC
IN-
IN+
PD
VS+
OUT
VS-
THERMAL
2V5+
2V5-2
1MPATH2
1MPATH502
C57
710?
FB and OUT
are connected
internally for
lowest input C
BNC input
BNCIN1
INPATH2
RF relay
RF relay
OUTPATH2
50PATH2
50PATH2
Pi attenuator
1/5, -14dB
50 Ohm
FILTIN2
FILTOUT2
RF relay
RF relay
NOFILT2
NOFILT2
AC/DC coupling
CATHODE
ANODE
DRAIN_1
DRAIN_2
ACDC_CONTROL2
TLP3475R_TP,F
K6
OUTPATHFILT2
OUTPATHMAIN2
Z~1.5 Ohm at 2 GHz
for CL05A105KA5NQNC
To input amps
on next sheet
RF relay for input Z
K4
G6K-2F-RF-T-TR03_DC5
5V
50PATH2_2
INPATH2_3
1MPATH2_4
COIL1-2
50PATH2
OUTPATH2
1MPATH502
RF relay for attenuator
K5
G6K-2F-RF-T-TR03_DC5
5V
NOFILT2_2
OUTPATH2
FILTIN2_4
COIL2-2
NOFILT2
OUTPATHFILT2
FILTOUT2
5V USB for front panel
J2
VCC
D-
D+
GND
SHELL
USB TypeA
5V
RF relay driver
for input Z
COIL1-2
50_1M_CONTROL2
Q4
S8050
RF relay driver
for attenuator
COIL2-2
ATT_CONTROL2
Q5
S8050

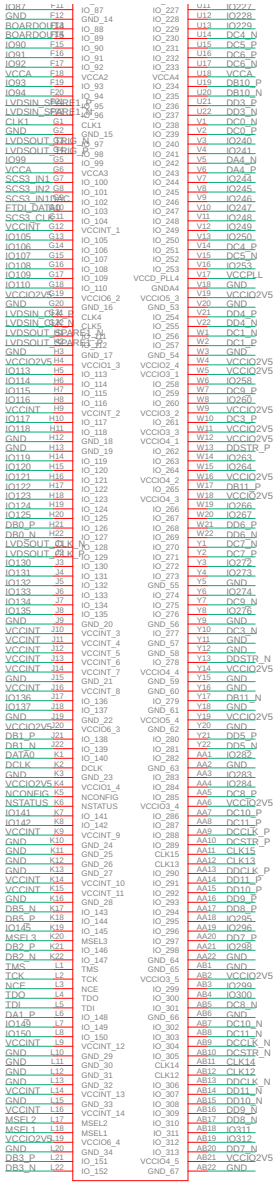

50 Ohm input
from previous sheet
OUTPATHMAIN2
AOFFSET2
OFFSETOUT2
LMH5401IRMST
IC21
AOUTSMA2_N
AOUTSMA2_P
LMH6401IRMZR
IC29
AMPOUT2_N
AMPOUT2_P
INA_P
INA_N
To ADC input A
Note that we have to switch
P and N so we don't need vias...
just invert ADC A result
FL4
OPA859IDSGR
DACAMPOUT2
Nearly identical to input amps for channel 1
See comments on sheet 2 for details
IC30
SN74AVC4T774PWR
IC33
TLV9102IPWR
1V25OUT-2
2V5DACOUT
DAC is on sheet 2
We use DAC output 2
for this channel, and
also the 2.5V ref voltage

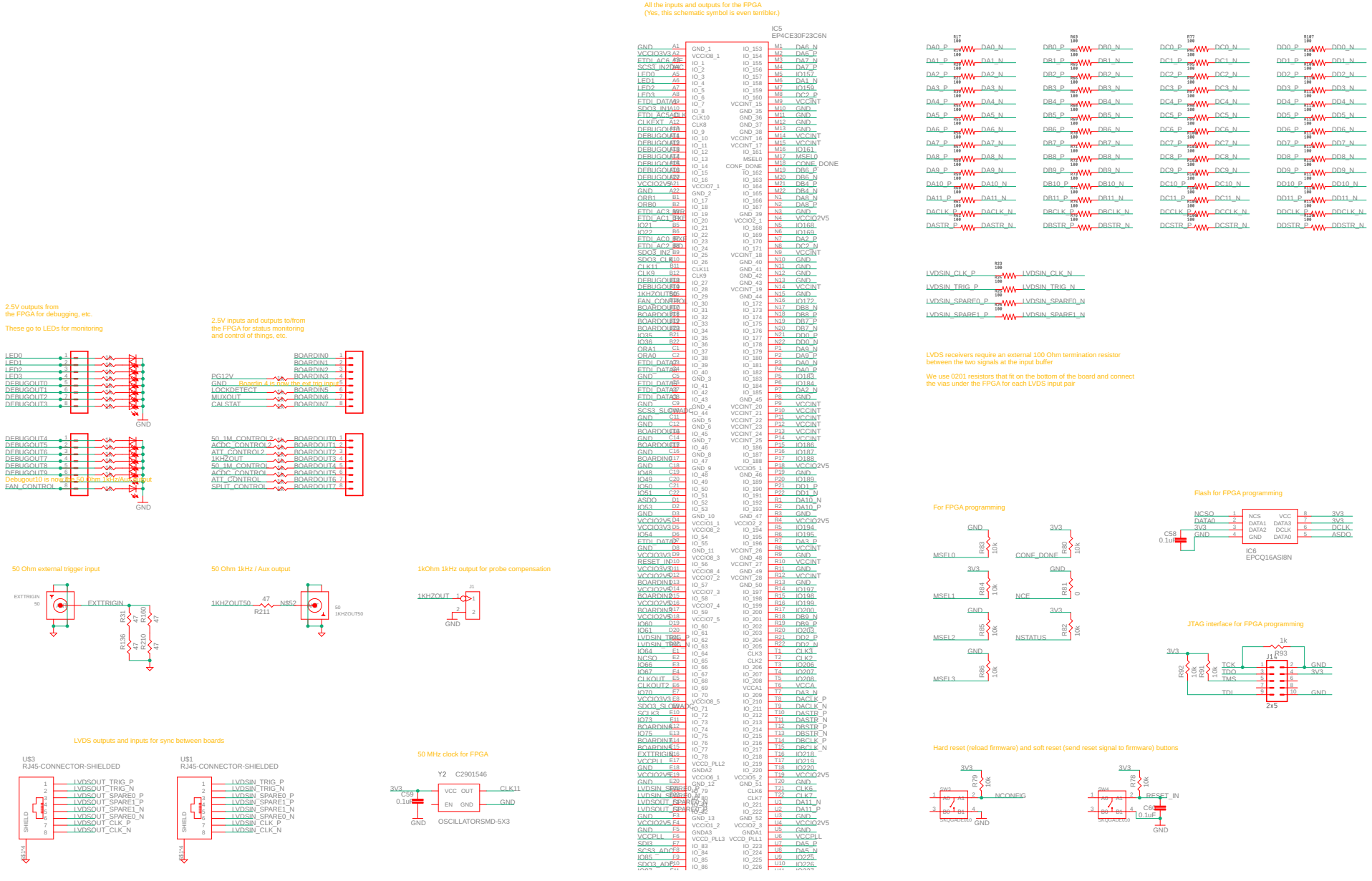

CLKOUT
50 MHz input clock from FPGA
REF_CLK
Status outputs to FPGA
MUXOUT
LOCKDETECT
SPI from FPGA
SCLK3
SDI3
SCS3_CLK
ADFCE
CPOUT
VTUNE
U2G$1
ADF4350BCPZ
CLK
DATA
LE
CE
SW
VP
CPOUT
CPGND
SDVDD
SDGND
MUXOUT
REFIN
DVDD
DGND
PDBRF
LD
VREF
VCOM
RSET
AGNDVCO
VTUNE
TEMP
AGNDVCO
VVCO
AGND
AVDD
AGNDVCO
RFOUTA+
RFOUTA-
RFOUTB+
RFOUTB-
VVCO
Filter for PLL bandwidth
REFOUTA_N
REFOUTA_P
CLK_P
CLK_N
1.6 GHz differential output clock to ADC
GND
+3V3

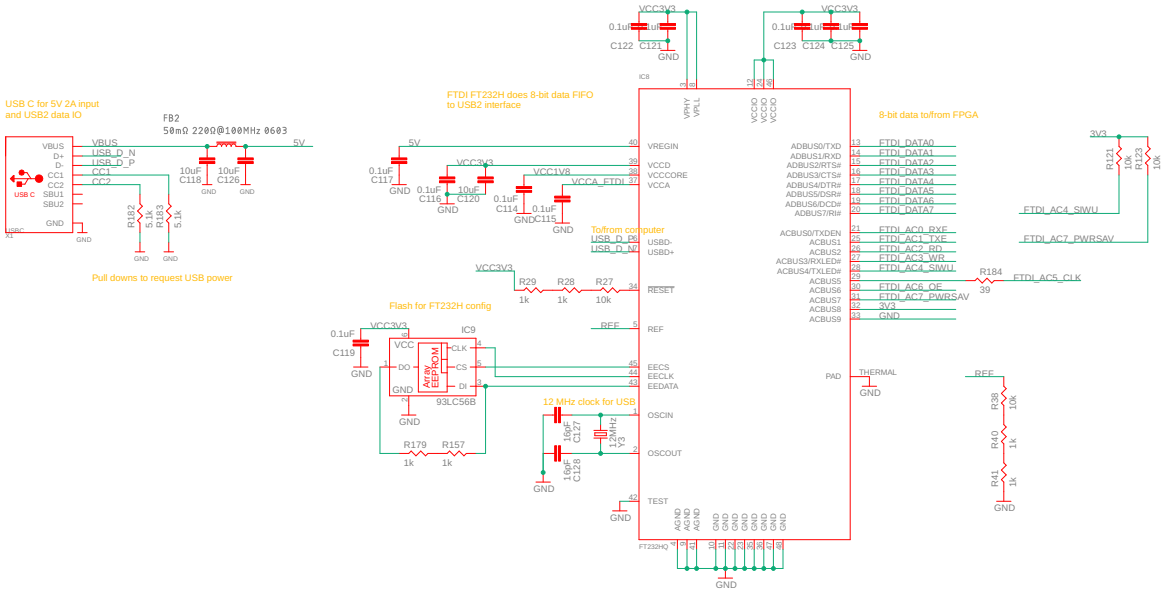

All the connections to the main ADC
(Yes, the schematic symbol is terrible.)
IC1
ADC12DL2500ACF
Level shifter for SPI
ADC <-> FPGA
1.9V <-> 3.3V
IC2
SN74AVC4T774PWR
SPI to/from shifter
SPI to/from ADC
ADC eval board terminates
the SPI from the ADC
with 100 Ohm
before level shifting
Tie powerdown to GND
so ADC is turned on

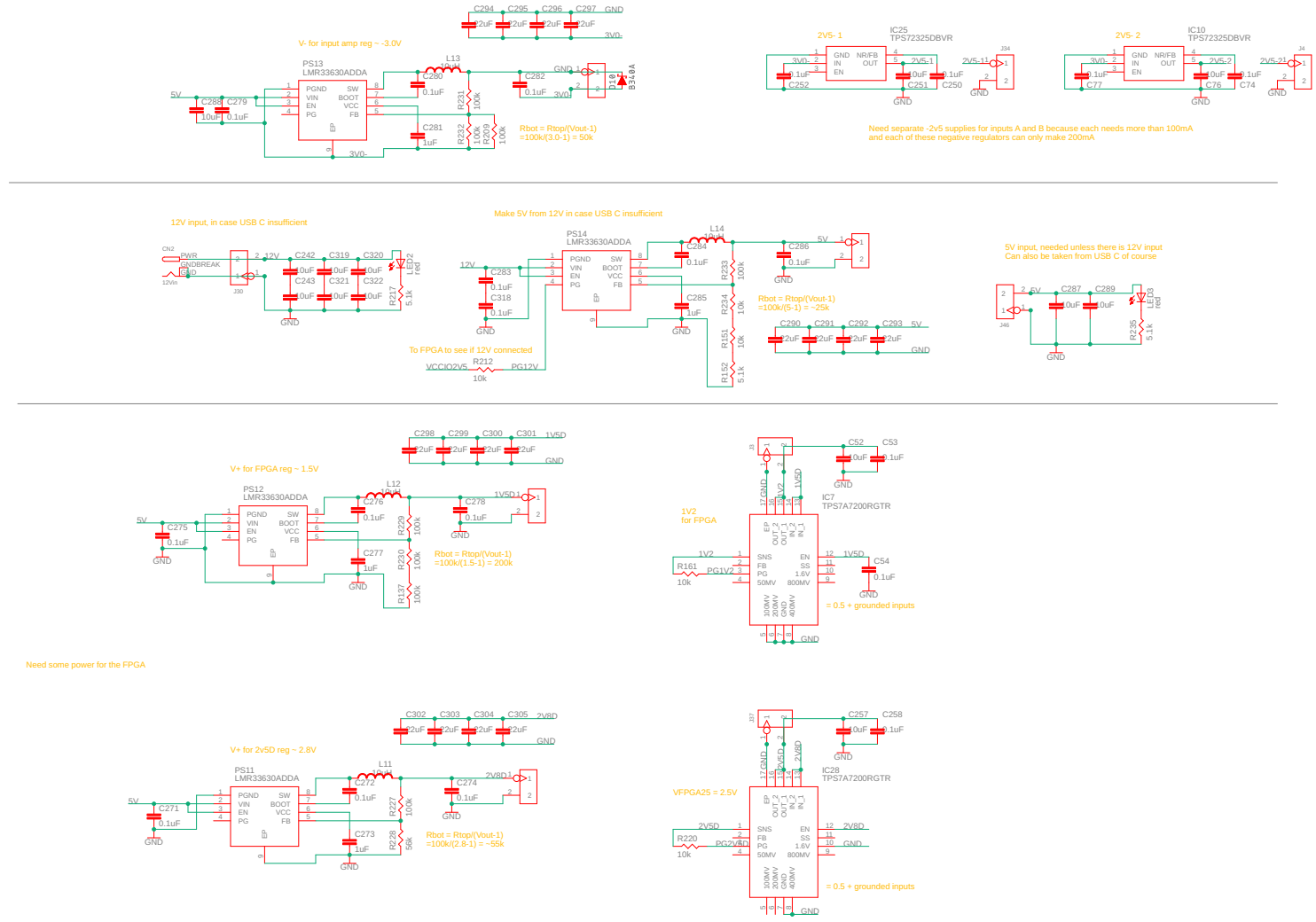
Cyclone IV E left and right I/O banks support
true LVDS transmitters, so use them for LVDS outputs

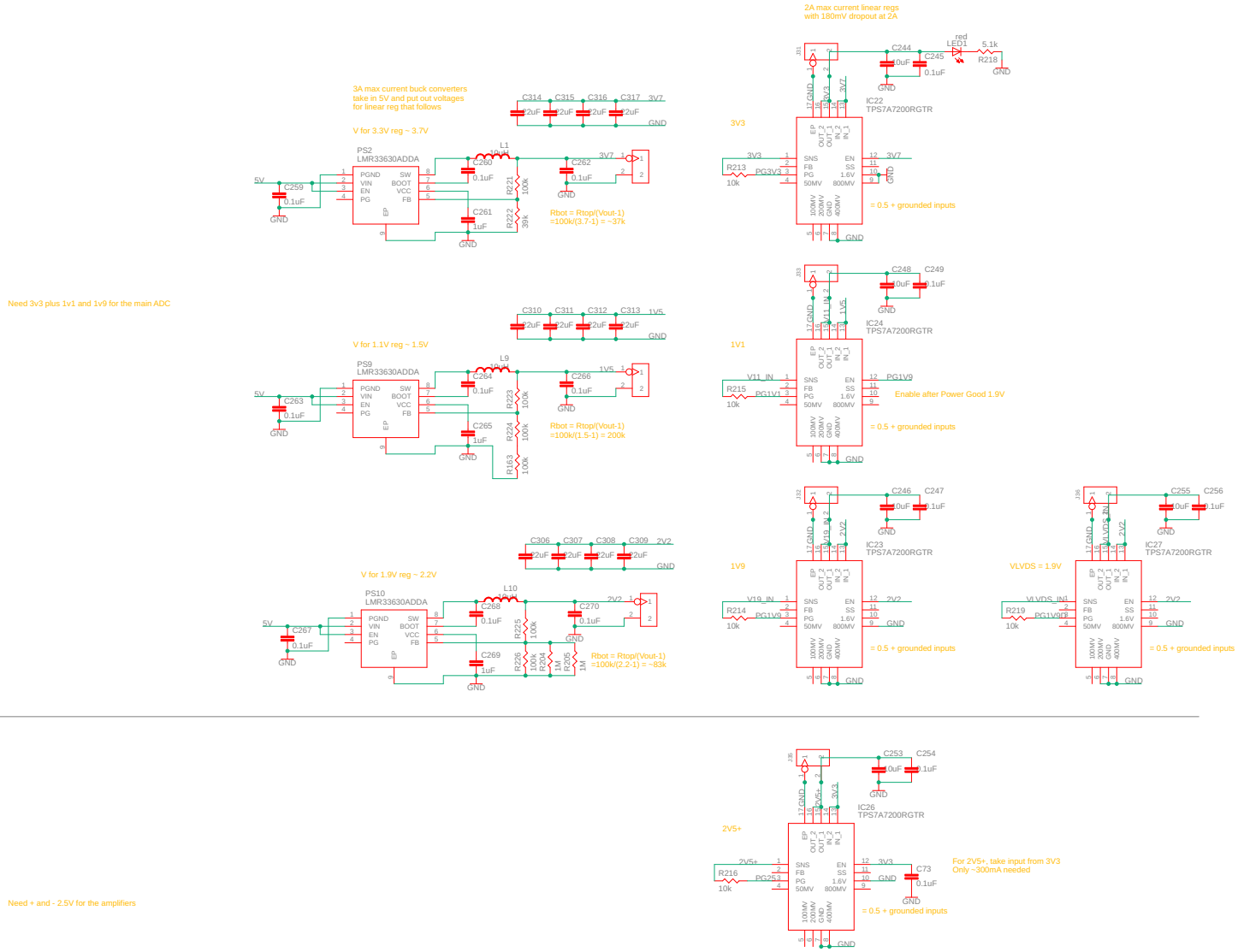
Extra clock input and output

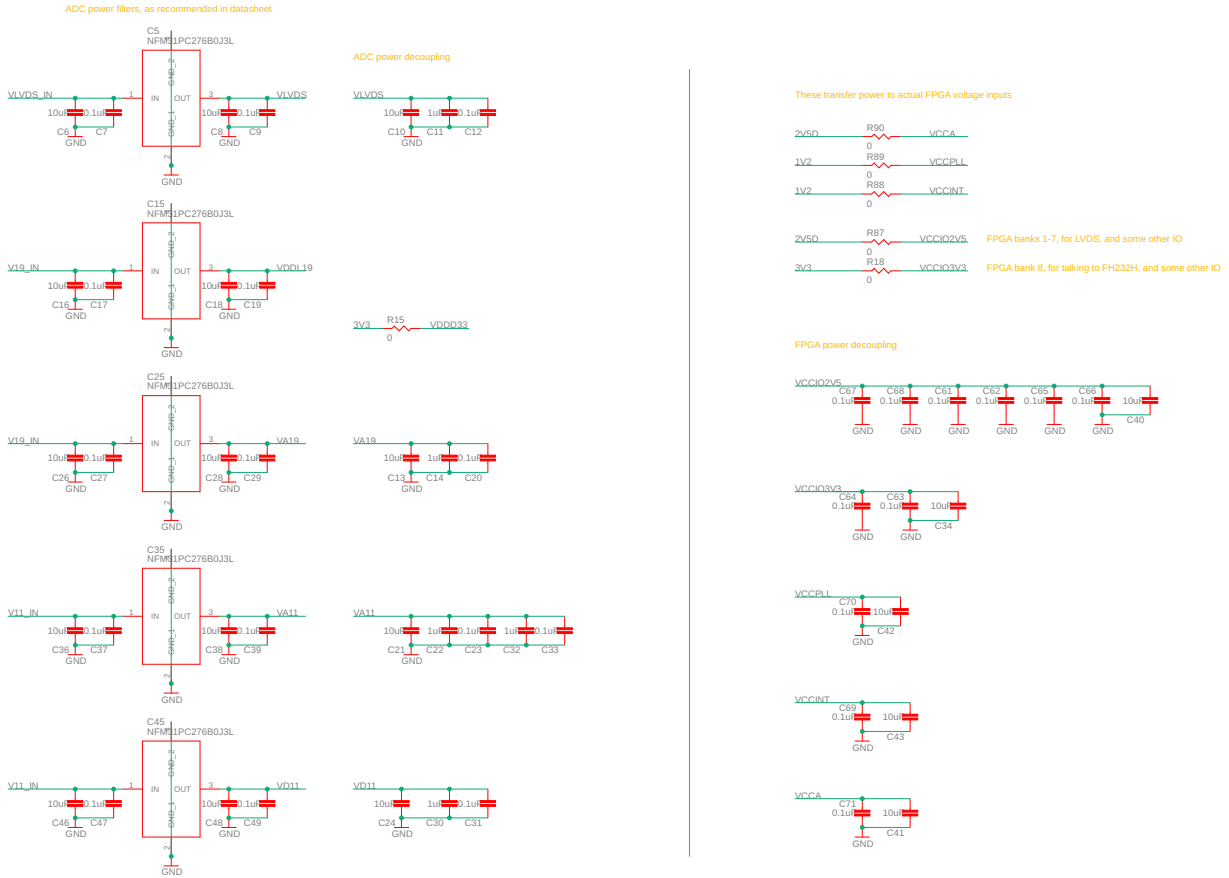



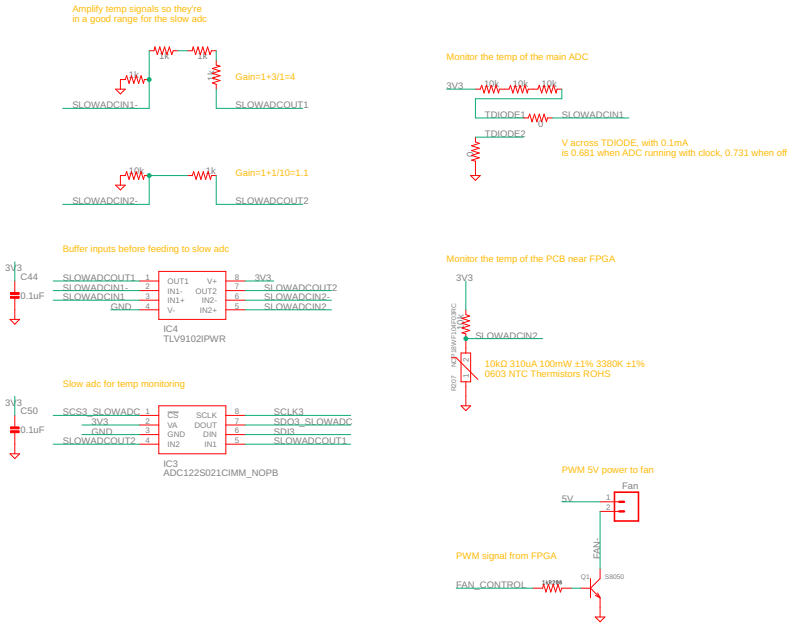

All the inputs and outputs for the FPGA
(Yes, this schematic symbol is even terribler.)
IC5
EP4CE30F23C6N
2.5V outputs from
the FPGA for debugging, etc.
These go to LEDs for monitoring
LED0
LED1
LED2
LED3
DEBUGOUT0
DEBUGOUT1
DEBUGOUT2
DEBUGOUT3
DEBUGOUT4
DEBUGOUT5
DEBUGOUT6
DEBUGOUT7
DEBUGOUT8
DEBUGOUT9
Debugout10 is now R4 50 Ohm 1kHz/Aux output
FAN_CONTROL
GND
2.5V inputs and outputs to/from
the FPGA for status monitoring
and control of things, etc.
BOARDIN0
BOARDIN1
BOARDIN2
BOARDIN3
+12V
GND Boardin 4 is now the ext trig input
LOCKDETECT
MUXOUT
CALSTAT
BOARDIN4
BOARDIN5
BOARDIN6
BOARDIN7
50_1M_CONTROL2
ACDC_CONTROL2
ATT_CONTROL2
1KHZOUT
50_1M_CONTROL
ACDC_CONTROL
ATT_CONTROL
SPLIT_CONTROL
BOARDOUT0
BOARDOUT1
BOARDOUT2
BOARDOUT3
BOARDOUT4
BOARDOUT5
BOARDOUT6
BOARDOUT7
LVDS receivers require an external 100 Ohm termination resistor
between the two signals at the input buffer
We use 0201 resistors that fit on the bottom of the board and connect
the vias under the FPGA for each LVDS input pair
LVDSIN_CLK_P
LVDSIN_CLK_N
LVDSIN_TRIG_P
LVDSIN_TRIG_N
LVDSIN_SPARE0_P
LVDSIN_SPARE0_N
LVDSIN_SPARE1_P
LVDSIN_SPARE1_N
For FPGA programming
MSEL0
MSEL1
MSEL2
MSEL3
CONF_DONE
NCE
NSTATUS
3V3
Flash for FPGA programming
NCSO
DATA0
DCLK
ASDO
IC6
EPCQ16ASI8N
JTAG interface for FPGA programming
TCK
TDO
TMS
TDI
2x5
50 Ohm external trigger input
EXTTRIGIN
50 Ohm 1kHz / Aux output
1KHZOUT50
1kOhm 1kHz output for probe compensation
1KHZOUT
LVDS outputs and inputs for sync between boards
U$3
RJ45-CONNECTOR-SHIELDED
LVDSOUT_TRIG_P
LVDSOUT_TRIG_N
LVDSOUT_SPARE0_P
LVDSOUT_SPARE1_P
LVDSOUT_SPARE1_N
LVDSOUT_SPARE0_N
LVDSOUT_CLK_P
LVDSOUT_CLK_N
U$1
RJ45-CONNECTOR-SHIELDED
LVDSIN_TRIG_P
LVDSIN_TRIG_N
LVDSIN_SPARE0_P
LVDSIN_SPARE1_P
LVDSIN_SPARE1_N
LVDSIN_SPARE0_N
LVDSIN_CLK_P
LVDSIN_CLK_N
50 MHz clock for FPGA
Y2 C2901546
OSCILLATORSMD-5X3
Hard reset (reload firmware) and soft reset (send reset signal to firmware) buttons
NCONFIG
RESET_IN


USB C for 5V 2A input
and USB2 data IO
FB2
50mΩ 220Ω@100MHz 0603
5V
Pull downs to request USB power
FTDI FT232H does 8-bit data FIFO
to USB2 interface
8-bit data to/from FPGA
To/from computer
Flash for FT232H config
12 MHz clock for USB
FTDI_DATA0
FTDI_DATA1
FTDI_DATA2
FTDI_DATA3
FTDI_DATA4
FTDI_DATA5
FTDI_DATA6
FTDI_DATA7
FTDI_AC0_RXF
FTDI_AC1_TXE
FTDI_AC2_RD
FTDI_AC3_WR
FTDI_AC4_SIWU
FTDI_AC5_CLK
FTDI_AC6_OE
FTDI_AC7_PWRSAV
93LC56B
FT232HQ
GND
3V3
VCC3V3
VCC1V8


V- for input amp reg ~ -3.0V
PS13
LMR33630ADDA
L13
Rbot = Rtop/(Vout-1)
=100k/(3.0-1) = 50k
2V5- 1
IC25
TPS72325DBVR
2V5- 2
IC10
TPS72325DBVR
Need separate -2v5 supplies for inputs A and B because each needs more than 100mA
and each of these negative regulators can only make 200mA
12V input, in case USB C insufficient
Make 5V from 12V in case USB C insufficient
PS14
LMR33630ADDA
L14
Rbot = Rtop/(Vout-1)
=100k/(5-1) = ~25k
To FPGA to see if 12V connected
5V input, needed unless there is 12V input
Can also be taken from USB C of course
V+ for FPGA reg ~ 1.5V
PS12
LMR33630ADDA
L12
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
1V2
for FPGA
IC7
TPS7A7200RGTR
= 0.5 + grounded inputs
Need some power for the FPGA
V+ for 2v5D reg ~ 2.8V
PS11
LMR33630ADDA
L11
Rbot = Rtop/(Vout-1)
=100k/(2.8-1) = ~55k
VFPGA25 = 2.5V
IC28
TPS7A7200RGTR
= 0.5 + grounded inputs


3A max current buck converters take in 5V and put out voltages for linear reg that follows
V for 3.3V reg ~ 3.7V
PS2
LMR33630ADDA
L1
1uH
C314 C315 C316 C317 3V7
2uF 2uF 2uF 2uF
GND
5V
C259 0.1uF
C260 0.1uF
C261 1uF
C262 0.1uF
R221 100k
R222 39k
Rbot = Rtop/(Vout-1)
=100k/(3.7-1) = ~37k
2A max current linear regs with 180mV dropout at 2A
IC22
TPS7A7200RGTR
3V3
C244 10uF
C245 0.1uF
red
LED1
5.1k
R218
R213 10k
PG3V3
= 0.5 + grounded inputs
Need 3v3 plus 1v1 and 1v9 for the main ADC
V for 1.1V reg ~ 1.5V
PS9
LMR33630ADDA
L9
1uH
C310 C311 C312 C313 1V5
C263 0.1uF
C264 0.1uF
C265 1uF
C266 0.1uF
R223 100k
R224 100k
R163 100k
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
IC24
TPS7A7200RGTR
1V1
C248 10uF
C249 0.1uF
V11_IN
R215 10k
PG1V1
Enable after Power Good 1.9V
V for 1.9V reg ~ 2.2V
PS10
LMR33630ADDA
L10
1uH
C306 C307 C308 C309 2V2
C267 0.1uF
C268 0.1uF
C269 1uF
C270 0.1uF
R225 100k
R226 100k
R204 1M
R205 1M
Rbot = Rtop/(Vout-1)
=100k/(2.2-1) = ~83k
IC23
TPS7A7200RGTR
1V9
C246 10uF
C247 0.1uF
V19_IN
R214 10k
PG1V9
IC27
TPS7A7200RGTR
VLVDS = 1.9V
C255 10uF
C256 0.1uF
VLVDS_IN
R219 10k
PG1V9
Need + and - 2.5V for the amplifiers
IC26
TPS7A7200RGTR
2V5+
C253 10uF
C254 0.1uF
R216 10k
PG2V5
C73 0.1uF
For 2V5+, take input from 3V3
Only ~300mA needed


ADC power filters, as recommended in datasheet
C5
NFM31PC276B0J3L
VLVDS_IN
VLVDS
C6
C7
C8
C9
GND
ADC power decoupling
VLVDS
C10
C11
C12
C15
NFM31PC276B0J3L
V19_IN
VDDL19
C16
C17
C18
C19
3V3
R15
0
VDDD33
C25
NFM31PC276B0J3L
V19_IN
VA19
C26
C27
C28
C29
VA19
C13
C14
C20
C35
NFM31PC276B0J3L
V11_IN
VA11
C36
C37
C38
C39
VA11
C21
C22
C23
C32
C33
C45
NFM31PC276B0J3L
V11_IN
VD11
C46
C47
C48
C49
VD11
C24
C30
C31
These transfer power to actual FPGA voltage inputs
2V5D
R90
0
VCCA
1V2
R89
0
VCCPLL
1V2
R88
0
VCCINT
2V5D
R87
0
VCCIO2V5
FPGA banks 1-7, for LVDS, and some other IO
3V3
R18
0
VCCIO3V3
FPGA bank 8, for talking to FH232H, and some other IO
FPGA power decoupling
VCCIO2V5
C67
C68
C61
C62
C65
C66
C40
VCCIO3V3
C64
C63
C34
VCCPLL
C70
C42
VCCINT
C69
C43
VCCA
C71
C41


Amplify temp signals so they're in a good range for the slow adc
1k
1k
1k
Gain=1+3/1=4
SLOWADCIN1-
SLOWADCOUT1
10k
1k
Gain=1+1/10=1.1
SLOWADCIN2-
SLOWADCOUT2
Buffer inputs before feeding to slow adc
3V3
C44
0.1uF
SLOWADCOUT1
SLOWADCIN1-
SLOWADCIN1
GND
OUT1
IN1-
IN1+
V-
V+
OUT2
IN2-
IN2+
3V3
SLOWADCOUT2
SLOWADCIN2-
SLOWADCIN2
IC4
TLV9102IPWR
Slow adc for temp monitoring
3V3
C50
0.1uF
SCS3_SLOWADC
3V3
GND
SLOWADCOUT2
CS
VA
GND
IN2
SCLK
DOUT
DIN
IN1
SCLK3
SDO3_SLOWADC
SDI3
SLOWADCOUT1
IC3
ADC122S021CIMM_NOPB
Monitor the temp of the main ADC
3V3
10k
10k
10k
TDIODE1
SLOWADCIN1
TDIODE2
V across TDIODE, with 0.1mA
is 0.681 when ADC running with clock, 0.731 when off
Monitor the temp of the PCB near FPGA
3V3
SLOWADCIN2
10kΩ 310uA 100mW ±1% 3380K ±1%
0603 NTC Thermistors ROHS
PWM 5V power to fan
Fan
5V
FAN
PWM signal from FPGA
FAN_CONTROL
10k
Q1
S8050