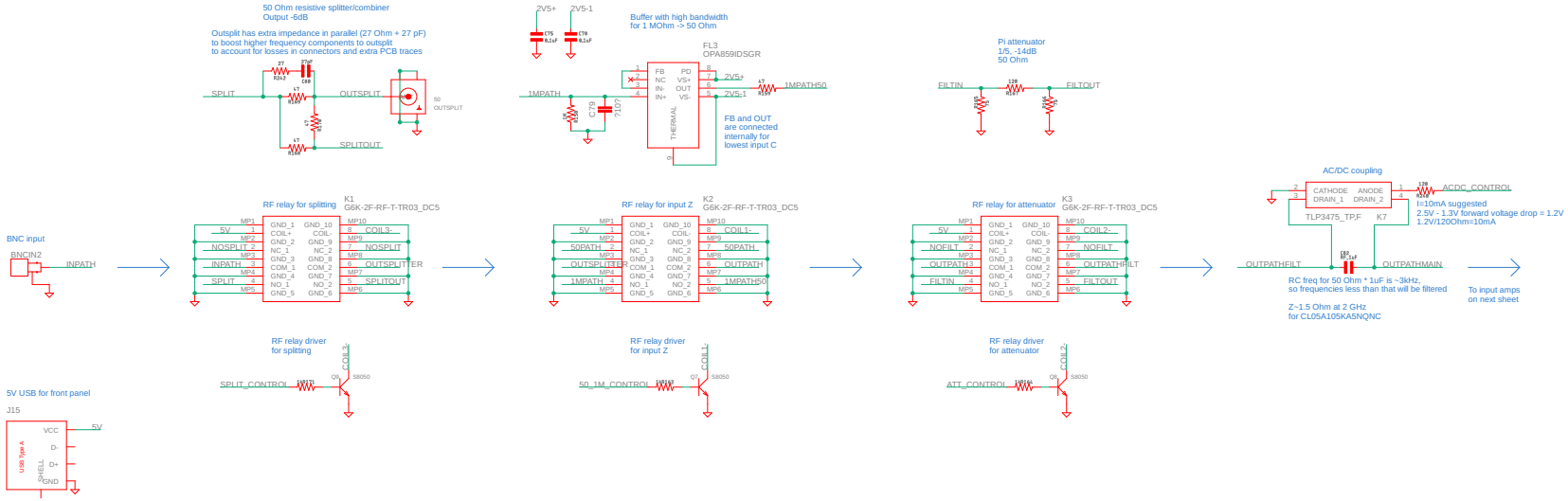
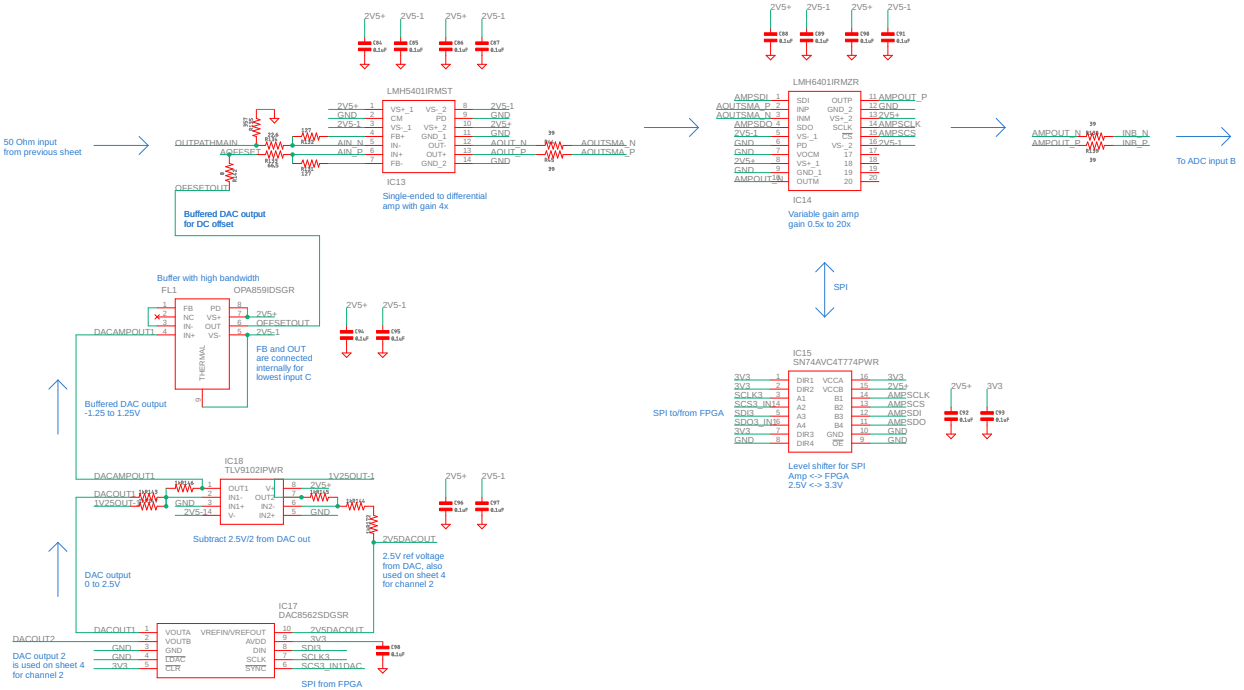
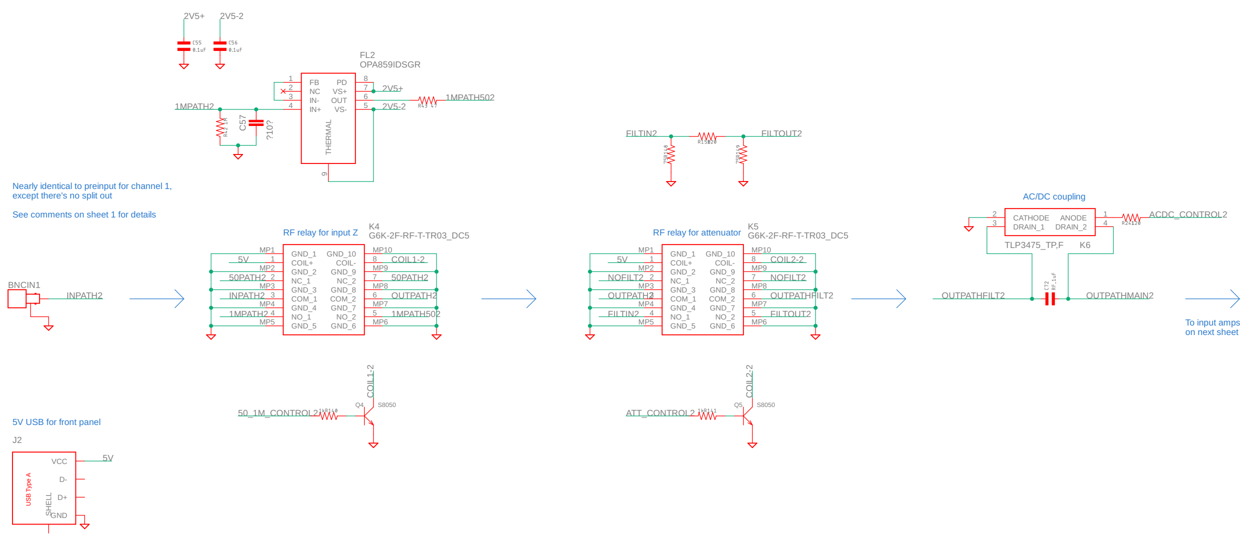
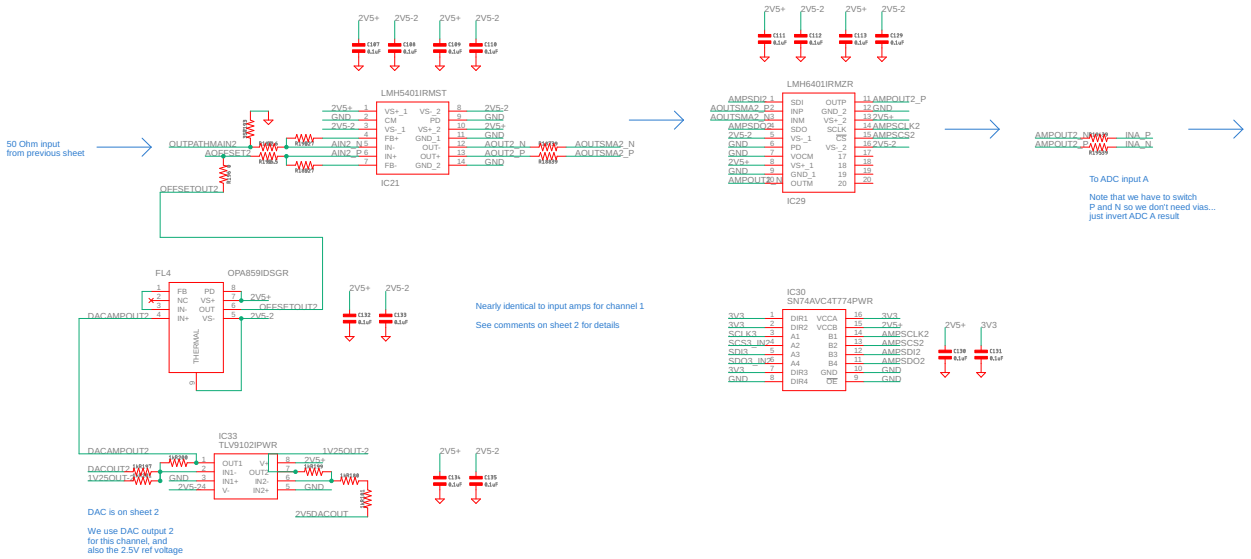

50 Ohm resistive splitter/combiner
Output -6dB
Outsplit has extra impedance in parallel (27 Ohm + 27 pF)
to boost higher frequency components to outsplit
to account for losses in connectors and extra PCB traces
SPLIT
OUTSPLIT
SPLITOUT
50
OUTSPLIT
2V5+
2V5-1
Buffer with high bandwidth
for 1 MOhm -> 50 Ohm
FL3
OPA859IDSGR
1MPATH
1MPATH50
2V5-1
FB and OUT
are connected
internally for
lowest input C
Pi attenuator
1/5, -14dB
50 Ohm
FILTIN
FILTOUT
AC/DC coupling
ACDC_CONTROL
I=10mA suggested
2.5V - 1.3V forward voltage drop = 1.2V
1.2V/120Ohm=10mA
TLP3475_TP,F
K7
OUTPATHFILT
OUTPATHMAIN
RC freq for 50 Ohm * 1uF is ~3kHz,
so frequencies less than that will be filtered
Z~1.5 Ohm at 2 GHz
for CL05A105KA5NQNC
To input amps
on next sheet
BNC input
BNCIN2
INPATH
RF relay for splitting
K1
G6K-2F-RF-T-TR03_DC5
5V
NOSPLIT
INPATH
SPLIT
COIL3-
NOSPLIT
OUTSPLITTER
SPLITOUT
RF relay for input Z
K2
G6K-2F-RF-T-TR03_DC5
5V
50PATH
OUTSPLITTER
1MPATH
COIL1-
50PATH
OUTPATH
1MPATH50
RF relay for attenuator
K3
G6K-2F-RF-T-TR03_DC5
5V
NOFILT
OUTPATH
FILTIN
COIL2-
NOFILT
OUTPATHFILT
FILTOUT
RF relay driver
for splitting
SPLIT_CONTROL
COIL3-
RF relay driver
for input Z
50_1M_CONTROL
COIL1-
RF relay driver
for attenuator
ATT_CONTROL
COIL2-
5V USB for front panel
J15
USB Type A
VCC
D-
D+
GND
SHELL
5V

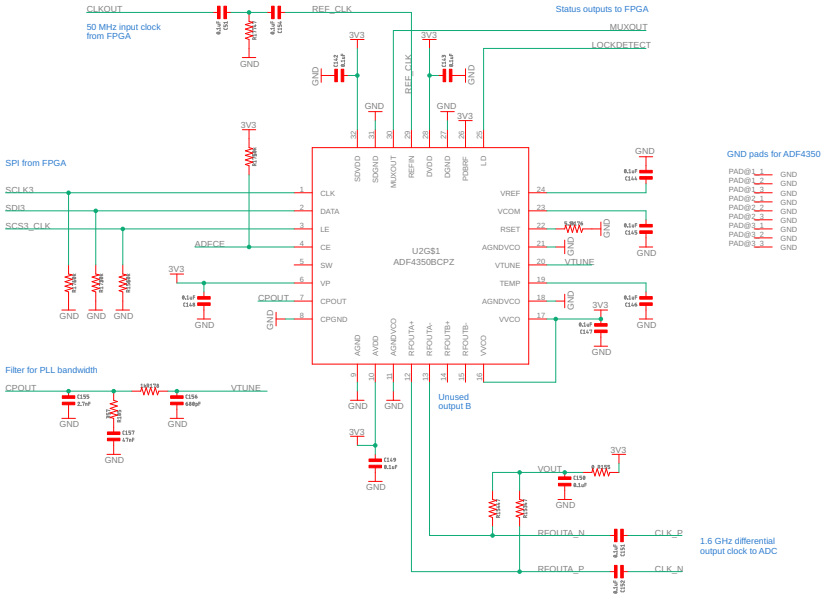

50 Ohm input
from previous sheet
OUTPATHMAIN
AOFFSET
OFFSETOUT
LMH5401IRMST
IC13
Single-ended to differential
amp with gain 4x
AOUTSMA_N
AOUTSMA_P
Buffered DAC output
for DC offset
LMH6401IRMZR
IC14
Variable gain amp
gain 0.5x to 20x
AMPOUT_N
AMPOUT_P
INB_N
INB_P
To ADC input B
SPI
Buffer with high bandwidth
FL1
OPA859IDSGR
DACAMPOUT1
FB and OUT
are connected
internally for
lowest input C
Buffered DAC output
-1.25 to 1.25V
IC15
SN74AVC4T774PWR
SPI to/from FPGA
Level shifter for SPI
Amp <-> FPGA
2.5V <-> 3.3V
IC18
TLV9102IPWR
1V25OUT-1
Subtract 2.5V/2 from DAC out
2V5DACOUT
2.5V ref voltage
from DAC, also
used on sheet 4
for channel 2
DAC output
0 to 2.5V
IC17
DAC8562SDGSR
DACOUT2
DAC output 2
is used on sheet 4
for channel 2
SPI from FPGA

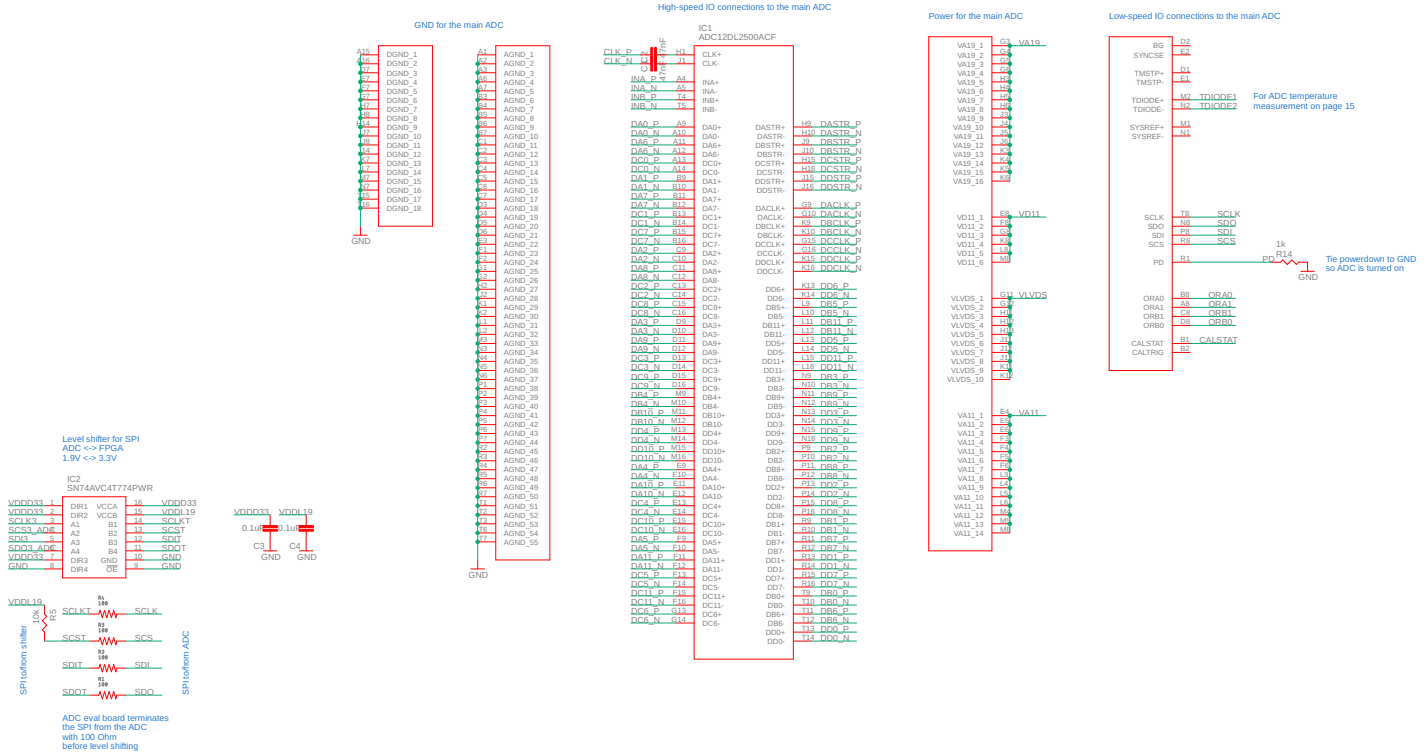


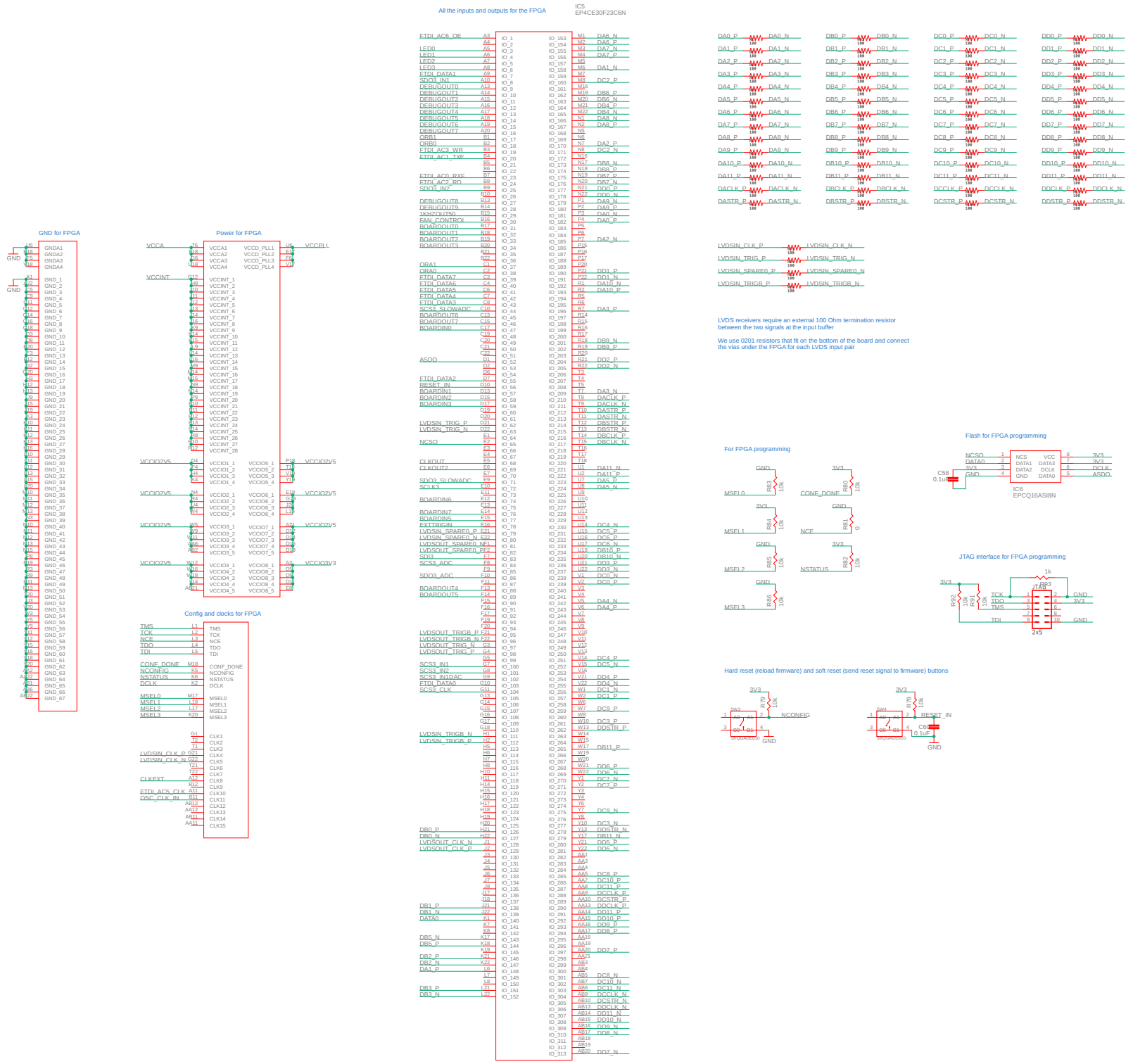
2V5+
2V5-2
FL2
OPA859IDSGR
FB
NC
IN-
IN+
PD
VS+
OUT
VS-
THERMAL
1MPATH2
1MPATH502
C57
FILTIN2
FILTOUT2
Nearly identical to preinput for channel 1,
except there's no split out
See comments on sheet 1 for details
RF relay for input Z
K4
G6K-2F-RF-T-TR03_DC5
RF relay for attenuator
K5
G6K-2F-RF-T-TR03_DC5
AC/DC coupling
CATHODE
ANODE
DRAIN_1
DRAIN_2
TLP3475_TP,F
K6
ACDC_CONTROL2
BNCIN1
INPATH2
5V
50PATH2_2
INPATH2_3
1MPATH2_4
COIL1-2
50PATH2
OUTPATH2
NOFILT2_2
OUTPATH2
FILTIN2
COIL2-2
NOFILT2
OUTPATHFILT2
FILTOUT2
OUTPATHMAIN2
To input amps
on next sheet
50_1M_CONTROL2
Q4
S8050
ATT_CONTROL2
Q5
S8050
5V USB for front panel
J2
USB Type A
VCC
D-
D+
GND
SHELL

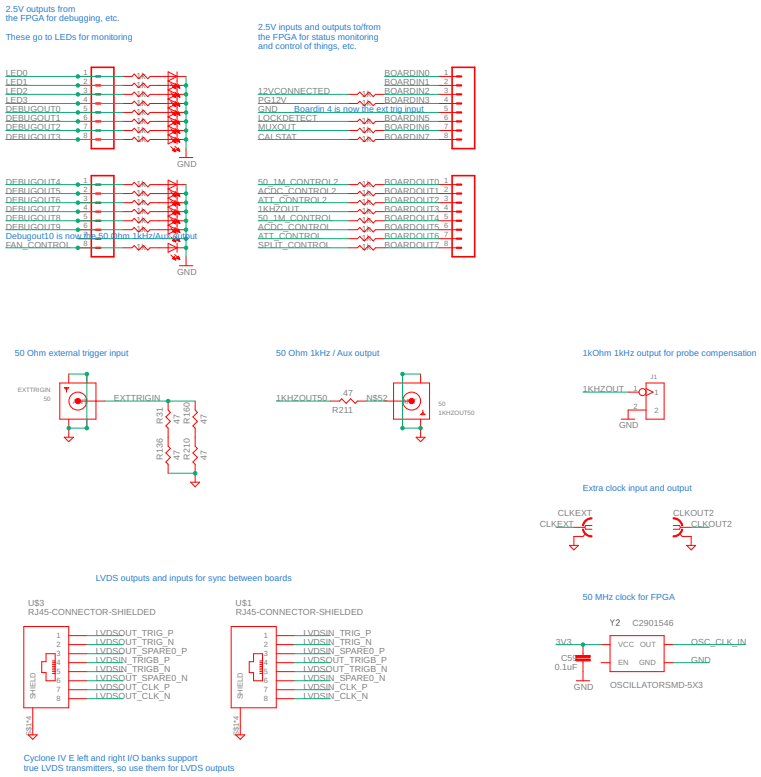
12/12/2024 7:56 PM f=0.47 C:\gitwork\master\HaasoscopePro\adc board\haasoscope_pro_adc_fpga_board.sch (Sheet: 3/15)

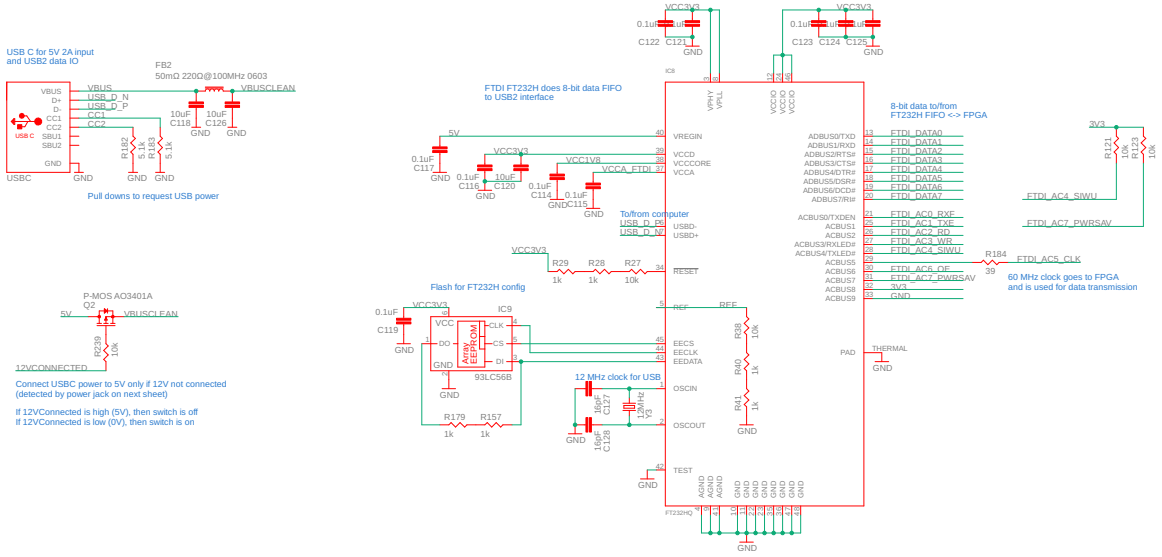

50 Ohm input
from previous sheet
OUTPATHMAIN2
ADCSET2
OFFSETOUT2
LMH5401IRMST
IC21
AIN2_N
AIN2_P
AOUTSMA2_N
AOUTSMA2_P
AOUT2_N
AOUT2_P
LMH6401IRMZR
IC29
AMPSDI2
AMPSDO2
AMPSCLK2
AMPSCS2
AMPOUT2_N
AMPOUT2_P
INA_P
INA_N
To ADC input A
Note that we have to switch
P and N so we don't need vias...
just invert ADC A result
FL4
OPA859IDSGR
DACAMPOUT2
Nearly identical to input amps for channel 1
See comments on sheet 2 for details
IC30
SN74AVC4T774PWR
IC33
TLV9102IPWR
DACOUT2
1V25OUT-2
1V25OUT-2
2V5DACOUT
DAC is on sheet 2
We use DAC output 2
for this channel, and
also the 2.5V ref voltage

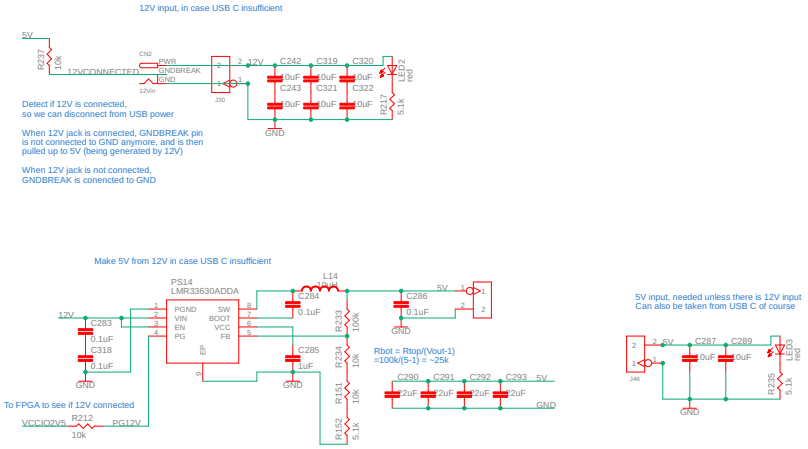

CLKOUT
50 MHz input clock from FPGA
REF_CLK
Status outputs to FPGA
MUXOUT
LOCKDETECT
SPI from FPGA
SCLK3
SDI3
SCS3_CLK
ADFCE
CPOUT
U2G$1
ADF4350BCPZ
CLK
DATA
LE
CE
SW
VP
CPGND
VREF
VCOM
RSET
AGNDVCO
VTUNE
TEMP
VVCO
GND pads for ADF4350
Filter for PLL bandwidth
Unused output B
VOUT
REOUTA_N
REOUTA_P
CLK_P
CLK_N
1.6 GHz differential output clock to ADC
3V3
GND

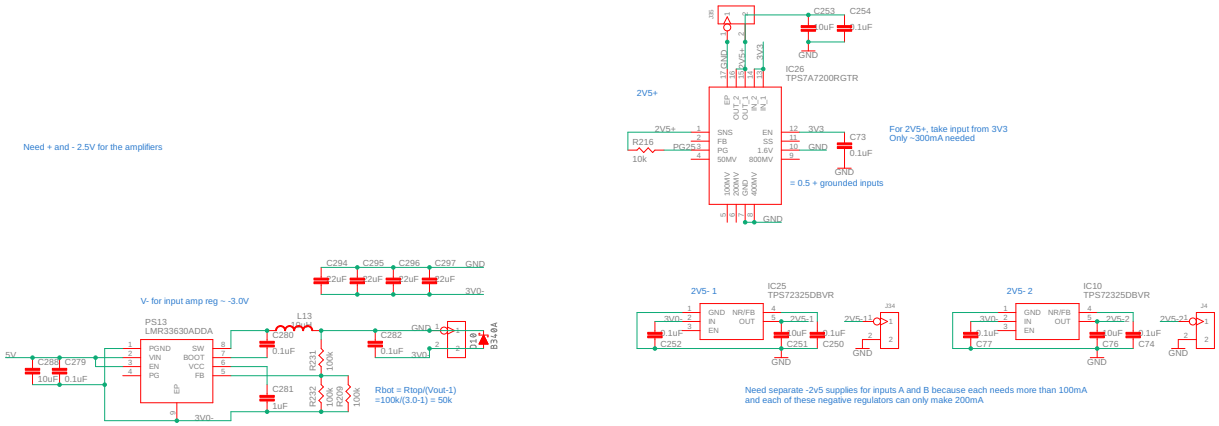

GND for the main ADC
High-speed IO connections to the main ADC
IC1
ADC12DL2500ACF
Power for the main ADC
Low-speed IO connections to the main ADC
For ADC temperature measurement on page 15
Tie powerdown to GND so ADC is turned on
Level shifter for SPI
ADC <-> FPGA
1.9V <-> 3.3V
IC2
SN74AVC4T774PWR
SPI to/from shifter
SPI to/from ADC
ADC eval board terminates the SPI from the ADC with 100 Ohm before level shifting

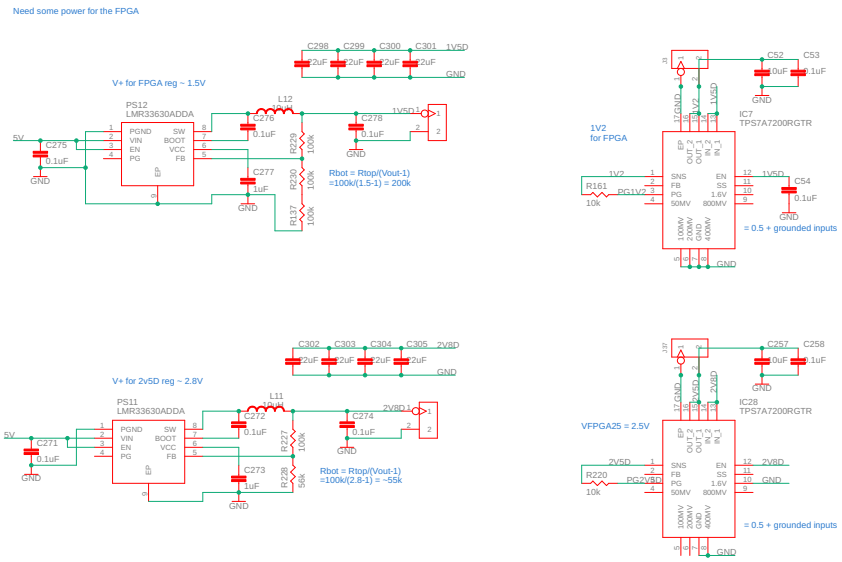

All the inputs and outputs for the FPGA
IC5
EP4CE30F23C6N
GND for FPGA
Power for FPGA
Config and clocks for FPGA
LVDS receivers require an external 100 Ohm termination resistor between the two signals at the input buffer
We use 0201 resistors that fit on the bottom of the board and connect the vias under the FPGA for each LVDS input pair
For FPGA programming
Flash for FPGA programming
IC6
EPCQ16ASI8N
JTAG interface for FPGA programming
Hard reset (reload firmware) and soft reset (send reset signal to firmware) buttons
NCONFIG
RESET_IN

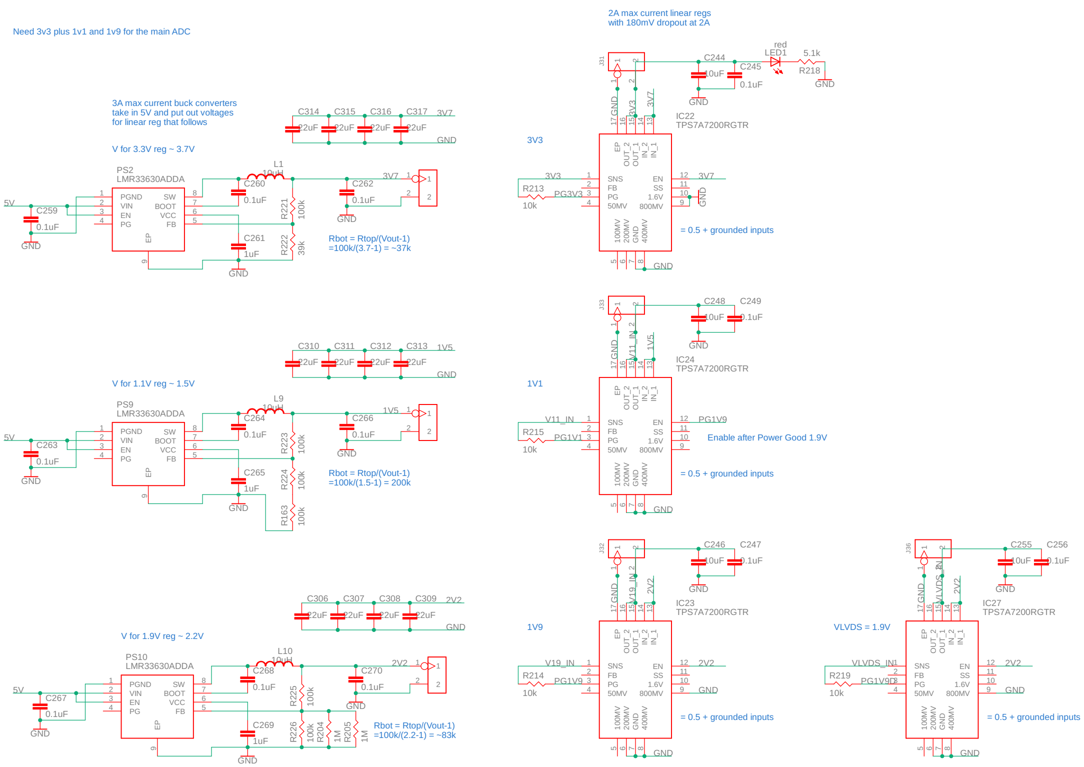

2.5V outputs from
the FPGA for debugging, etc.
These go to LEDs for monitoring
LED0
LED1
LED2
LED3
DEBUGOUT0
DEBUGOUT1
DEBUGOUT2
DEBUGOUT3
GND
DEBUGOUT4
DEBUGOUT5
DEBUGOUT6
DEBUGOUT7
DEBUGOUT8
DEBUGOUT9
Debugout10 is now the 50 Ohm 1kHz/Aux output
FAN_CONTROL
GND
2.5V inputs and outputs to/from
the FPGA for status monitoring
and control of things, etc.
12VCONNECTED
PG12V
GND Boardin 4 is now the ext trig input
LOCKDETECT
MUXOUT
CAL STAT
BOARDIN0
BOARDIN1
BOARDIN2
BOARDIN3
BOARDIN5
BOARDIN6
BOARDIN7
50_1M_CONTROL2
ACDC_CONTROL2
ATT_CONTROL2
1KHZOUT
50_1M_CONTROL
ACDC_CONTROL
ATT_CONTROL
SPLIT_CONTROL
BOARDOUT0
BOARDOUT1
BOARDOUT2
BOARDOUT3
BOARDOUT4
BOARDOUT5
BOARDOUT6
BOARDOUT7
50 Ohm external trigger input
EXTTRIGIN
50
EXTTRIGIN
R31
47
R160
47
R136
47
R210
47
50 Ohm 1kHz / Aux output
1KHZOUT50
47
R211
NS52
50
1KHZOUT50
1kOhm 1kHz output for probe compensation
1KHZOUT
J1
GND
Extra clock input and output
CLKEXT
CLKEXT
CLKOUT2
CLKOUT2
LVDS outputs and inputs for sync between boards
U$3
RJ45-CONNECTOR-SHIELDED
LVDSOUT_TRIG_P
LVDSOUT_TRIG_N
LVDSOUT_SPARE0_P
LVDSIN_TRIGB_P
LVDSIN_TRIGB_N
LVDSOUT_SPARE0_N
LVDSOUT_CLK_P
LVDSOUT_CLK_N
SHIELD
GND
U$1
RJ45-CONNECTOR-SHIELDED
LVDSIN_TRIG_P
LVDSIN_TRIG_N
LVDSIN_SPARE0_P
LVDSOUT_TRIGB_P
LVDSOUT_TRIGB_N
LVDSIN_SPARE0_N
LVDSIN_CLK_P
LVDSIN_CLK_N
SHIELD
GND
Cyclone IV E left and right I/O banks support
true LVDS transmitters, so use them for LVDS outputs
50 MHz clock for FPGA
Y2
C2901546
3V3
C58
0.1uF
GND
VCC
OUT
EN
GND
OSC_CLK_IN
GND
OSCILLATORSMD-5X3

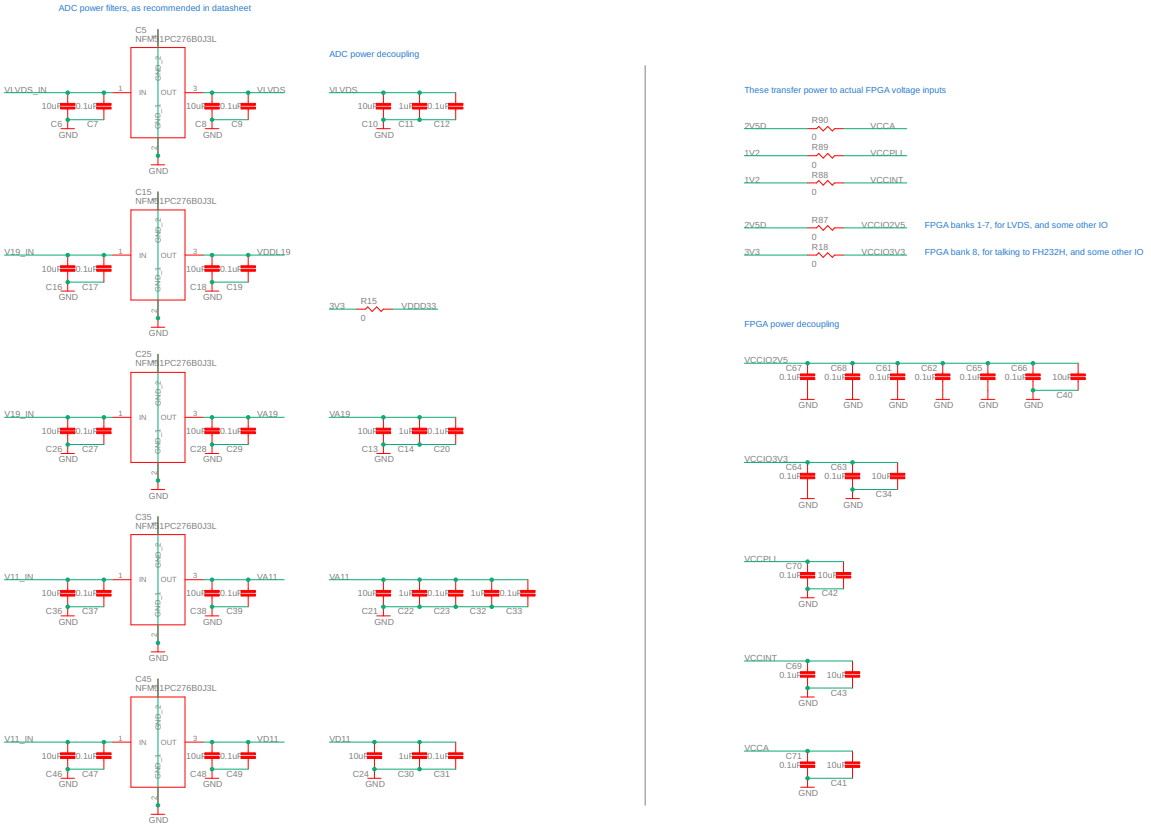

USB C for 5V 2A input
and USB2 data IO
FB2
50mΩ 220Ω@100MHz 0603
VBUS
USB_D_N
USB_D_P
CC1
CC2
VBUSCLEAN
USBC
Pull downs to request USB power
P-MOS AO3401A
Q2
5V
VBUSCLEAN
12VCONNECTED
Connect USBC power to 5V only if 12V not connected
(detected by power jack on next sheet)
If 12VConnected is high (5V), then switch is off
If 12VConnected is low (0V), then switch is on
FTDI FT232H does 8-bit data FIFO
to USB2 interface
VCC3V3
VCC1V8
VCCA_FTDI
To/from computer
USB_D_P
USB_D_N
Flash for FT232H config
93LC56B
12 MHz clock for USB
8-bit data to/from
FT232H FIFO <-> FPGA
FTDI_DATA0
FTDI_DATA1
FTDI_DATA2
FTDI_DATA3
FTDI_DATA4
FTDI_DATA5
FTDI_DATA6
FTDI_DATA7
FTDI_AC0_RXF
FTDI_AC1_TXE
FTDI_AC2_RD
FTDI_AC3_WR
FTDI_AC4_SIWU
FTDI_AC5_CLK
FTDI_AC6_OE
FTDI_AC7_PWRSAV
60 MHz clock goes to FPGA
and is used for data transmission
GND

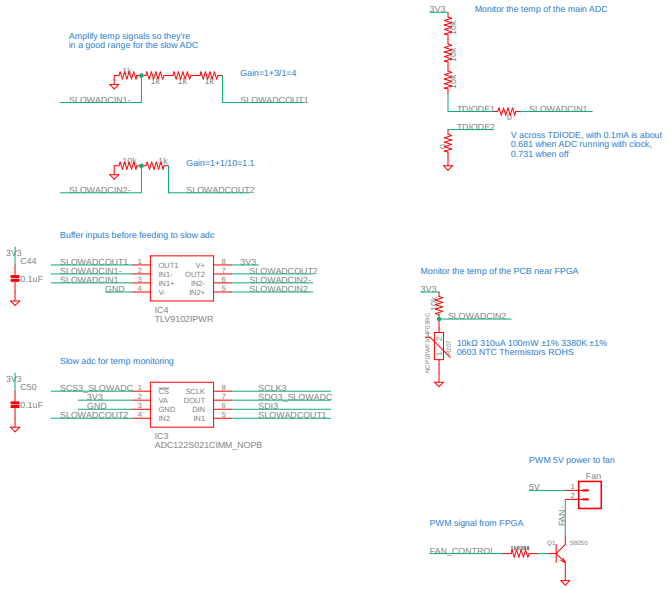

12V input, in case USB C insufficient
5V
R237
10k
12VCONNECTED
CN2
PWR
GNDBREAK
GND
12Vin
J10
12V
C242
C319
C320
0uF
C243
C321
C322
LED2
red
R217
5.1K
GND
Detect if 12V is connected,
so we can disconnect from USB power
When 12V jack is connected, GNDBREAK pin
is not connected to GND anymore, and is then
pulled up to 5V (being generated by 12V)
When 12V jack is not connected,
GNDBREAK is conencted to GND
Make 5V from 12V in case USB C insufficient
PS14
LMR33630ADDA
PGND
VIN
EN
PG
SW
BOOT
VCC
FB
EP
L14
2.2uH
C284
0.1uF
R233
100k
R234
10k
R151
10k
R152
5.1k
C285
1uF
C286
0.1uF
5V
C283
0.1uF
C318
0.1uF
12V
GND
Rbot = Rtop/(Vout-1)
=100k/(5-1) = ~25k
C290
C291
C292
C293
2uF
To FPGA to see if 12V connected
VCCIO2V5
R212
10k
PG12V
5V input, needed unless there is 12V input
Can also be taken from USB C of course
J46
C287
C289
R235
5.1K
LED3
red


Need + and - 2.5V for the amplifiers
V- for input amp reg ~ -3.0V
PS13
LMR33630ADDA
L13
4.7uH
C280
0.1uF
C281
1uF
C282
0.1uF
C288
10uF
C279
0.1uF
5V
3V0-
C294
2uF
C295
2uF
C296
2uF
C297
2uF
GND
R231
100k
R232
100k
R229
100k
R230
100k
Rbot = Rtop/(Vout-1)
=100k/(3.0-1) = 50k
J36
C253
10uF
C254
0.1uF
GND
IC26
TPS7A7200RGTR
2V5+
3V3
R216
10k
PG253
C73
0.1uF
For 2V5+, take input from 3V3
Only ~300mA needed
= 0.5 + grounded inputs
2V5- 1
IC25
TPS72325DBVR
C252
0.1uF
C251
10uF
C250
0.1uF
2V5-1
J34
2V5- 2
IC10
TPS72325DBVR
C77
0.1uF
C76
10uF
C74
0.1uF
2V5-2
J4
Need separate -2v5 supplies for inputs A and B because each needs more than 100mA
and each of these negative regulators can only make 200mA


Need some power for the FPGA
V+ for FPGA reg ~ 1.5V
PS12
LMR33630ADDA
L12
5V
1V5D
GND
C298
C299
C300
C301
2uF
C275
0.1uF
C276
C277
1uF
C278
R229
R230
R231
100k
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
1V2
for FPGA
IC7
TPS7A7200RGTR
C52
C53
10uF
C54
R161
10k
PG1V2
= 0.5 + grounded inputs
V+ for 2v5D reg ~ 2.8V
PS11
LMR33630ADDA
L11
2V8D
C302
C303
C304
C305
C271
C272
C273
C274
R227
R228
10k
5k6
Rbot = Rtop/(Vout-1)
=100k/(2.8-1) = ~55k
VFPGA25 = 2.5V
IC28
TPS7A7200RGTR
C257
C258
R220
PG2V8D


Need 3v3 plus 1v1 and 1v9 for the main ADC
3A max current buck converters
take in 5V and put out voltages
for linear reg that follows
V for 3.3V reg ~ 3.7V
PS2
LMR33630ADDA
Rbot = Rtop/(Vout-1)
=100k/(3.7-1) = ~37k
V for 1.1V reg ~ 1.5V
PS9
LMR33630ADDA
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
V for 1.9V reg ~ 2.2V
PS10
LMR33630ADDA
Rbot = Rtop/(Vout-1)
=100k/(2.2-1) = ~83k
2A max current linear regs
with 180mV dropout at 2A
3V3
IC22
TPS7A7200RGTR
= 0.5 + grounded inputs
1V1
IC24
TPS7A7200RGTR
Enable after Power Good 1.9V
= 0.5 + grounded inputs
1V9
IC23
TPS7A7200RGTR
= 0.5 + grounded inputs
VLVDS = 1.9V
IC27
TPS7A7200RGTR
= 0.5 + grounded inputs


ADC power filters, as recommended in datasheet
ADC power decoupling
These transfer power to actual FPGA voltage inputs
FPGA power decoupling
FPGA banks 1-7, for LVDS, and some other IO
FPGA bank 8, for talking to FH232H, and some other IO
C5
NFM21PC276B0J3L
V1VDS_IN
V1VDS
C6
C7
C8
C9
C10
C11
C12
C15
V19_IN
VDDL19
C16
C17
C18
C19
3V3
R15
VDDD33
C25
VA19
C26
C27
C28
C29
C13
C14
C20
C35
V11_IN
VA11
C36
C37
C38
C39
C21
C22
C23
C32
C33
C45
VD11
C46
C47
C48
C49
C24
C30
C31
2V5D
R90
VCCA
1V2
R89
VCCPLL
R88
VCCINT
R87
VCCIO2V5
3V3
R18
VCCIO3V3
C67
C68
C61
C62
C65
C66
C40
C64
C63
C34
C70
C42
C69
C43
C71
C41
GND


Amplify temp signals so they're
in a good range for the slow ADC
1k
1k
1k
1k
Gain=1+3/1=4
SLOWADCIN1-
SLOWADCOUT1
10k
1k
Gain=1+1/10=1.1
SLOWADCIN2-
SLOWADCOUT2
Buffer inputs before feeding to slow adc
3V3
C44
0.1uF
SLOWADCOUT1
SLOWADCIN1-
SLOWADCIN1
GND
OUT1
IN1-
IN1+
V-
V+
OUT2
IN2-
IN2+
3V3
SLOWADCOUT2
SLOWADCIN2-
SLOWADCIN2
IC4
TLV9102IPWR
Slow adc for temp monitoring
3V3
C50
0.1uF
SCS3_SLOWADC
3V3
GND
SLOWADCOUT2
CS
VA
GND
IN2
SCLK
DOUT
DIN
IN1
SCLK3
SDO3_SLOWADC
SDI3
SLOWADCOUT1
IC3
ADC122S021CIMM_NOPB
3V3
Monitor the temp of the main ADC
10k
10k
10k
TDIODE1
SLOWADCIN1
TDIODE2
0
V across TDIODE, with 0.1mA is about
0.681 when ADC running with clock,
0.731 when off
Monitor the temp of the PCB near FPGA
3V3
10k
SLOWADCIN2
NCP18WB473F03RC
10kΩ 310uA 100mW ±1% 3380K ±1%
0603 NTC Thermistors ROHS
PWM 5V power to fan
Fan
5V
FAN-
PWM signal from FPGA
FAN_CONTROL
10k
Q1
S8050