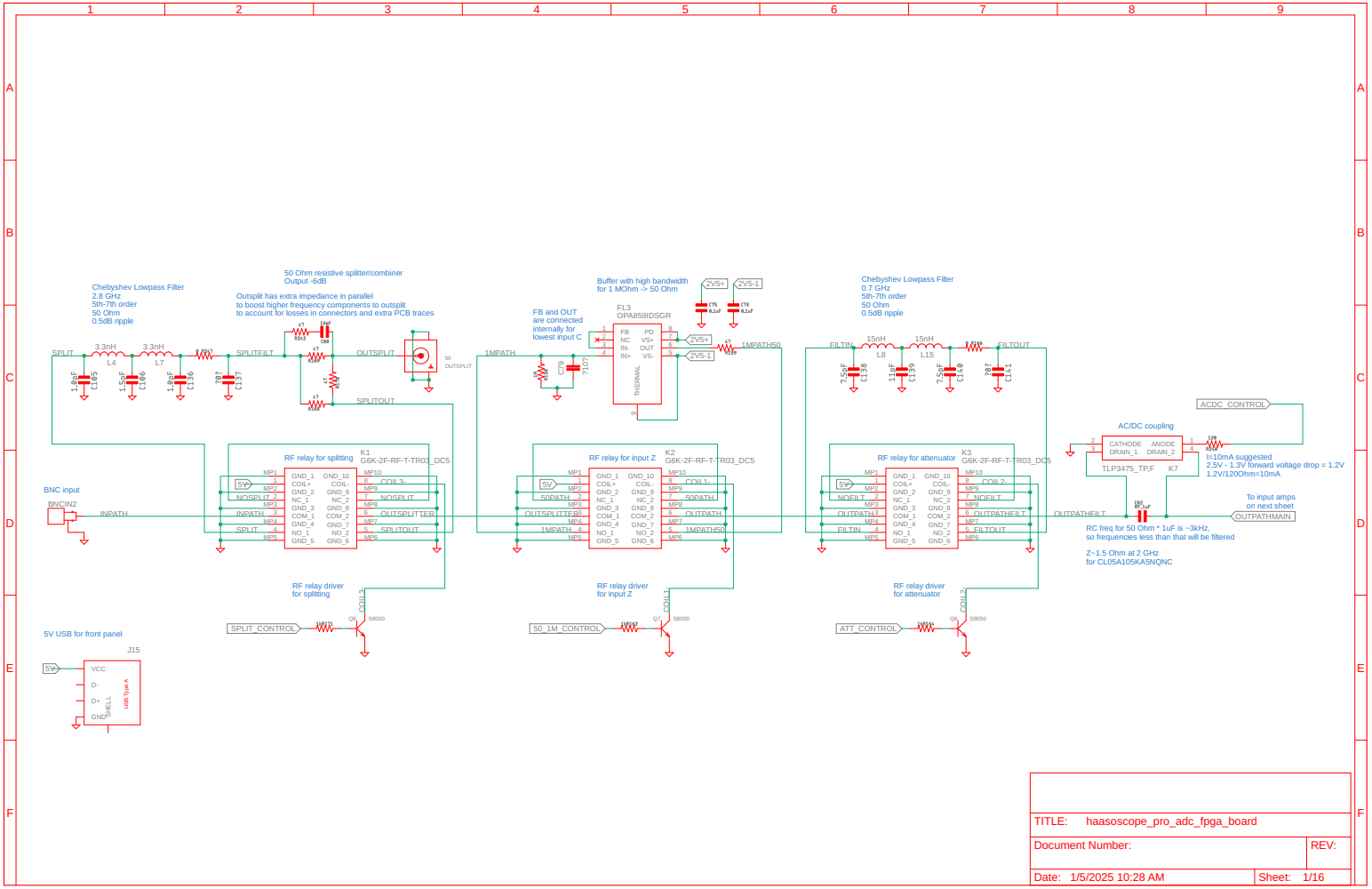
Chebyshev Lowpass Filter
2.8 GHz
5th-7th order
50 Ohm
0.5dB ripple
50 Ohm resistive splitter/combiner
Output -6dB
Outsplit has extra impedance in parallel
to boost higher frequency components to outsplit
to account for losses in connectors and extra PCB traces
Buffer with high bandwidth
for 1 MOhm -> 50 Ohm
FB and OUT
are connected
internally for
lowest input C
FL3
OPA859IDSGR
Chebyshev Lowpass Filter
0.7 GHz
5th-7th order
50 Ohm
0.5dB ripple
AC/DC coupling
TLP3475_TP,F
K7
Ie:10mA suggested
2.5V - 1.3V forward voltage drop = 1.2V
1.2V/120Ohm=10mA
To input amps
on next sheet
RC freq for 50 Ohm * 1uF is ~3kHz,
so frequencies less than that will be filtered
Z~1.5 Ohm at 2 GHz
for CL05A105KA5NQNC
RF relay for splitting
K1
G6K-2F-RF-T-TR03_DC5
RF relay for input Z
K2
G6K-2F-RF-T-TR03_DC5
RF relay for attenuator
K3
G6K-2F-RF-T-TR03_DC5
BNC input
BNCIN2
5V USB for front panel
J15
RF relay driver
for splitting
RF relay driver
for input Z
RF relay driver
for attenuator
SPLIT_CONTROL
50_1M_CONTROL
ATT_CONTROL
ACDC_CONTROL
OUTPATHMAIN
SPLIT
SPLITEILT
OUTSPLIT
SPLITOUT
1MPATH
1MPATH50
FILTIN
FILTOUT
INPATH
OUTPATHEILT
TITLE: haasoscope_pro_adc_fpga_board
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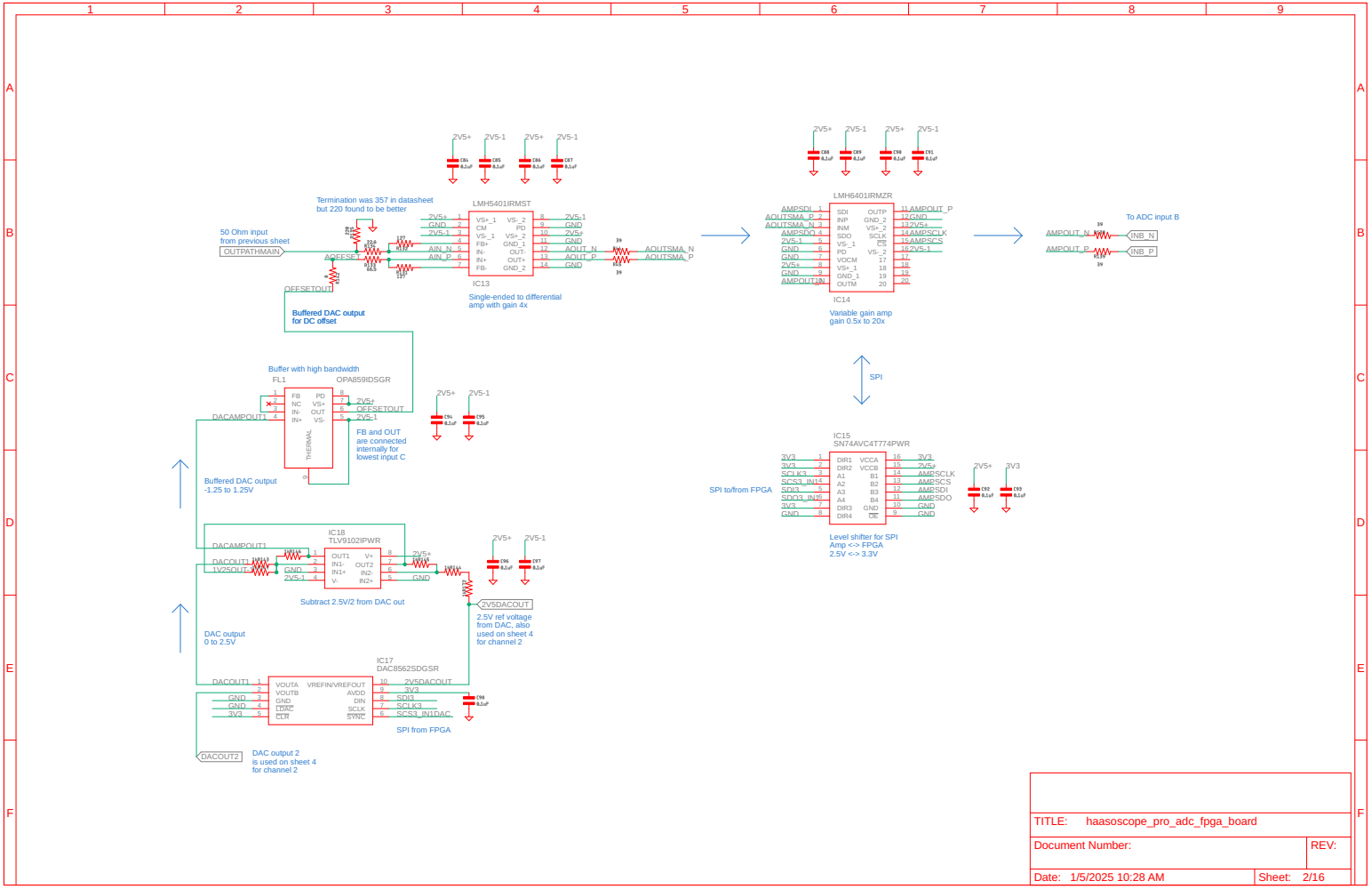
Termination was 357 in datasheet
but 220 found to be better
50 Ohm input
from previous sheet
OUTPATHMAIN
AOFFSET
OFFSETOUT
LMH5401IRMST
IC13
Single-ended to differential
amp with gain 4x
AOUTSMA_N
AOUTSMA_P
LMH6401IRMZR
IC14
Variable gain amp
gain 0.5x to 20x
To ADC input B
INB_N
INB_P
Buffered DAC output
for DC offset
Buffer with high bandwidth
FL1
OPA859IDSGR
DACAMPOUT1
FB and OUT
are connected
internally for
lowest input C
Buffered DAC output
-1.25 to 1.25V
SPI
IC15
SN74AVC4T774PWR
SPI to/from FPGA
Level shifter for SPI
Amp <-> FPGA
2.5V <-> 3.3V
IC18
TLV9102IPWR
Subtract 2.5V/2 from DAC out
2V5DACOUT
2.5V ref voltage
from DAC, also
used on sheet 4
for channel 2
DAC output
0 to 2.5V
IC17
DAC8562SDGSR
SPI from FPGA
DACOUT2
DAC output 2
is used on sheet 4
for channel 2
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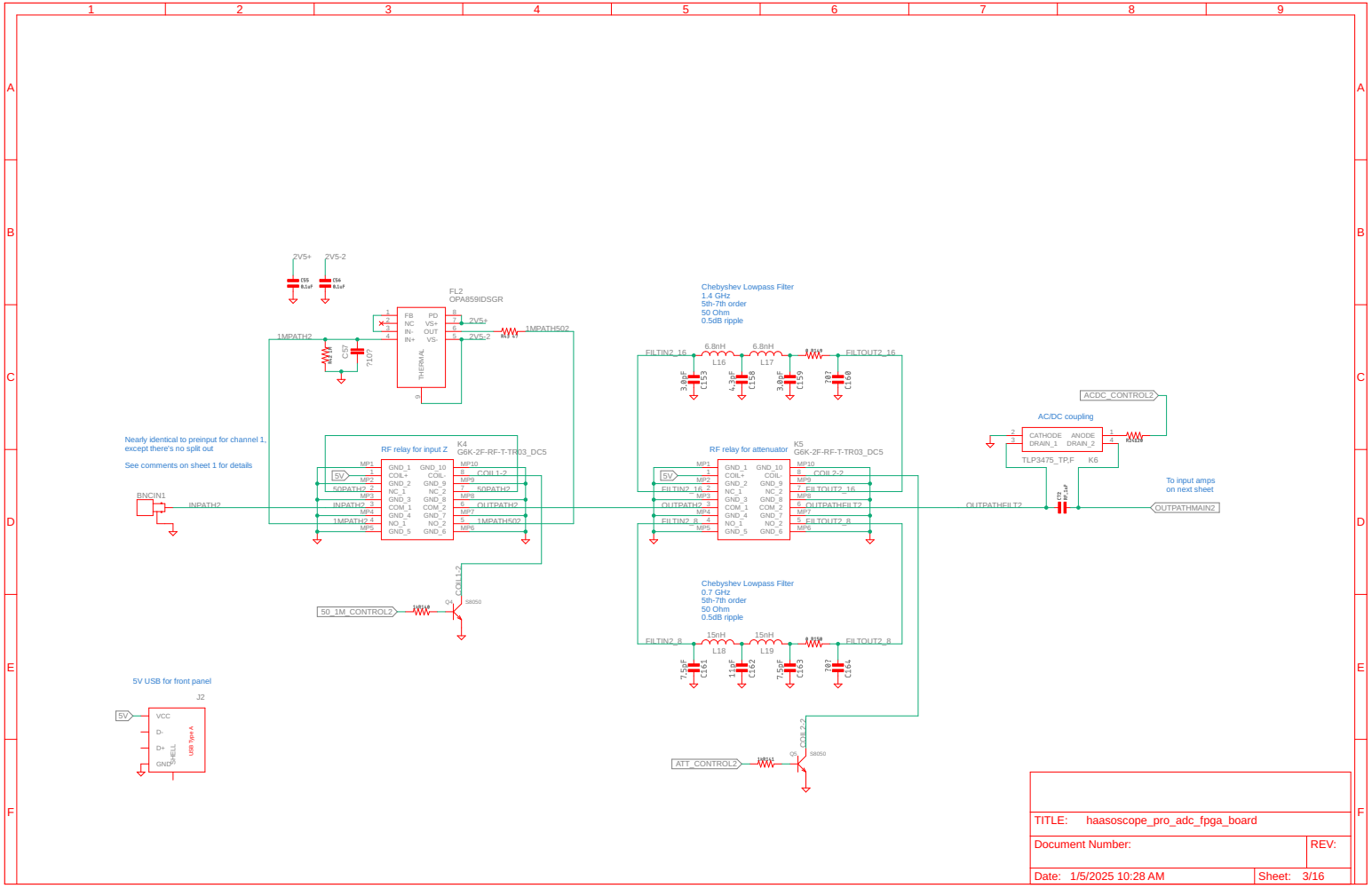
2V5+
2V5-2
C55 0.1uF
C56 0.1uF
FL2
OPA859IDSGR
FB
NC
IN-
IN+
PD
VS+
OUT
VS-
THERMAL
2V5+
2V5-2
1MPATH502
1MPATH2
C57 7107
Nearly identical to preinput for channel 1, except there's no split out
See comments on sheet 1 for details
RF relay for input Z
K4
G6K-2F-RF-T-TR03_DC5
5V
50PATH2
INPATH2
1MPATH2
COIL 1-2
OUTPATH2
1MPATH502
BNCIN1
INPATH2
COIL 1-2
50_1M_CONTROL2
Q4
S8050
Chebyshev Lowpass Filter
1.4 GHz
5th-7th order
50 Ohm
0.5dB ripple
FILTIN2_16
6.8nH
L16
6.8nH
L17
FILTOUT2_16
3.9pF C159
4.7pF C158
3.9pF C159
787 C160
RF relay for attenuator
K5
G6K-2F-RF-T-TR03_DC5
5V
FILTIN2_16
OUTPATH2
FILTIN2_8
COIL 2-2
FILTOUT2_16
OUTPATHFILT2
FILTOUT2_8
Chebyshev Lowpass Filter
0.7 GHz
5th-7th order
50 Ohm
0.5dB ripple
FILTIN2_8
15nH
L18
15nH
L19
FILTOUT2_8
7.5pF C161
11pF C162
7.5pF C163
787 C164
COIL 2-2
ATT_CONTROL2
Q5
S8050
ACDC_CONTROL2
AC/DC coupling
CATHODE
ANODE
DRAIN_1
DRAIN_2
TLP3475_TP,F
K6
OUTPATHFILT2
C72 0.1uF
To input amps on next sheet
OUTPATHMAIN2
5V USB for front panel
J2
5V
VCC
D-
D+
GND
SHELL
USB Type A
TITLE: haasoscope_pro_adc_fpga_board
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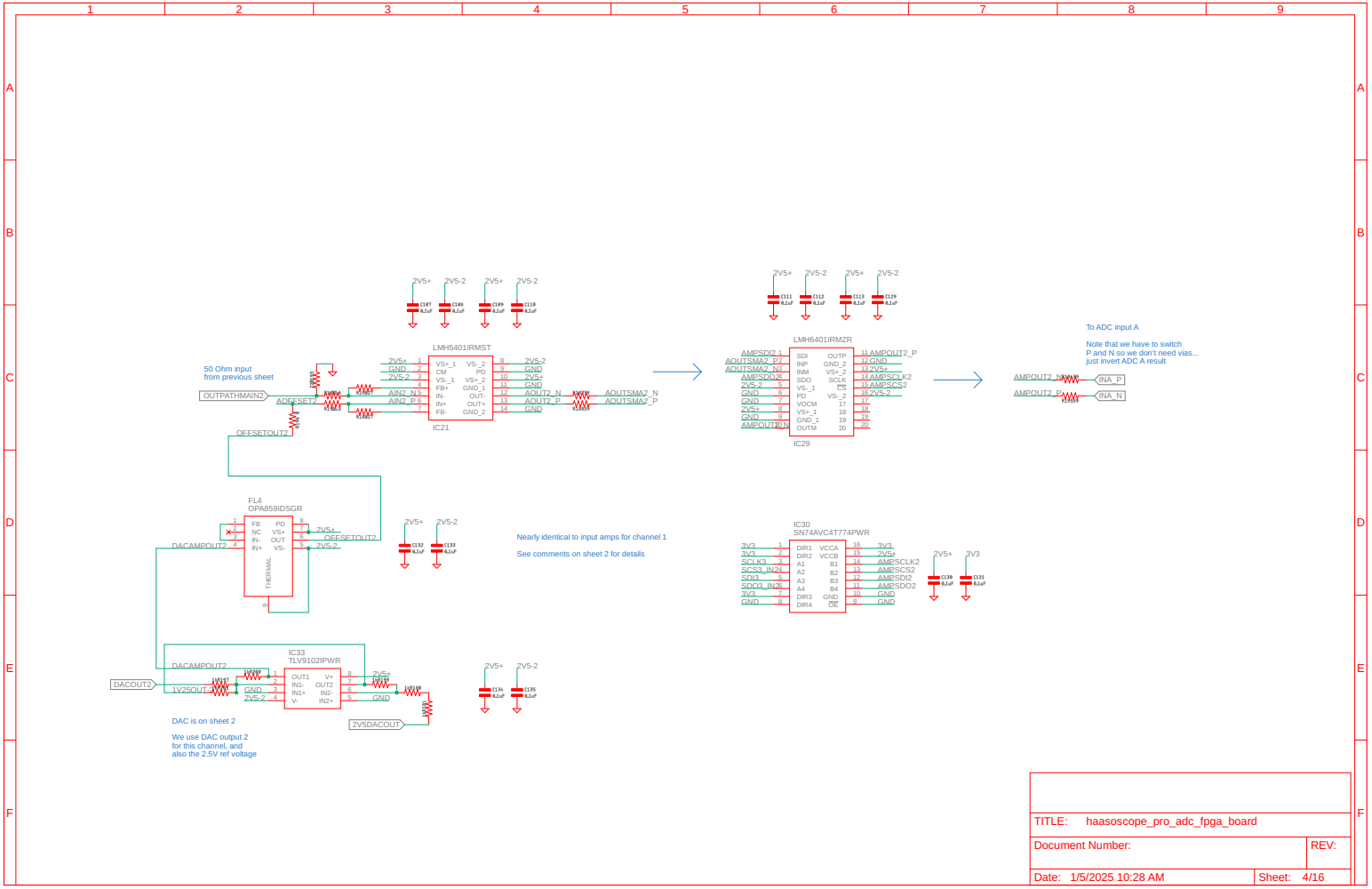
50 Ohm input
from previous sheet
OUTPATHMAIN2
OFFSETOUT2
LMH5401IRMST
IC21
LMH6401IRMZR
IC29
To ADC input A
Note that we have to switch
P and N so we don't need vias...
just invert ADC A result
FL4
OPA859IDSGR
THERMAL
Nearly identical to input amps for channel 1
See comments on sheet 2 for details
IC30
SN74AVC4T774PWR
IC33
TLV9102IPWR
DACOUT2
DACAMPOUT2
1V25OUT2
2V5DACOUT
DAC is on sheet 2
We use DAC output 2
for this channel, and
also the 2.5V ref voltage
TITLE: haasoscope_pro_adc_fpga_board
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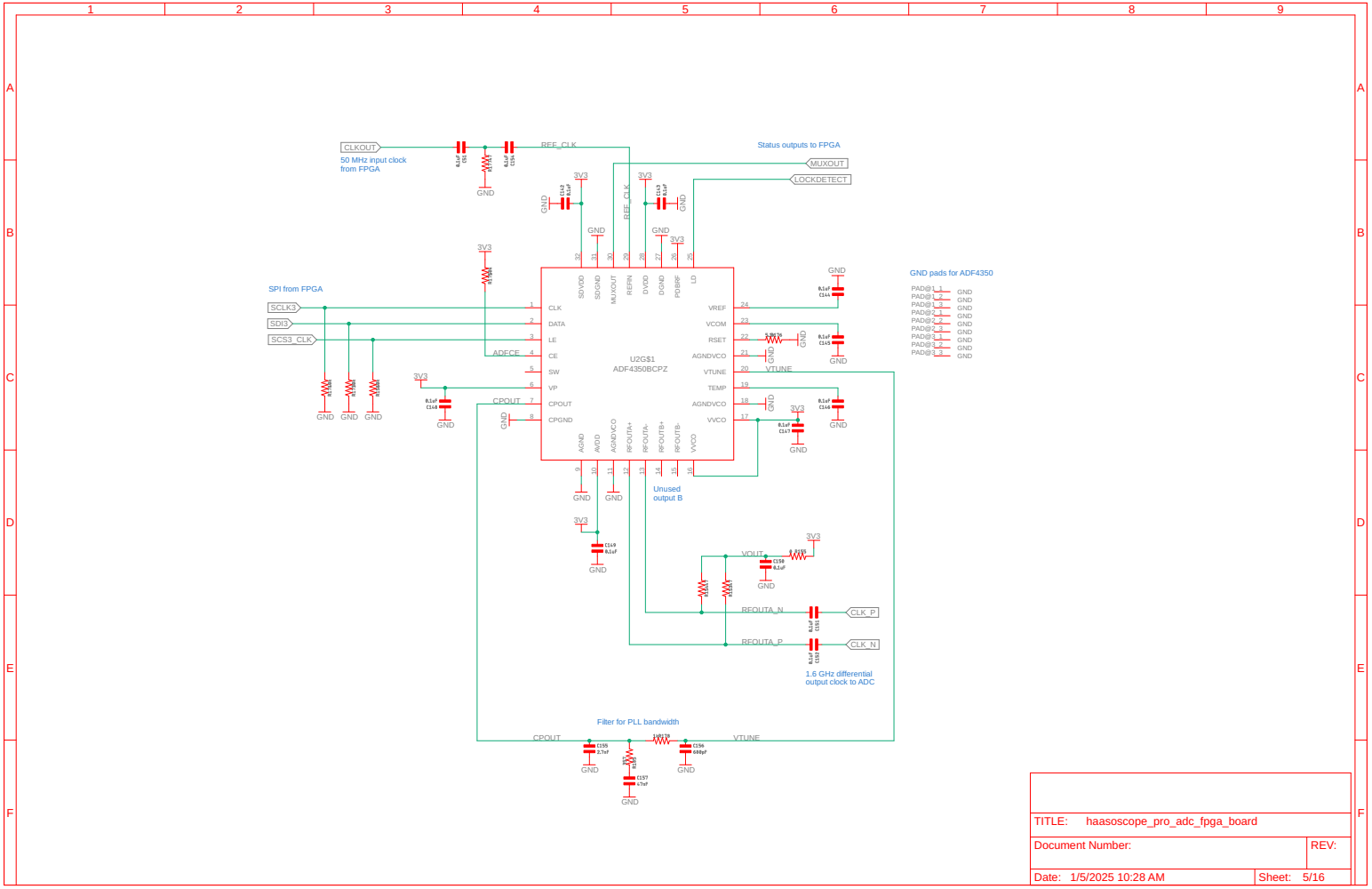

TITLE: haasoscope_pro_adc_fpga_board	
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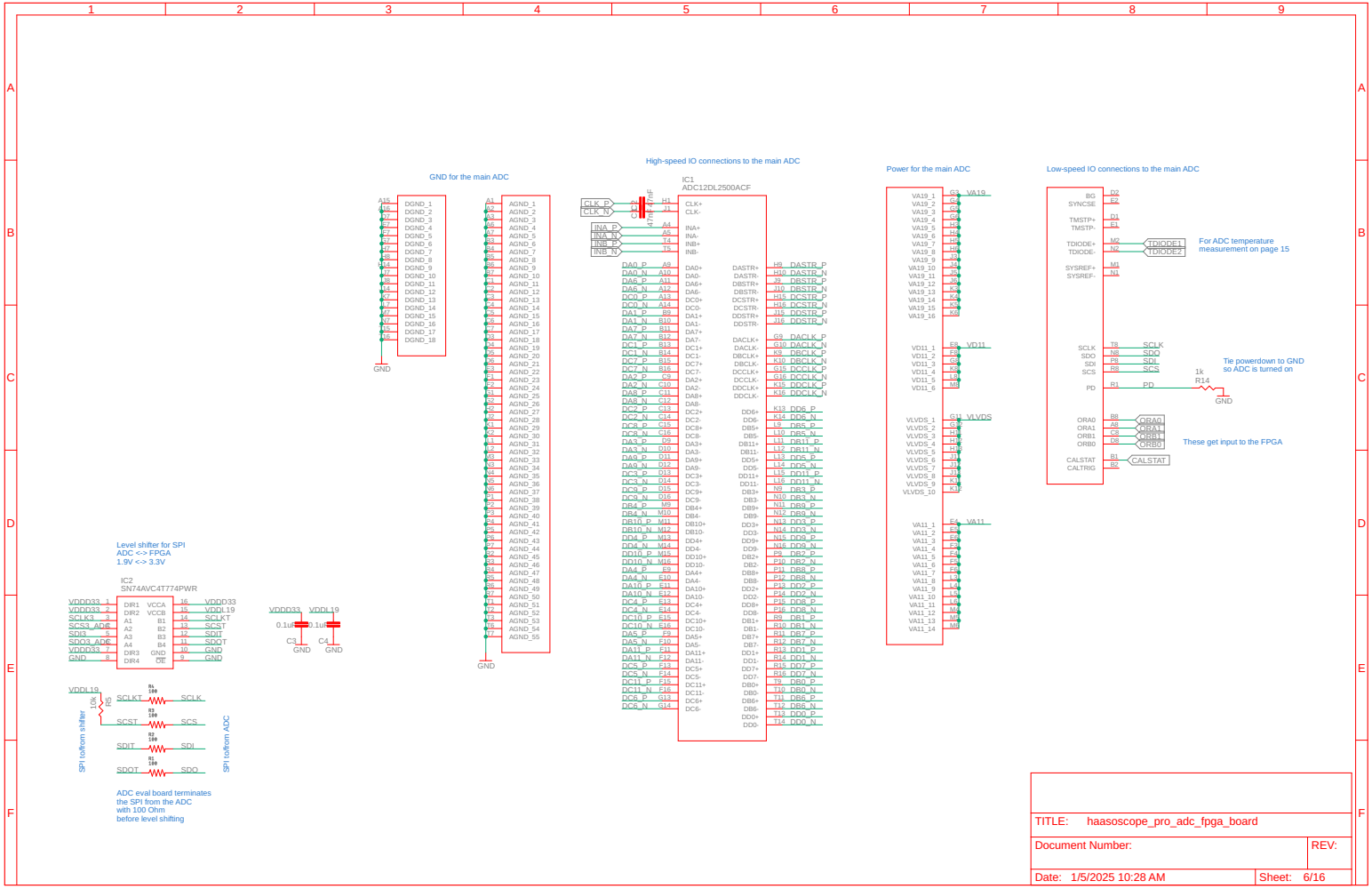
GND for the main ADC
High-speed IO connections to the main ADC
IC1
ADC12DL2500ACF
Power for the main ADC
Low-speed IO connections to the main ADC
For ADC temperature measurement on page 15
Tie powerdown to GND so ADC is turned on
These get input to the FPGA
Level shifter for SPI ADC <-> FPGA 1.9V <-> 3.3V
IC2
SN74AVC4T774PWR
SPI to/from shifter
SPI to/from ADC
ADC eval board terminates the SPI from the ADC with 100 Ohm before level shifting
TITLE: haasoscope_pro_adc_fpga_board
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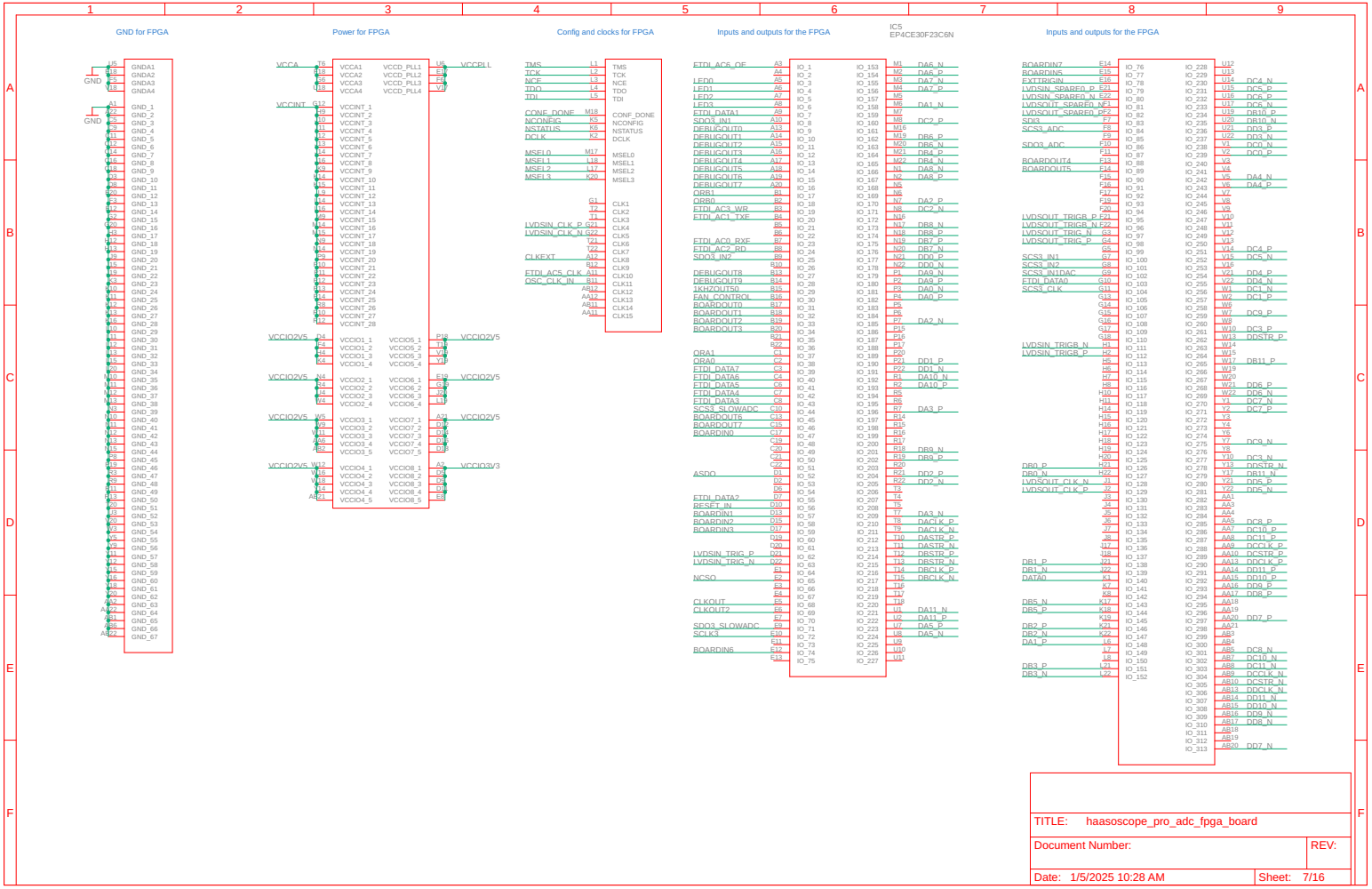
GND for FPGA
Power for FPGA
Config and clocks for FPGA
Inputs and outputs for the FPGA
IC5
EP4CE30F23C6N
Inputs and outputs for the FPGA
TITLE: haasoscope_pro_adc_fpga_board
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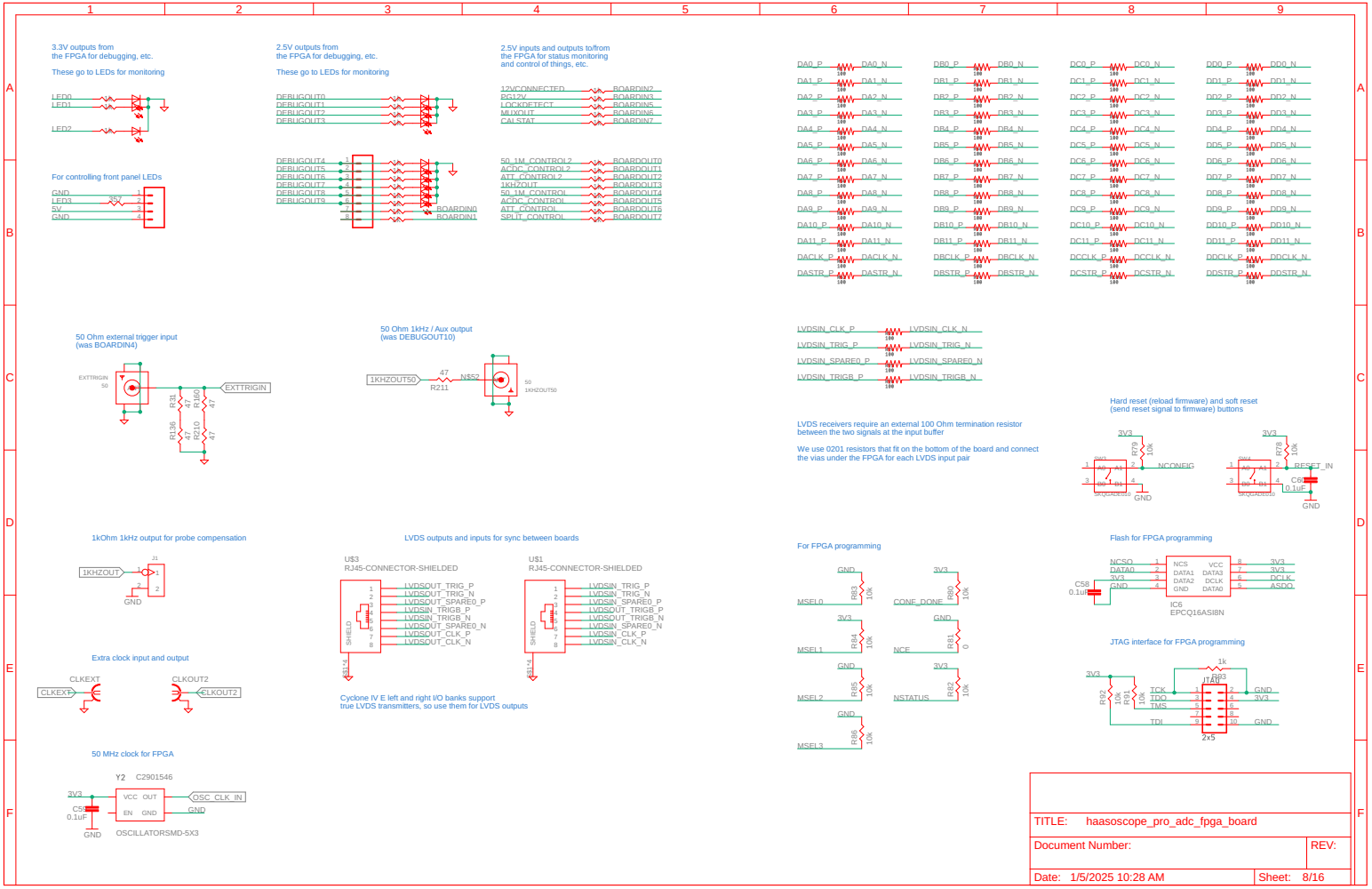

TITLE: haasoscope_pro_adc_fpga_board

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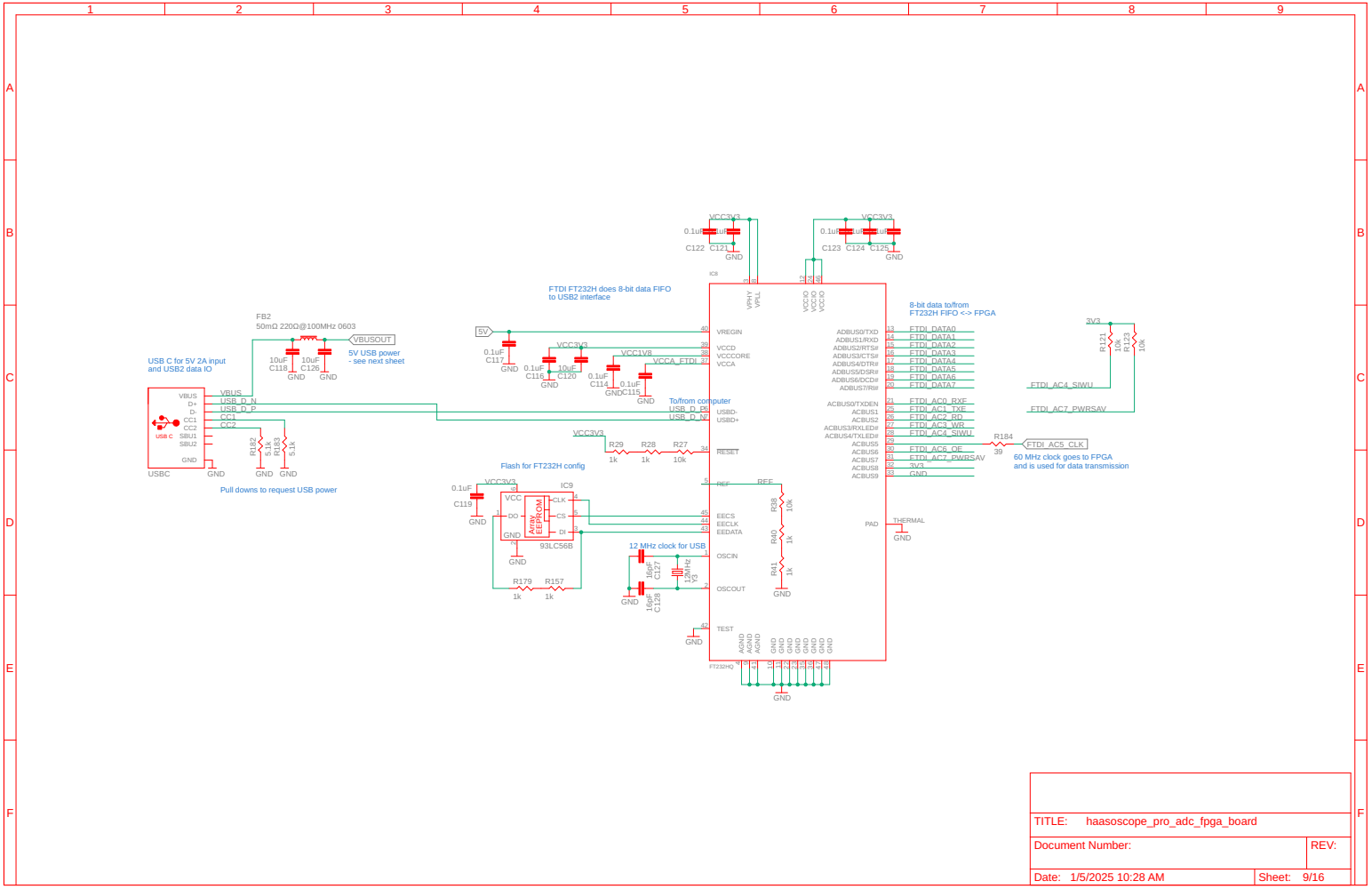

TITLE: haasoscope_pro_adc_fpga_board	
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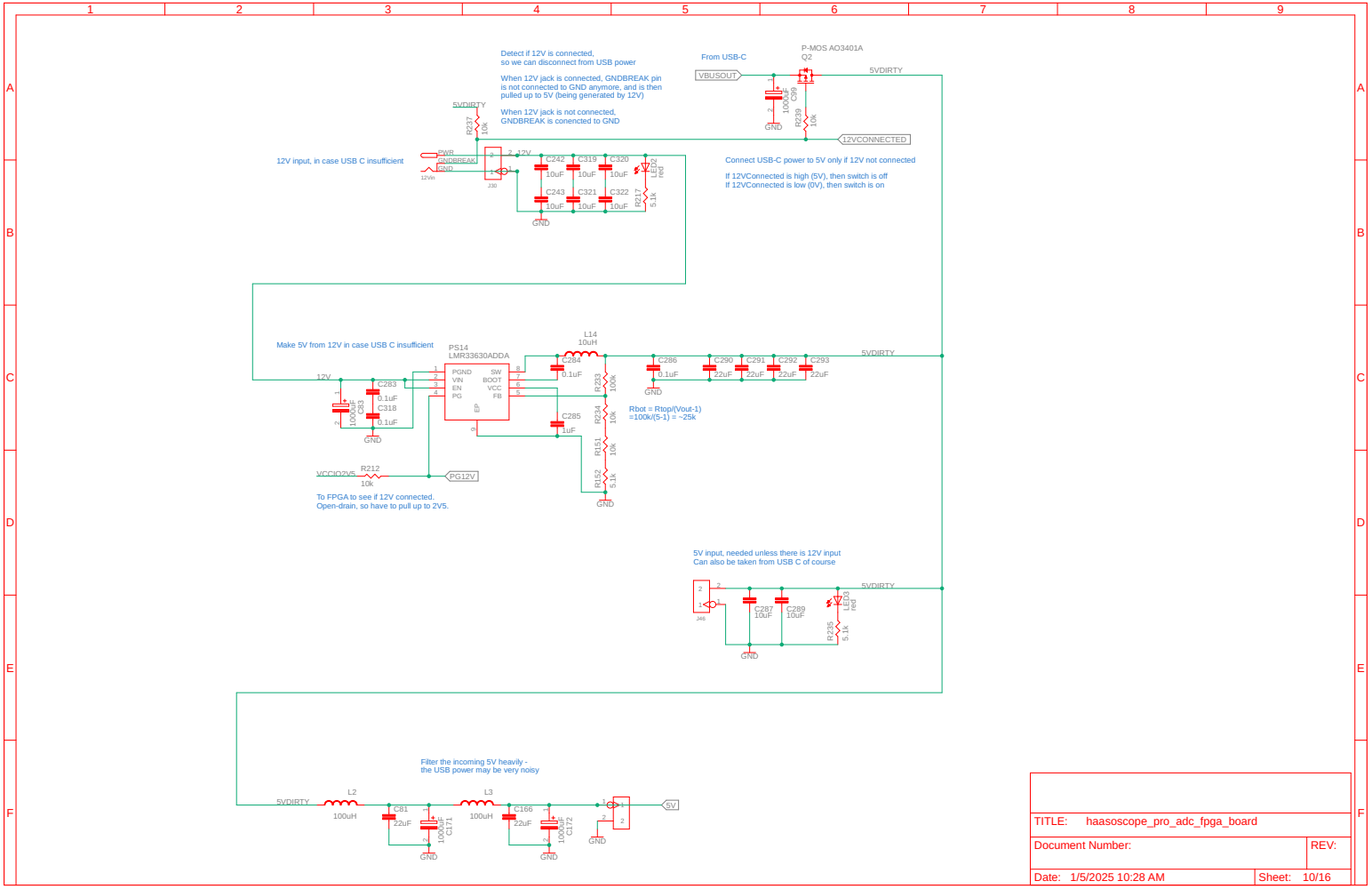

TITLE: haasoscope_pro_adc_fpga_board	
Document Number:	REV:
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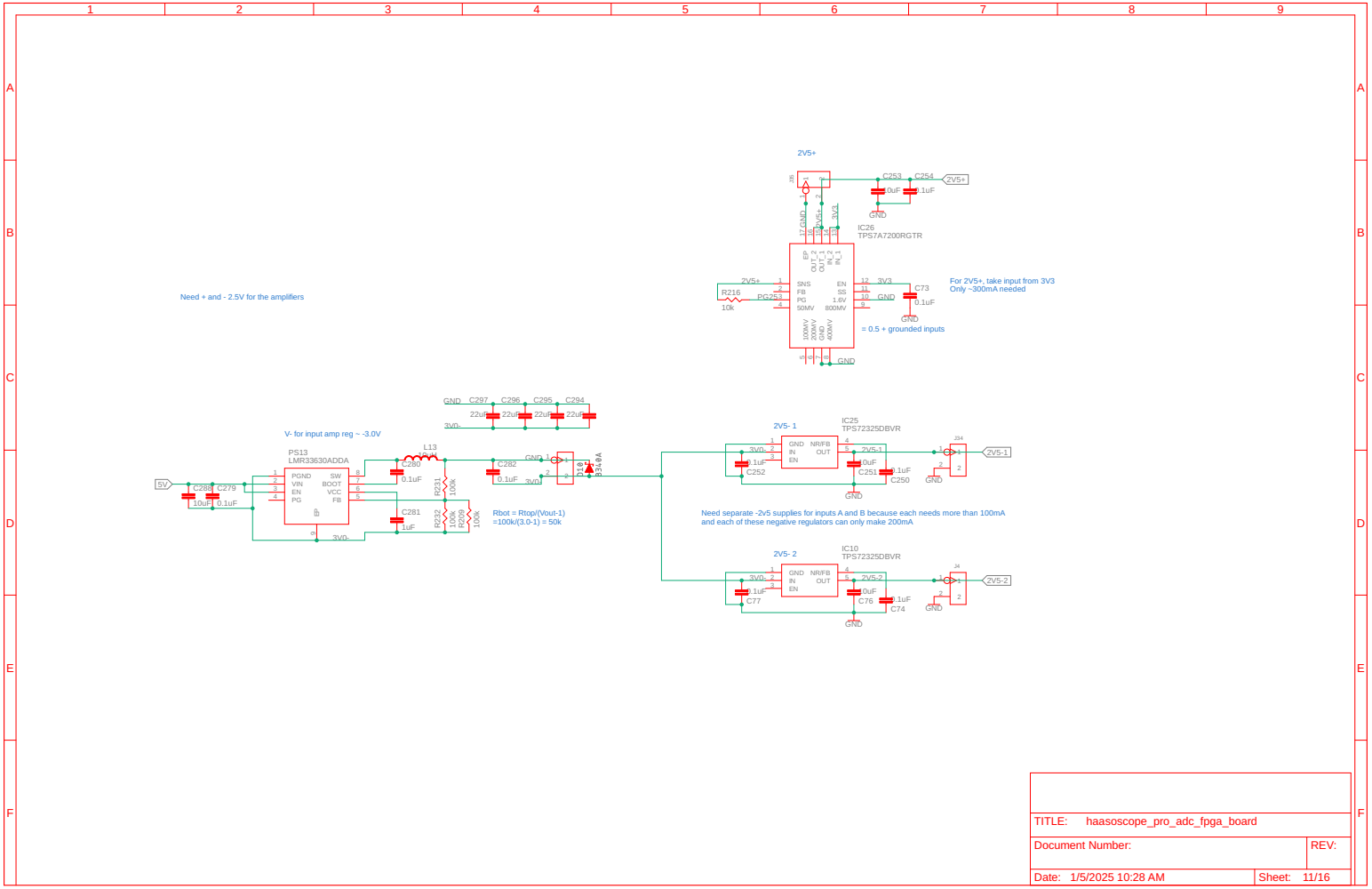

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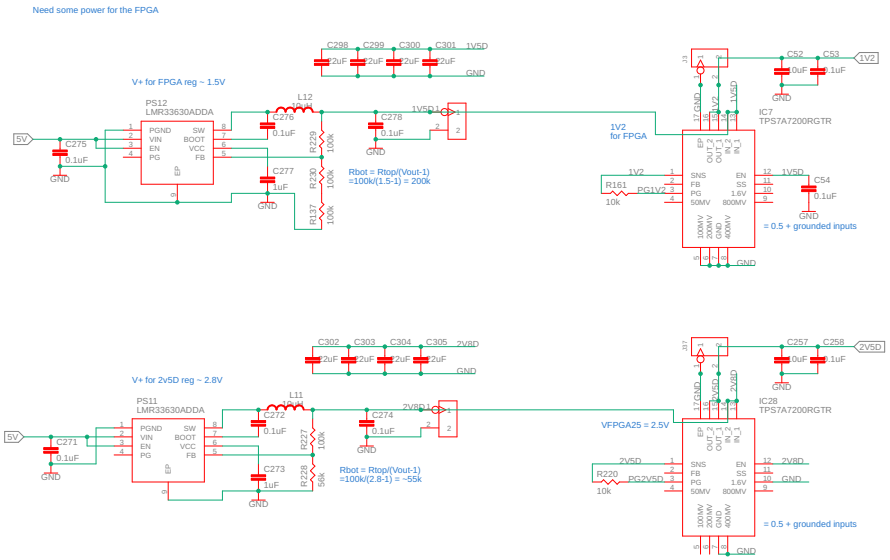

TITLE: haasoscope_pro_adc_fpga_board	
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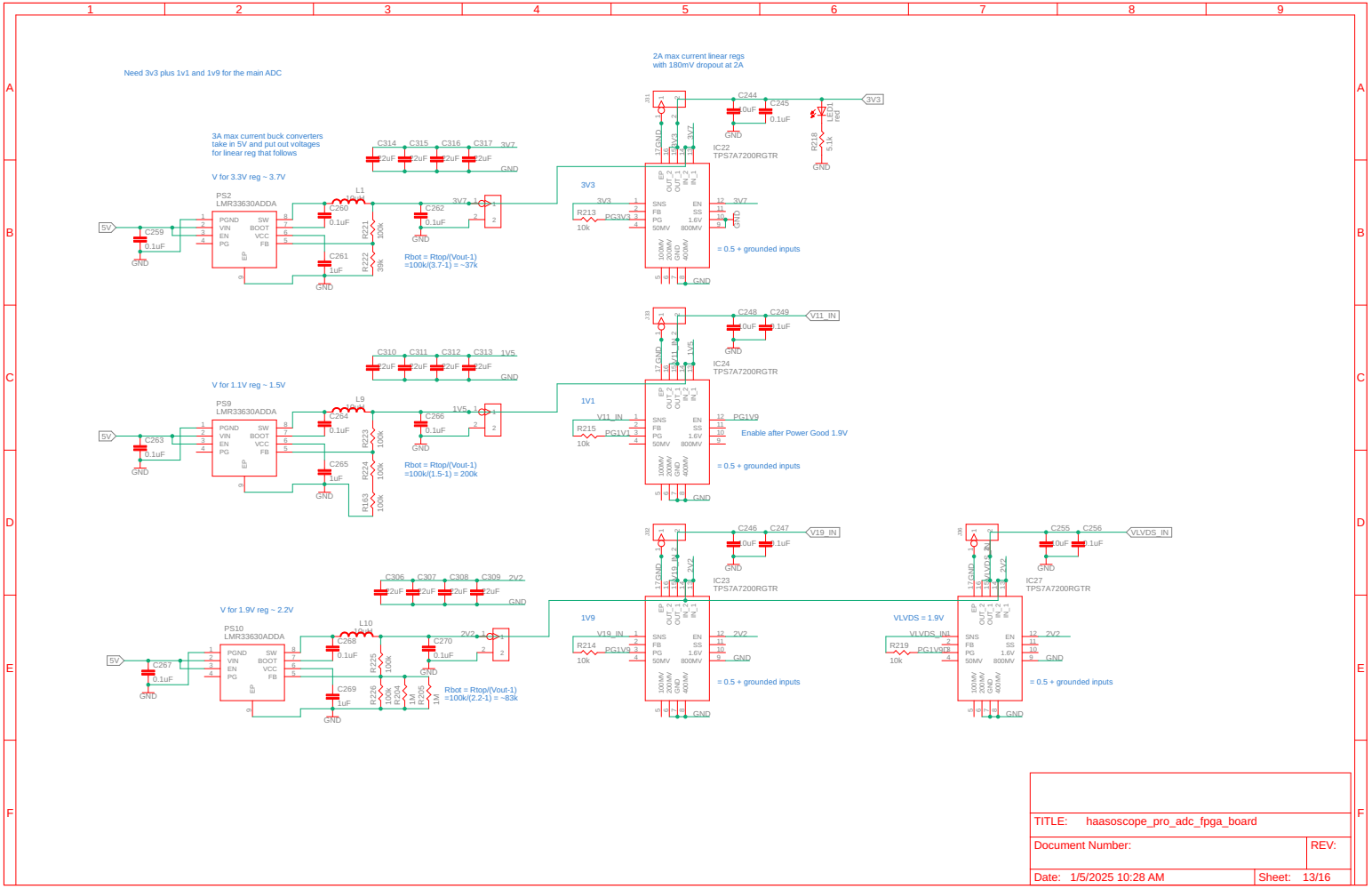
Need 3v3 plus 1v1 and 1v9 for the main ADC
2A max current linear regs
with 180mV dropout at 2A
3A max current buck converters
take in 5V and put out voltages
for linear reg that follows
V for 3.3V reg ~ 3.7V
PS2
LMR33630ADDA
Rbot = Rtop/(Vout-1)
=100k/(3.7-1) = ~37k
IC22
TPS7A7200RGTR
= 0.5 + grounded inputs
V for 1.1V reg ~ 1.5V
PS9
LMR33630ADDA
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
IC24
TPS7A7200RGTR
Enable after Power Good 1.9V
= 0.5 + grounded inputs
V for 1.9V reg ~ 2.2V
PS10
LMR33630ADDA
Rbot = Rtop/(Vout-1)
=100k/(2.2-1) = ~83k
IC23
TPS7A7200RGTR
= 0.5 + grounded inputs
VLVDS = 1.9V
IC27
TPS7A7200RGTR
= 0.5 + grounded inputs
TITLE: haasoscope_pro_adc_fpga_board
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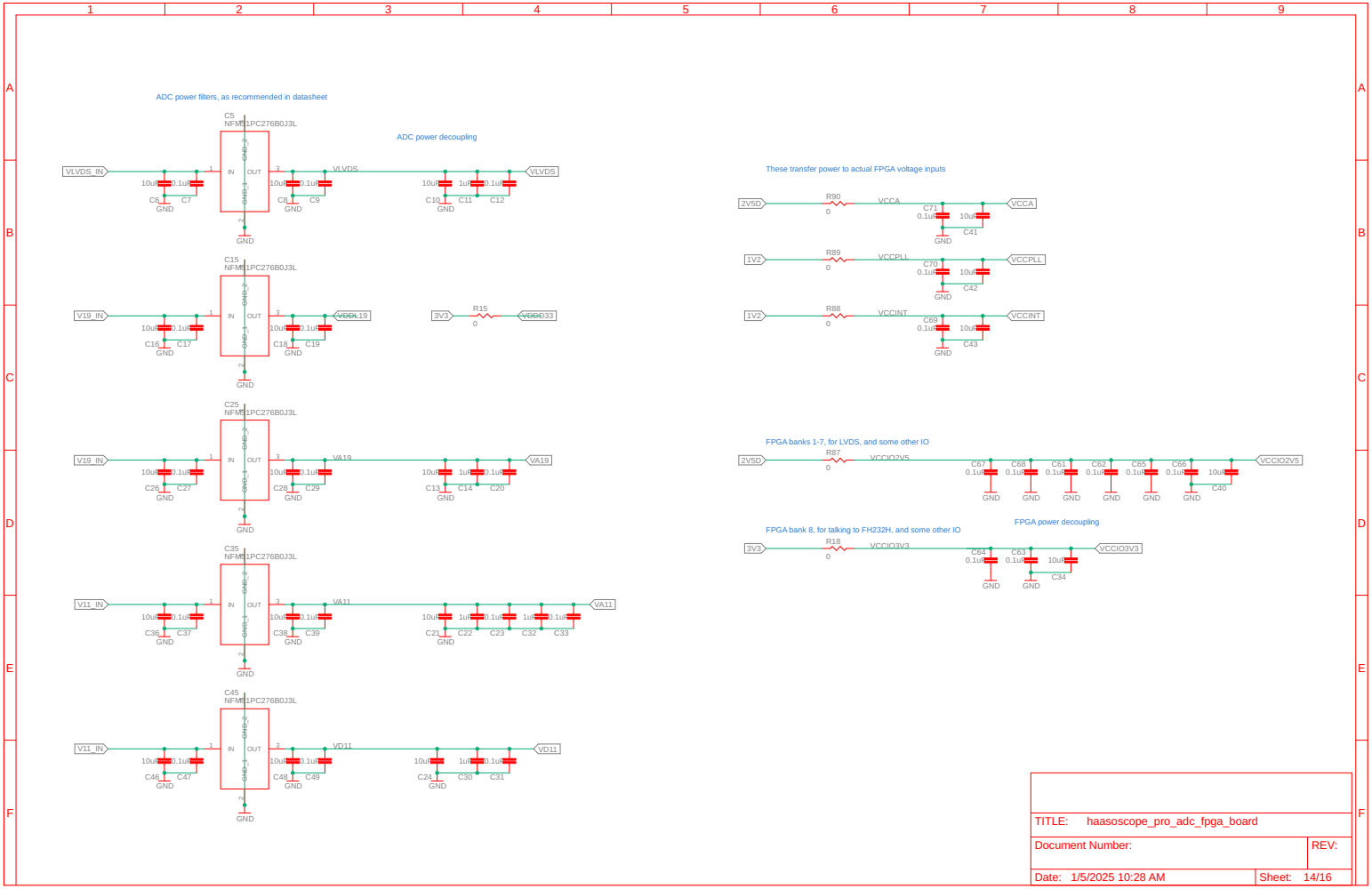
ADC power filters, as recommended in datasheet
ADC power decoupling
These transfer power to actual FPGA voltage inputs
FPGA banks 1-7, for LVDS, and some other IO
FPGA bank 8, for talking to FH232H, and some other IO
FPGA power decoupling
C5 NFM21PC276B0J3L
C15 NFM21PC276B0J3L
C25 NFM21PC276B0J3L
C35 NFM21PC276B0J3L
C45 NFM21PC276B0J3L
VLVDS_IN
V19_IN
V11_IN
VLVDS
VDDL19
VDDD33
VA19
VA11
VD11
3V3
R15
2V5D
1V2
R90
R89
R88
VCCA
VCCPLL
VCCINT
R87
VCCIO2V5
R18
VCCIO3V3
GND
TITLE: haasoscope_pro_adc_fpga_board
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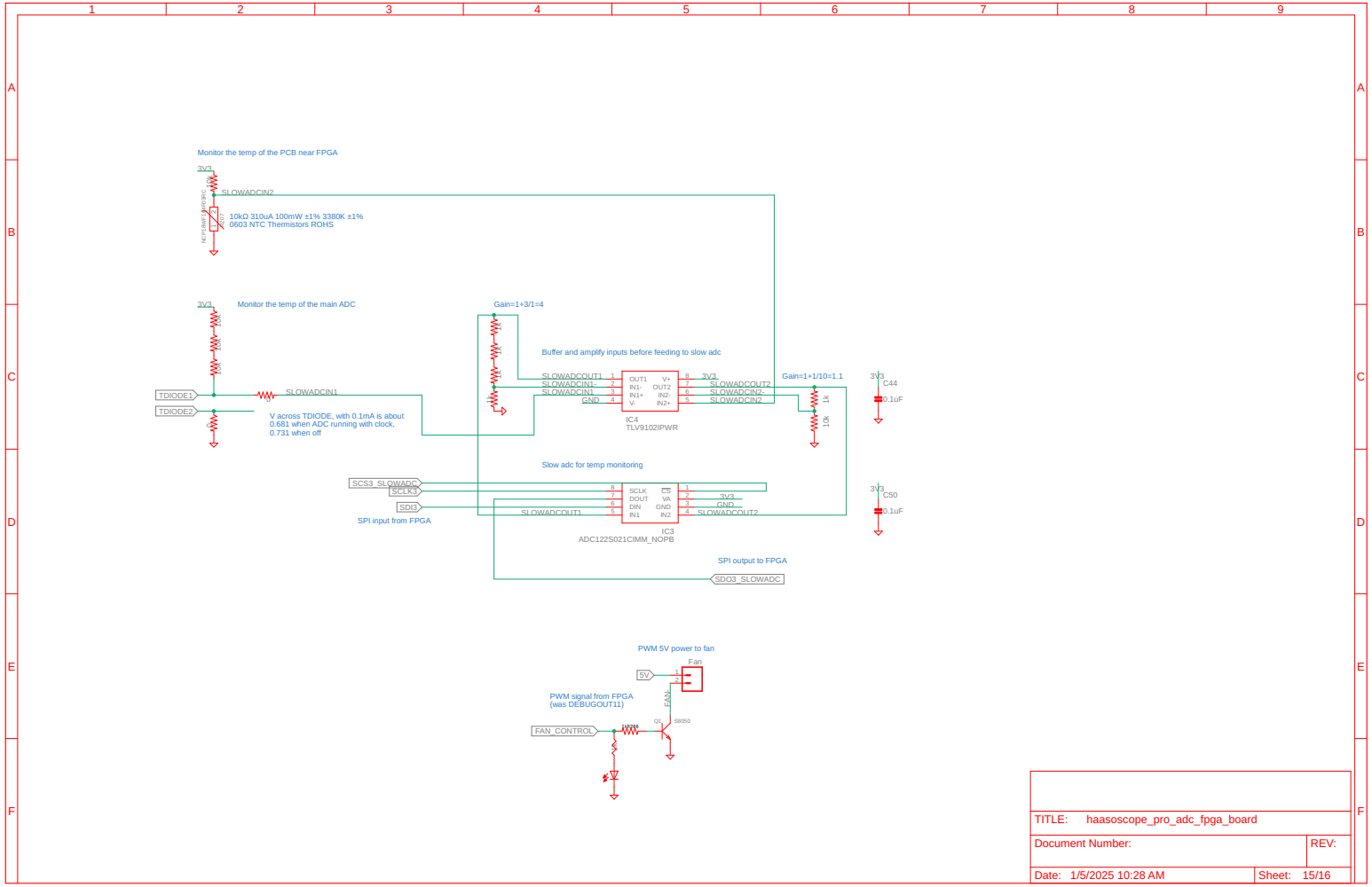

TITLE: haasoscope_pro_adc_fpga_board	
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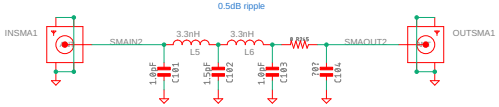
Some extra things to put on
the board for testing only

Not connected to the rest of the system!

Chebyshev Lowpass Filter
2.8 GHz
5th-7th order
50 Ohm
0.5dB ripple



TITLE: haasoscope_pro_adc_fpga_board	
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