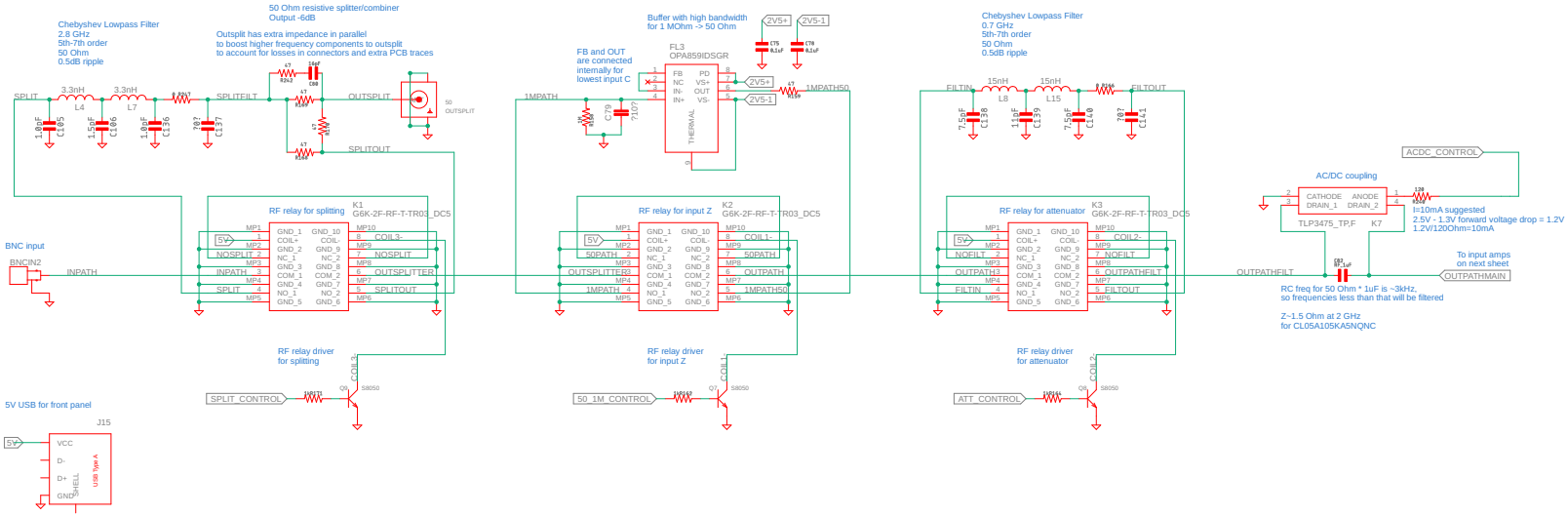
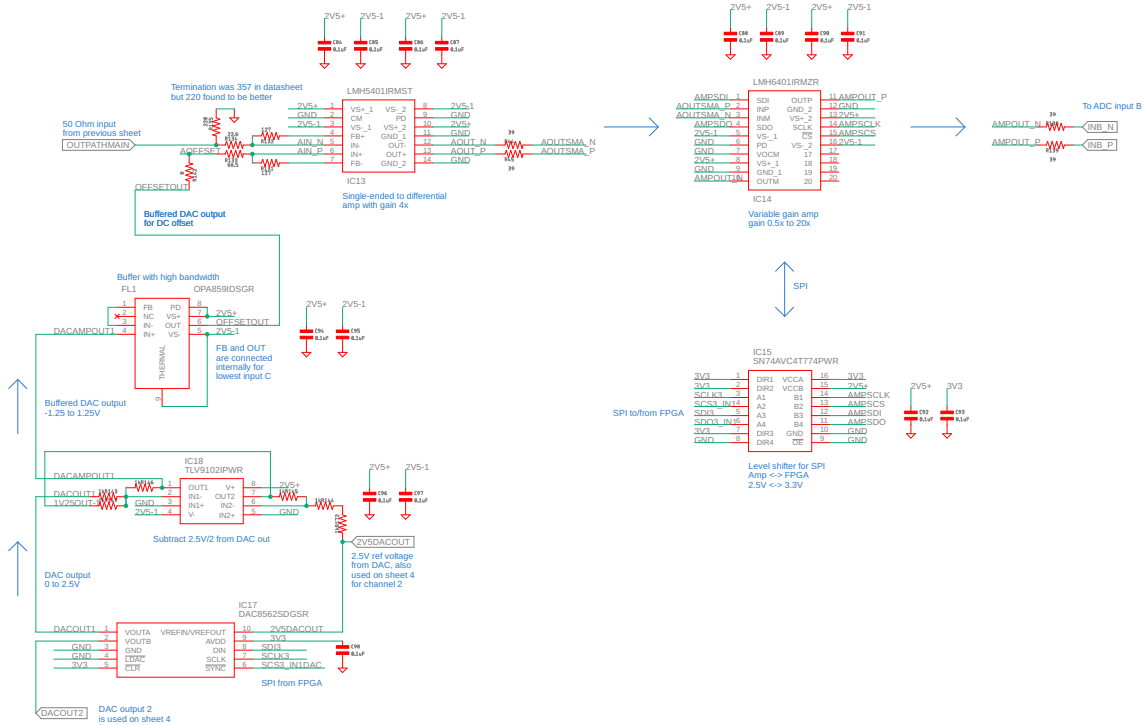
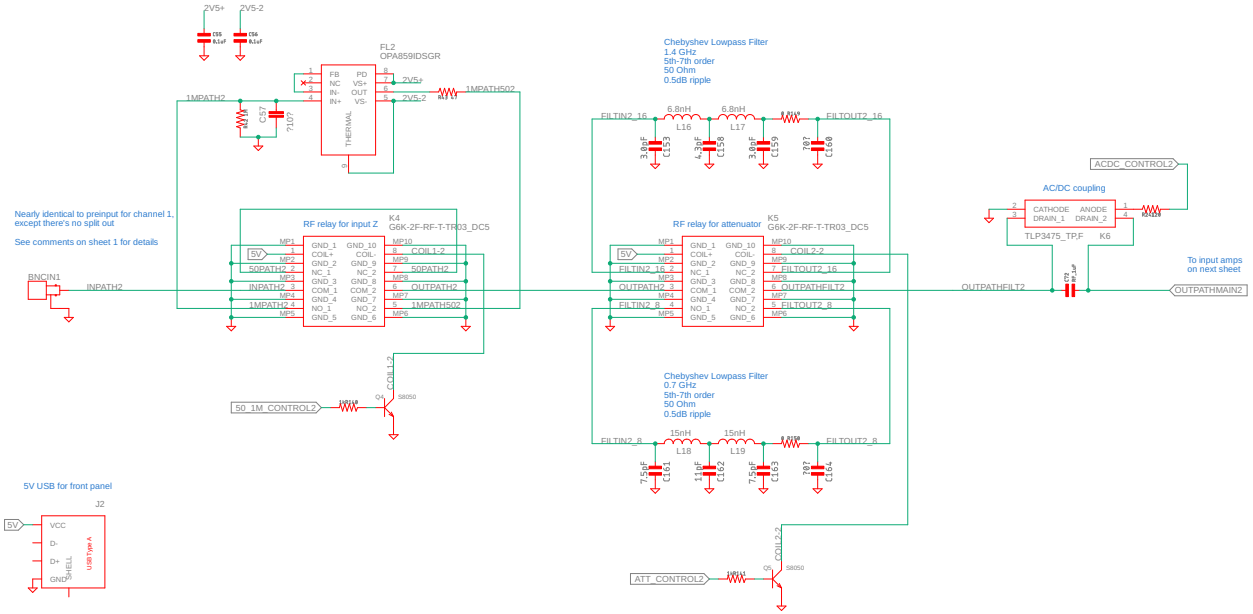
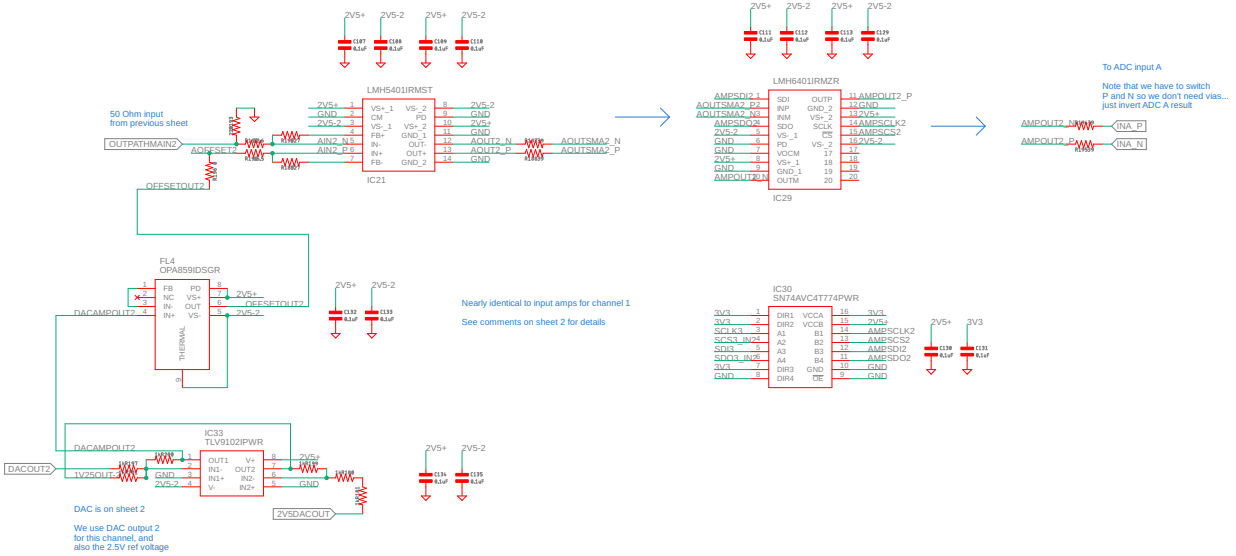
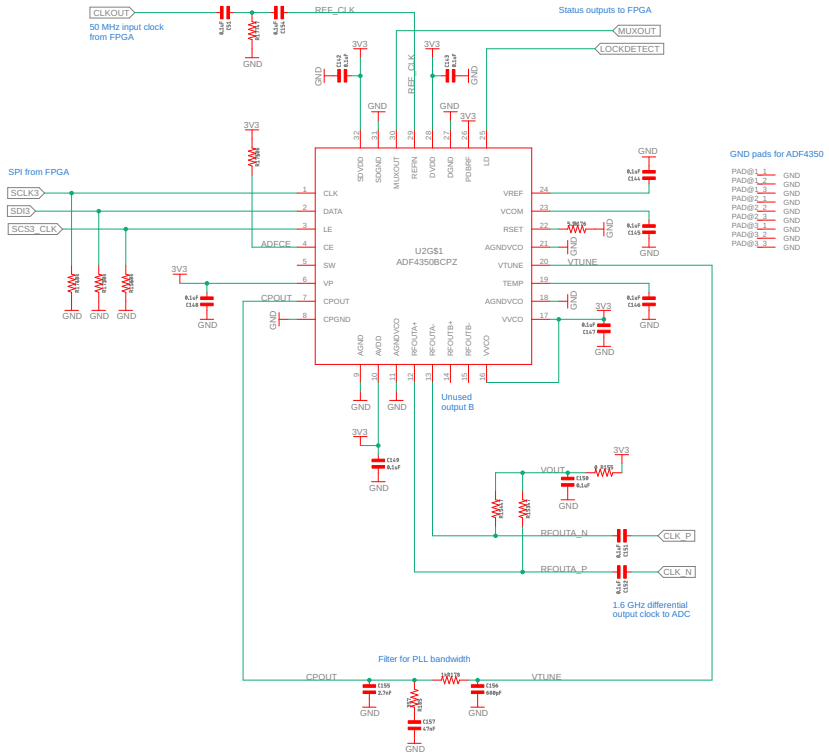
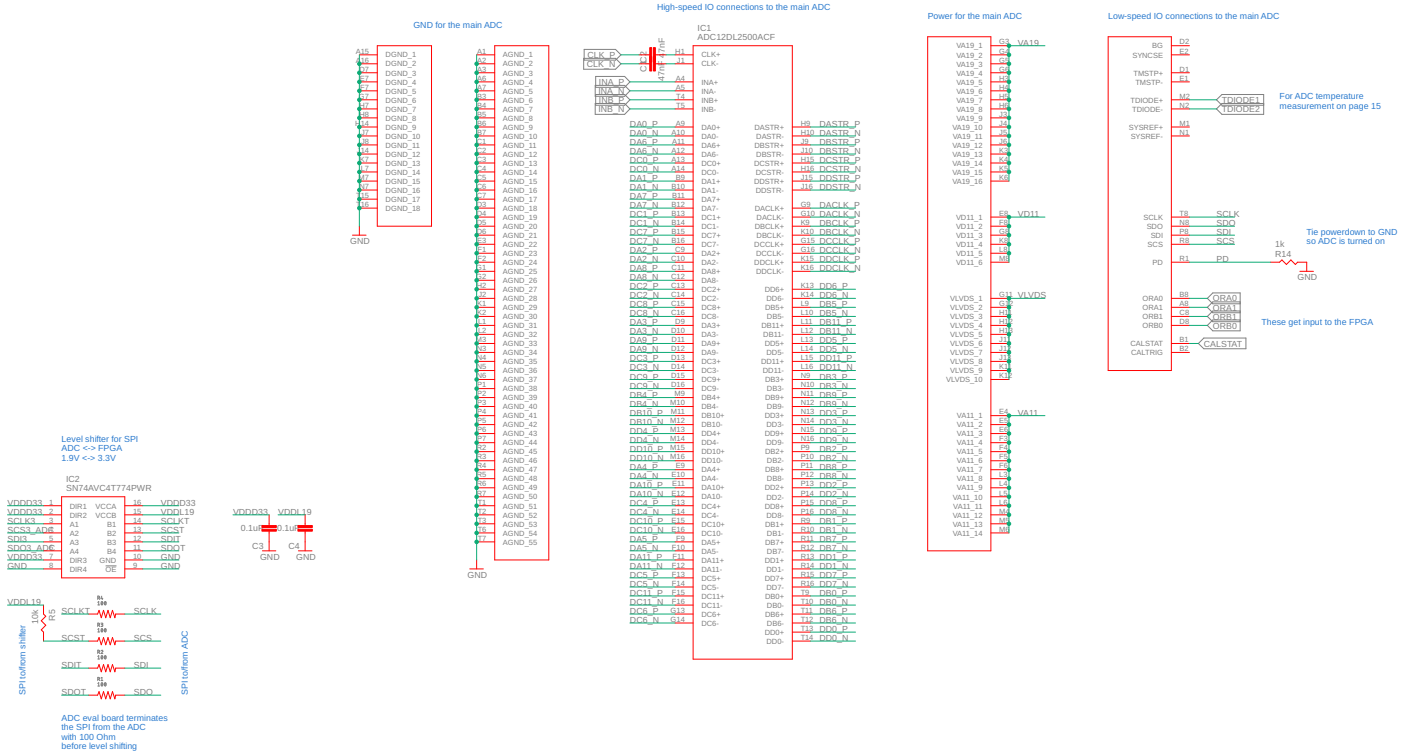

Chebyshev Lowpass Filter
2.8 GHz
5th-7th order
50 Ohm
0.5dB ripple
50 Ohm resistive splitter/combiner
Output -6dB
Outsplit has extra impedance in parallel
to boost higher frequency components to outsplit
to account for losses in connectors and extra PCB traces
SPLIT
SPLITFILT
OUTSPLIT
SPLITOUT
Buffer with high bandwidth
for 1 MOhm -> 50 Ohm
FB and OUT
are connected
internally for
lowest input C
FL3
OPA859IDSGR
1MPATH
1MPATH50
Chebyshev Lowpass Filter
0.7 GHz
5th-7th order
50 Ohm
0.5dB ripple
FILTIN
FILTOUT
AC/DC coupling
ACDC_CONTROL
TLP3475_TP,F
K7
I=10mA suggested
2.5V - 1.3V forward voltage drop = 1.2V
1.2V/120Ohm=10mA
To input amps
on next sheet
OUTPATHMAIN
OUTPATHFILT
RC freq for 50 Ohm * 1uF is ~3kHz,
so frequencies less than that will be filtered
Z~1.5 Ohm at 2 GHz
for CL05A105KA5NQNC
BNC input
BNCIN2
INPATH
RF relay for splitting
K1
G6K-2F-RF-T-TR03_DC5
RF relay for input Z
K2
G6K-2F-RF-T-TR03_DC5
RF relay for attenuator
K3
G6K-2F-RF-T-TR03_DC5
RF relay driver
for splitting
RF relay driver
for input Z
RF relay driver
for attenuator
SPLIT_CONTROL
50_1M_CONTROL
ATT_CONTROL
5V USB for front panel
J15

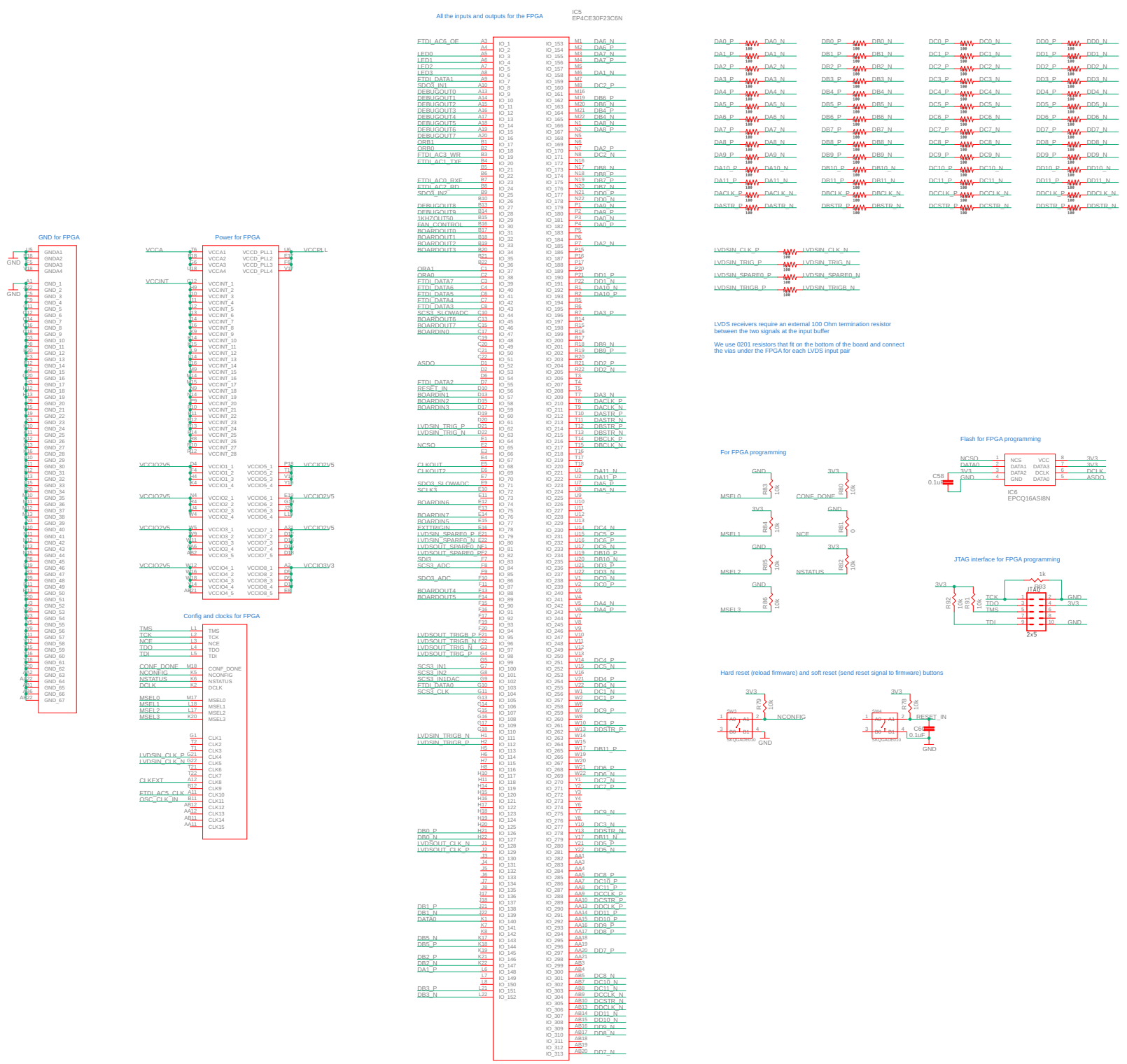

Termination was 357 in datasheet
but 220 found to be better
50 Ohm input
from previous sheet
OUTPATHMAIN
LMH5401IRMST
IC13
Single-ended to differential
amp with gain 4x
Buffered DAC output
for DC offset
OFFESETOUT1
LMH6401IRMZR
IC14
Variable gain amp
gain 0.5x to 20x
To ADC input B
SPI
Buffer with high bandwidth
FL1
OPA859IDSGR
FB and OUT
are connected
internally for
lowest input C
Buffered DAC output
-1.25 to 1.25V
IC15
SN74AVC4T774PWR
SPI to/from FPGA
Level shifter for SPI
Amp <-> FPGA
2.5V <-> 3.3V
IC18
TLV9102IPWR
Subtract 2.5V/2 from DAC out
2V5DACOUT
2.5V ref voltage
from DAC, also
used on sheet 4
for channel 2
DAC output
0 to 2.5V
IC17
DAC8562SDGSR
SPI from FPGA
DACOUT2
DAC output 2
is used on sheet 4
for channel 2

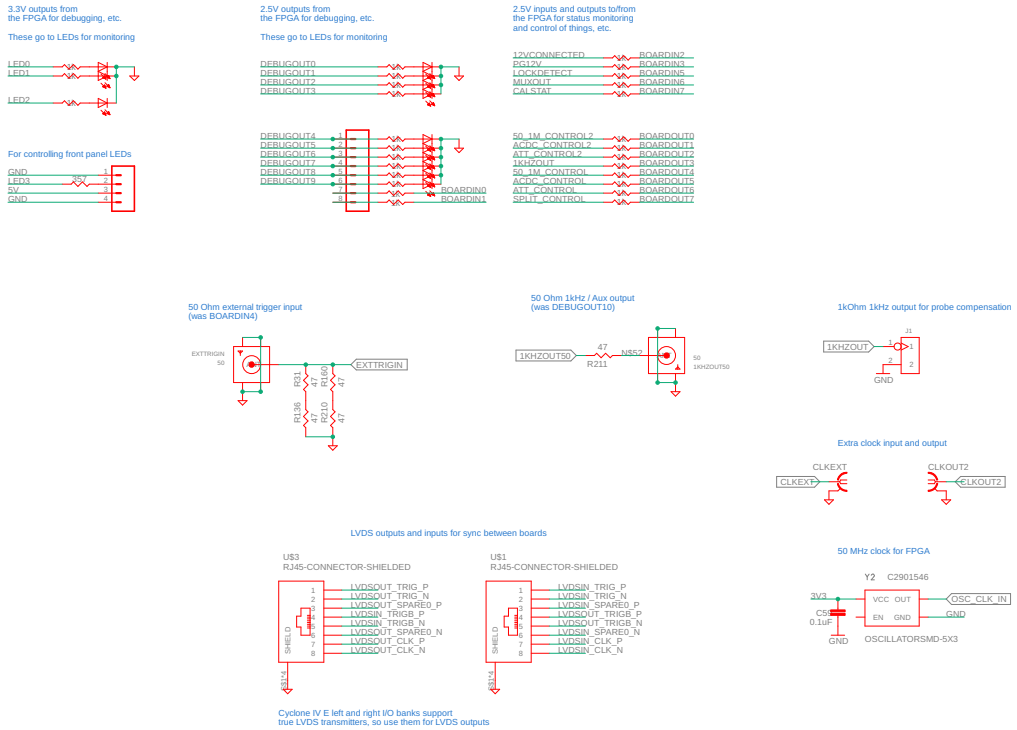

2V5+
2V5-2
FL2
OPA859IDSGR
1MPATH2
1MPATH502
Nearly identical to preinput for channel 1, except there's no split out
See comments on sheet 1 for details
RF relay for input Z
K4
G6K-2F-RF-T-TR03_DC5
BNCIN1
INPATH2
50_1M_CONTROL2
COIL1-2
Chebyshev Lowpass Filter
1.4 GHz
5th-7th order
50 Ohm
0.5dB ripple
FILTIN2_16
FILTOUT2_16
6.8nH
L16
L17
RF relay for attenuator
K5
G6K-2F-RF-T-TR03_DC5
OUTPATH2_3
FILTIN2_16_2
FILTOUT2_16
FILTIN2_8_4
FILTOUT2_8
OUTPATHFILT2
Chebyshev Lowpass Filter
0.7 GHz
5th-7th order
50 Ohm
0.5dB ripple
FILTIN2_8
15nH
L18
L19
ATT_CONTROL2
COIL2-2
ACDC_CONTROL2
AC/DC coupling
TLP3475_TP,F
K6
To input amps on next sheet
OUTPATHMAIN2
5V USB for front panel
J2
VCC
D-
D+
GND
SHELL
USB Type A

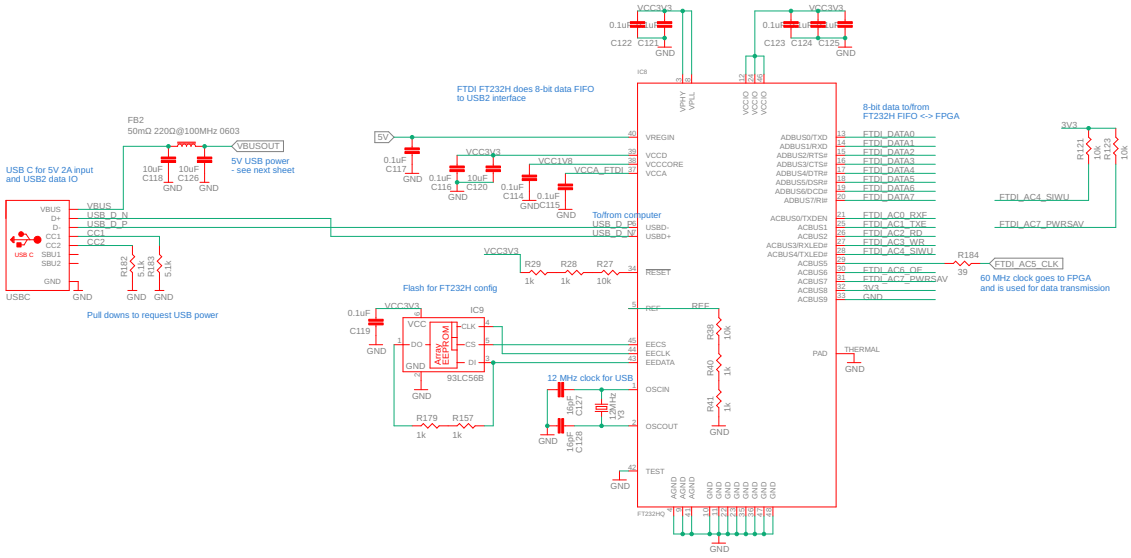

50 Ohm input
from previous sheet
OUTPATHMAIN2
AOFFSET2
OFFSETOUT2
LMH5401IRMST
IC21
AOUTSMA2_N
AOUTSMA2_P
LMH6401IRMZR
IC29
To ADC input A
Note that we have to switch
P and N so we don't need vias...
just invert ADC A result
INA_P
INA_N
FL4
OPA859IDSGR
DACAMPOUT2
Nearly identical to input amps for channel 1
See comments on sheet 2 for details
IC30
SN74AVC4T774PWR
IC33
TLV9102IPWR
DACOUT2
1V25OUT2
2V5DACOUT
DAC is on sheet 2
We use DAC output 2
for this channel, and
also the 2.5V ref voltage

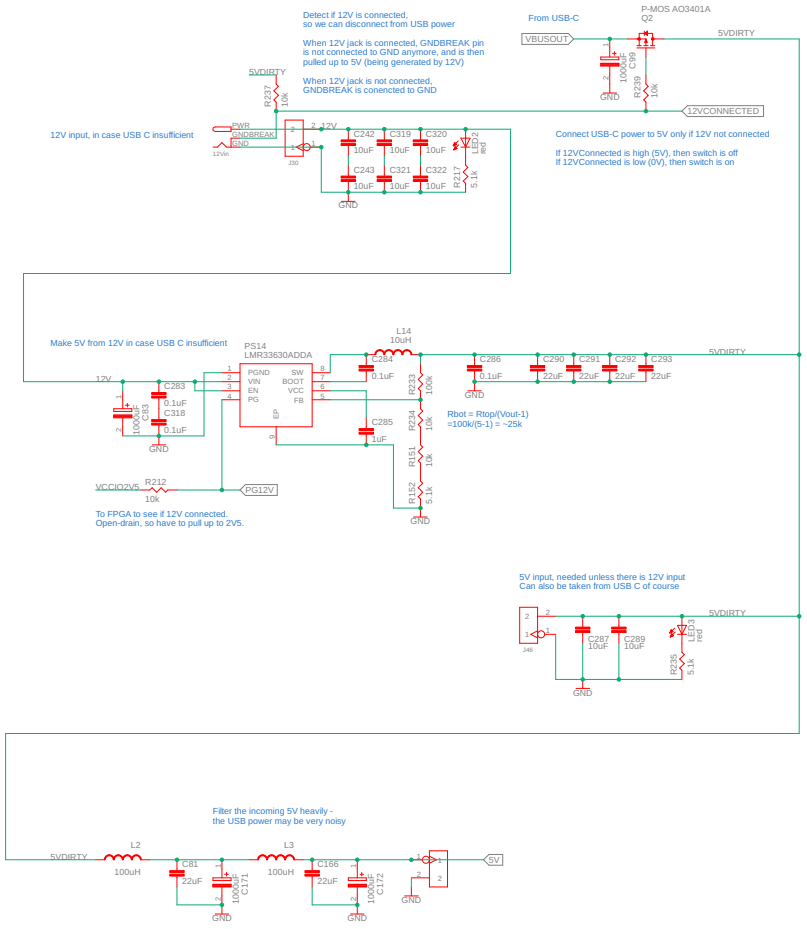

CLKOUT
50 MHz input clock from FPGA
REF_CLK
Status outputs to FPGA
MUXOUT
LOCKDETECT
3V3
GND
SPI from FPGA
SCLK3
SDI3
SCS3_CLK
ADECE
CPOUT
U2G$1
ADF4350BCPZ
CLK
DATA
LE
CE
SW
VP
CPGND
SDVDD
SDGND
MUXOUT
REFIN
DVDD
DGND
PDBRF
LD
VREF
VCOM
RSET
AGNDVCO
VTUNE
TEMP
AGNDVCO
VVCO
AGND
AVDD
AGNDVCO
RFOUTA+
RFOUTA-
RFOUTB+
RFOUTB-
VVCO
VTUNE
GND pads for ADF4350
Unused output B
VOUT
REFOUTA_N
REFOUTA_P
CLK_P
CLK_N
1.6 GHz differential output clock to ADC
Filter for PLL bandwidth

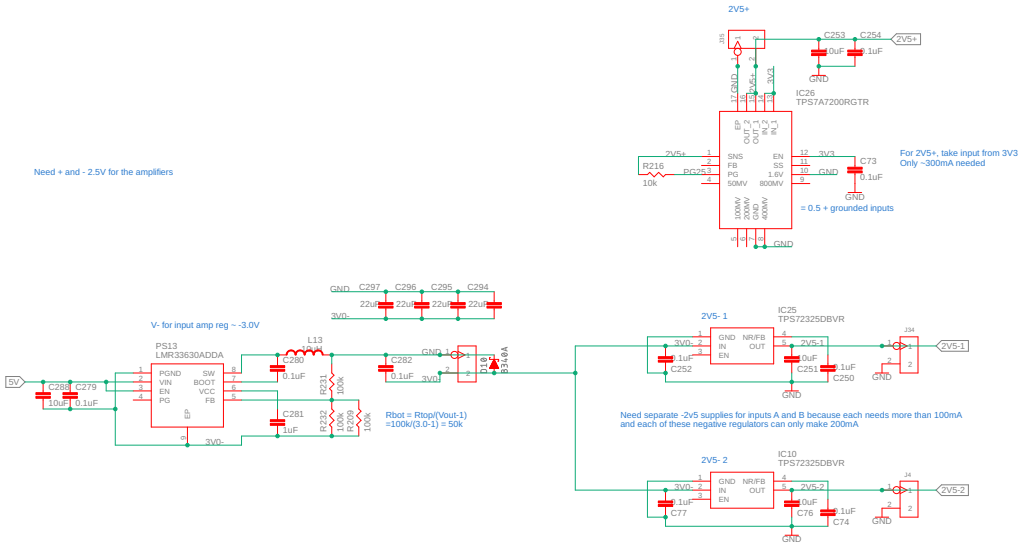

GND for the main ADC
High-speed IO connections to the main ADC
IC1
ADC12DL2500ACF
Power for the main ADC
Low-speed IO connections to the main ADC
For ADC temperature measurement on page 15
Tie powerdown to GND so ADC is turned on
These get input to the FPGA
Level shifter for SPI ADC <-> FPGA 1.9V <-> 3.3V
IC2
SN74AVC4T774PWR
SPI to/from shifter
SPI to/from ADC
ADC eval board terminates the SPI from the ADC with 100 Ohm before level shifting

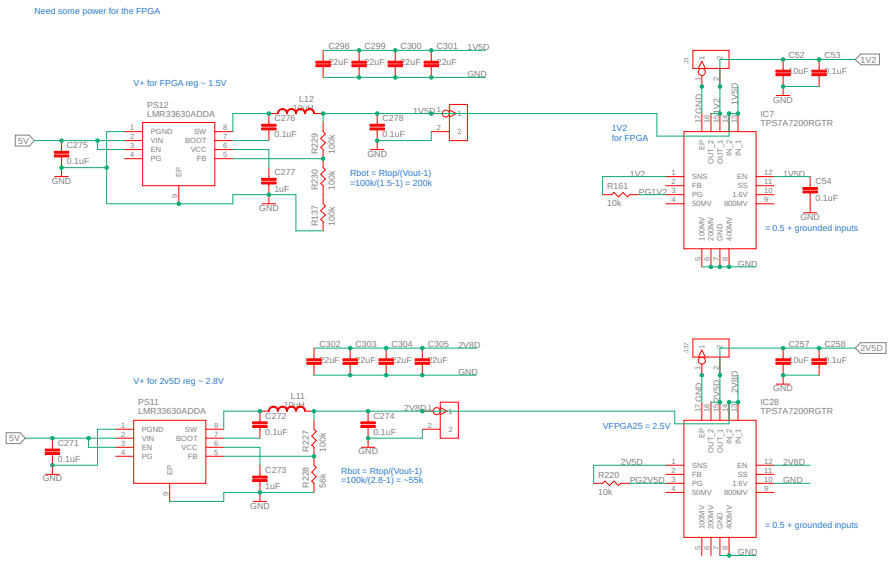

All the inputs and outputs for the FPGA
IC5
EP4CE30F23C6N
GND for FPGA
Power for FPGA
Config and clocks for FPGA
LVDS receivers require an external 100 Ohm termination resistor between the two signals at the input buffer
We use 0201 resistors that fit on the bottom of the board and connect the vias under the FPGA for each LVDS input pair
For FPGA programming
Flash for FPGA programming
IC6
EPCQ16ASI8N
JTAG interface for FPGA programming
Hard reset (reload firmware) and soft reset (send reset signal to firmware) buttons
NCONFIG
RESET_IN

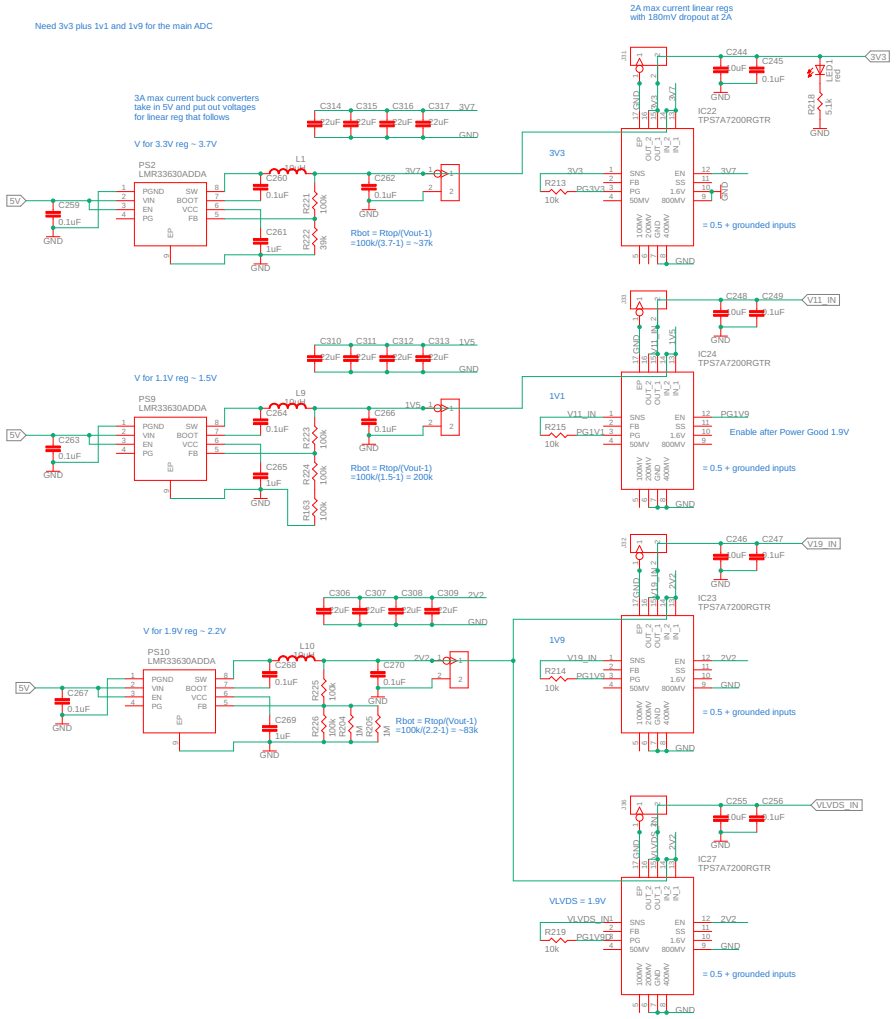

3.3V outputs from
the FPGA for debugging, etc.
These go to LEDs for monitoring
LED0
LED1
LED2
For controlling front panel LEDs
GND
LED3
5V
GND
JS7
2.5V outputs from
the FPGA for debugging, etc.
These go to LEDs for monitoring
DEBUGOUT0
DEBUGOUT1
DEBUGOUT2
DEBUGOUT3
DEBUGOUT4
DEBUGOUT5
DEBUGOUT6
DEBUGOUT7
DEBUGOUT8
DEBUGOUT9
BOARDIN0
BOARDIN1
2.5V inputs and outputs to/from
the FPGA for status monitoring
and control of things, etc.
12VCONNECTED
PG12V
LOCKDETECT
MUXOUT
CAL STAT
BOARDIN2
BOARDIN3
BOARDIN5
BOARDIN6
BOARDIN7
50_1M_CONTROL2
ACDC_CONTROL2
ATT_CONTROL2
1KHZOUT
50_1M_CONTROL
ACDC_CONTROL
ATT_CONTROL
SPLIT_CONTROL
BOARDOUT0
BOARDOUT1
BOARDOUT2
BOARDOUT3
BOARDOUT4
BOARDOUT5
BOARDOUT6
BOARDOUT7
50 Ohm external trigger input
(was BOARDIN4)
EXTTRIGIN
50
R91
47
R105
47
R106
47
R210
47
EXTTRIGIN
50 Ohm 1kHz / Aux output
(was DEBUGOUT10)
1KHZOUT50
47
R211
NS52
50
1KHZOUT50
1kOhm 1kHz output for probe compensation
1KHZOUT
J1
GND
Extra clock input and output
CLKEXT
CLKEXT
CLKOUT2
CLKOUT2
LVDS outputs and inputs for sync between boards
U$3
RJ45-CONNECTOR-SHIELDED
SHIELD
GND
LVDSOUT_TRIG_P
LVDSOUT_TRIG_N
LVDSOUT_SPARE0_P
LVDSIN_TRIGB_P
LVDSIN_TRIGB_N
LVDSOUT_SPARE0_N
LVDSOUT_CLK_P
LVDSOUT_CLK_N
U$1
RJ45-CONNECTOR-SHIELDED
SHIELD
GND
LVDSIN_TRIG_P
LVDSIN_TRIG_N
LVDSIN_SPARE0_P
LVDSOUT_TRIGB_P
LVDSOUT_TRIGB_N
LVDSIN_SPARE0_N
LVDSIN_CLK_P
LVDSIN_CLK_N
Cyclone IV E left and right I/O banks support
true LVDS transmitters, so use them for LVDS outputs
50 MHz clock for FPGA
Y2
C2901546
3V3
C5
0.1uF
GND
VCC
OUT
EN
GND
OSC_CLK_IN
GND
OSCILLATORSMD-5X3

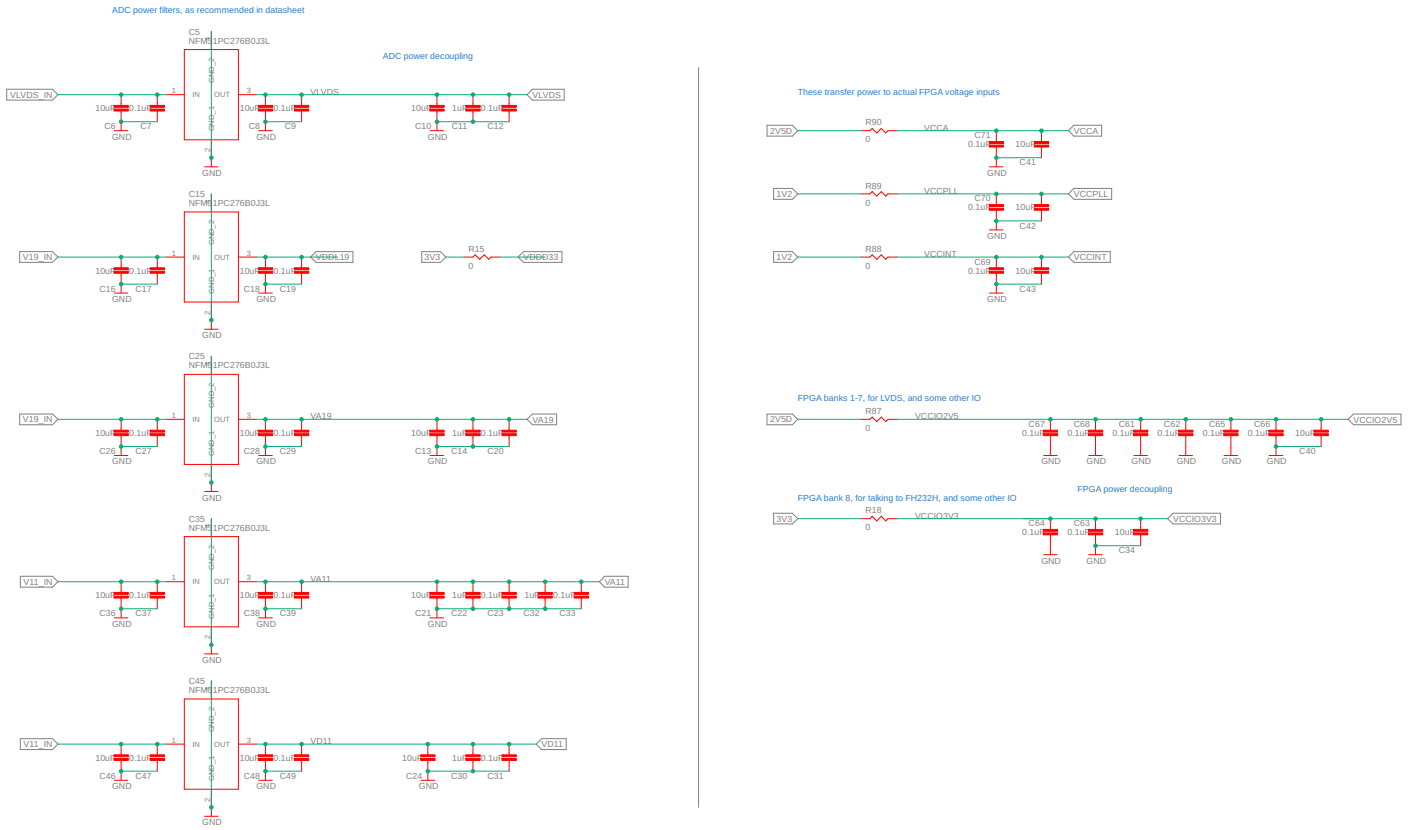

FTDI FT232H does 8-bit data FIFO to USB2 interface
8-bit data to/from FT232H FIFO <-> FPGA
USB C for 5V 2A input and USB2 data IO
5V USB power - see next sheet
To/from computer
Flash for FT232H config
12 MHz clock for USB
60 MHz clock goes to FPGA and is used for data transmission
Pull downs to request USB power
FTDI_AC4_SIWU
FTDI_AC7_PWRSAV
FTDI_AC5_CLK

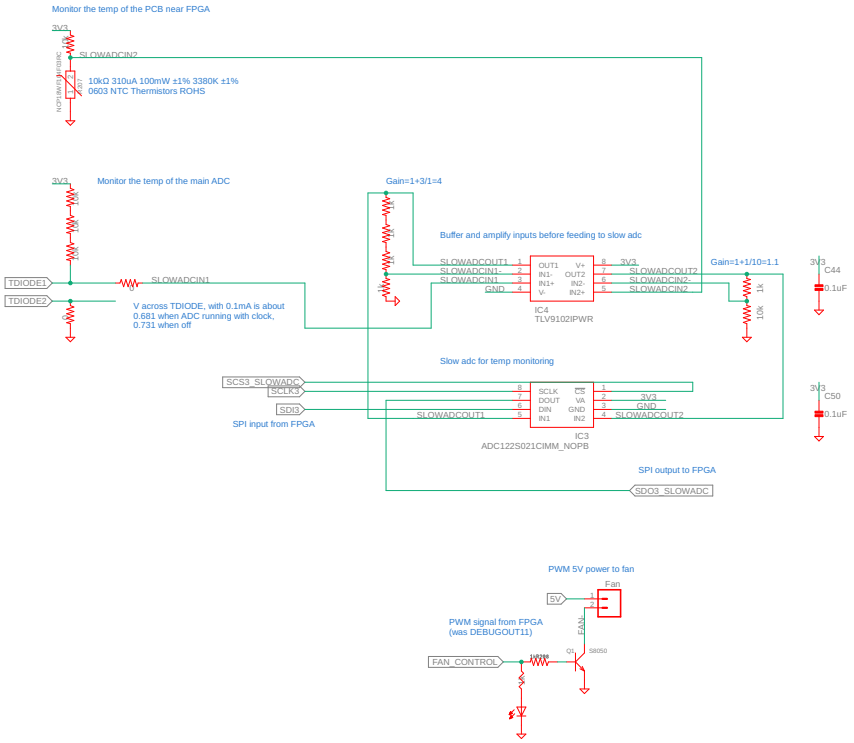

Detect if 12V is connected,
so we can disconnect from USB power
When 12V jack is connected, GNDBREAK pin
is not connected to GND anymore, and is then
pulled up to 5V (being generated by 12V)
When 12V jack is not connected,
GNDBREAK is conencted to GND
From USB-C
P-MOS AO3401A
Q2
VBUSOUT
5VDIRTY
R237
10k
12VCONNECTED
12V input, in case USB C insufficient
Connect USB-C power to 5V only if 12V not connected
If 12VConnected is high (5V), then switch is off
If 12VConnected is low (0V), then switch is on
Make 5V from 12V in case USB C insufficient
PS14
LMR33630ADDA
L14
10uH
12V
PGND
VIN
EN
PG
SW
BOOT
VCC
FB
EP
Rbot = Rtop/(Vout-1)
=100k/(5-1) = ~25k
VCCIO2V5
R212
10k
PG12V
To FPGA to see if 12V connected.
Open-drain, so have to pull up to 2V5.
5V input, needed unless there is 12V input
Can also be taken from USB C of course
Filter the incoming 5V heavily -
the USB power may be very noisy
L2
100uH
L3
100uH
5V
GND


2V5+
C253
C254
2V5+
10uF
0.1uF
GND
IC26
TPS7A7200RGTR
Need + and - 2.5V for the amplifiers
R216
10k
2V5+
3V3
C73
0.1uF
GND
For 2V5+, take input from 3V3
Only ~300mA needed
= 0.5 + grounded inputs
GND
C297
C296
C295
C294
22uF
22uF
22uF
22uF
3V0-
V- for input amp reg ~ -3.0V
PS13
LMR33630ADDA
L13
10uH
C280
0.1uF
C282
0.1uF
GND
3V0-
D15
SS16A
5V
C288
C279
10uF
0.1uF
C281
1uF
R231
100k
R232
100k
R209
100k
Rbot = Rtop/(Vout-1)
=100k/(3.0-1) = 50k
2V5- 1
IC25
TPS72325DBVR
3V0-
2V5-1
C252
0.1uF
C251
10uF
C250
0.1uF
GND
J34
2V5-1
Need separate -2v5 supplies for inputs A and B because each needs more than 100mA
and each of these negative regulators can only make 200mA
2V5- 2
IC10
TPS72325DBVR
3V0-
2V5-2
C77
0.1uF
C76
10uF
C74
0.1uF
GND
J4
2V5-2


Need some power for the FPGA
V+ for FPGA reg ~ 1.5V
PS12
LMR33630ADDA
L12
1uH
C275
0.1uF
C276
0.1uF
C277
1uF
C278
0.1uF
R229
100k
R230
100k
R137
100k
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
1V2
for FPGA
IC7
TPS7A7200RGTR
R161
10k
PG1V2
C54
0.1uF
= 0.5 + grounded inputs
V+ for 2v5D reg ~ 2.8V
PS11
LMR33630ADDA
L11
1uH
C271
0.1uF
C272
0.1uF
C273
1uF
C274
0.1uF
R227
100k
R228
56k
Rbot = Rtop/(Vout-1)
=100k/(2.8-1) = ~55k
VFPGA25 = 2.5V
IC28
TPS7A7200RGTR
R220
10k
PG2V5D
= 0.5 + grounded inputs


Need 3v3 plus 1v1 and 1v9 for the main ADC
2A max current linear regs
with 180mV dropout at 2A
3A max current buck converters
take in 5V and put out voltages
for linear reg that follows
V for 3.3V reg ~ 3.7V
PS2
LMR33630ADDA
L1
2.2uH
C260
0.1uF
C262
0.1uF
C259
0.1uF
C261
1uF
R221
100k
R222
39k
Rbot = Rtop/(Vout-1)
=100k/(3.7-1) = ~37k
C314
C315
C316
C317
2uF
3V7
5V
GND
3V3
R213
10k
PG3V3
IC22
TPS7A7200RGTR
C244
C245
0uF
0.1uF
R218
5.1k
LED1
red
= 0.5 + grounded inputs
V for 1.1V reg ~ 1.5V
PS9
LMR33630ADDA
L9
2.2uH
C264
0.1uF
C266
0.1uF
C263
0.1uF
C265
1uF
R223
100k
R224
100k
R183
100k
Rbot = Rtop/(Vout-1)
=100k/(1.5-1) = 200k
C310
C311
C312
C313
1V5
1V1
V11_IN
R215
10k
PG1V1
IC24
TPS7A7200RGTR
C248
C249
0uF
0.1uF
PG1V9
Enable after Power Good 1.9V
V for 1.9V reg ~ 2.2V
PS10
LMR33630ADDA
L10
2.2uH
C268
0.1uF
C270
0.1uF
C267
0.1uF
C269
1uF
R225
100k
R226
100k
R204
1M
R205
1M
Rbot = Rtop/(Vout-1)
=100k/(2.2-1) = ~83k
C306
C307
C308
C309
2V2
1V9
V19_IN
R214
10k
PG1V9
IC23
TPS7A7200RGTR
C246
C247
0uF
0.1uF
VLVDS = 1.9V
VLVDS_IN1
R219
10k
PG1V9
IC27
TPS7A7200RGTR
C255
C256
0uF
0.1uF
VLVDS_IN


ADC power filters, as recommended in datasheet
ADC power decoupling
C5
NFM61PC276B0J3L
VLVDS_IN
VLVDS
C15
NFM61PC276B0J3L
V19_IN
VDDL19
3V3
R15
0
VDDD33
C25
NFM61PC276B0J3L
V19_IN
VA19
C35
NFM61PC276B0J3L
V11_IN
VA11
C45
NFM61PC276B0J3L
V11_IN
VD11
GND
These transfer power to actual FPGA voltage inputs
2V5D
R90
0
VCCA
C71
0.1uF
10uF
C41
1V2
R89
0
VCCPLL
C70
0.1uF
10uF
C42
1V2
R88
0
VCCINT
C69
0.1uF
10uF
C43
FPGA banks 1-7, for LVDS, and some other IO
2V5D
R87
0
VCCIO2V5
C67
C68
C61
C62
C65
C66
0.1uF
10uF
C40
FPGA bank 8, for talking to FH232H, and some other IO
FPGA power decoupling
3V3
R18
0
VCCIO3V3
C64
C63
0.1uF
10uF
C34


Monitor the temp of the PCB near FPGA
3V3
SLOWADCIN2
10kΩ 310uA 100mW ±1% 3380K ±1%
0603 NTC Thermistors ROHS
Monitor the temp of the main ADC
Gain=1+3/1=4
Buffer and amplify inputs before feeding to slow adc
Gain=1+1/10=1.1
SLOWADCOUT1
SLOWADCIN1-
SLOWADCIN1
GND
SLOWADCOUT2
SLOWADCIN2-
SLOWADCIN2
IC4
TLV9102IPWR
C44
0.1uF
TDIODE1
TDIODE2
SLOWADCIN1
V across TDIODE, with 0.1mA is about
0.681 when ADC running with clock,
0.731 when off
Slow adc for temp monitoring
SCS3_SLOWADC
SCLK3
SDI3
SPI input from FPGA
SCLK
DOUT
DIN
IN1
CS
VA
GND
IN2
IC3
ADC122S021CIMM_NOPB
C50
SPI output to FPGA
SDO3_SLOWADC
PWM 5V power to fan
5V
Fan
PWM signal from FPGA
(was DEBUGOUT11)
FAN_CONTROL
FAN
Q1
S8050

Some extra things to put on
the board for testing only

Not connected to the rest of the system!