

**2021-2022 SPRING SEMESTER  
EE464 Hardware Project**

**Final Report**

**POWER CONVERTERS**

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An isolated DC-DC converter was designed under the following project specifications. In this project, switch-mode power supplies have isolated output; in other words, the input and output grounds are totally separated. In the topology selection section, why we chose the flyback converter quasi-resonant design and why we did not select other topologies will be explained in detail. Also, the required analytical calculations and simulations are given in this report. Moreover, the controller, winding, magnetic, PCB, box designs, and which components we used in this converter are clearly stated. In addition, the project's test results are clearly laid out. Furthermore, the cost analysis of the project is added to this report.

### **Project Specifications :**

Minimum Input Voltage: 24 V

Maximum Input Voltage: 48 V

Output Voltage: 15 V

Output Power: 45 W

Output Voltage Peak-to-Peak Ripple : 3%

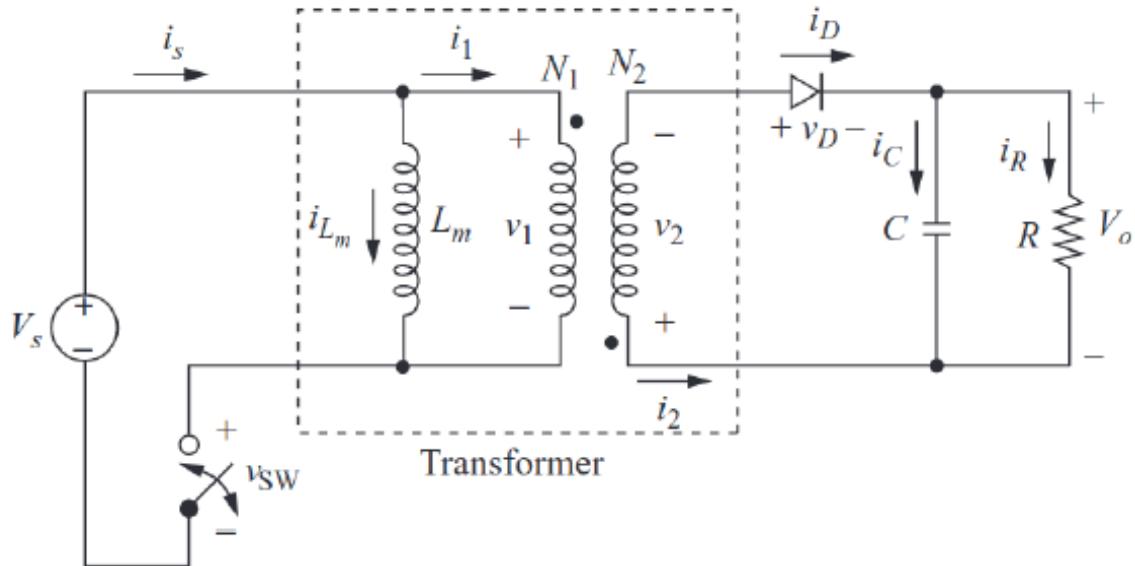
Line Regulation (Deviation of percent output voltage when the input voltage is changed from its minimum to maximum or vice versa) : 3%

Load Regulation (Deviation of percent output voltage when the load current is changed from 10% to 100% or vice versa) : 3%

### **Topology Selection**

There are three main topologies we have considered for this project. These are

a) **Flyback Converter Topology :**



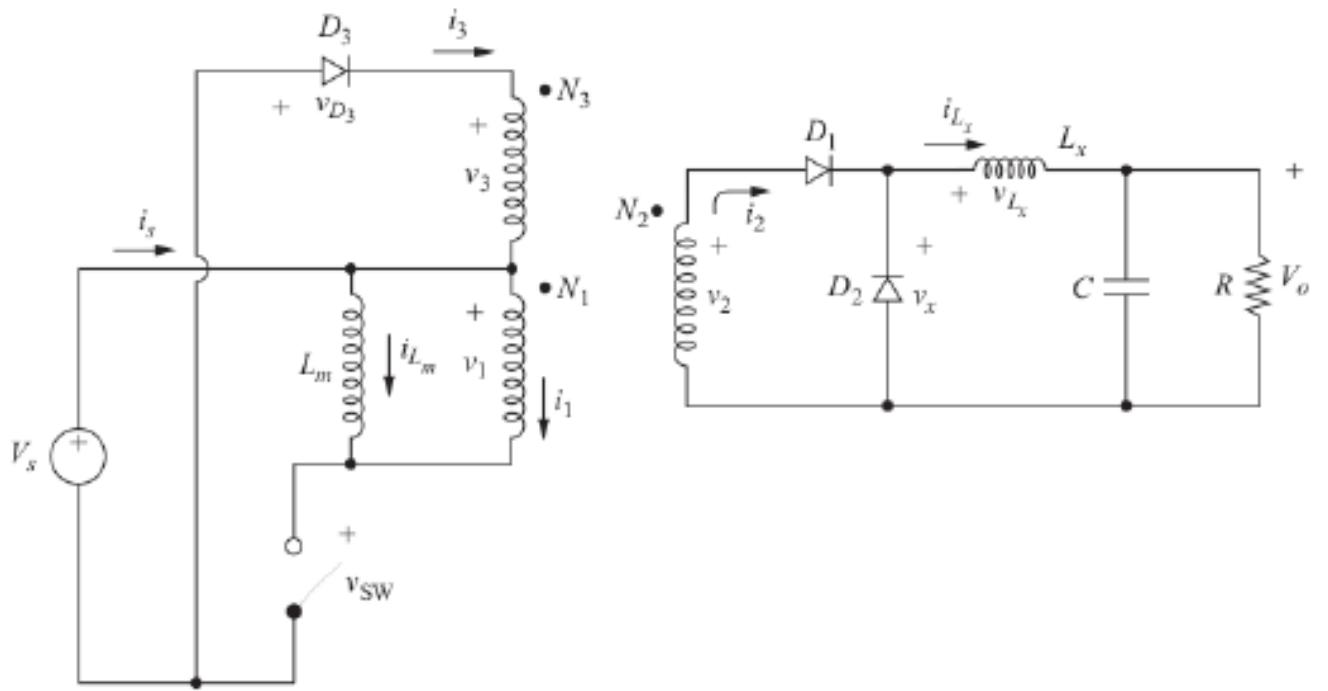
**Figure-1 : Flyback Converter with Transformer (1)**

As shown in Figure-1, there is no need to use output inductance. In this topology, the energy is stored in the transformer. So, this converter is implemented simply. Thanks to fewer components, it is cheap according to other topologies. Moreover, it can be controlled more easily as it will be a single switch.

The flyback converter operating in DCM mode helps us to limit flux density. So, the smaller core can be used. Also, there is no need to do a hard switching, thanks to zero current. Therefore the switching loss on diodes and the switch is getting smaller.

On the other hand, the oscillating output current exists. Also, the air-gapped transformer is needed.

b) **Forward Converter Topology :**

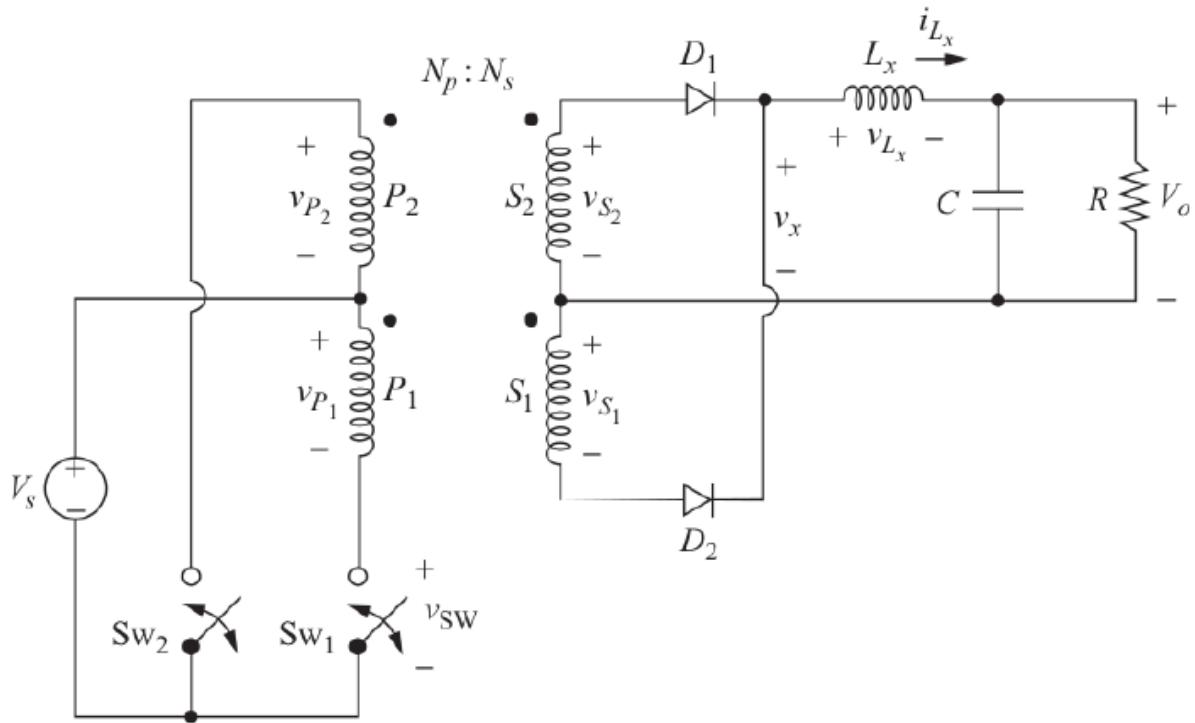


**Figure-2 : Practical Forward Converter (2)**

The topology given in Figure-2 has better utilization of the transformer. The energy is transferred whenever there is some current in the primary winding. Instead of storing it in the transformer first, the energy can be sent directly over to the load. Also, a gapless core can be used. Moreover, the output inductor and diode ensures continuous output current. So, the capacitor size can be reduced.

Although the forward converter has advantages over flyback, the cost is high because of the extra diode, inductor, and extra winding. Furthermore, the MOSFET requires a higher voltage. Whenever the switch is ON and OFF, the turn ratios N1, N2, and N3 will put some stress on the voltage.

c) **Push Pull Converter Topology :**



**Figure-3 : Push-Pull Converter (3)**

In the topology given in Figure-2, a center-tapped topology is used; in other words, there are two independent windings on primary and secondary, but they are electrically connected. Also, the waveforms are repeated for every  $T_s/2$ . This helps us to reduce the current ripples compared to other converters. It is as if the switching frequency is doubled. The most significant advantage of the push-pull converter is better utilizing the magnetic core. It can be seen from the B-H characteristics. Therefore, a smaller magnetic component can be used to transfer the same amount of energy.

On the other hand, because of the existence of two switches, it can be harder to control than other topologies mentioned above. For instance, there are restrictions such as not being able to turn two keys ON at the same time. Since an extra switch will be used, it will be a problem in terms of budget.

As stated above, when we examined the pros and cons of all topologies in detail as a power converters team, we chose flyback converter topology. When we looked at the project specifications mentioned in the introduction, as a team, we decided that the flyback converter was the most suitable topology for our project since the output power requirement is lower than 100 W. While making our decision, we considered fewer circuit elements, the magnetic design is more straightforward, and it is the most advantageous topology in terms of budget.

## **Operating Mode :**

Flyback has two different working conditions: Discontinuous Conduction Mode and Continuous Conduction Mode.

“Continuous-conduction-mode (CCM) means that the current in the energy transfer inductor or transformer never goes to zero between switching cycles. In discontinuous-conduction-mode (DCM) the current goes to zero during part of the switching cycle. You can use both modes in flyback design, normally it is easily go to CCM at low line and heavy load and it likely goes to DCM at high line and light load.” (4)

### **“ DCM advantages**

- Primary inductance lower comparing to CCM
- Maximum duty cycle is set by inductance
- Smaller transformer possible comparing to CCM
- No rectifier reverse, recovery losses
- Minimum MOSFET switching losses
- No right half-plane zero in the control loop
- Optimal for low output power

### **DCM disadvantages**

- Higher primary peak current
- Higher peak rectifier current
- Increased capacitance at input and output
- Electromagnetic interference sensitivity
- Increased bandwidth variation “ (5)

The mode we decided to use as a group is **quasi-resonant**. This means our flyback converter is exactly on the DCM and CCM boundary. In this way, the efficiency will be increased.

A quasi resonant flyback will operate in DCM at light load and approach transition mode at a very heavy load.

### **Advantages of Quasi-Resonant Flyback Converter Compared to a Flyback Converter:**

- It will offer lower switching losses comparing to CCM and DCM, especially when switching on the lowest points
- Since it can switch on the lowest points, it behaves in partial resonance, and with this, EMI will be better
- Parasitic elements will perform partial resonance action. Thus no more added parts count.
- It can handle multiple outputs at same time
- Broader input range
- It has a better response time
- Easier to compensate comparing to CCM and DCM

### **Drawbacks of Quasi-Resonant Flyback :**

- If it cannot turn on the lowest points, its advantage of having low switching losses will be compensated or surpassed by the effect of higher peak currents as it will operate in the DCM region.
- It may require a higher capacitance in the output operating in the DCM region.
- It is not usually recommended for applications of more than 100 Watts.

### **Analytical Calculations**

$$V_{in\_min} = 24 \text{ V} \& V_{in\_max} = 48 \text{ V} \& V_{out} = 15 \text{ V}$$
$$f_{sw} = 80 \text{ kHz}, \Delta V_o = 0.45, \eta = \%85, P_{out} = 45W$$

$$I_{pri\_peak} = 2 * P_{out}/(V_{min} * D_{max} * \eta), I_{pri\_peak} = 9.804 A$$

$$I_{pri\_rms} = I_{pri\_peak} * \sqrt{D_{max}/3}, I_{pri\_rms} = 3.69 A$$

### Inductance Calculation

$$L_{pri} = V_{in\_min} * (ton\_max)/(I_{pri\_peak}), L_{pri} = 12.4 \mu H,$$

### Capacitance Calculation

$$C = D_{max} * I_{out}/(f_{sw} * \Delta V_o), C = 35.41 \mu F$$

In order to decrease ripple as much as possible, three 100 capacitors connected parallel.

This calculation is done without the ESR value, which will be included later.

### Reflected Output and Turn Ratio Calculation

$$V_{or} = V_{in\_min} * \eta * D_{max}/(1 - D_{max}), V_{or} = 15.96 V$$

$$n = V_{or}/V_o = N_1/N_2 = 1.06,$$

### Core Selection

$$WaAc = P_{out}/(2 * f_{sw} * B_{max} * \eta * J_{max} * k_{cu})$$

Assume:  $B_{max} = 0.2 T, k_{cu\_min} = 0.3, J_{max} = 2A/mm^2$

$$WaAc = 1.95 [cm]^2$$

To avoid waiting for shipment and have an ease while wrapping the windings, the core named ETD 34/17/11 is chosen. It has a far higher WaAc value than the calculated value. However, core losses do not decrease our efficiency below the desired value of 90% (Not the one we get, unfortunately).

### Primary Turn

$$N_p = L_{pri} * (I_{pri\_peak})/(B_{max} * A_e), N_p \approx 9$$

### **Secondary Turn**

$$Ns = 9/n, Ns \approx 9,$$

### **Auxiliary Turn**

Also taken as 9 since each layer requires 9 windings. 5

### **Magnetizing Inductance**

$$Lm = Np^2 * Al = 12.05 \text{ mikroHenry}$$

### **Number of Parallel Cables**

$$Ipri_{rms} = 4.29$$

$$Isec_{rms} = 3.69$$

*awg 26 11 parallel cable winding for secondary side*

*awg 26 13 parallel cable winding for primary side*

The values are obtained by dividing RMS current values by the power transmission limits of AWG cables.

### **DC Resistance**

Calculated for  $Npri=Nsec=5$

$$R = Npri * L * R(\text{per mm})$$

$$L = 51.84 \text{ mm}$$

$$R = 347 \text{ mOhm}$$

$$Rpri = 43 \text{ mOhm}$$

for secondary side

$$R = Nsec * L * R(\text{per mm}) = 275.3 \text{ mOhm}$$

$$Rsec = 39.3 \text{ mOhm}$$

### **Recalculation for Bmax**

$$B = N * I/R * A = 0.1927 \text{ hence calculations are appropriate}$$

### **Input capacitor pri**

To get a better quality of DC input voltage, a DC link capacitor with  $2\mu\text{F}$  per watt is chosen.

$$Cin = 2\mu\text{F} * Pin, Cin = 100\mu\text{F}$$

### **Diode Calculations**

$$V_{D1_{peak}} = V_{out} + V_{IN,max} * n = 58.2 + \%40 \text{ safety} = 82 \text{ V}$$

The maximum reverse voltage of the diode is 82 V

Suppose the chosen diode causes too many losses. In that case, one has two options to reduce the diode loss by using SMPS with MOSFET to use a secondary side diode. The second way uses 2-3 parallel Schottky diodes with lower forward voltage. The reason is when a diode with 0.7 V forward voltage cause %5 of losses.

## MOSFET Calculation

$$V_{DS,max} = V_{IN,max} + (D_{MAX} * V_{IN,min}/(1 - D_{MAX})) = 64 + 20\% \text{ safety} = 76.8 V$$

## Snubber Circuit Design (8)

$$V_{C,max} = V_{DS,max} * 0.1 + (D_{MAX}/(1 - D_{MAX})) \times V_{IN,min} = 23.68 V$$

$$P_{R_{Snubber}} = I_{pri,peak} \times L_{leak} \times f_{sw}/2 = 0.999 W \text{ (0.8 for 60 kHz)}$$

$$R_{snubber} = V_{C,max}^2 / P_{R_{Snubber}} = 561.3 \Omega$$

Leakage inductance is calculated as %2 percent of primary inductance

The ripple of snubber capacitor taken as 10%

$$C_{snubber} = 1/(\Delta V_c * R_{snubber} * f_{sw}) = 223 nF$$

The voltage across the snubber diode;

$$V_{D_{snubber(peal)}} = 1.2 * V_{DS,max} = 92.16 V$$

## Core Loss

Core losses are calculated by using Kool Mu instructions; from there, one obtains the mW/cm<sup>3</sup> value by multiplying this value with our Volume value(5.8 cm<sup>3</sup>). It is close to 4 Watt at max

## Magnetic Design

The analytic calculations part gives turn ratio and winding number calculations.

Primary winding should be able to carry Mosfet RMS current = 3.602, A value found in simulation. Also, our winding cable must handle 70-80 kHz frequency. So we must use a 26 AWG cable with 107kHz Maximum frequency for 100% skin depth for solid conductor copper, but it has only 0.361 A current-carrying capacity. So we will combine  $3.602/0.361 = 9.98$ , 11 of those cables in parallel to achieve desired current carrying capacity (with safety margin). Similarly, Rms diode current = 4.331 A, so we will need  $4.331/0.361 = 12.0$ , 13 of those cables in parallel to achieve desired current carrying capacity in secondary.

Similarly, we can calculate copper resistance from that. We will have seven windings for both primary and secondary. Circumference of the core carcass is  $15.1(\text{diameter})\pi = 47.44$  mm. With nine windings, this makes 0.427 m. We can take these values as 0.7m taking non-idealities (such as spiraling windings, the circumference of windings being larger than carcass) into account. 26 AWG cables have a resistance of 133.8568 ohm/km. The primary resistance is  $133.8568 \times 0.0007/11 = 8.518 \times 10^{-3}$ , and the secondary resistance is  $133.8568 \times 0.0007/13 = 7.209 \times 10^{-3}$ .

The Max RMS Mosfet current = 3.602 A

The Max RMS Diode current = 4.331 A

So primary DC losses =  $3.602^2 \times 8.518 \times 10^{-3} = 0.111$  W

and secondary DC losses =  $4.331^2 \times 7.209 \times 10^{-3} = 0.135$  W

Although the maximum frequency for 100% skin depth is 107 kHz, which is higher than our switching frequency, a skin effect still increases AC resistance. Also, there is a proximity effect that increases AC resistance. We tried to reduce the proximity effect by spiraling cables using the drill. Our windings are not perfect.

So I will take AC resistances as 3 times DC resistances as an estimate.

So total copper losses =  $0.246 \times 3 = 0.738$  W

We also connected windings as interleaved to reduce leakage inductance. We measured around %10 leakage inductance without interleaved windings and around %5 with interleaved windings.

We tested the inductance values of our transformer. Our transformer has an AL of 2550nL/N<sup>2</sup>, and we have nine turns. So our total inductance without papers between cores is 206.55 uH, but we have used papers to reduce inductance to our first calculated value of 12uF. We used 4 papers to reach 12 uF. The papers affected the inductance more than we

predicted because, from the datasheet, our AL value for a 1mm core gap is 153 nH/N<sup>2</sup>, so inductance is 12.4 uF. But we reached 12.4 uF using four sheets of paper, and the thickness of 1 sheet of paper is 0.1 mm. We think this is caused by papers leaving a gap in both sides of the transformer, thus increasing inductance more than just leaving the core in the middle.

But we observed best load regulation and efficiency at 1 paper thick core efficiency values and output voltage was reduced with each added paper sheet. With 0 paper thick gap our inductance is 206.5 uH so our core saturates. So one paper thickness is adequate for our situation. We think we made a mistake while designing the transformer, and our inductance value is not enough.

We had a problem while designing a transformer for a quasi-resonant converter. In comparison, formulas for DCM and CCM converters are straightforward. But we do not precisely know how to calculate transformer inductance for quasi-resonant converters. If we use the maximum inductance calculation formula given in the formula for the DCM converter with our specifications

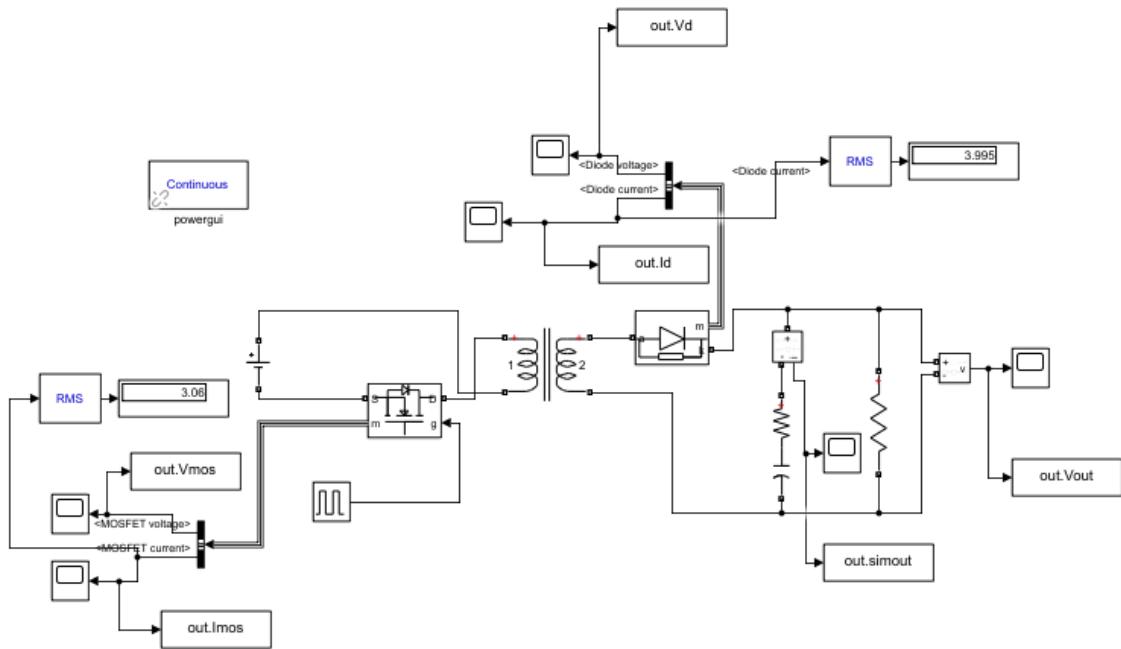
$$L_P = \frac{\eta \times D_{MAX^2} \times V_{IN\_MAX^2}}{2 \times f_{SW} \times K_{FR} \times P_O}$$

Lp = 64 uF.

This is also min inductance value calculation for CCM converter.

Our inductance value for the transformer with one paper thick (A4) gap should be close to this value. If we had more time, we were planning to rethink transformer core calculations and remake our core using different cores. We should have chosen inductance value closer to that range and should have chosen core according to that.

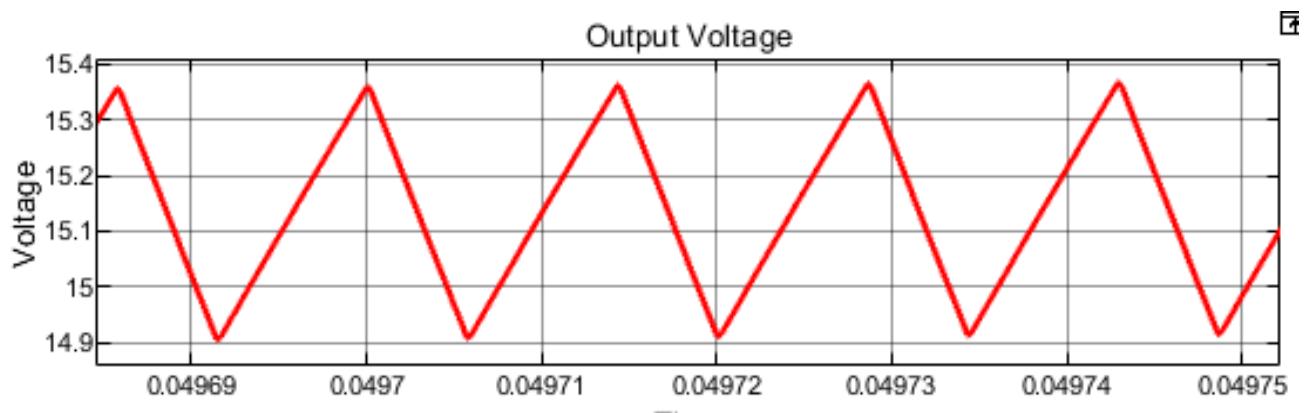
## Simulations



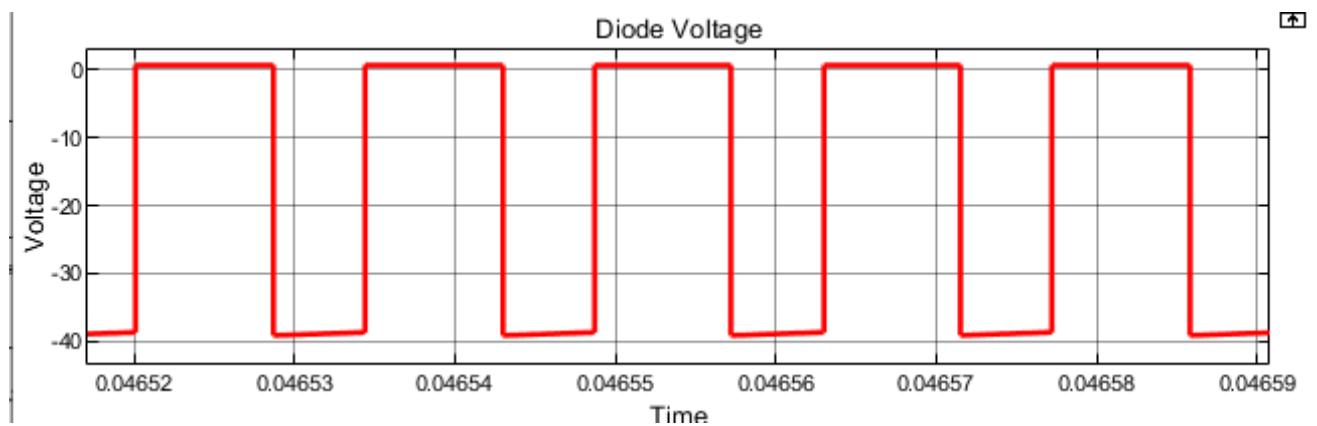
**Figure-4:** Simulation Schematic with Non-Idealities

Simulation schematic for flyback converter. We did not add simulation results for our entire circuit because we could not find a model for our controller (L6565).

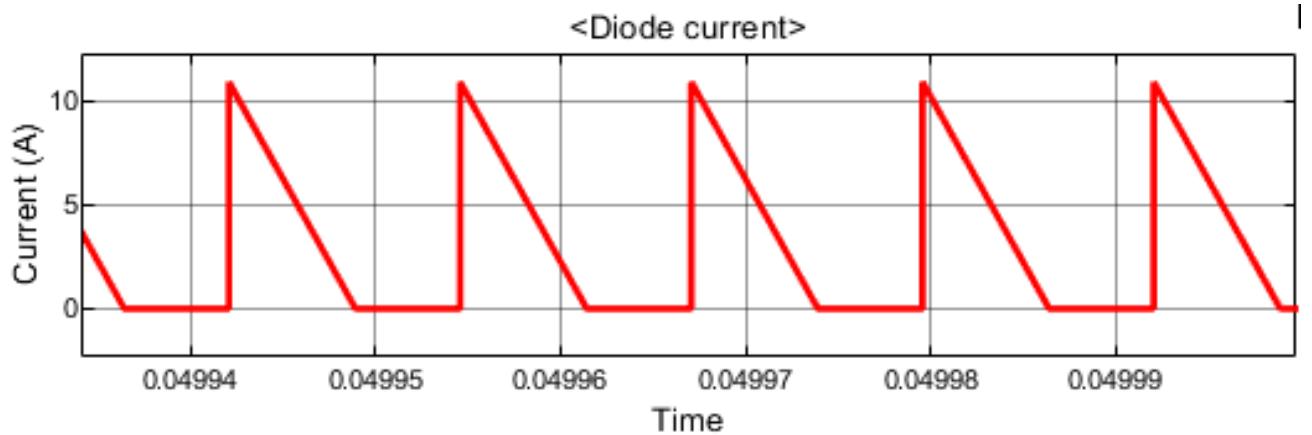
**Simulation results for 24 V input are as follows :**



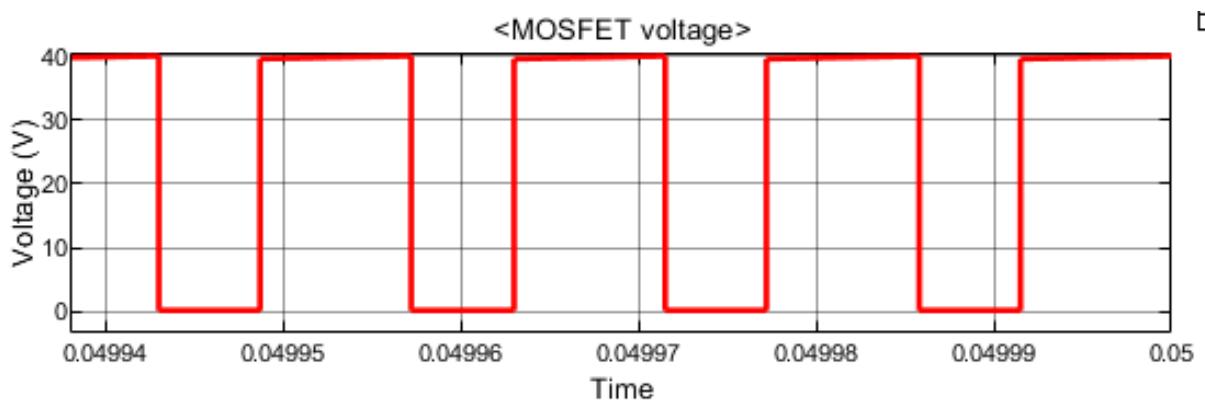
**Figure-5 : Output Voltage Graph for 24V Input**



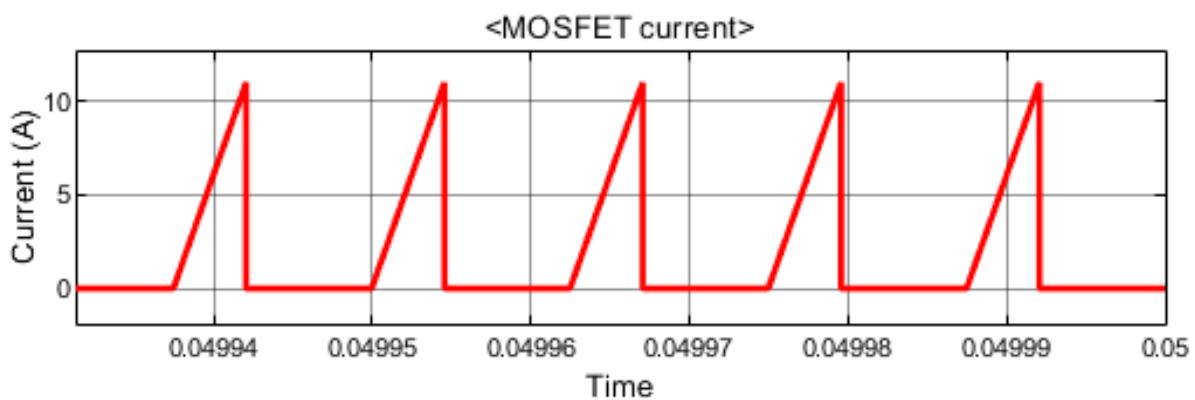
**Figure-6** : Diode Voltage Graph for 24V Input



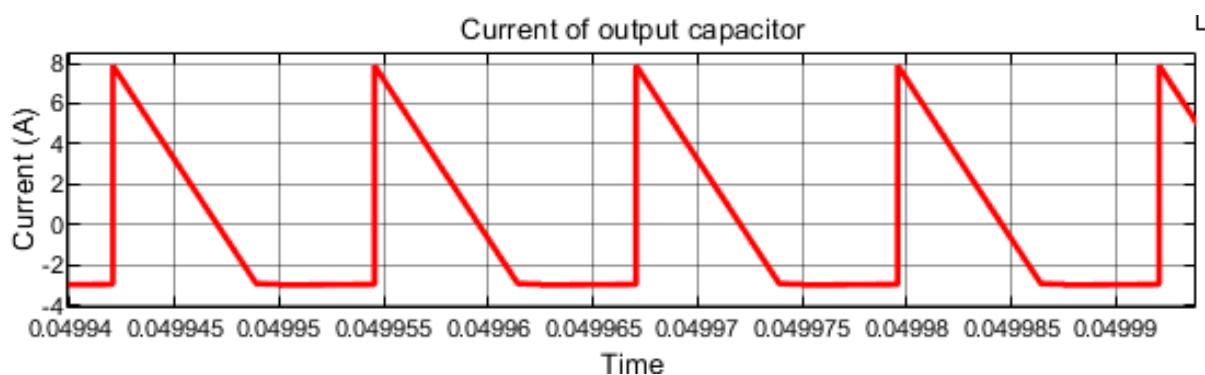
**Figure-7** : Diode Current Graph for 24V Input



**Figure-8** : Mosfet Voltage Graph for 24V Input

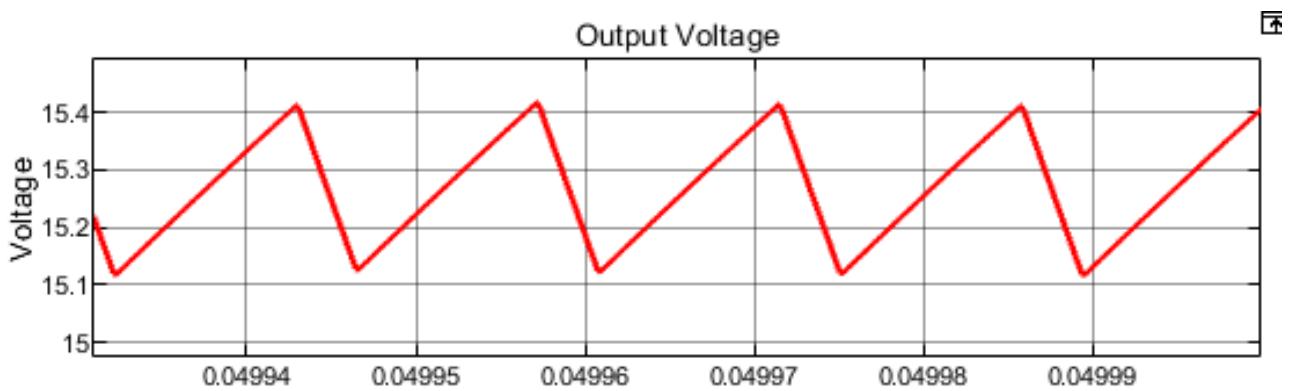


**Figure-9 : Mosfet Current Graph for 24V Input**

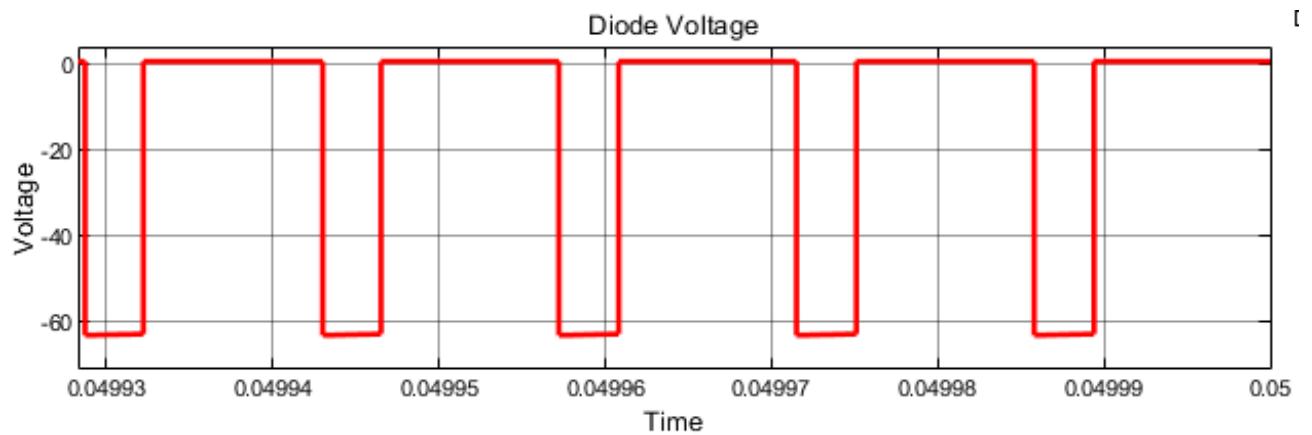


**Figure-10 : Output Capacitor Current Graph for 24V Input**

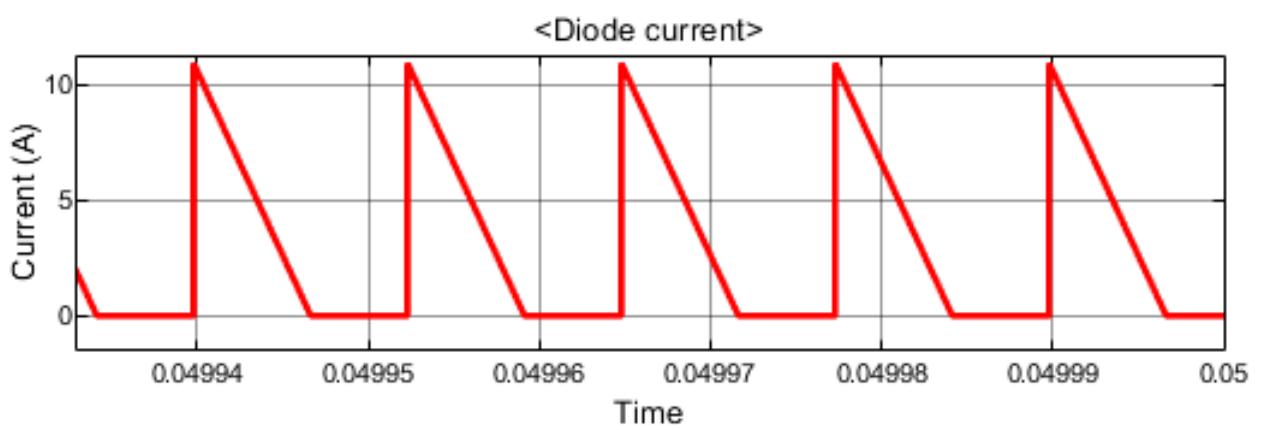
**Simulation results for 48 V input as follows :**



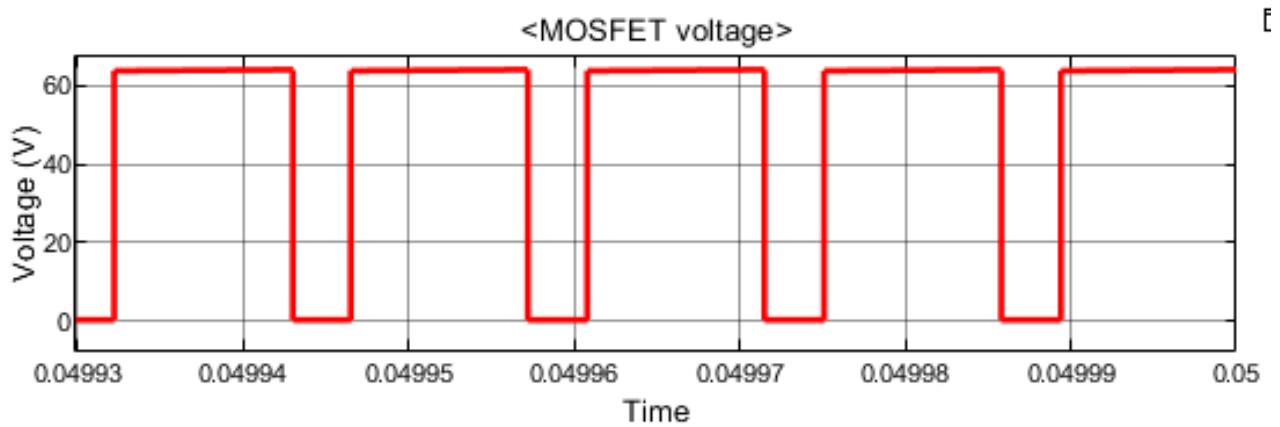
**Figure-11 : Output Voltage Graph for 48V Input**



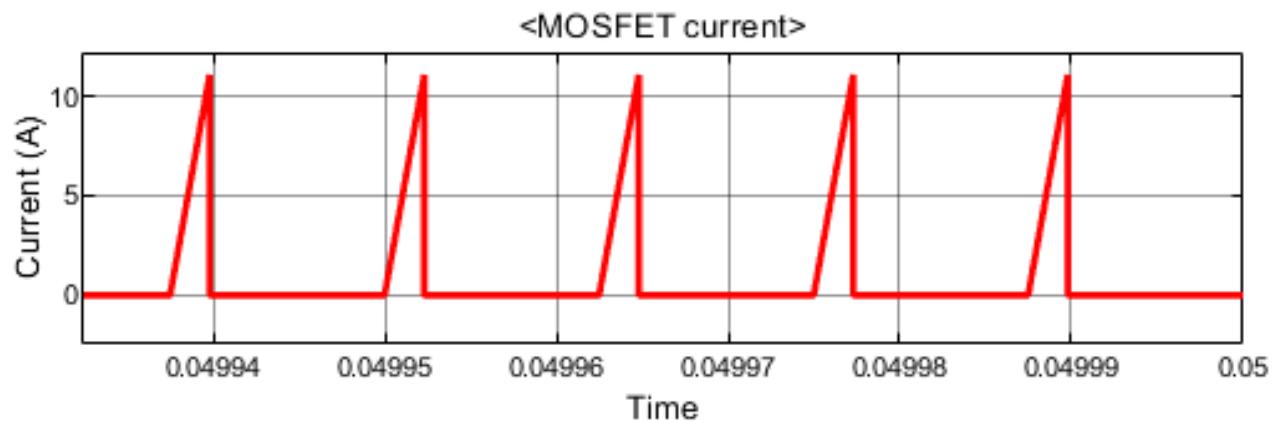
**Figure-12 :** Diode Voltage Graph for 48V Input



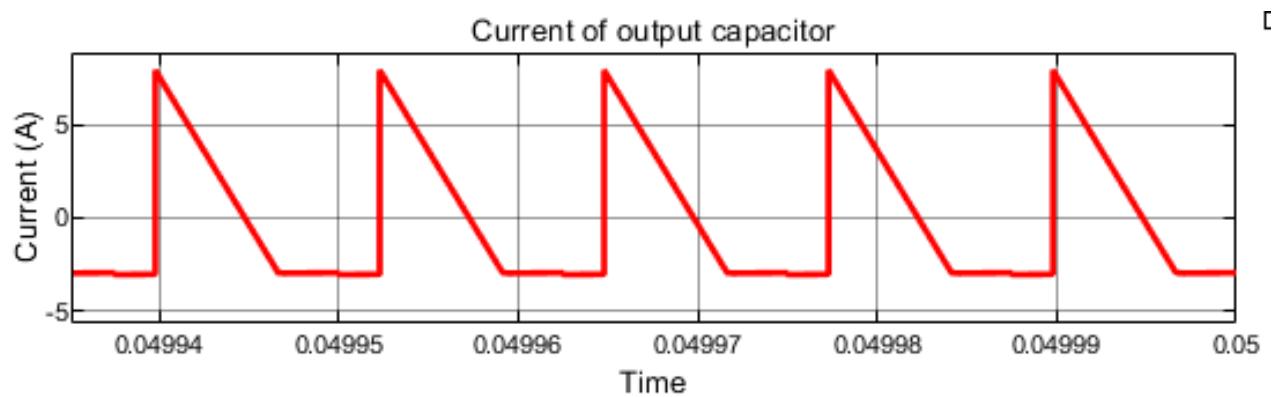
**Figure-13 :** Diode Current Graph for 48V Input



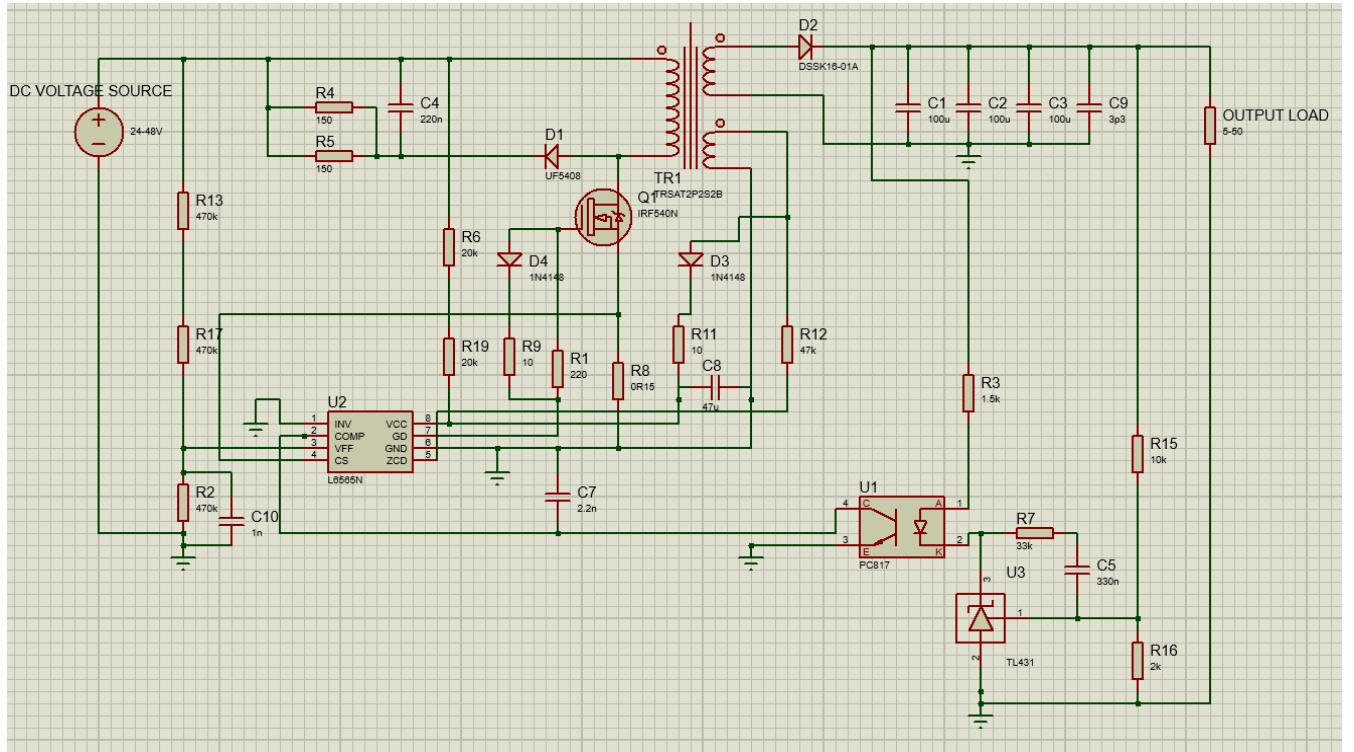
**Figure-14 :** Mosfet Voltage Graph for 48V Input



**Figure-15 : Mosfet Current Graph for 48V Input**



**Figure-16 : Output Capacitor Current Graph for 48V Input**

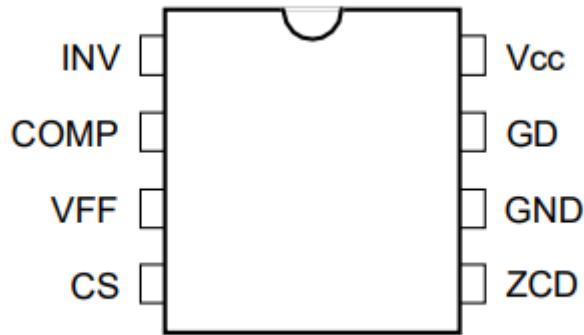


**Figure-17a:** Schematic of our circuit

We could not simulate the circuit because we could not find a model for our controller. But the schematic of our design is given in the above figure.

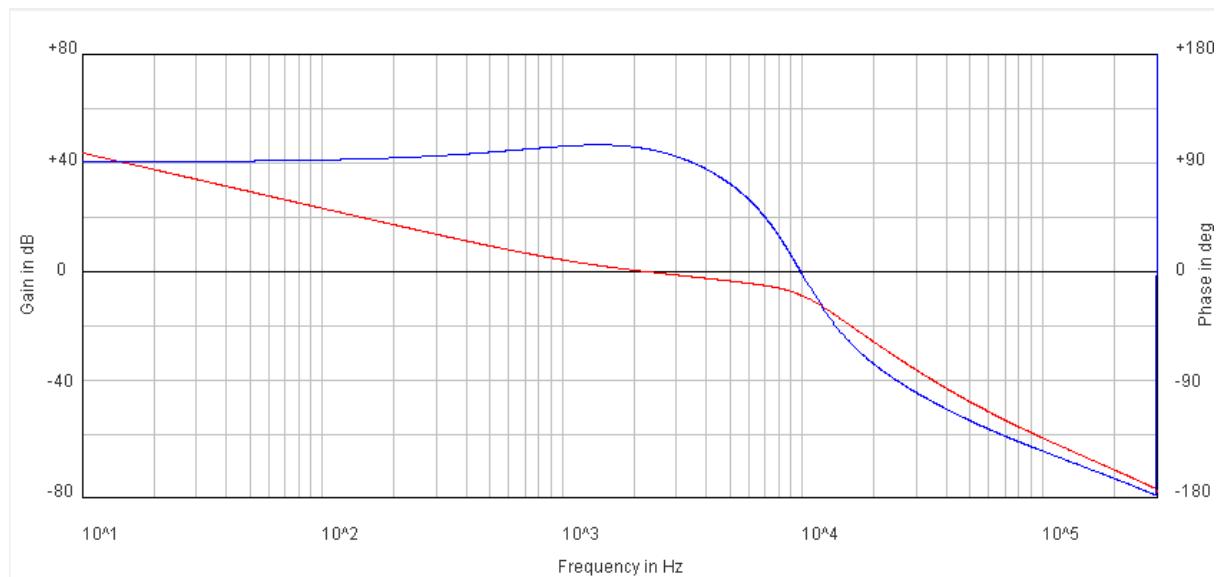
## Controller Design

Since our objective is to design quasi-resonant flyback we could not use any ordinary flyback PWM controller since our frequency changes while other modes keep it constant. While we were looking for a proper model we could not find any model with simulation and can be bought in Turkey, hence, we chose ST electronics' L6565 Quasi Resonant Smps controller. However, it has no simulation model for either Itspice or powersim. Therefore, we designed it by calculating pin by pin from datasheets and application notes.



**Figure-17b : Pinout of our controller**

One can see the pinout and circuit schematics above from Fig 17a and Fig 17b the schematics of design with former resistance and capacitive values and pinout of the controller. In the design one simply uses datasheet pin values and application notes approaches. The operation of frequency changing in Quasi-Resonant is executed by Cs and Vff pins. Current Sense pin is getting information from Mosfets source and comparing it to Vff value. From this comparison it turns off the Mosfet if needed. One gets two feedbacks, one from the auxiliary winding which is connected to ZCD pin and the pin is demagnetization sense pin which turns on Mosfet if conditions are safe and it has a blanked trigger circuit which protects circuits from overload and helps safer operation. The second feedback is Type 2 isolated output with inner loop feedback by using optocoupler and tl431. The feedback is isolated properly and the pins which are isolated are connected to INV and COMP pins. In order to decrease complexity of the controller if any pin can be grounded under any schemes, it is used and pins are grounded. The compensation network is used as the same schematics from application notes (Type 2 isolated output with inner loop feedback). We just change values in order to get the most stable performance.



**Figure-17b: Bode of total gain and**

Our simulated controller feedback designs' bode plot is added above.

### Box Design

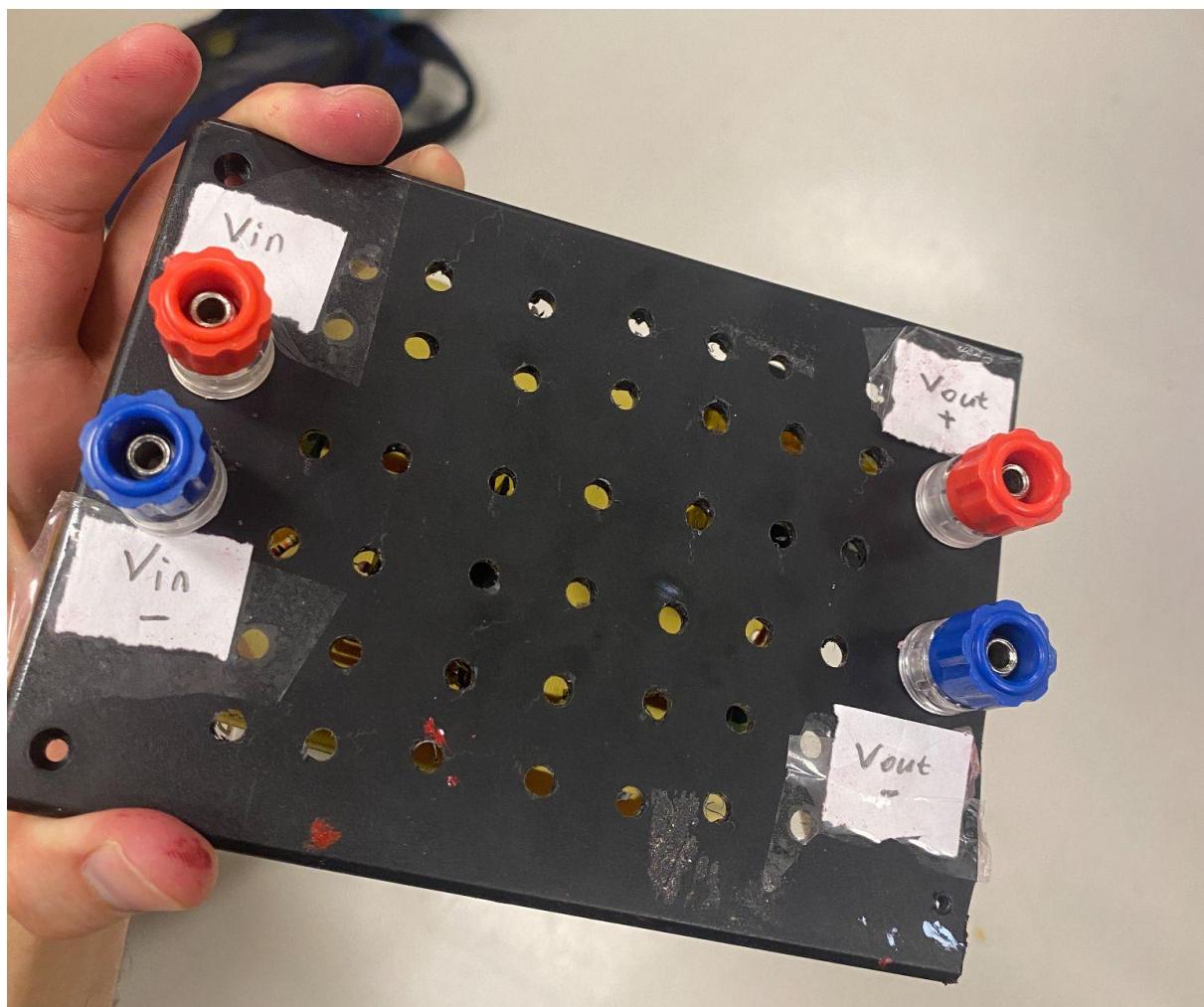


**Figure-18a** : The Box for the PCB



**Figure-18b** : The Inside of the Box for the PCB

Purchased the box that best fits our PCB drawing. However, our box was still bigger than our PCB. That's why our box was cut using the materials from the ground lab. A piece of wood was placed on the cut side of the box and glued. In this way, there was an area where we could screw our cover. Thus, we ensured easy access to our circuit inside our box. In addition, we drilled holes on the sides and lid of our box to allow the airflow of our circuit. Thus, we designed our box without the need to use a fan. The dimensions of our box are 15.5 cm long, 6 cm wide, and 8 cm high. The final version of our box can be viewed from the figures.



**Figure-19** : The Final Version of the Project

## **Component Selection, Losses and Thermal Considerations**

### **Capacitor Selection**

We are asked to have a maximum of %3 voltage regulation. Which means

$$\Delta V_{out(max)} = 15 * 0.03 = 0.45 \text{ V}$$

Capacitor Peak-Peak current can be found as 10.8 A from simulation.

$$\Delta V_{ESR} = ESR * Ic(pp) = 10.8 * ESR$$

$$\Delta V_C = Iout(avg) * Dmax / (Cout * fs) = 1.5 * 10^{-5} / Cout$$

$$\Delta V_{out} = \Delta V_{ESR} + \Delta V_C = 10.8 * ESR + 1.5 * 10^{-5} / Cout$$

If  $Cout$  is infinite, the minimum value of  $ESR$  is 41.67 mohm and From simulation with 41.67 mohm  $ESR$  and 0.01 F capacitance we find % 2.89 voltage ripple so our calculation holds.

Suppose  $ESR$  is 0 minimum value of  $Cout$  = 33.3 uF. The simulation result shows %2.95 voltage ripple confirming the calculation.

We must choose a capacitor with low  $ESR$  because  $ESR$  also lowers output voltage. Many capacitors ( like most electrolytic capacitors) have higher  $ESR$  than 41.67 m ohm, so we think  $ESR$  will be the limiting factor when choosing a capacitor, not capacitance value for our case. So for output, we used three 100 uF electrolytic capacitors, but these capacitors have as much as 1-2 ohm of  $ESR$ , which will increase our output voltage ripple, so we added a 220nF ceramic capacitor. We achieved around 200mV voltage ripple, which means its voltage ripple is %1.3, which is significantly smaller than the required %3 value. We did not measure exact  $ESR$  values of capacitors because they are hard to measure precisely. Low  $ESR$  of ceramic capacitors will practically negate electrolytic ones when connected in parallel.

## **Semiconductor Selection, Losses and Thermal Considerations**

From simulations, we can see maximum voltage and current values for semiconductors.

At 48V input voltage

Maximum diode current = 10.7 A

Maximum reverse bias diode voltage with safety margin = 82 V

Maximum Mosfet current = 10.8 A

Maximum Mosfet blocking voltage = 63.9 V

At 24V input voltage

Maximum diode current = 10.7 A

Max Rms diode current = 4.331A

Maximum Mosfet current = 10.8 A

Max Rms Mosfet current = 3.602 A

We will use the Schottky diode because the chosen diode must be able to work at 80k frequency without significant switching losses.

DSSK16-01A 2X8A 100V Schottky Diode fits our criterias. It has a 0.63 forward voltage bias which is acceptable. It has a TO220 design, so the heatsink can be attached to it. Also, its two diodes are connected in a single package, so heating and losses will be even less of a problem. Diode forward voltage loss is  $4.331 \times 0.63 = 2.73$  W at max loading. For switching losses,  $dv/dt$  is given as 50000 V/ $\mu$ s. Our diode voltage is between 63 and 39 depending on input voltage, so the switching time is, at worst 1.26 ns which is very small. Switching losses will not be a major problem because of the nature of the diode.

The heatsink we used for the diode is fairly small, so we can take its thermal resistance is 10 C/W. Case to junction thermal resistance of the diode is 1.7 C/W. In the end, our total thermal resistance is around 11.7 C/W. And diodes temperature will rise at most 32 degrees which is acceptable. In practical tests, we observed diodes do not heat much, and losses might be even lower than calculated.

IRF540 N Channel Power MOSFET TO-220 fits our criteria with 33A continuous drain current and 100V Drain-to-Source Breakdown Voltage. It also has a low RDS(on) of 44 m ohm. We could have used IRF510 N, which is cheaper (Although by a small margin) and has a 5.56A continuous drain current closer to our current limit. But it has a much higher 540 m ohm RDS(on). With IRF510 N, losses will be much more significant, and we might need an oversized heatsink.

With 0.63 V forward voltage drop and 4.331 A max diode current, resistive diode power loss is 2.73 W.

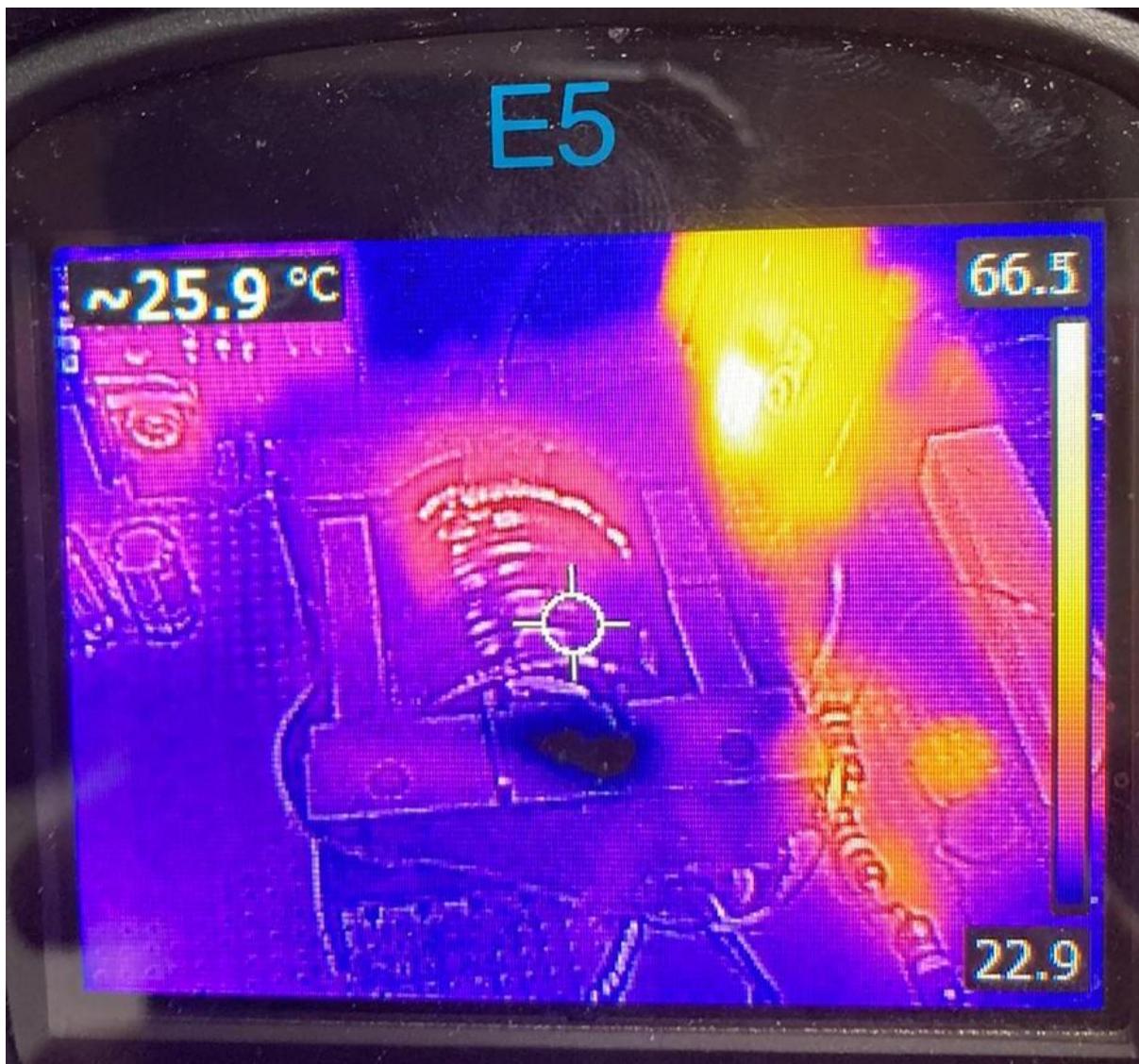
With 0.043 Ron and 3.602 A max RMS current, resistive MOSFET power loss is 0.558 W. Gate losses are  $P_{gate} = f_{sw} * Q_{tot} * V_{gate} = 72\text{kHz} * 71\text{nC} * 18\text{V} = 0.092 \text{ W}$ . Switching losses are  $P_{sw} = V_{in} * I_D * f_{sw} * (t_r + t_f) / 2 = 0.224 \text{ W}$ . But measured rise and fall times are around 200ns rise time and 600ns total for 57ns and 55ns respectively. So switching loss is 1.6 W. Total power loss at mosfet = 1.7 W

For MOSFET, thermal junction to ambient resistance is 62 C/W. Without a heatsink temperature will rise 105.4 degrees, which will be a problem, so a heatsink is needed. Our heatsink has approximately 5 C/W thermal resistance. Case to junction thermal resistance of MOSFET is 1.25 C/W, and we can take the case to heatsink resistance as 1 C/W. So total thermal resistance is 7.25 C/W. Our MOSFET should heat at the max of 12.33 degrees. But we observed much higher heat dissipated at MOSFET in our tests. We suspect this discrepancy is caused by much higher than expected switching losses caused by improper transformer design. Our gate signal switches more than twice per period negatively affect our efficiency and thermal design. It is unlikely that conductive loss is an issue because the resistance of our diode is minimal (40 m ohm).

These semiconductors are above our voltage and current ratings requirements, so we used them in our system. Also, IRF540N MOSFET is present in the lab, so attaining it will not be a problem.



**Figure-20:** Thermal photos of the circuit



**Figure-21 : Thermal photos of the circuit**

From the figure, we can see that MOSFET is the main source of heat in our circuit. We suspect most of the losses happen at MOSFET. Another major contributor to the loss of efficiency is the core losses. But heating the core is not a problem because of its already large size. As we can see core temperature is low,

We must consider I-sense resistance when computing the efficiency because a high amount of current passes through. Its I-sense resistance is 0.15 ohms. Max current passes through 4.2 Arms. So I-sense resistance loss is 2.646 W. We used an 11W resistor to handle this loss

From the datasheet, we can find that the average no-load loss for the controller is 0.5 W, so we will take control loss as 0.5 W.

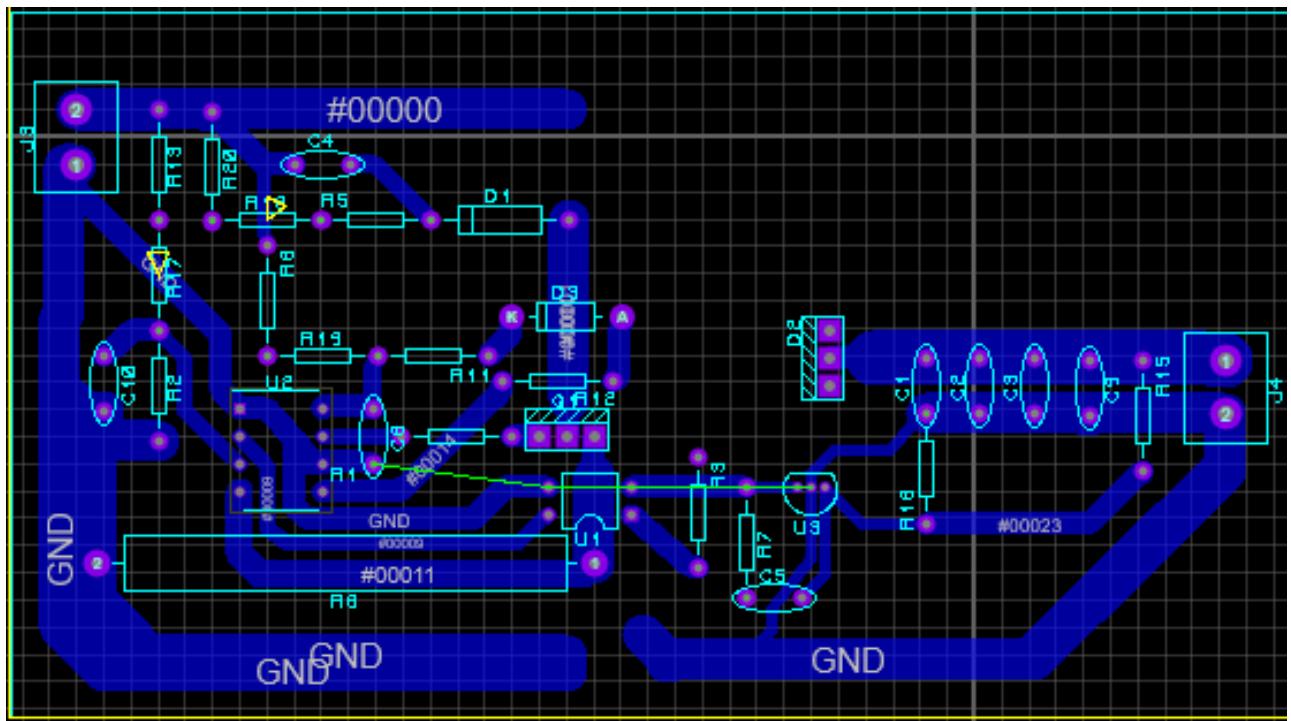
Snubber loss is calculated as 1 W

Maximum total losses of our system are

$P_{\text{loss}} = P_{\text{copper}} + P_{\text{core}} + P_{\text{diode}} + P_{\text{MOSFET}} + P_{\text{I-sense}} + P_{\text{controller}} + P_{\text{snubber}} = 12.8 \text{ W}$ . This means minimum efficiency is %78. Although we reach this loss value for some loads and voltages, the worst efficiency we observed is around %68. We suspect our mistake while designing the transformer is the culprit of this issue.

## PCB Design

We have drawn a PCB circuit using Altium as given in figure. We used through-hole elements because they are easier to change and implement. We used thick trace to minimize parasitic elements and reduce losses. Traces where power passes are selected as extra thick. Even the most minor traces in the PCB should be able to handle 4.2 A. From the trace width calculator, we found that a six mil wide trace is enough for 4.2 A. Smallest trace in the PCB is 40 mils wide.



**Figure-22 :** PCB of our circuit

We have made our PCB at ulus using the copper sheet, iron, and hydrogen peroxide.

## Test Results

Our demo and test results observed that our circuit provides a stable 15 V load for loads smaller than 15 ohms. But output voltage starts to reduce to around 13.7 V for 24 V input and 12 for 48 V. Output current ripple is 200 mV, and it is within the given limit. Also, our efficiency was between 70-80% for most cases. At smaller loads, our efficiency was higher; for more oversized loads, it was smaller. We observed the worst efficiency at the demo, with 68% efficiency at 48 V input full load.



**Figure-23 :** Inductance value of the primary of our first transformer



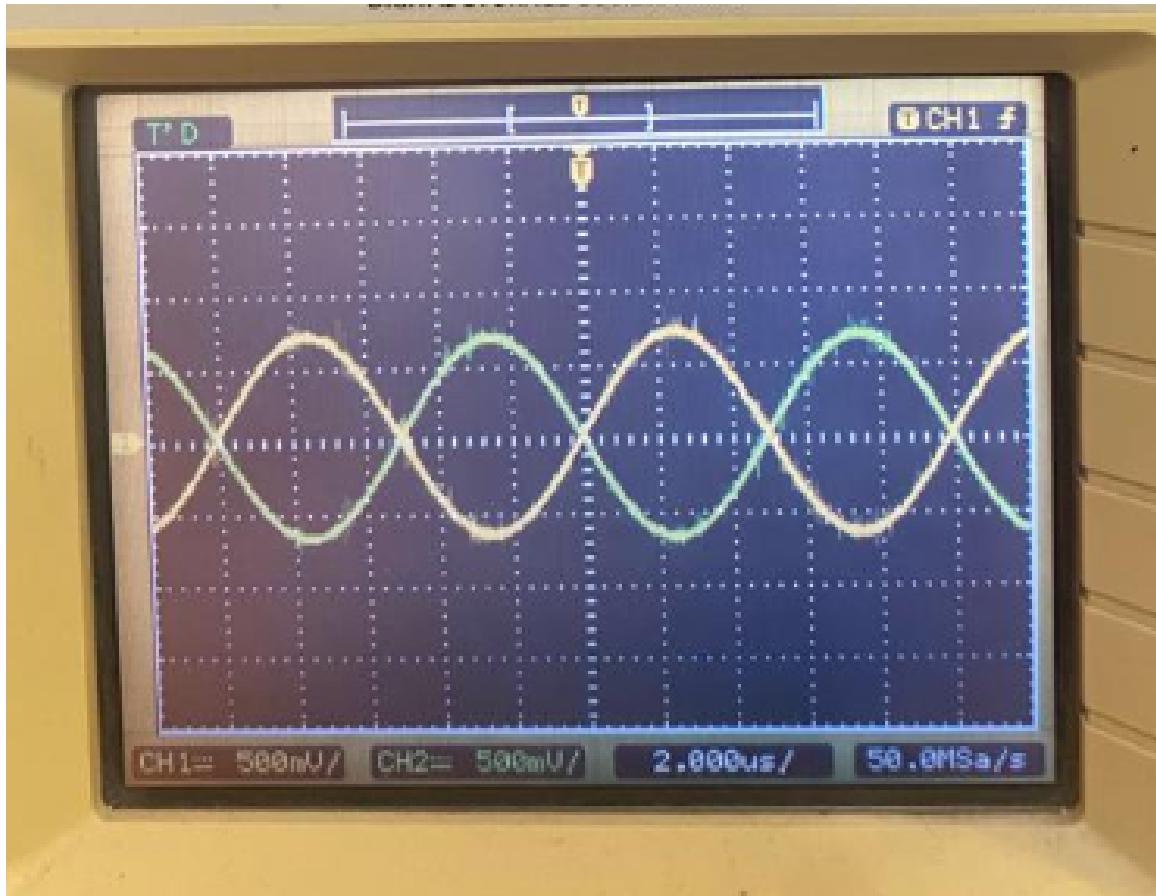
**Figure-24** : Inductance value of the secondary of our first transformer

As we can see from the figure, our inductance values are close to the expected 12 uF.



**Figure-25** : Leakage Inductance value of our first transformer

The leakage inductance value of our transformer is 0.6 uF, around %5 of our magnetizing inductance. Up to %10 leakage is acceptable for hand-winded transformers, although machine-winded ones can be as low as %1.



**Figure-26** : Primary vs Secondary waveform of our transformer when it is independently tested.

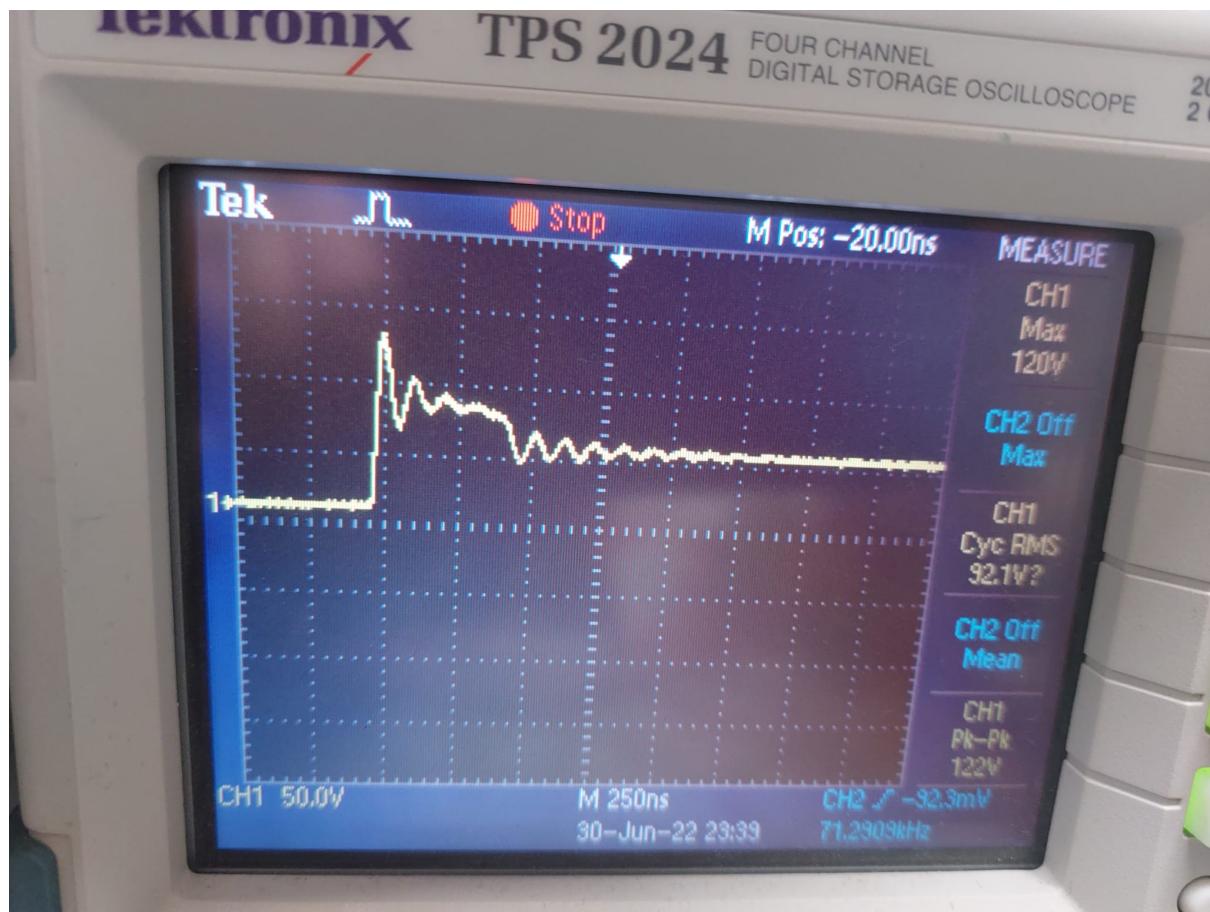
From the figure we tested if our transformer has a turn ratio. As we can see, its primary and secondary voltages are the same. We also tested this with primary and auxiliary windings as well.



**Figure-27 :** Drain to source voltage of our mosfet with 560 ohm snubber.

As we can see with 560 ohm snubber our mosfet has high voltage peaks. Voltage waveform is close to the flyback converter without snubber and this is a problem. Higher than mosfet rating of 100 V in fact. Which may damage the mosfet but we did not observe any damage to the mosfet because transients happen in a very short amount of time. According to our calculations these snubber values must be enough. I think the problem is that our leakage inductance value is much higher than ones used in analytical calculations. Generally %1 leakage is taken and we measured %5 leakage. This is expected because we wrapped these winding by hand not with machines like in industrial applications.

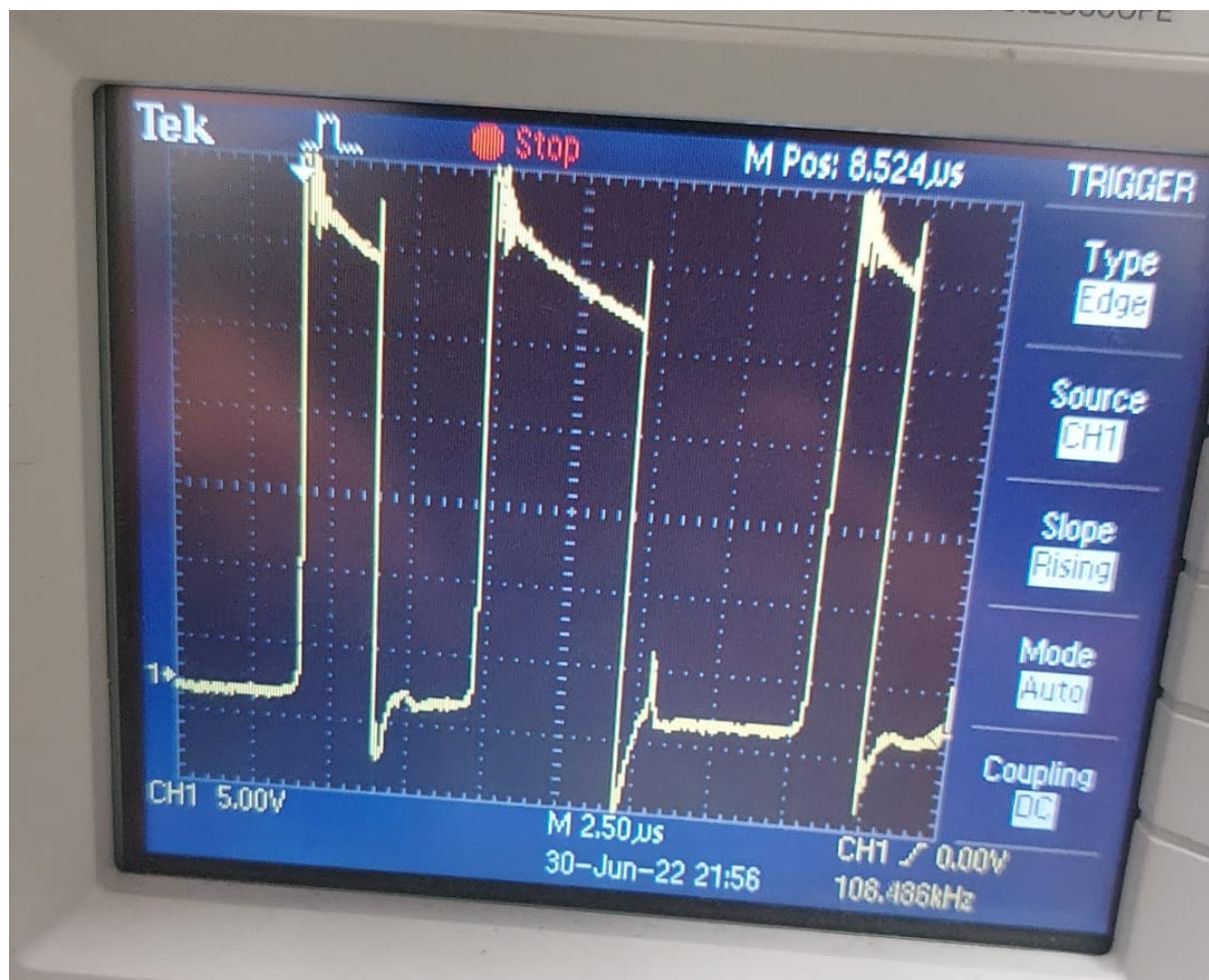
Later we tried 280 ohm resistor like in the figure



**Figure-28** : Drain to source voltage of our mosfet with 280 ohm snubber.

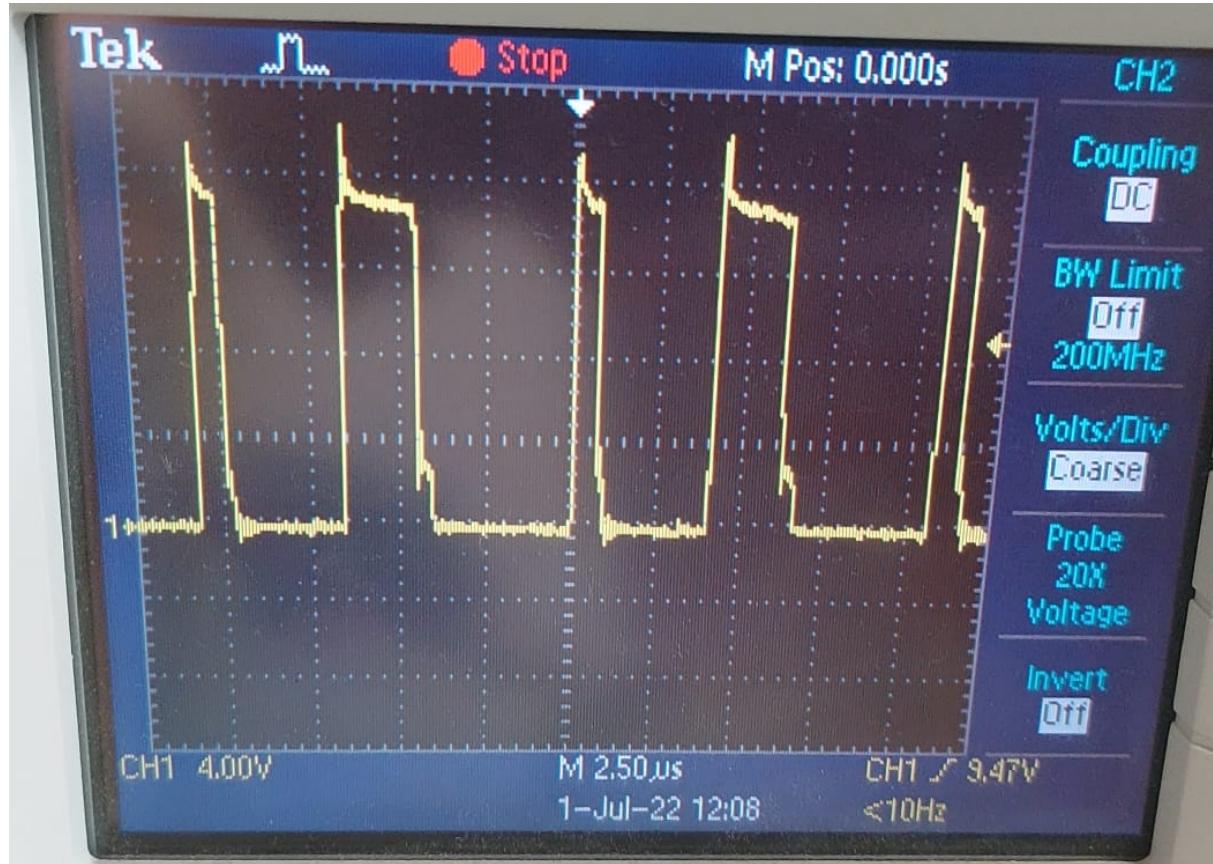
As we can see, our drain-source voltage peak is still too high. Also we find ringing frequency as 100ns in this example. We tried to calculate snubber values according to that and leakage inductance but we did not achieve any success in that.

We thought maybe snubbers diode opening speed maybe a problem so we have taken voltage waveform of snubber diode like in figure



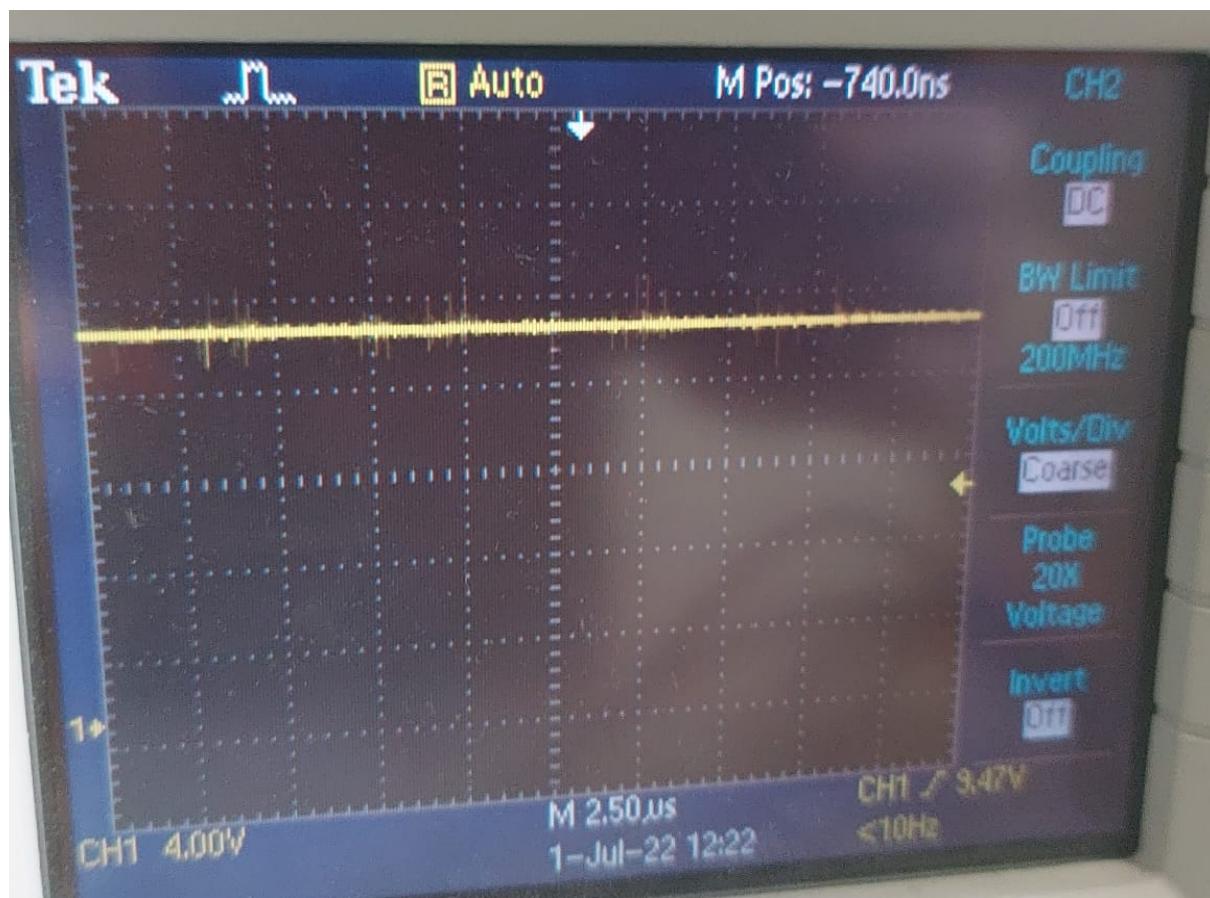
**Figure-29** : Voltage through diode

As we can see our snubber diodes open very fast and this is not a problem. So in the end we decided to add a 75 ohm resistor as snubber resistance.



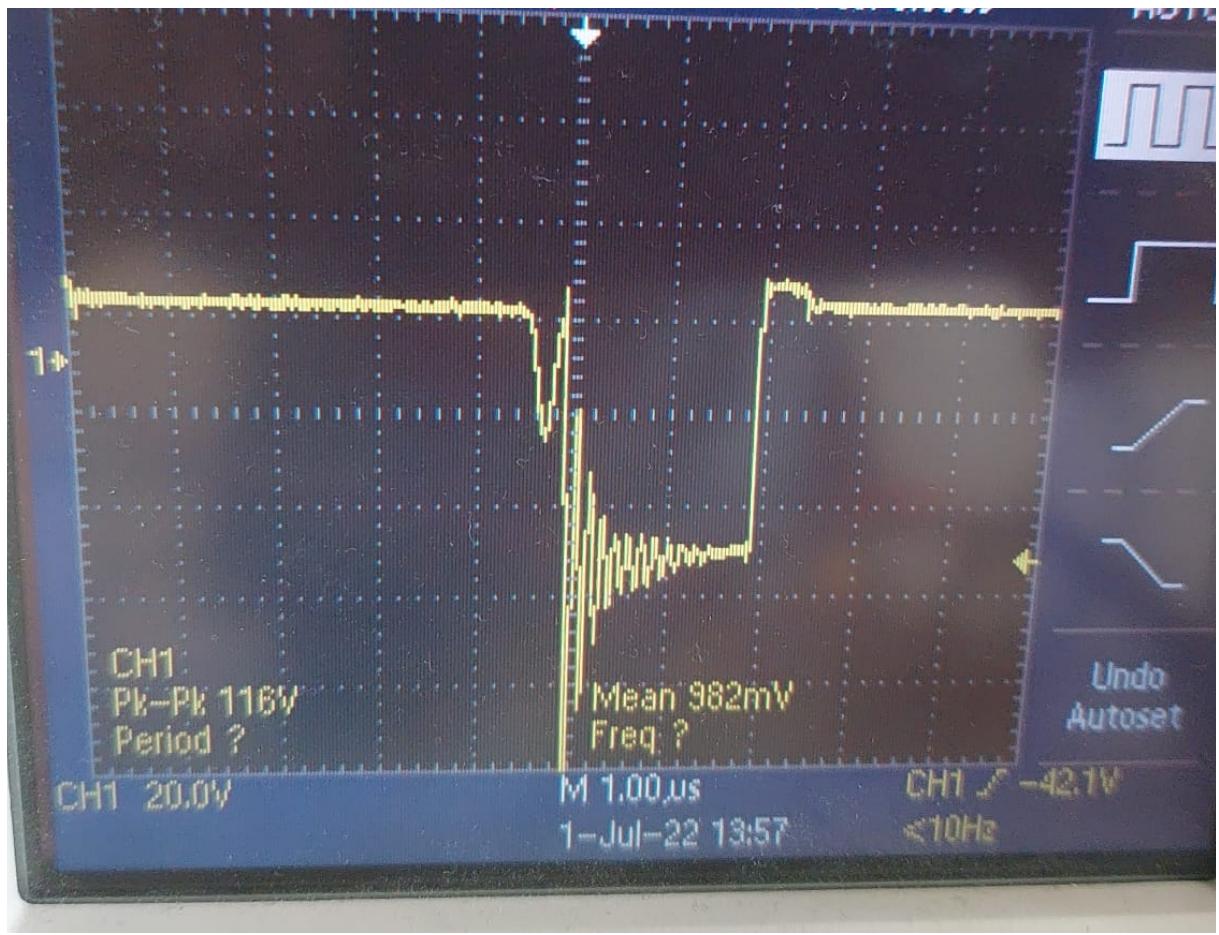
**Figure-30 :** Voltage waveform of gate signal.

As we can see from the gate signal gate voltage is 17 V which is smaller than VCC given in figure like in the datasheet. Gate switches 4 times every period instead of 2. This will increase mosfet losses.



**Figure-31** : VCC voltage of controller

VCC voltage of the controller is 18 V which is operating limit of our controller



**Figure-32 :** Voltage waveform of our auxiliary winding at full load and 48 V.

As we can see from figure 26 voltage waveform of auxiliary voltage is constant 15 V most of the time but sometimes its reduced to around -40 V. This is maybe the cause off our voltage regulation problems at close to full load. Average of our auxiliary winding is the same as the secondary winding so this waveform shows us that the average of output voltage is lower than 15. We also observed that our output voltage changes from 13,7 to around 12 when at full load for input voltage of 24 to 48 V. Difference of output voltage from 15 V is proportional to input voltage. Our best guess for why this happens is that our core was inadequate because when we increased the inductance of the transformer by removing papers between cores voltage regulation and efficiency problems were reduced.

## Cost Analysis

Material	Cost for single purchase (TL)
I6565n (integrated circuit)	15,54
PC817 (Optocoupler)	1,78
TL431 TO92 (voltage regulator)	1,78
IRF540N (Mosfet)	12,85
DSSK16-01A (Schotky diode)	15,27
2*1N4148 Diode	0,40
3*100uf 63V Electrolytic Capacitor	2,97
47uf 63V Electrolytic Capacitor	0,59
12*1/4W resistor	1,32
2*2W snubber resistor	1,18
0.15 ohm 11W I sense resistor	5,00
5 ceramic capacitors	1,25
UF5408 1000V 3A Fast Diode	1,98
Heatsinks (approximate)	20,00
ETD 34/17/11 carcass	8,78
2*ETD 34/17/11 core	42,88
Transformer cables	26,80
PCB board	24
2*Terminal box connector	4
Transformer band (approximate)	4,00
<b>Total</b>	<b>190,59</b>

Table 1: Cost analysis

Distance of one turn is 47.44 mm and there are 9 windings. We can take total length as 50 cm with some wiggle room.

Cost of 26 awg wire is 4 cent per foot so from this we can calculate the price as 1.6 dollars. This equals to approximately

It is important to point out these prices are single purchase prices. Manufacturers provide discount for bulk purchases so actual production cost will be much lower. For example IRF540N mosfets price is reduced to almost %50 when more than 1000 units are bought at the same time. Same thing is true for all other components.

## Conclusion

As the power converter team, we chose the most suitable topology for our project's specifications as the flyback converter and explained its reasons. Then, we chose our operation mode of this converter as quasi-resonant and stated its advantages. The necessary analytical calculations and simulation results have been added to our report. The controller we intend to use and the essential calculations are also added. Then we made our magnetic, winding design and prepared our transformer physically. Moreover, necessary calculations for other necessary components such as capacitor and diode have been added to our report. Also the related PCB and box design details are explained detailly. Furthermore, the test values taken and the interpretations of these values were also clearly revealed. Finally, the total amount of money we spent on our project was stated in the cost analysis.

We gained a lot of experience in this instructive project, which made us feel like we took a real step into engineering. We have learned very well the importance of teamwork and how we should struggle when faced with difficulties. Even if it works in simulations, we have experienced once again that we are faced with many important parameters when implemented in real life.

## References

- (1) EE464 Static Power Conversion II -Isolated Switching Power Supplies - Ozan Keysan -  
p.21
- (2) EE464 Static Power Conversion II -Isolated Switching Power Supplies - Ozan Keysan  
p.43
- (3) EE464 Static Power Conversion II -Isolated Switching Power Supplies - Ozan Keysan -  
p.60
- (4) Power Integrations web page ,  
<https://www.power.com/community/forum/ac-dc-conversion-forum/2011/ccm-dcm>  
, accessed on 12/5/2022
- (5) Power Electronics News web page,  
[https://www.powerelectronicsnews.com/design-features-of-a-dcm-flyback-converter/#:~:text=Flyback%20converters%20can%20operate%20either,%2Dconduction%20mode%20\(DCM\).&text=DCM%20operation%20is%20characterized%20by,of%20the%20next%20switching%20cycle.](https://www.powerelectronicsnews.com/design-features-of-a-dcm-flyback-converter/#:~:text=Flyback%20converters%20can%20operate%20either,%2Dconduction%20mode%20(DCM).&text=DCM%20operation%20is%20characterized%20by,of%20the%20next%20switching%20cycle.) , accessed on 13/5/2022
- (6) L6565n datasheet.  
<https://www.st.com/resource/en/datasheet/l6565.pdf>
- (7) DSSK 16-01A datasheet  
[https://cdn.ozdisan.com/ETicaret\\_Dosya/427303\\_9469765.pdf](https://cdn.ozdisan.com/ETicaret_Dosya/427303_9469765.pdf)
- (8) <https://www.monolithicpower.com/en/how-to-design-a-flyback-converter-in-seven-steps>
- (9) Microsemi Forward and Flyback Core Selection using the LX7309 and Industry Recommendations guide
- (10) Liu FengHua: Chen LeiResearch About Quasi-resonant Converter Module for EV. Auto Electric 2013 Section 3 16-19
- (11) S. L. Jeng , M. T. Peng , C. Y. Hsu , W. H. Chieng , Jet P.H. Shu, Quasi-Resonant Flyback DC/DC Converter Using GaN Power Transistors, World Electric Vehicle Journal Vol. 5, 2012
- (12) DSSK 16-01A datasheet

- (13) [https://www.ti.com/lit/an/slva589/slva589.pdf?ts=1656765265553&ref\\_url=https%253A%252F%252Fwww.google.com%252F#:~:text=In%20a%20flyback%20converter%2C%20when,current%20collapses%20immediately%20to%20zero.](https://www.ti.com/lit/an/slva589/slva589.pdf?ts=1656765265553&ref_url=https%253A%252F%252Fwww.google.com%252F#:~:text=In%20a%20flyback%20converter%2C%20when,current%20collapses%20immediately%20to%20zero.)
- (14) AN1326 APPLICATION NOTES L6565 QUASI-RESONANT CONTROLLER
- (15) AN1376 APPLICATION NOTE L6565 QUASI-RESONANT CONTROLLER
- (16) L6565 Quasi resonant controller datasheet
- (17) Practical Feedback Loop Design Considerations for Flyback Converter Using UCC28740, Texas Instruments