Analysis & Synthesis report for atm
Fri Jul 14 20:00:15 2023
Quartus Prime Version 22.1std.1 Build 917 02/14/2023 SC Lite Edition

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; Table of Contents ;
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---
; Legal Notice ;
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+----------------------------------------------------------------------------
+
; Analysis & Synthesis Summary
;
+---------------------------------+------------------------------------------
+
; Analysis & Synthesis Status     ; Successful - Fri Jul 14 19:15:55 2023
;
; Quartus Prime Version           ; 22.1std.1 Build 917 02/14/2023 SC Lite Edition
;
; Revision Name                   ; atm
;
; Top-level Entity Name           ; atm
;
; Family                          ; Cyclone V
;
; Logic utilization (in ALMs)     ; N/A
;
; Total registers                 ; 199
;
; Total pins                      ; 34
;
; Total virtual pins              ; 0
;
; Total block memory bits         ; 0
;
; Total DSP Blocks                ; 1
;
; Total HSSI RX PCSs              ; 0
;
; Total HSSI PMA RX Deserializers ; 0
;
; Total HSSI TX PCSs              ; 0
;
; Total HSSI PMA TX Serializers   ; 0
;
; Total PLLs                      ; 0
;
; Total DLLs                      ; 0
;
+---------------------------------+------------------------------------------
+


+----------------------------------------------------------------------------
----------------------------------------+
; Analysis & Synthesis Settings
                                        ;
+----------------------------------------------------------------------------+
--------------------+--------------------+

```
; Option                                                                                ;
Setting            ; Default Value      ;
+-------------------------------------------------------------------------------------+
--------------------+--------------------+
; Device                                                                               ;
5CSEMA5F31C6       ;                    ;
; Top-level entity name                                                               ;
atm                ; atm                ;
; Family name                                                                         ;
Cyclone V          ; Cyclone V          ;
; Use smart compilation                                                               ;
Off                ; Off                ;
; Enable parallel Assembler and Timing Analyzer during compilation                    ;
On                 ; On                 ;
; Enable compact report table                                                         ;
Off                ; Off                ;
; Restructure Multiplexers                                                            ;
Auto               ; Auto               ;
; MLAB Add Timing Constraints For Mixed-Port Feed-Through Mode Setting Don't Care     ;
Off                ; Off                ;
; Create Debugging Nodes for IP Cores                                                 ;
Off                ; Off                ;
; Preserve fewer node names                                                           ;
On                 ; On                 ;
; Intel FPGA IP Evaluation Mode                                                       ;
Enable             ; Enable             ;
; Verilog Version                                                                     ;
Verilog_2001       ; Verilog_2001       ;
; VHDL Version                                                                        ;
VHDL_1993          ; VHDL_1993          ;
; State Machine Processing                                                            ;
Auto               ; Auto               ;
; Safe State Machine                                                                  ;
Off                ; Off                ;
; Extract Verilog State Machines                                                      ;
On                 ; On                 ;
; Extract VHDL State Machines                                                         ;
On                 ; On                 ;
; Ignore Verilog initial constructs                                                   ;
Off                ; Off                ;
; Iteration limit for constant Verilog loops                                          ;
5000               ; 5000               ;
; Iteration limit for non-constant Verilog loops                                      ;
250                ; 250                ;
; Add Pass-Through Logic to Inferred RAMs                                             ;
On                 ; On                 ;
; Infer RAMs from Raw Logic                                                           ;
On                 ; On                 ;
; Parallel Synthesis                                                                  ;
On                 ; On                 ;
```

; DSP Block Balancing ;
Auto ; Auto ;
; NOT Gate Push-Back ;
On ; On ;
; Power-Up Don't Care ;
On ; On ;
; Remove Redundant Logic Cells ;
Off ; Off ;
; Remove Duplicate Registers ;
On ; On ;
; Ignore CARRY Buffers ;
Off ; Off ;
; Ignore CASCADE Buffers ;
Off ; Off ;
; Ignore GLOBAL Buffers ;
Off ; Off ;
; Ignore ROW GLOBAL Buffers ;
Off ; Off ;
; Ignore LCELL Buffers ;
Off ; Off ;
; Ignore SOFT Buffers ;
On ; On ;
; Limit AHDL Integers to 32 Bits ;
Off ; Off ;
; Optimization Technique ;
Balanced ; Balanced ;
; Carry Chain Length ;
70 ; 70 ;
; Auto Carry Chains ;
On ; On ;
; Auto Open-Drain Pins ;
On ; On ;
; Perform WYSIWYG Primitive Resynthesis ;
Off ; Off ;
; Auto ROM Replacement ;
On ; On ;
; Auto RAM Replacement ;
On ; On ;
; Auto DSP Block Replacement ;
On ; On ;
; Auto Shift Register Replacement ;
Auto ; Auto ;
; Allow Shift Register Merging across Hierarchies ;
Auto ; Auto ;
; Auto Clock Enable Replacement ;
On ; On ;
; Strict RAM Replacement ;
Off ; Off ;
; Allow Synchronous Control Signals ;
On ; On ;

; Force Use of Synchronous Clear Signals ;
Off ; Off ;
; Auto Resource Sharing ;
Off ; Off ;
; Allow Any RAM Size For Recognition ;
Off ; Off ;
; Allow Any ROM Size For Recognition ;
Off ; Off ;
; Allow Any Shift Register Size For Recognition ;
Off ; Off ;
; Use LogicLock Constraints during Resource Balancing ;
On ; On ;
; Ignore translate_off and synthesis_off directives ;
Off ; Off ;
; Timing-Driven Synthesis ;
On ; On ;
; Report Parameter Settings ;
On ; On ;
; Report Source Assignments ;
On ; On ;
; Report Connectivity Checks ;
On ; On ;
; Ignore Maximum Fan-Out Assignments ;
Off ; Off ;
; Synchronization Register Chain Length ;
3 ; 3 ;
; Power Optimization During Synthesis ;
Normal compilation ; Normal compilation ;
; HDL message level ;
Level2 ; Level2 ;
; Suppress Register Optimization Related Messages ;
Off ; Off ;
; Number of Removed Registers Reported in Synthesis Report ;
5000 ; 5000 ;
; Number of Swept Nodes Reported in Synthesis Report ;
5000 ; 5000 ;
; Number of Inverted Registers Reported in Synthesis Report ;
100 ; 100 ;
; Clock MUX Protection ;
On ; On ;
; Auto Gated Clock Conversion ;
Off ; Off ;
; Block Design Naming ;
Auto ; Auto ;
; SDC constraint protection ;
Off ; Off ;
; Synthesis Effort ;
Auto ; Auto ;
; Shift Register Replacement - Allow Asynchronous Clear Signal ;
On ; On ;

```
; Pre-Mapping Resynthesis Optimization                                                ;
Off                ; Off                ;
; Analysis & Synthesis Message Level                                                  ;
Medium             ; Medium             ;
; Disable Register Merging Across Hierarchies                                         ;
Auto               ; Auto               ;
; Resource Aware Inference For Block RAM                                              ;
On                 ; On                 ;
; Automatic Parallel Synthesis                                                        ;
On                 ; On                 ;
; Partial Reconfiguration Bitstream ID                                                ;
Off                ; Off                ;
+-----------------------------------------------------------------------------------+
-------------------+--------------------+


+-----------------------------------------+
; Parallel Compilation                    ;
+-----------------------------+-------------+
; Processors                  ; Number      ;
+-----------------------------+-------------+
; Number detected on machine ; 12          ;
; Maximum allowed            ; 6           ;
;                            ;             ;
; Average used               ; 1.00        ;
; Maximum used               ; 6           ;
;                            ;             ;
; Usage by Processor         ; % Time Used ;
;     Processor 1            ; 100.0%      ;
;     Processor 2            ;   0.0%      ;
;     Processor 3            ;   0.0%      ;
;     Processor 4            ;   0.0%      ;
;     Processor 5            ;   0.0%      ;
;     Processor 6            ;   0.0%      ;
+-----------------------------+-------------+


+-------------------------------------------------------------------------------------
-----------------------------------------------+
; Analysis & Synthesis Source Files Read
                                                ;
+----------------------------------+-----------------+------------------------+----
---------------------------------------+---------+
; File Name with User-Entered Path ; Used in Netlist ; File Type              ;
File Name with Absolute Path             ; Library ;
+----------------------------------+-----------------+------------------------+----
---------------------------------------+---------+
; atm.v                            ; yes             ; User Verilog HDL File  ;
D:/INTEL UNNATI/Atm_mini/atm.v           ;         ;
; Clock_divider.v                  ; yes             ; User Verilog HDL File  ;
```

```
D:/INTEL UNNATI/Atm_mini/Clock_divider.v ;         ;
+-----------------------------------+----------------+------------------------+----
-------------------------------------+---------+


+-----------------------------------------------------------+
; Analysis & Synthesis Resource Usage Summary              ;
+---------------------------------------------+-------------+
; Resource                                    ; Usage       ;
+---------------------------------------------+-------------+
; Estimate of Logic utilization (ALMs needed) ; 247         ;
;                                             ;             ;
; Combinational ALUT usage for logic          ; 419         ;
;     -- 7 input functions                    ; 1           ;
;     -- 6 input functions                    ; 73          ;
;     -- 5 input functions                    ; 84          ;
;     -- 4 input functions                    ; 68          ;
;     -- <=3 input functions                  ; 193         ;
;                                             ;             ;
; Dedicated logic registers                   ; 199         ;
;                                             ;             ;
; I/O pins                                    ; 34          ;
;                                             ;             ;
; Total DSP Blocks                            ; 1           ;
;                                             ;             ;
; Maximum fan-out node                        ; clk~input   ;
; Maximum fan-out                             ; 200         ;
; Total fan-out                               ; 2562        ;
; Average fan-out                             ; 3.73        ;
+---------------------------------------------+-------------+


+-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
------------------+
; Analysis & Synthesis Resource Utilization by Entity

                 ;
+----------------------------+--------------------+--------------------------+---
----------------+------------+------+--------------+---------------------+---------
----+--------------+
; Compilation Hierarchy Node ; Combinational ALUTs ; Dedicated Logic Registers ;
Block Memory Bits ; DSP Blocks ; Pins ; Virtual Pins ; Full Hierarchy Name ; Entity
Name ; Library Name ;
+----------------------------+--------------------+--------------------------+---
----------------+------------+------+--------------+---------------------+---------
----+--------------+
; |atm                       ; 419 (419)           ; 199 (199)                ; 0
              ; 1          ; 34   ; 0            ; |atm                ; atm
  ; work         ;
```

```
+----------------------------+--------------------+---------------------------+---
---------------+------------+------+-------------+--------------------+---------
----+-------------+
```
Note: For table entries with two numbers listed, the numbers in parentheses indicate the number of resources of the given type used by the specific entity alone. The numbers listed outside of parentheses indicate the total resources of the given type used by the specific entity and all of its sub-entities in the hierarchy.

```
+-----------------------------------------------+
; Analysis & Synthesis DSP Block Usage Summary  ;
+---------------------------------+-------------+
; Statistic                       ; Number Used ;
+---------------------------------+-------------+
; Independent 9x9                 ; 1           ;
; Total number of DSP blocks      ; 1           ;
;                                 ;             ;
; Fixed Point Unsigned Multiplier ; 1           ;
+---------------------------------+-------------+
```

```
Encoding Type:  One-Hot
+-------------------------------------------------------------------------------
-------------------------------------------------------------------------------
-------------------------------------------------+
; State Machine - |atm|state

                                                 ;
+-------------------------+-------------------------+--------------------------+----
-----------+--------------+----------------------+---------------+----------------+
------------+-------------------------+------------+
; Name                     ; state.Pin_Verification3 ; state.Pin_Verification2 ;
state.Blocked ; state.Finish ; state.Mini_Statement ; state.Deposit ;
state.Withdraw ; state.Menu ; state.Pin_Verification ; state.Idle ;
+-------------------------+-------------------------+--------------------------+----
-----------+--------------+----------------------+---------------+----------------+
------------+-------------------------+------------+
; state.Idle               ; 0                       ; 0                        ; 0
          ; 0            ; 0                    ; 0             ; 0              ;
0          ; 0                       ; 0          ;
; state.Pin_Verification  ; 0                       ; 0                        ; 0
          ; 0            ; 0                    ; 0             ; 0              ;
0          ; 1                       ; 1          ;
; state.Menu               ; 0                       ; 0                        ; 0
          ; 0            ; 0                    ; 0             ; 0              ;
1          ; 0                       ; 1          ;
; state.Withdraw           ; 0                       ; 0                        ; 0
          ; 0            ; 0                    ; 0             ; 1              ;
0          ; 0                       ; 1          ;
```

```
; state.Deposit           ; 0                       ; 0                       ; 0
          ; 0            ; 0                     ; 1            ; 0             ;
0          ; 0                       ; 1          ;
; state.Mini_Statement    ; 0                       ; 0                       ; 0
          ; 0            ; 1                     ; 0            ; 0             ;
0          ; 0                       ; 1          ;
; state.Finish            ; 0                       ; 0                       ; 0
          ; 1            ; 0                     ; 0            ; 0             ;
0          ; 0                       ; 1          ;
; state.Blocked           ; 0                       ; 0                       ; 1
          ; 0            ; 0                     ; 0            ; 0             ;
0          ; 0                       ; 1          ;
; state.Pin_Verification2 ; 0                       ; 1                       ; 0
          ; 0            ; 0                     ; 0            ; 0             ;
0          ; 0                       ; 1          ;
; state.Pin_Verification3 ; 1                       ; 0                       ; 0
          ; 0            ; 0                     ; 0            ; 0             ;
0          ; 0                       ; 1          ;
+-------------------------+-------------------------+-------------------------+----
-----------+--------------+----------------------+--------------+----------------+
------------+-------------------------+------------+
```

```
+-----------------------------------------------------------------------------+
; Registers Removed During Synthesis                                          ;
+--------------------------------------+--------------------------------------+
; Register name                        ; Reason for Removal                   ;
+--------------------------------------+--------------------------------------+
; deposit_success                      ; Stuck at GND due to stuck port data_in ;
; withdraw_success                     ; Stuck at GND due to stuck port data_in ;
; amount[14,15]                        ; Merged with amount[13]               ;
; accCount                             ; Stuck at GND due to stuck port data_in ;
; amount[13]                           ; Stuck at GND due to stuck port data_in ;
; state~13                             ; Lost fanout                          ;
; state~14                             ; Lost fanout                          ;
; state~15                             ; Lost fanout                          ;
; state~16                             ; Lost fanout                          ;
; pin_database~0                       ; Stuck at GND due to stuck port clock   ;
; pin_database~1                       ; Stuck at GND due to stuck port clock   ;
; pin_database~2                       ; Stuck at GND due to stuck port clock   ;
; pin_database~3                       ; Stuck at GND due to stuck port clock   ;
; pin_database~4                       ; Stuck at GND due to stuck port clock   ;
; pin_database~5                       ; Stuck at GND due to stuck port clock   ;
; pin_database~6                       ; Stuck at GND due to stuck port clock   ;
; pin_database~7                       ; Stuck at GND due to stuck port clock   ;
; Total Number of Removed Registers = 18 ;                                     ;
+--------------------------------------+--------------------------------------+
```

```
+-----------------------------------------------------------------------------
```

```
----+
; Removed Registers Triggering Further Register Optimizations
   ;
+-----------------+---------------------------+-----------------------------------
----+
; Register name   ; Reason for Removal        ; Registers Removed due to This
Register ;
+-----------------+---------------------------+-----------------------------------
----+
; deposit_success ; Stuck at GND              ; amount[13]
   ;
;                 ; due to stuck port data_in ;
   ;
+-----------------+---------------------------+-----------------------------------
----+


+-----------------------------------------------------+
; General Register Statistics                         ;
+---------------------------------------------+-------+
; Statistic                                   ; Value ;
+---------------------------------------------+-------+
; Total registers                             ; 199   ;
; Number of registers using Synchronous Clear ; 85    ;
; Number of registers using Synchronous Load  ; 46    ;
; Number of registers using Asynchronous Clear ; 108   ;
; Number of registers using Asynchronous Load ; 0     ;
; Number of registers using Clock Enable      ; 183   ;
; Number of registers using Preset            ; 0     ;
+---------------------------------------------+-------+


+-------------------------------------------------+
; Inverted Register Statistics                    ;
+-----------------------------------------+---------+
; Inverted Register                       ; Fan out ;
+-----------------------------------------+---------+
; balance_database[1][2]                  ; 2       ;
; balance_database[2][2]                  ; 2       ;
; balance_database[3][2]                  ; 2       ;
; balance_database[1][7]                  ; 2       ;
; balance_database[2][7]                  ; 2       ;
; balance_database[3][7]                  ; 2       ;
; balance_database[1][6]                  ; 2       ;
; balance_database[2][6]                  ; 2       ;
; balance_database[3][6]                  ; 2       ;
; balance_database[1][5]                  ; 2       ;
; balance_database[2][5]                  ; 2       ;
; balance_database[3][5]                  ; 2       ;
; balance_database[1][4]                  ; 2       ;
```

```
; balance_database[2][4]                  ; 2       ;
; balance_database[3][4]                  ; 2       ;
; balance_database[1][8]                  ; 2       ;
; balance_database[2][8]                  ; 2       ;
; balance_database[3][8]                  ; 2       ;
; Total number of inverted registers = 18 ;         ;
+-----------------------------------------+---------+


+-------------------------------------------------------------------------------
-------------------------------------------------------+
; Multiplexer Restructuring Statistics (Restructuring Performed)
                                                       ;
+--------------------+-----------+---------------+----------------------+----------
--------------+------------+-----------------------------+
; Multiplexer Inputs ; Bus Width ; Baseline Area ; Area if Restructured ; Saving if
Restructured ; Registered ; Example Multiplexer Output  ;
+--------------------+-----------+---------------+----------------------+----------
--------------+------------+-----------------------------+
; 4:1                ; 3 bits    ; 6 LEs         ; 6 LEs                ; 0 LEs
             ; Yes        ; |atm|Acc_valid              ;
; 5:1                ; 46 bits   ; 138 LEs       ; 0 LEs                ; 138 LEs
             ; Yes        ; |atm|balance_database[2][3] ;
; 11:1               ; 16 bits   ; 112 LEs       ; 80 LEs               ; 32 LEs
             ; Yes        ; |atm|balance[5]~reg0        ;
; 9:1                ; 14 bits   ; 84 LEs        ; 0 LEs                ; 84 LEs
             ; Yes        ; |atm|amount[2]             ;
; 14:1               ; 2 bits    ; 18 LEs        ; 4 LEs                ; 14 LEs
             ; Yes        ; |atm|count[3][1]           ;
; 14:1               ; 2 bits    ; 18 LEs        ; 4 LEs                ; 14 LEs
             ; Yes        ; |atm|count[2][1]           ;
; 14:1               ; 2 bits    ; 18 LEs        ; 4 LEs                ; 14 LEs
             ; Yes        ; |atm|count[1][1]           ;
; 14:1               ; 2 bits    ; 18 LEs        ; 4 LEs                ; 14 LEs
             ; Yes        ; |atm|count[0][1]           ;
; 5:1                ; 18 bits   ; 54 LEs        ; 18 LEs               ; 36 LEs
             ; Yes        ; |atm|balance_database[3][8] ;
; 4:1                ; 19 bits   ; 38 LEs        ; 38 LEs               ; 0 LEs
             ; No         ; |atm|Mux5                  ;
; 32:1               ; 10 bits   ; 210 LEs       ; 90 LEs               ; 120 LEs
             ; No         ; |atm|Selector3             ;
+--------------------+-----------+---------------+----------------------+----------
--------------+------------+-----------------------------+


+-----------------------------------------------------------------+
; Parameter Settings for User Entity Instance: Clock_divider:clk_div ;
+----------------+--------------------------------+---------------+
; Parameter Name ; Value                          ; Type          ;
+----------------+--------------------------------+---------------+
```

; DIVISOR        ; 00000000000000000000000010 ; Unsigned Binary    ;
+---------------+------------------------------+--------------------+
Note: In order to hide this table in the UI and the text report file, please set the "Show Parameter Settings in Synthesis Report" option in "Analysis and Synthesis Settings -> More Settings" to "Off".

+-----------------------------------------------------+
; Post-Synthesis Netlist Statistics for Top Partition ;
+----------------------+------------------------------+
; Type                 ; Count                        ;
+----------------------+------------------------------+
; arriav_ff            ; 199                          ;
;     CLR              ; 10                           ;
;     ENA              ; 26                           ;
;     ENA CLR          ; 26                           ;
;     ENA CLR SCLR     ; 72                           ;
;     ENA SCLR         ; 13                           ;
;     ENA SLD          ; 46                           ;
;     plain            ; 6                            ;
; arriav_lcell_comb    ; 419                          ;
;     arith            ; 105                          ;
;         0 data inputs ; 1                           ;
;         1 data inputs ; 78                          ;
;         5 data inputs ; 26                          ;
;     extend           ; 1                            ;
;         7 data inputs ; 1                           ;
;     normal           ; 313                          ;
;         2 data inputs ; 14                          ;
;         3 data inputs ; 100                         ;
;         4 data inputs ; 68                          ;
;         5 data inputs ; 58                          ;
;         6 data inputs ; 73                          ;
; arriav_mac           ; 1                            ;
; boundary_port        ; 34                           ;
;                      ;                              ;
; Max LUT depth        ; 6.00                         ;
; Average LUT depth    ; 3.97                         ;
+----------------------+------------------------------+

+-------------------------------+
; Elapsed Time Per Partition    ;
+----------------+--------------+
; Partition Name ; Elapsed Time ;
+----------------+--------------+
; Top            ; 00:00:01     ;
+----------------+--------------+

```
+-------------------------------+
; Analysis & Synthesis Messages ;
+-------------------------------+
Info: *******************************************************************
Info: Running Quartus Prime Analysis & Synthesis
    Info: Version 22.1std.1 Build 917 02/14/2023 SC Lite Edition
    Info: Processing started: Fri Jul 14 19:15:46 2023
Info: Command: quartus_map --read_settings_files=on --write_settings_files=off atm
-c atm
Warning (18236): Number of processors has not been specified which may cause
overloading on shared machines.  Set the global assignment NUM_PARALLEL_PROCESSORS
in your QSF to an appropriate value for best performance.
Info (20030): Parallel compilation is enabled and will use 6 of the 6 processors
detected
Info (12021): Found 1 design units, including 1 entities, in source file atm.v
    Info (12023): Found entity 1: atm File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 2
Info (12021): Found 1 design units, including 1 entities, in source file atm_tb.v
    Info (12023): Found entity 1: atm_tb File: D:/INTEL UNNATI/Atm_mini/atm_tb.v
Line: 2
Info (12021): Found 1 design units, including 1 entities, in source file
clock_divider.v
    Info (12023): Found entity 1: Clock_divider File: D:/INTEL
UNNATI/Atm_mini/Clock_divider.v Line: 1
Info (12127): Elaborating entity "atm" for the top level hierarchy
Warning (10036): Verilog HDL or VHDL warning at atm.v(49): object
"statement_success" assigned a value but never read File: D:/INTEL
UNNATI/Atm_mini/atm.v Line: 49
Info (10648): Verilog HDL Display System Task info at atm.v(77): Welcome to the ATM
File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 77
Warning (10230): Verilog HDL assignment warning at atm.v(201): truncated value with
size 32 to match size of target (2) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 201
Warning (10230): Verilog HDL assignment warning at atm.v(249): truncated value with
size 32 to match size of target (2) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 249
Warning (10230): Verilog HDL assignment warning at atm.v(283): truncated value with
size 32 to match size of target (2) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 283
Warning (10230): Verilog HDL assignment warning at atm.v(316): truncated value with
size 32 to match size of target (2) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 316
Warning (10230): Verilog HDL assignment warning at atm.v(356): truncated value with
size 32 to match size of target (16) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 356
Warning (10230): Verilog HDL assignment warning at atm.v(394): truncated value with
size 32 to match size of target (3) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 394
Warning (10230): Verilog HDL assignment warning at atm.v(420): truncated value with
size 32 to match size of target (16) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 420
Warning (10230): Verilog HDL assignment warning at atm.v(457): truncated value with
size 32 to match size of target (3) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 457
Warning (10230): Verilog HDL assignment warning at atm.v(505): truncated value with
size 32 to match size of target (24) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 505
Warning (10230): Verilog HDL assignment warning at atm.v(514): truncated value with
size 32 to match size of target (24) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 514
Warning (10230): Verilog HDL assignment warning at atm.v(523): truncated value with
```

size 32 to match size of target (24) File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 523
Warning (10030): Net "pin_database.data_a" at atm.v(40) has no driver or initial value, using a default initial value '0' File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 40
Warning (10030): Net "pin_database.waddr_a" at atm.v(40) has no driver or initial value, using a default initial value '0' File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 40
Warning (10030): Net "pin_database.we_a" at atm.v(40) has no driver or initial value, using a default initial value '0' File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 40
Info (12128): Elaborating entity "Clock_divider" for hierarchy "Clock_divider:clk_div" File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 23
Warning (10036): Verilog HDL or VHDL warning at Clock_divider.v(6): object "clock_out" assigned a value but never read File: D:/INTEL UNNATI/Atm_mini/Clock_divider.v Line: 6
Info (276014): Found 1 instances of uninferred RAM logic
    Info (276004): RAM logic "pin_database" is uninferred due to inappropriate RAM size File: D:/INTEL UNNATI/Atm_mini/atm.v Line: 40
Info (286030): Timing-Driven Synthesis is running
Info (17049): 4 registers lost all their fanouts during netlist optimizations.
Info (144001): Generated suppressed messages file D:/INTEL UNNATI/Atm_mini/output_files/atm.map.smsg
Info (16010): Generating hard_block partition "hard_block:auto_generated_inst"
    Info (16011): Adding 0 node(s), including 0 DDIO, 0 PLL, 0 transceiver and 0 LCELL
Info (21057): Implemented 477 device resources after synthesis - the final resource count might be different
    Info (21058): Implemented 15 input pins
    Info (21059): Implemented 19 output pins
    Info (21061): Implemented 442 logic cells
    Info (21062): Implemented 1 DSP elements
Info: Quartus Prime Analysis & Synthesis was successful. 0 errors, 17 warnings
    Info: Peak virtual memory: 4893 megabytes
    Info: Processing ended: Fri Jul 14 19:15:55 2023
    Info: Elapsed time: 00:00:09
    Info: Total CPU time (on all processors): 00:00:10


+----------------------------------------+
; Analysis & Synthesis Suppressed Messages ;
+----------------------------------------+
The suppressed messages can be found in D:/INTEL UNNATI/Atm_mini/atm.map.smsg.