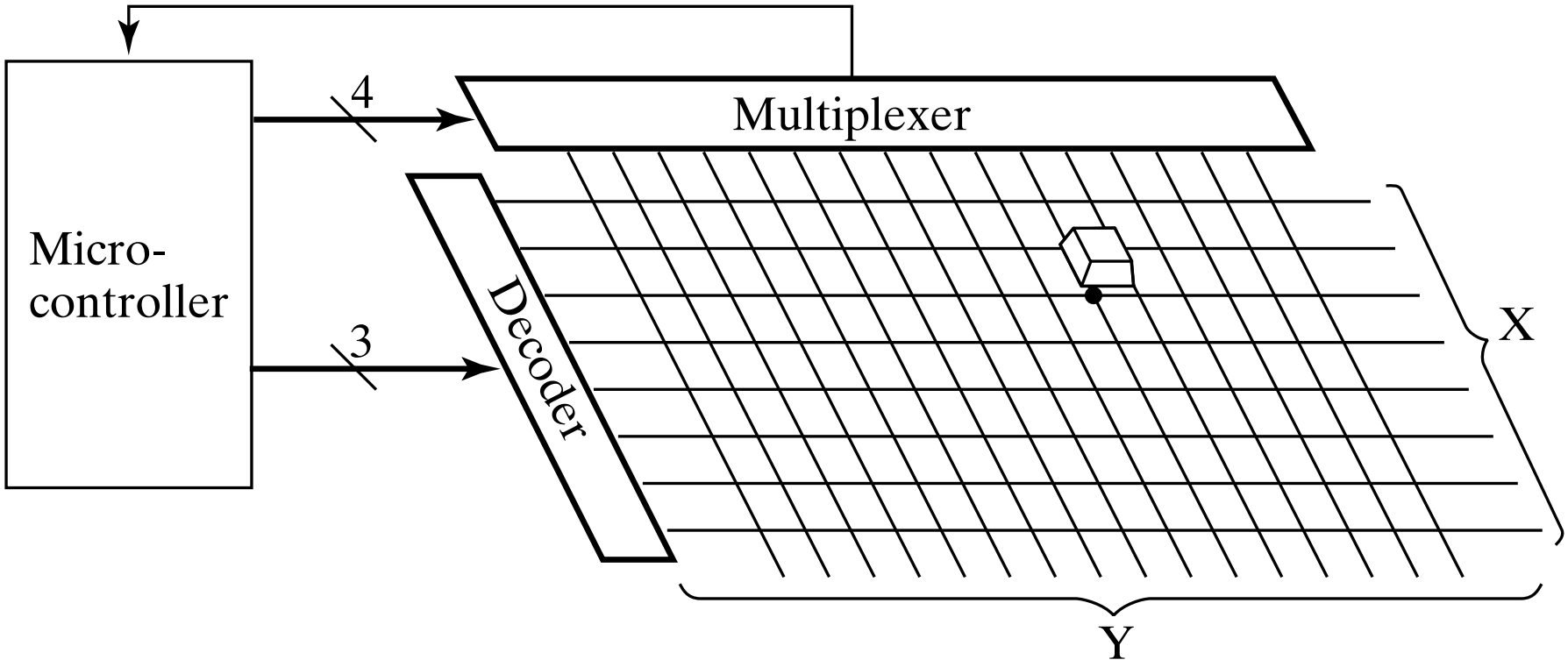
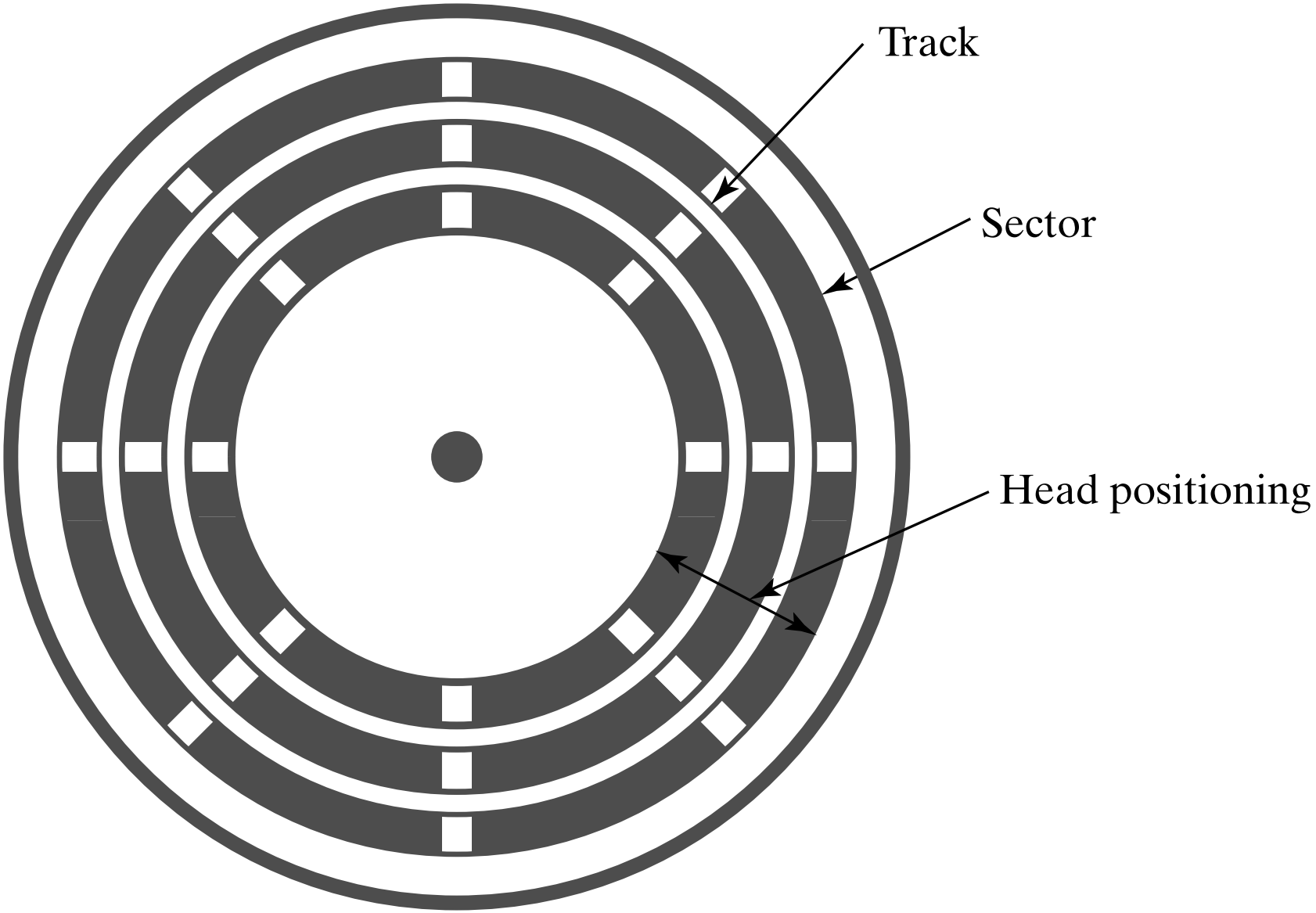
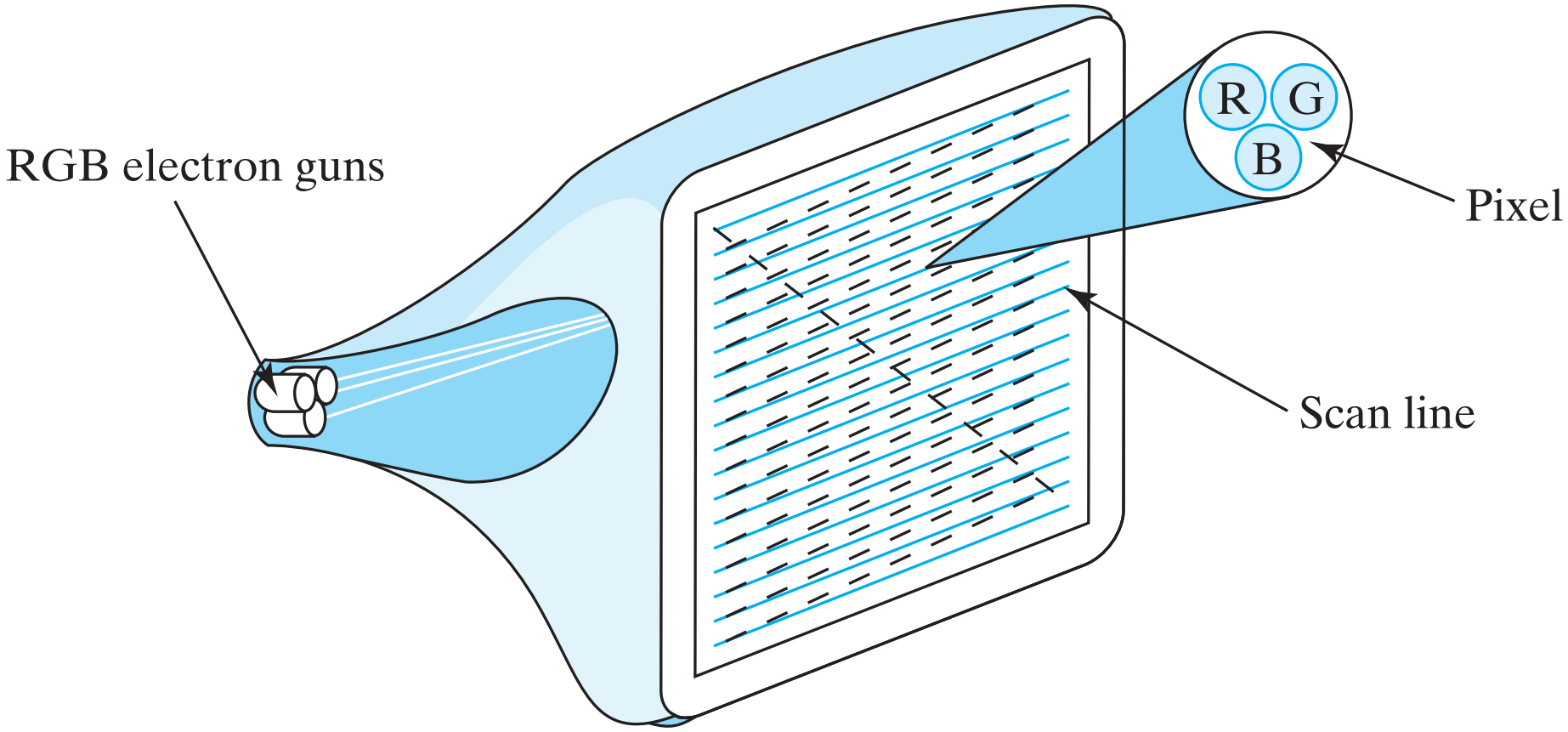
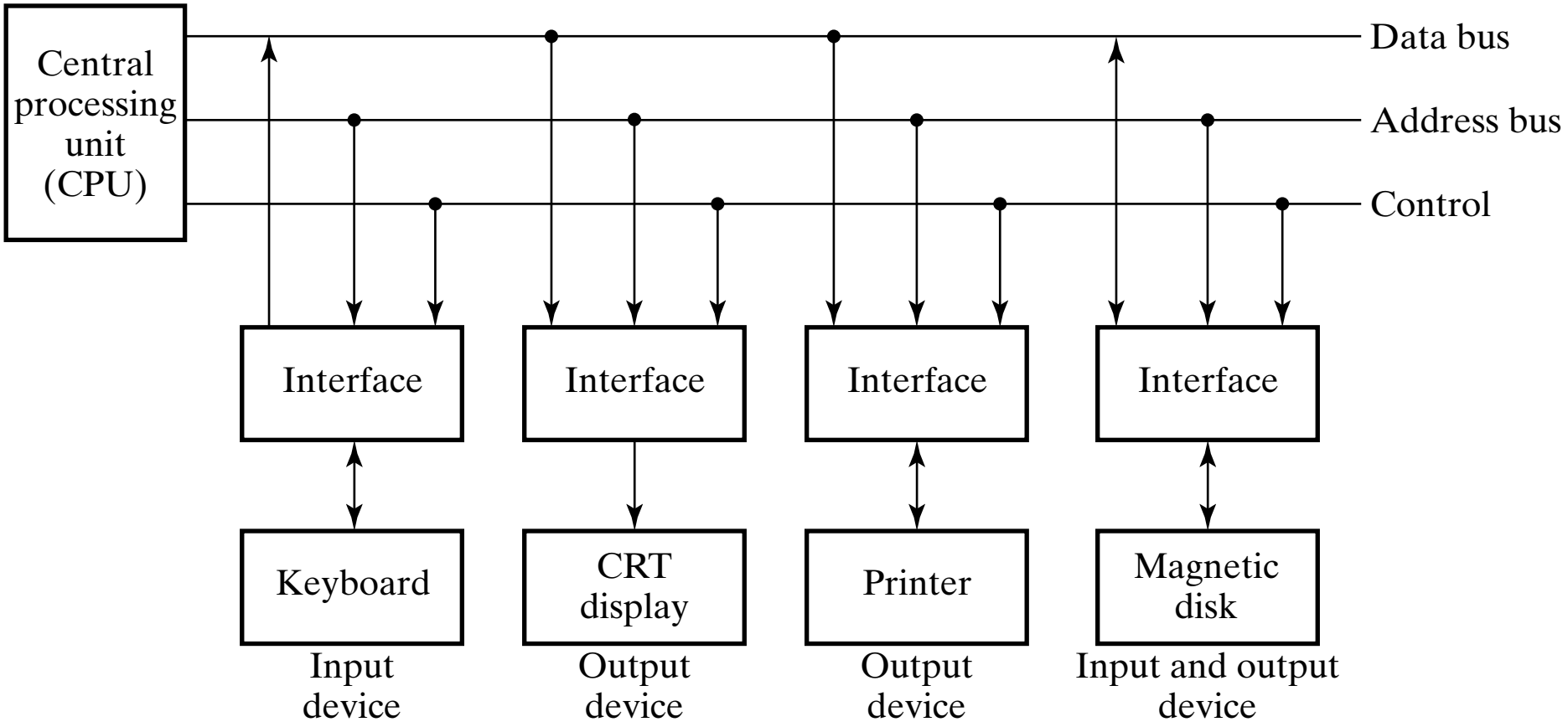
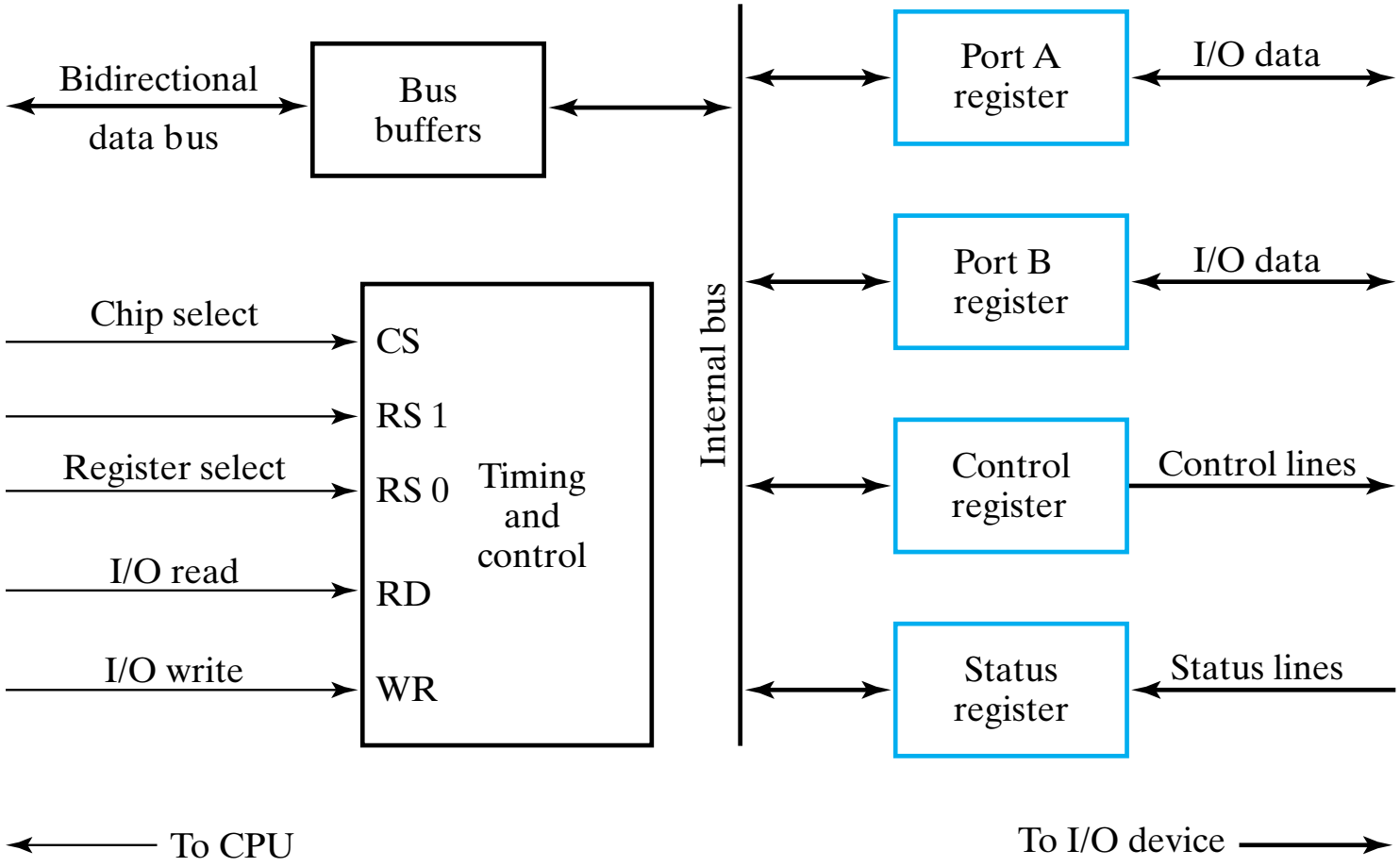


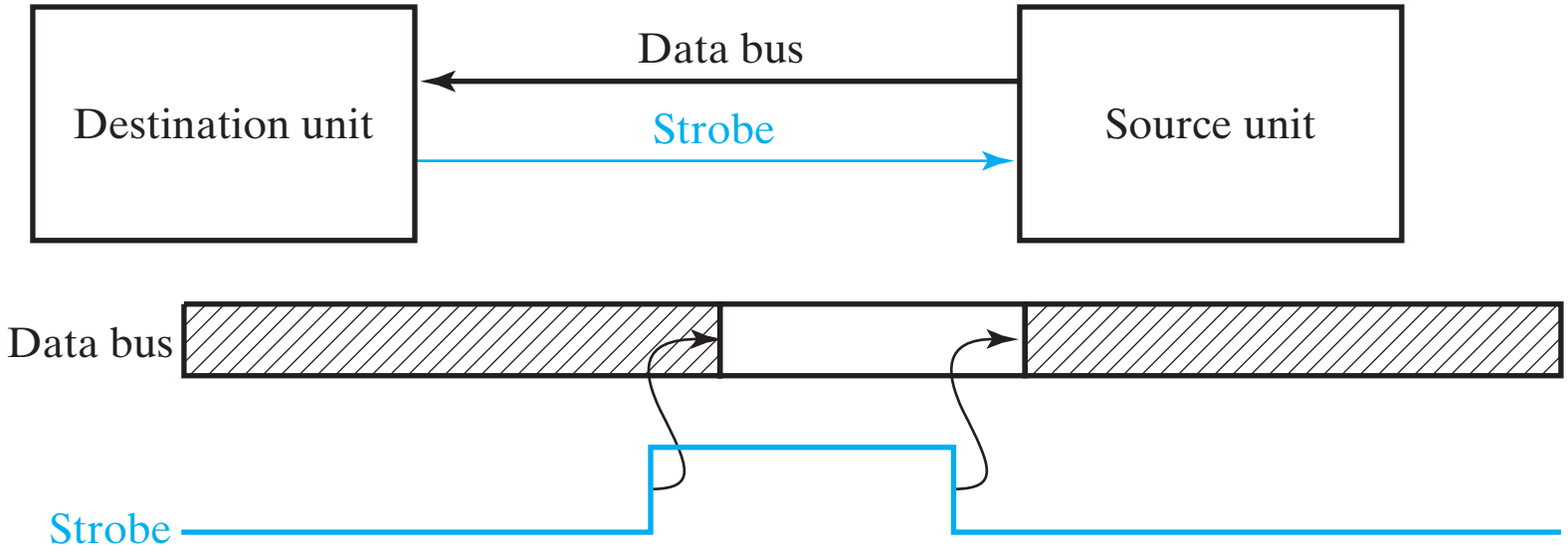




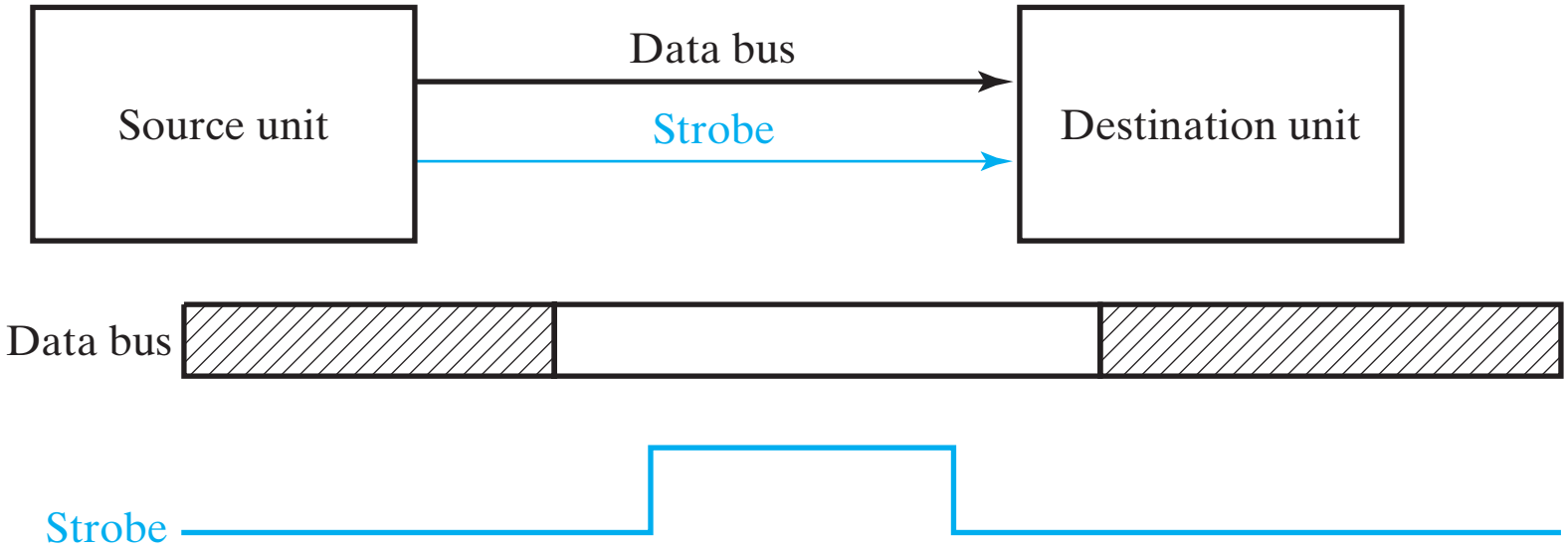




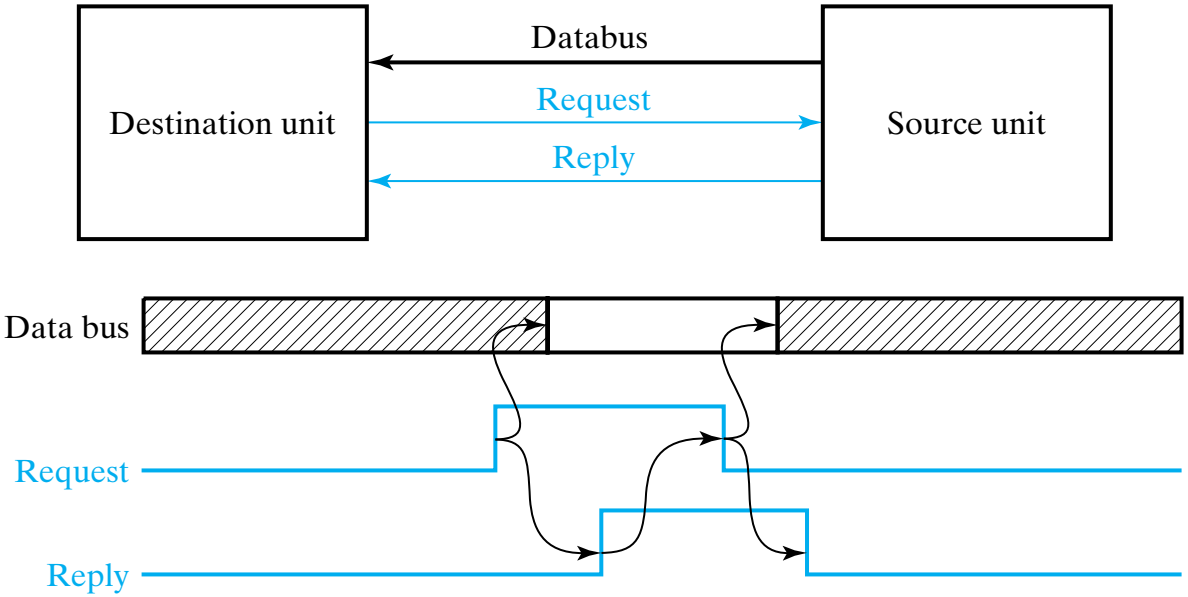
CS	RS1	RS0	Register selected
0	x	x	None: data bus in high-impedance state
1	0	0	Port A register
1	0	1	Port B register
1	1	0	Control register
1	1	1	Status register



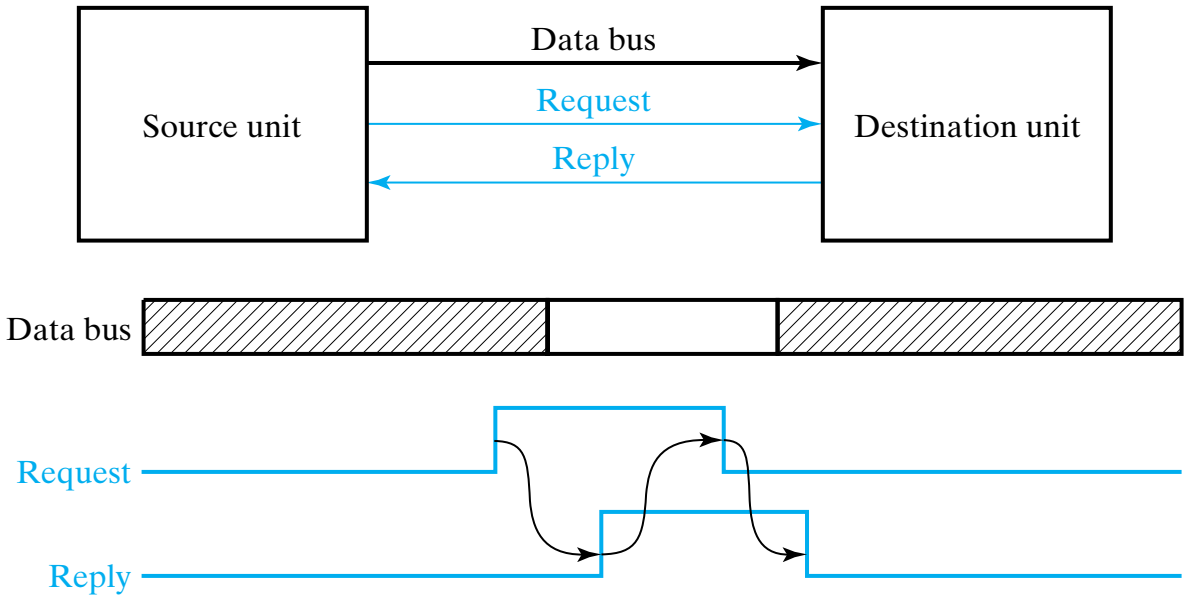
(a) Destination-initiated transfer



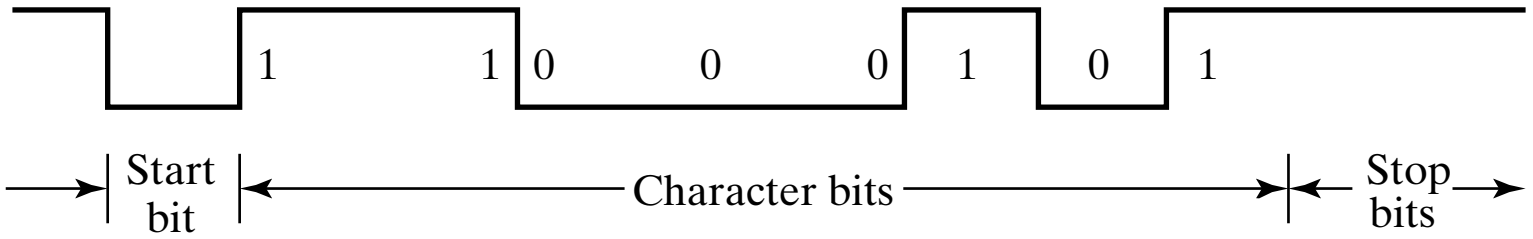
(b) Source-initiated transfer

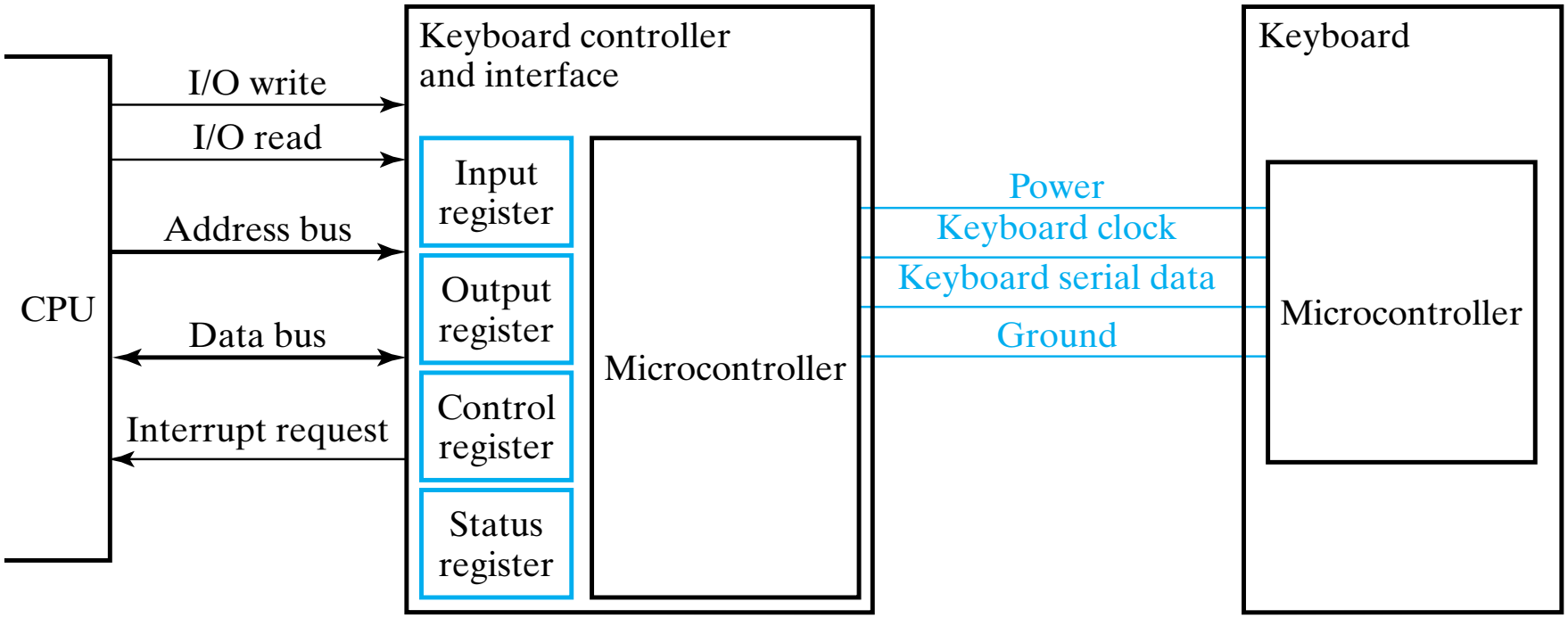


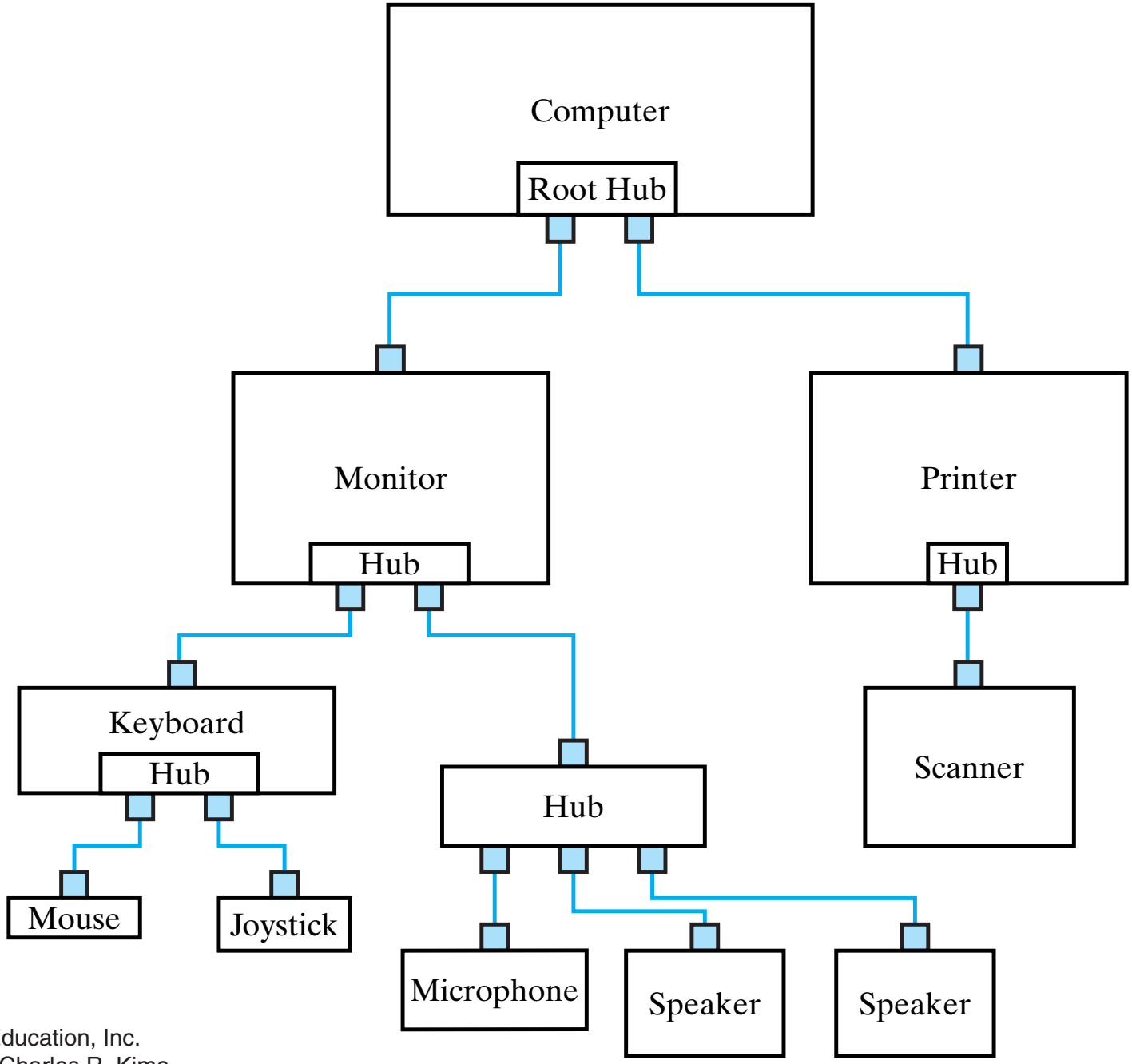
(a) Destination-initiated transfer

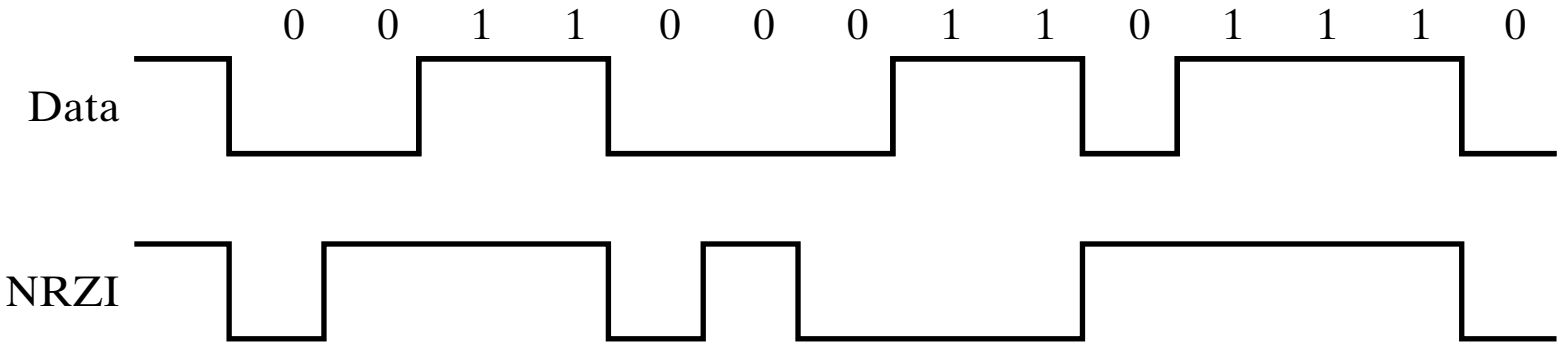


(b) Source-initiated transfer





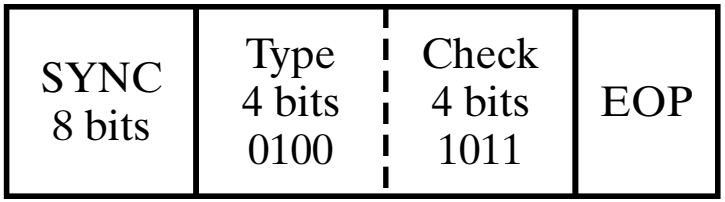




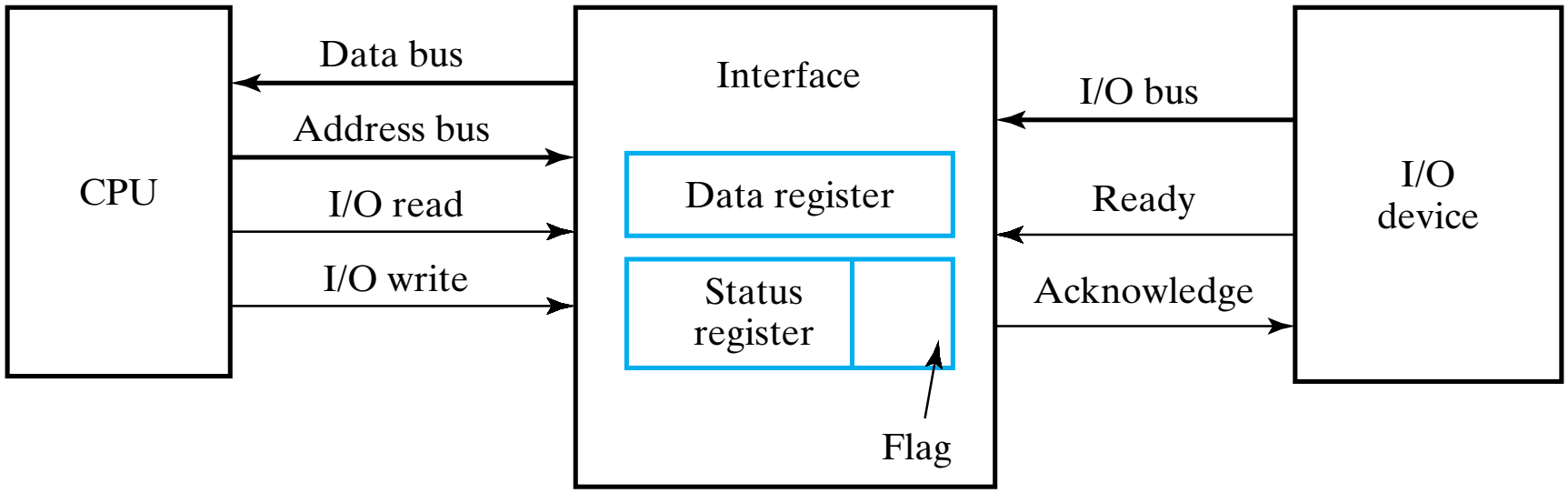
(a) General packet format

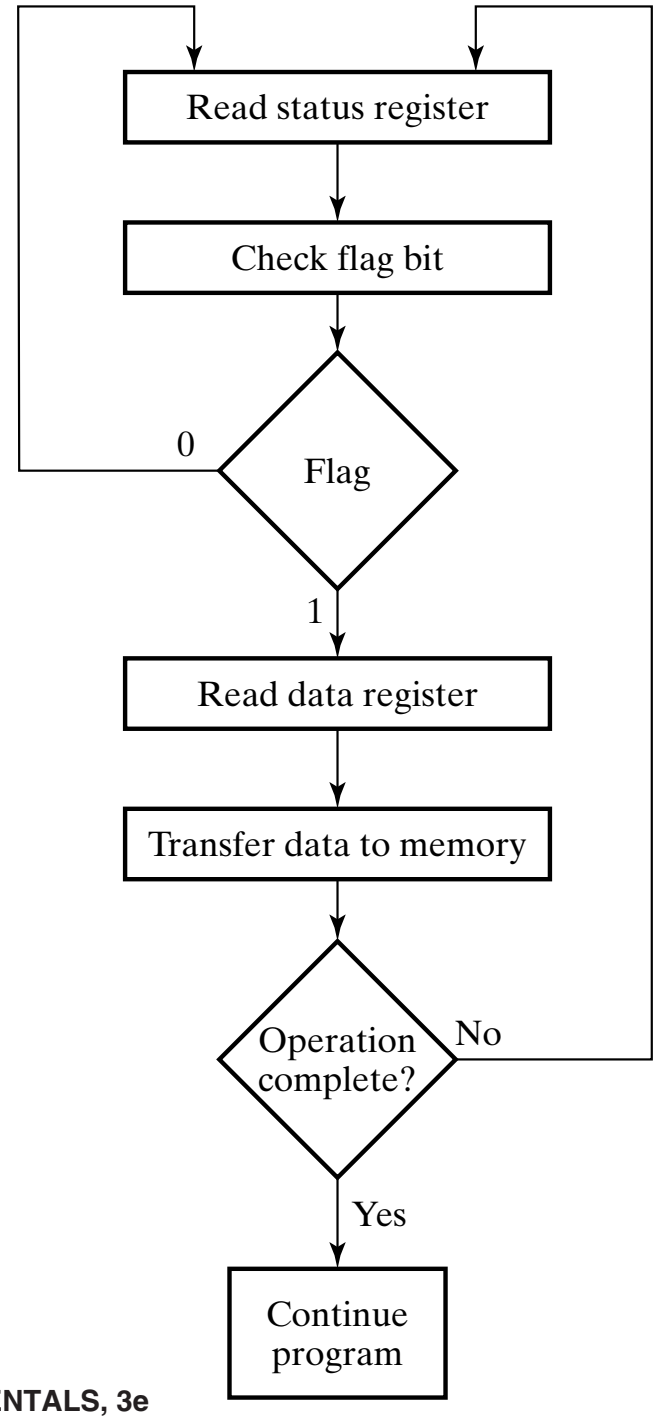
(b) Output packet

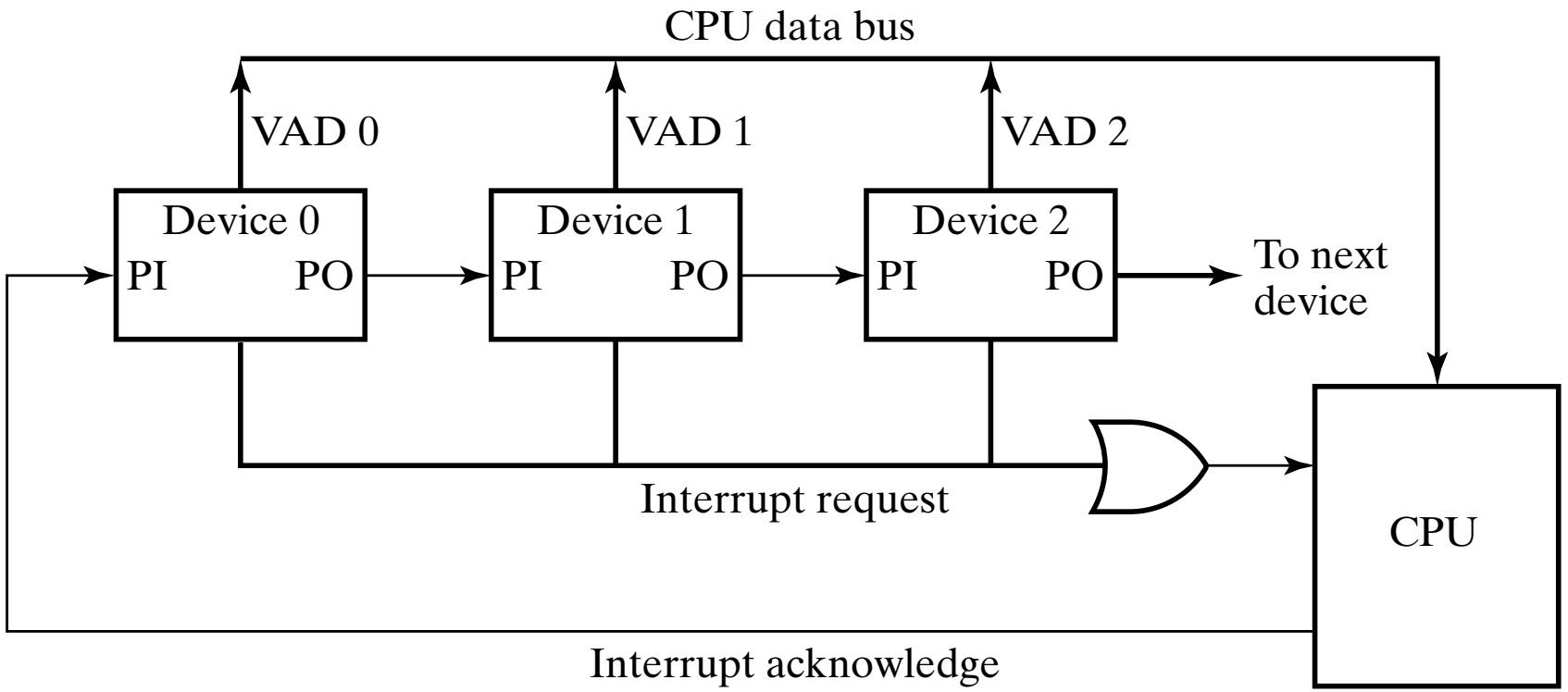
(c) Data packet (Data0 type)

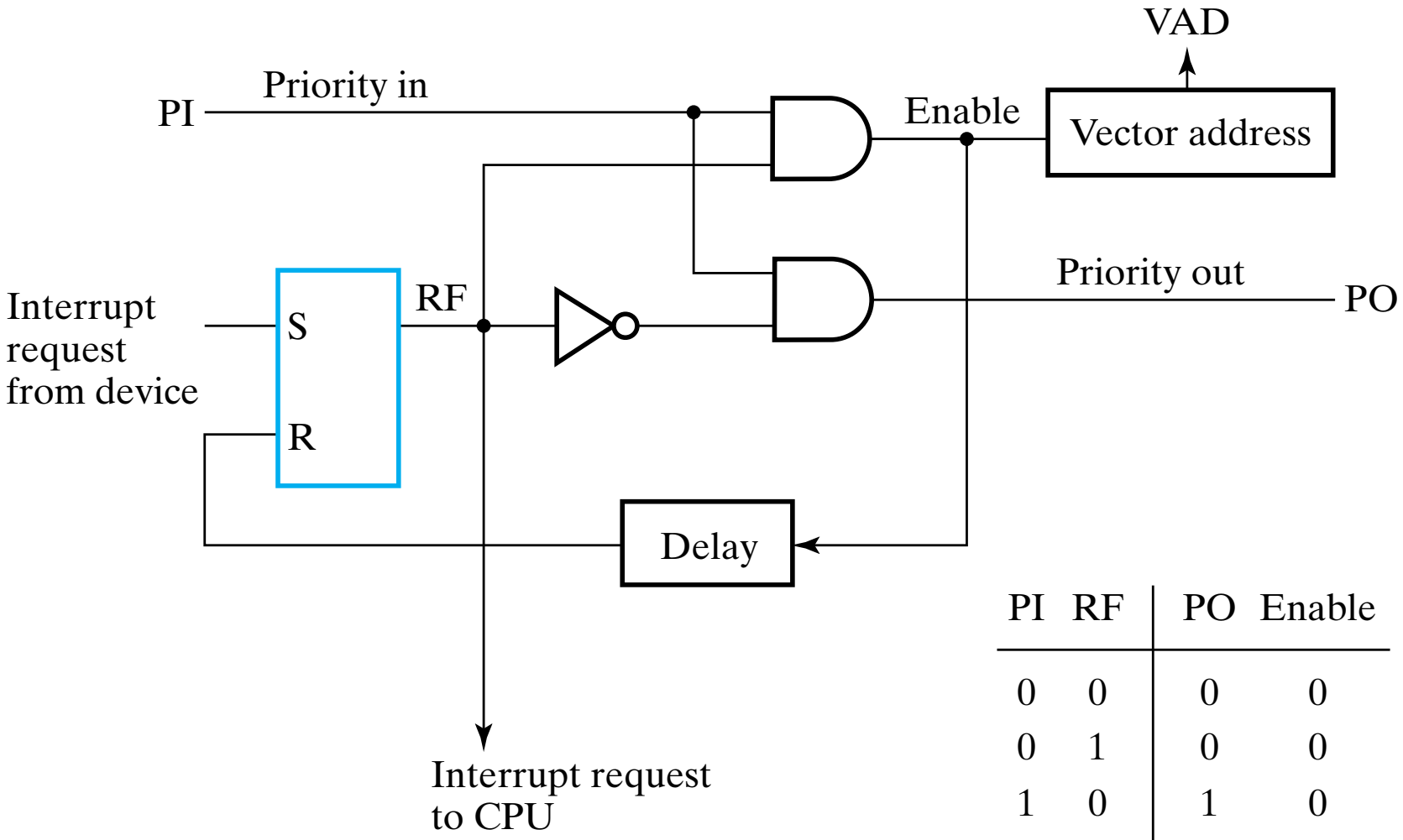


(d) Handshake packet (Acknowledge type)









PI	RF	PO	Enable
0	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1