SDLS027

SN5402, SN54LS02, SN54S02,
SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES
DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs

- Dependable Texas Instruments Quality and Reliability

description

These devices contain four independent 2-input-NOR gates.

The SN5402, SN54LS02, and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02, and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic symbol†

1A (2)
1B (3)
≥1
(1) 1Y
2A (5)
2B (6)
(4) 2Y
3A (8)
3B (9)
(10) 3Y
4A (11)
4B (12)
(13) 4Y
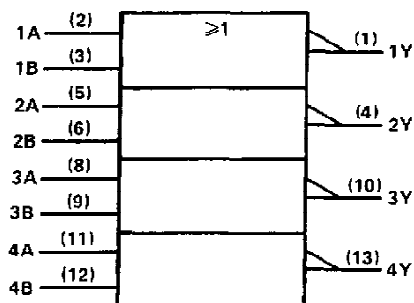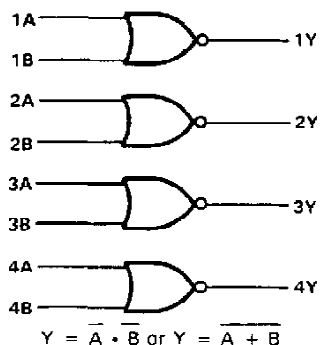
†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

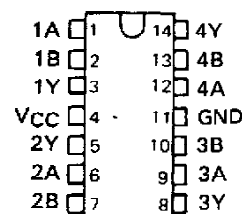### logic diagram (positive logic)

1A
1B
1Y

2A
2B
2Y

3A
3B
3Y

4A
4B
4Y

Y = $\overline{A \cdot B}$ or Y = $\overline{A + B}$

SN5402 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . N PACKAGE
SN74LS02, SN74S02 . . . D OR N PACKAGE
(TOP VIEW)

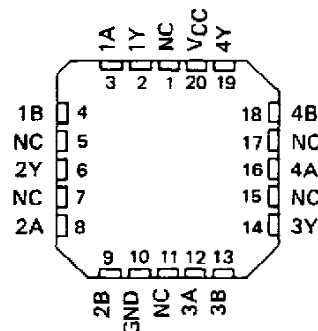|		
1Y	1	14	VCC
1A	2	13	4Y
1B	3	12	4B
2Y	4	11	4A
2A	5	10	3Y
2B	6	9	3B
GND	7	8	3A
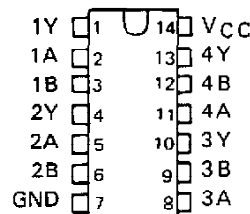
SN5402 . . . W PACKAGE
(TOP VIEW)

1A	1	14	4Y
1B	2	13	4B
1Y	3	12	4A
VCC	4	11	GND
2Y	5	10	3B
2A	6	9	3A
2B	7	8	3Y

SN54LS02, SN54S02 . . . FK PACKAGE
(TOP VIEW)

1A 1Y NC VCC 4Y
3   2   1   20   19

1B   4   18   4B
NC   5   17   NC
2Y   6   16   4A
NC   7   15   NC
2A   8   14   3Y

9 10 11 12 13
2B GND NC 3A 3B

NC - No internal connection

TEXAS
INSTRUMENTS

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SN5402, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

schematics (each gate)

'02

'LS02

'S02

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage: '02, 'S02 . . . . 5.5 V
             'LS02 . . . . 7 V
Off-state output voltage . . . . 7 V
Operating free-air temperature range: SN54' . . . . −55°C to 125°C
                                  SN74' . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5402			SN7402			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN5402			SN7402			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −12 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX			−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			8	16		8	16	mA
I_{CCL}	V_{CC} = MAX,	See Note 2			14	27		14	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω,	C_L = 15 pF		12	22	ns
t_{PHL}						8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS02			SN74LS02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			− 0.4			− 0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †			SN54LS02			SN74LS02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = − 18 mA				− 1.5			− 1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = − 0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				− 0.4			− 0.4	mA
I_{OS}§	V_{CC} = MAX			− 20		− 100	− 20		− 100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.6	3.2		1.6	3.2	mA
I_{CCL}	V_{CC} = MAX,	See Note 2			2.8	5.4		2.8	5.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ,	C_L = 15 pF		10	15	ns
t_{PHL}						10	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54S02 MIN	SN54S02 NOM	SN54S02 MAX	SN74S02 MIN	SN74S02 NOM	SN74S02 MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †		SN54S02 MIN	SN54S02 TYP‡	SN54S02 MAX	SN74S02 MIN	SN74S02 TYP‡	SN74S02 MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−2			−2	mA
I_{OS} §	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V		17	29		17	29	mA
I_{CCL}	V_{CC} = MAX,	See Note 2		26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω,	C_L = 15 pF			3.5	5.5	ns
t_{PHL}							3.5	5.5	ns
t_{PLH}			R_L = 280 Ω,	C_L = 50 pF			5		ns
t_{PHL}							5		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
JM38510/00401BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/00401BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/07301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/07301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301B2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301BCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301BDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301SCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301SCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
JM38510/30301SDA	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
SN5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SN5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SN54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SN54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SN54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SN7402N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7402N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7402N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7402N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7402NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN7402NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LS02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS02J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN74LS02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS02N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74LS02NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS02NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74S02DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S02DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI
SN74S02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S02N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S02N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S02N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74S02NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74S02NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ5402J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ5402W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
SNJ5402W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS02FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SNJ54LS02FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS02W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54LS02W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54S02FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54S02FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54S02J	ACTIVE	CDIP	J	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54S02W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type
SNJ54S02W	ACTIVE	CFP	W	14	1	TBD	Call TI	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

A

0°−15°

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package is hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
          E.   Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R−GDFP−F14)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.260 (6,60)
0.235 (5,97)

0.080 (2,03)
0.045 (1,14)

0.006 (0,15)
0.004 (0,10)

0.280 (7,11) MAX

0.019 (0,48)
0.015 (0,38)

1   14

0.050 (1,27)

0.390 (9,91)
0.335 (8,51)

0.005 (0,13) MIN
4 Places

7   8

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

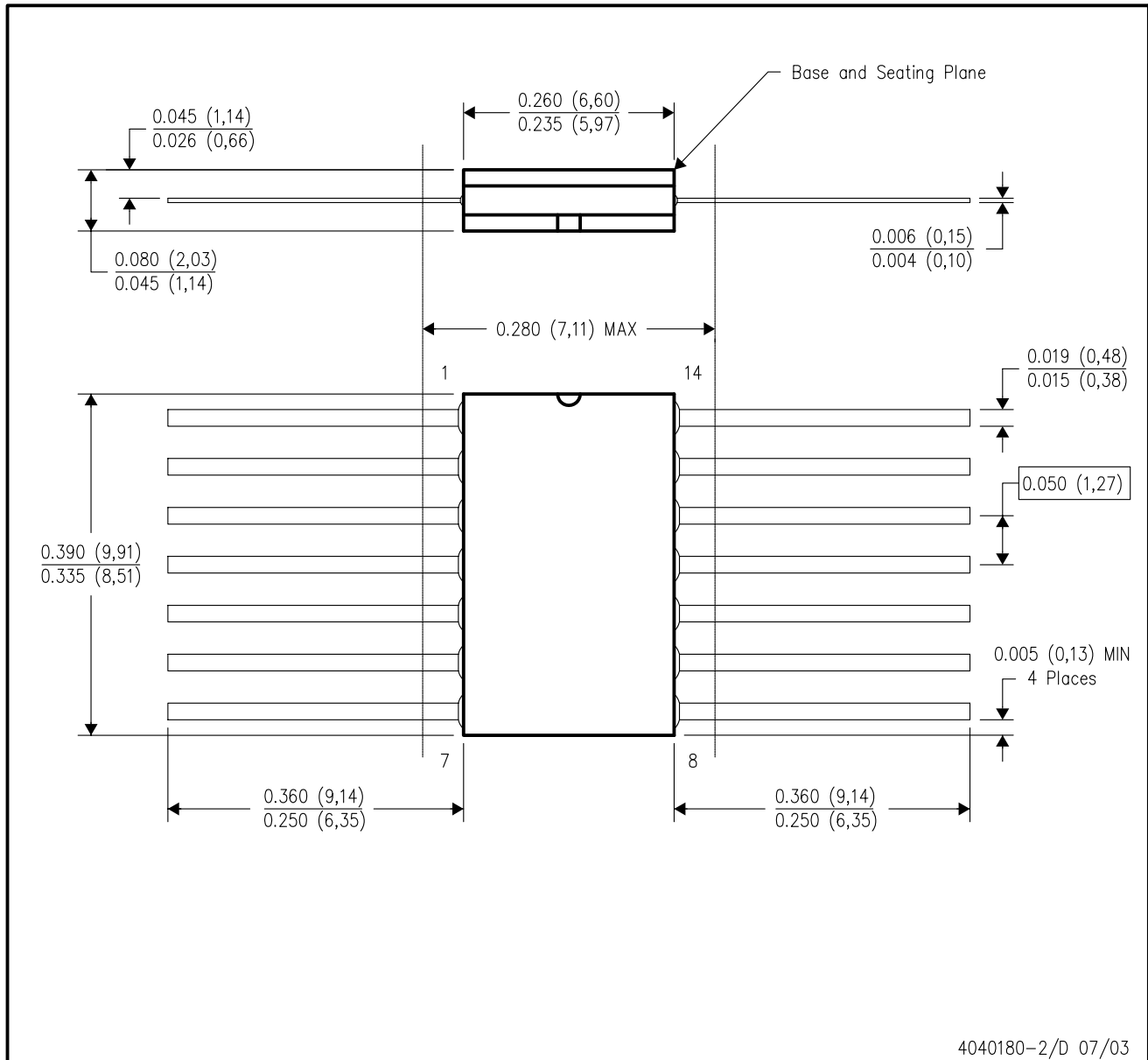4040180−2/D 07/03

NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   This package can be hermetically sealed with a ceramic lid using glass frit.
          D.   Index point is provided on cap for terminal identification only.
          E.   Falls within MIL STD 1835 GDFP1−F14 and JEDEC MO−092AB

MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) D

0.045 (1,14)
0.030 (0,76) D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) M

14/18 Pin Only
20 Pin vendor option D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane
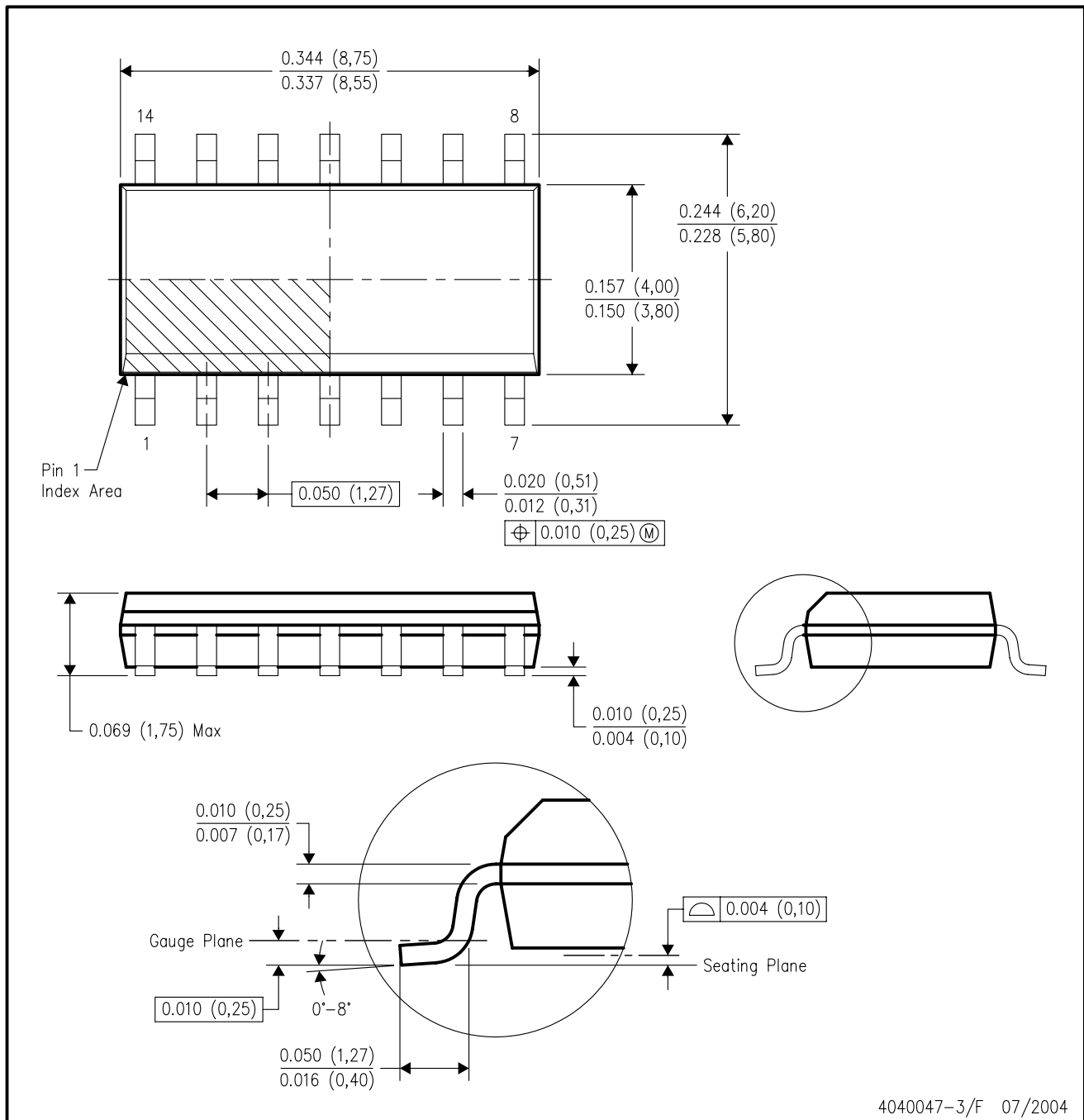
0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R−PDSO−G14)   PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

14

8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1

7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/F   07/2004

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−012 variation AB.

NS (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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