CHAPTER 2
MEMORY AND INPUT/OUTPUT CYCLE TIMING

2.1 INTRODUCTION

This section explains the bus operation of the Z80185/195 and the signaling and timing associated with them.

2.2 BASIC TIMING

The basic CPU operation consists of one or more "Machine Cycles" (MC). A machine cycle consists of an access to internal or external memory or I/O, and includes at least three system clocks called T_1, T_2, and T_3. Optional wait states can be inserted between T_2 and T_3, either by one of the on-chip wait state generators or by external logic driving the $\overline{WAIT}$ pin. In this manual, externally-idle system clocks, during the execution of an instruction, are not considered machine cycles. Thus, the execution of an instruction includes one or more machine cycles and for some instructions one or more externally-idle system clocks.

A system clock cycle may be one or two cycles on the XTAL pin(s), depending on the clock divide option in the CPU Control Register (CCR), as described in the later CPU Options section.

To avoid undue complexity at this point, the following descriptions and waveforms assume that the MIE and IOC bits in the Operating Mode Control Register (OMCR) are both 1. The later CPU Options section, describes the effects of setting these bits differently.

Instruction (op-code) Fetch Timing. Figure 2-1 shows the instruction (op-code) fetch timing with no wait states. An op-code fetch cycle is externally indicated when the $\overline{M1}$ output pin is Low.

In the first half of T_1, the address bus (A19-A0) is driven from the contents of the Program Counter (PC). Note that this is the translated address output of the on-chip MMU.

In the second half of T_1, the $\overline{MREQ}$ (Memory Request) and $\overline{RD}$ (Read) signals are asserted Low, enabling the memory.

The op-code on the data bus is latched at the rising edge of T_3 and the bus cycle terminates at the end of T_3.

Figure 2.2 illustrates the insertion of wait states (Tw) into the op-code fetch cycle. Wait states (Tw) are controlled by the external $\overline{WAIT}$ input combined with on-chip programmable wait state generators. At the falling edge of T_2 the combined $\overline{WAIT}$ input is sampled. If $\overline{WAIT}$ input is asserted Low, a wait state (Tw) is inserted. The address bus, $\overline{MREQ}$, $\overline{RD}$ and $\overline{M1}$ are held stable during wait states. When the WAIT is sampled inactive High at the falling edge of Tw, the bus cycle enters T_3 and completes at the end of T_3.

2.2 BASIC TIMING (Continued)

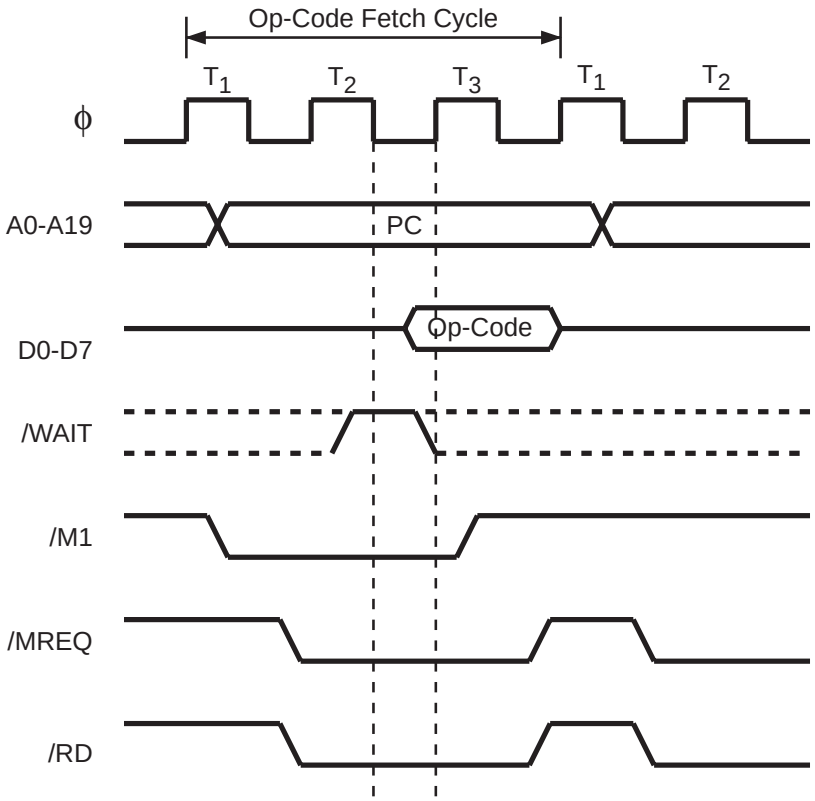


Figure 2-1. Op-code Fetch Timing (without Wait State)

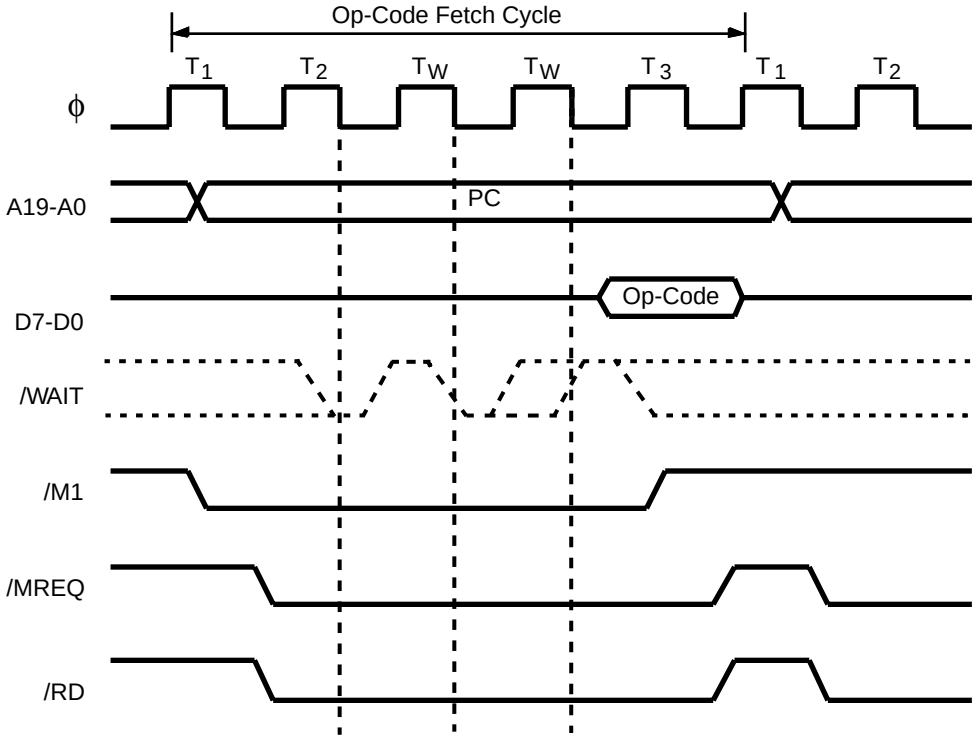


Figure 2-2. Op-code Fetch Timing (with Wait State)

Operand and Data Read/Write Timing. The instruction operand and data read/write timing differs from op-code fetch timing in two ways. First, the $\overline{M1}$ output is held inactive. Second, the read cycle timing is relaxed by one-half clock cycle since data is latched at the falling edge of T_3.

Instruction operands include immediate data, displacement, and extended addresses, and have the same timing as memory data reads.

During memory write cycles the $\overline{MREQ}$ signal goes active in the second half of T_1, the data bus is driven with the write data.

At the start of T_2, the $\overline{WR}$ signal is asserted Low enabling the memory. $\overline{MREQ}$ and $\overline{WR}$ go inactive in the second half of T_3 followed by disabling of the write data on the data bus.

Wait states (Tw) are inserted as previously described for op-code fetch cycles. Figure 2.3 illustrates the read/write timing without wait states (Tw), while Figure 2.4 illustrates read/write timing with wait states (Tw).

2.2 BASIC TIMING (Continued)

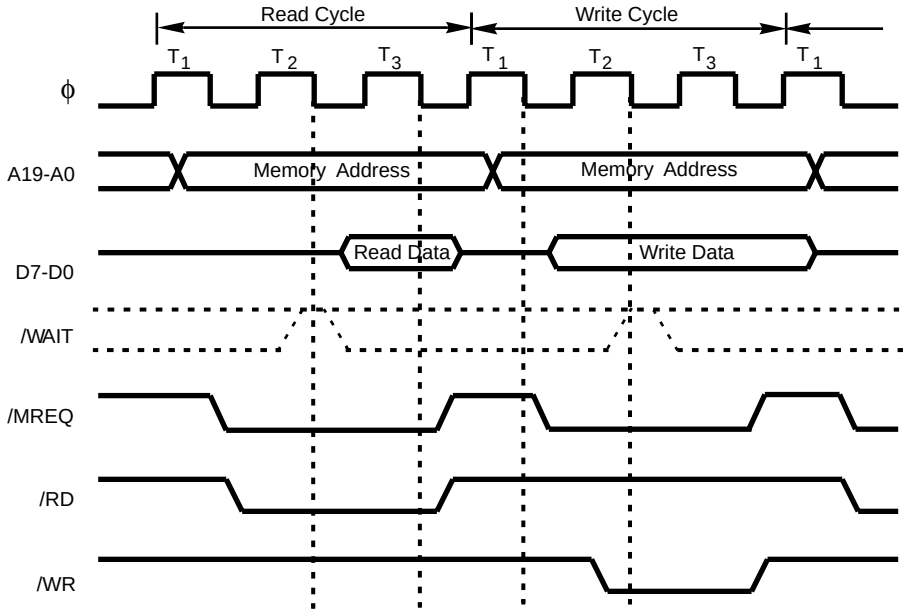


Figure 2-3. Memory Read/Write Timing (without Wait State)

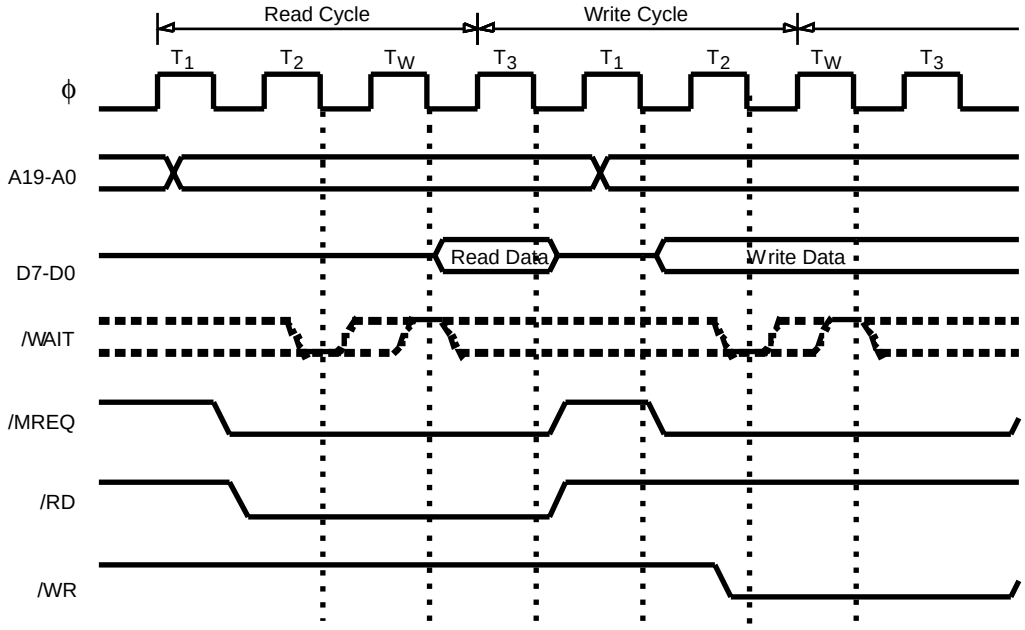


Figure 2-4. Memory Read/Write Timing (with Wait State)

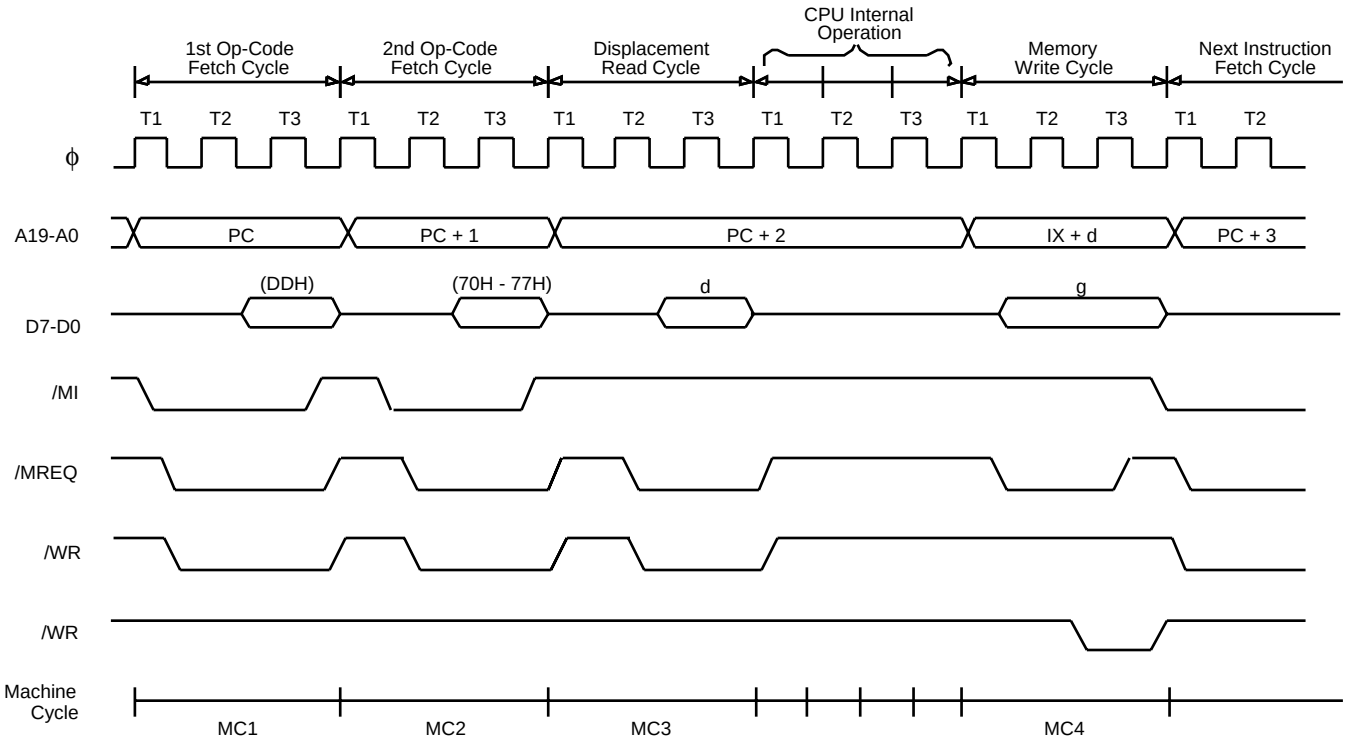
Basic Instruction Timing. An instruction may consist of a number of machine cycles including op-code fetch, operand fetch, and data read/write cycles. An instruction may also include clock cycles for internal processes which make the bus idle.

The example in Figure 2.5 illustrates the bus timing for the data transfer instruction (LD (IX+d),g. This instruction moves the contents of a CPU register (g) to the memory location with address computed by adding a signed 8-bit displacement (d) to the contents of an index register (IX).

The instruction cycle starts with the two machine cycles to read the two byte instruction op-code as indicated by $\overline{M1}$ Low. Next, the instruction operand (d) is fetched.

The external bus is idle while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing. Figure 2.6 shows the Z80185 hardware RESET timing. If the $\overline{RESET}$ pin is Low for six or more clock cycles, processing is terminated and the Z80180 restarts execution from (logical and physical) address 00000H.



Note: d = displacement
g = regulat contents

Figure 2-5. Instruction Timing

2.2 BASIC TIMING (Continued)

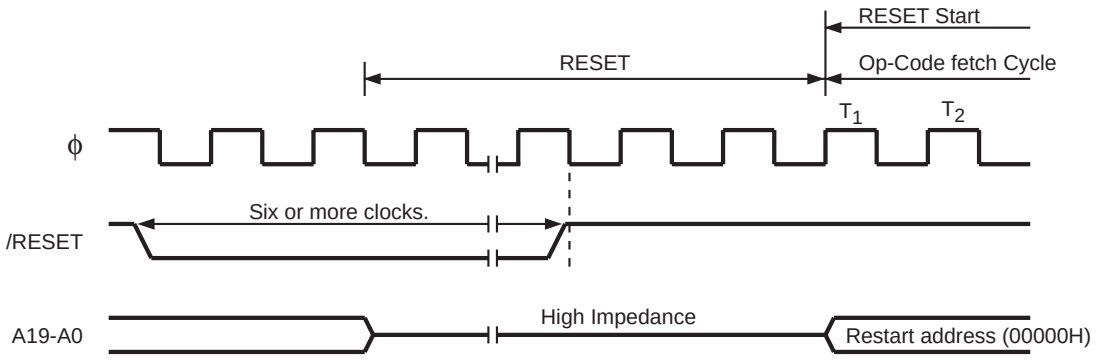


Figure 2-6. Reset Timing

$\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ Bus Exchange Timing. The Z80185 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the $\overline{\text{BUSREQ}}$ (Bus Request) input Low. After the Z80185 releases the bus, it relinquishes control to the alternate bus master by asserting the $\overline{\text{BUSACK}}$ (Bus Acknowledge) output Low.

The bus may be released by the Z80185 at the end of a machine cycle or an externally-idle clock cycle.

When the bus is released, the address (A1-A19), data (D0-D7), and control ($\overline{\text{MREQ}}$, $\overline{\text{IORG}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) signals are placed in the high impedance state.

Note that dynamic RAM refresh is not performed when the Z80185 has released the bus. The alternate bus master must provide dynamic memory refreshing if the bus is released for long periods of time.

Figure 2.7 illustrates $\overline{\text{BUSREQ}}$/$\overline{\text{BUSACK}}$ bus exchange during a memory read cycle. Figure 2.8 illustrates bus exchange when the bus release is requested during a Z80185 CPU internal operation. $\overline{\text{BUSREQ}}$ is sampled at the falling edge of the system clock prior to T_3, Ti and Tx (BUS RELEASE state). If $\overline{\text{BUSREQ}}$ is asserted Low at the falling edge of the clock state prior to Tx, another Tx is executed.

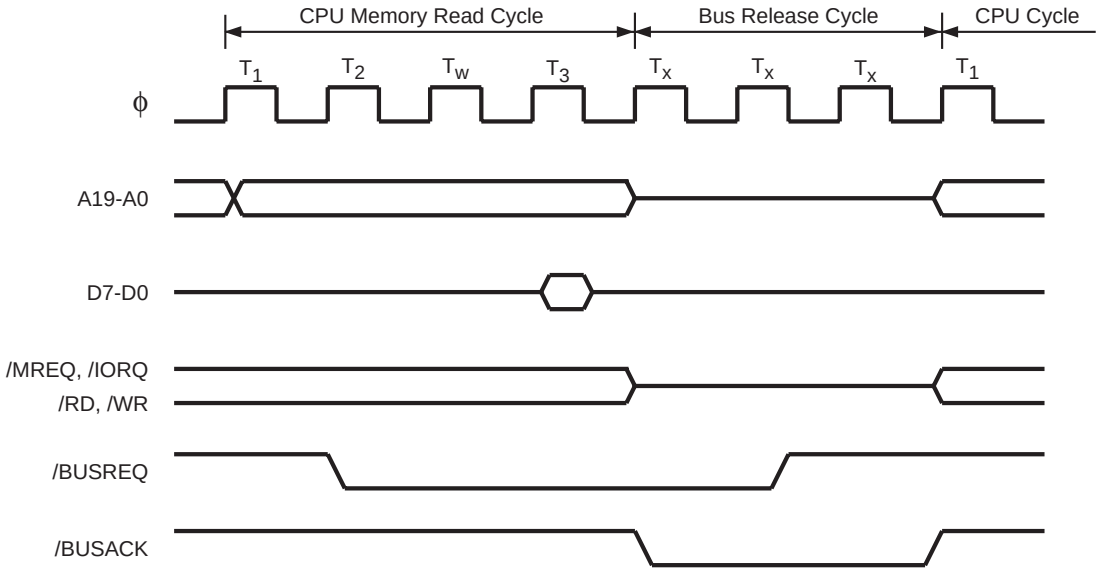


Figure 2-7. Bus Exchange Timing (Memory Read Cycle)

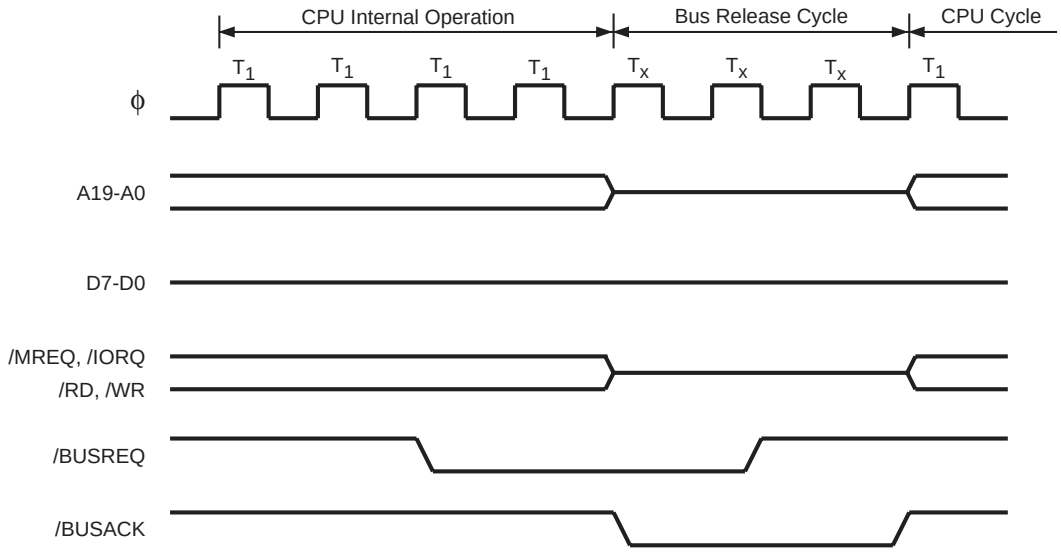


Figure 2-8. Bus Exchange Timing (Z185 CPU Internal Operation)

2.3 INPUT/OUTPUT

Input/output devices and registers reside in a separate address space from memory. In the original Z80, I/O addresses were 8 bits wide and were carried on the A7-A0 lines, with A15-A8 being driven from various CPU registers and being largely ignored by I/O devices. With the Z8018X family, I/O addresses are extended to 16 bits, and special instructions like IN0 and OUT0 are included which insure that the A15-8 lines are all zero.

2.3.1 Internal I/O Registers

The Z80185 includes two groups of I/O registers. Group 1 includes the registers for the MMU, DMA, ASCIs, PRT and CSI/O, and has the following characteristics:

- Decodes 16-bit I/O addresses.
- Resides at addresses 0000-003F after Reset, but can be relocated to 00040-007F or 0080-00BF by programming the I/O Control Register (ICR).
- Is accessed in three clock machine cycles.

Group 2 includes the registers for the ESCC, parallel ports, Bidirectional Centronics controller, CTCs, chip select, and Watch-Dog Timer, and has the following characteristics:

- May decode 8- or 16-bit addresses depending on the Decode High bit in the System Configuration Register.
- Resides at addresses xxD8-xxF1.
- Is accessed using four clock machine cycles, like off-chip I/O devices.

2.3.2 I/O Read/Write Timing

I/O instructions cause data read/write transfers which differ from memory data transfers in the following ways:

1. The /IORQ (I/O Request) signal is asserted Low instead of the /MREQ signal.
2. The 16-bit I/O address is not translated by the MMU.
3. A19-A16 are held Low.
4. A15-A8 may or may not be decoded by the I/O device. At least one wait state (Tw) is always inserted for I/O ready and write cycles (except Group 1 internal I/O cycles).

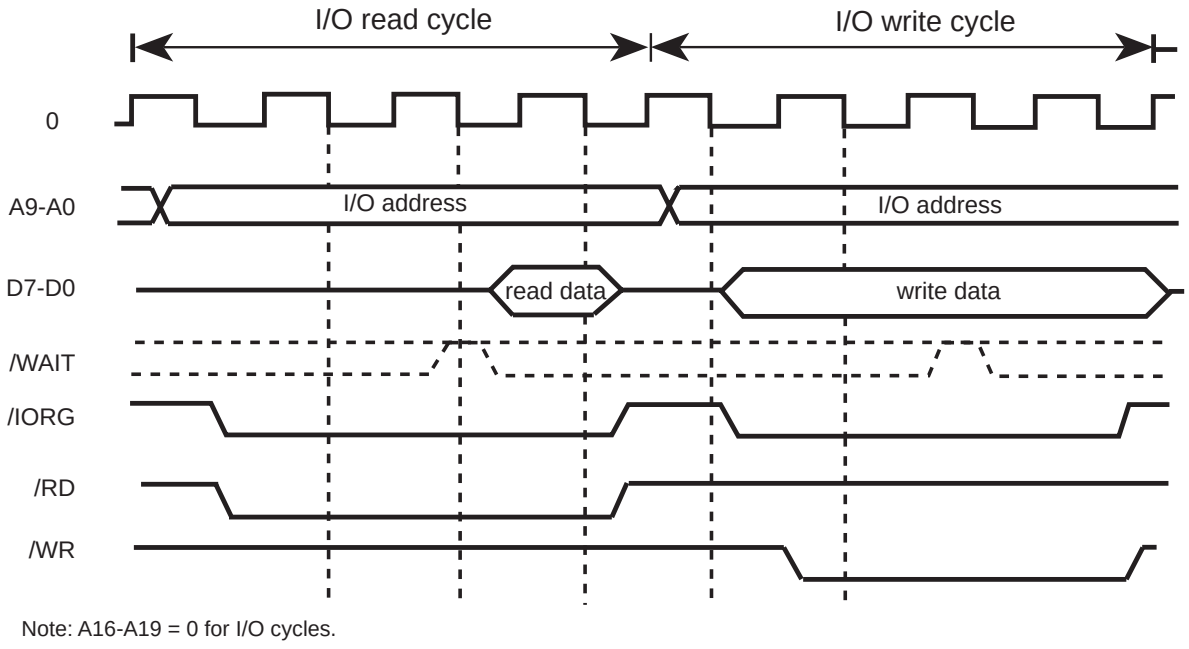


Figure 2-9. I/O Read/Write Timing

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com