APPLICATION NOTE

SKY65111-348LF: Amplifier Layout Optimization

Introduction

Skyworks SKY65111-348LF is a high performance 3-stage power amplifier IC. Typical applications include automatic meter readers and RFID. The IC is manufactured on an advanced InGaP HBT process and packaged in a small 3 x 3 mm QFN package.

Typically the SKY65111-348LF is used in the 800–1100 MHz frequency band. It is tuned for very high efficiency, input and output return loss, and gain while still maintaining good output third order intercept (OIP3) and harmonic performance.

The SKY65111-348LF data sheet references long lengths of two lines on V_{CC3}, RFOUT, and V_{CC2}. In efforts to reduce the overall board space required by the device and matching circuit, this application note describes how to replace these traces with surface mount inductors. As a result, the bandwidth of operation has been expanded to 700–1200 MHz. DC bias variation and harmonic filtering are also described.

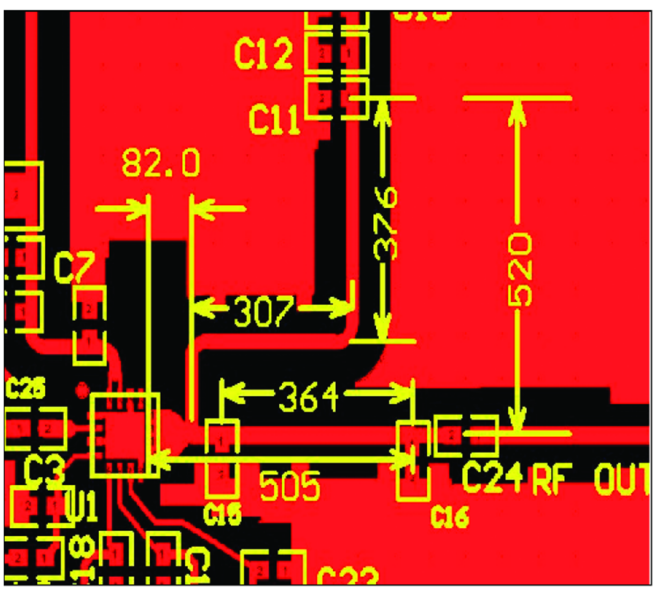

Figure 1. SKY65111 Evaluation Board Without Layout Optimizations

Evaluation Board Circuit Description

Figure 2 describes the application circuit schematic used for the wideband 700–1200 MHz tuning. The operation of each device pin is detailed below.

Ground, (Pins 1, 3, 8, 14). Attach all ground pins to the RF ground plane with multiple largest diameter, lowest inductance vias that the layout will allow. It is extremely important that the device paddle be sufficiently grounded for both thermal and stability reasons.

RFIN, (Pin 2). A lumped element matching structure for good in-band return loss has been realized on the RF input, Pin 2. This structure is comprised of a DC blocking capacitor (C1), low pass LC filter (L1 and C2) and finally at the device input a series capacitor (C25). This combination of devices will yield a return loss of better than -11 dB over the entire 700–1200 MHz band. The actual placement of C1 is not critical; it can be moved as close to L1, C2 and C25 as desired. C25 should be placed as close to the device pin as possible to replicate performance when measured on the applications board.

V_{CC1}, (Pin 4). V_{CC1} is the collector bias input for the first amplifier stage in the SKY65111. Multiple bypass capacitors, C3–C5, C17 and a series inductor L2, have been utilized to ensure stability both in and out of the usable bandwidth of the device. L2 and C3 should be placed in the approximate location shown on the applications board layout, but absolute placement is not critical.

V_{APC1}, (Pin 5). V_{APC1} is the bias control voltage input for amplifier stages 1 and 2. Nominal operating range is between 2.6 V and 3.0 V, with 3.0 V producing maximum gain. V_{APC1} can also be set to 0 V, if it is desired to place amplifier stages 1 and 2 into standby mode to reduce current consumption.

V_{APC2}, (Pin 6). V_{APC2} is the bias control voltage input for amplifier stage 3. Nominal operating range is between 2.6 V and 3.0 V, with 3.0 V producing maximum gain. V_{APC2} can also be set to 0 V, if it is desired to place amplifier stage 3 into standby mode to reduce current consumption. In most applications the V_{APC1} and V_{APC2} pins are tied directly together and biased from the same control voltage. V_{APC1} and V_{APC2} may also be split if independent control is desired.

V_{REF}, (Pin 7). V_{REF} is the bias reference voltage input for amplifier stages 2 and 3. V_{REF} should be operated over the same voltage range as V_{CC}, with a nominal voltage of 3.5 V. Bypassing of V_{REF} is accomplished with C23 and C24, both of which should be placed close to the device pin.

RFOUT, V_{CC3} (Pins 9–12). RFOUT and V_{CC3} are the inputs for the power supply connection to the stage 3 collectors as well as the RF output port. These pins should be tied together to enable current sharing. Bias is applied to the RF output through L5, a high current rated 10 nH inductor. Capacitors C11 through C14 provide proper RF bypassing and should be placed closely to L5 as shown in the applications circuit. Output matching for optimal power gain is accomplished with capacitors C15, L3 and C16. C15 should be placed about 141 mils (3.6 mm) from the RF output.

Pin 13. No connection and must be left open circuit.

V_{CC2}, (Pins 15 and 16). V_{CC2} is the collector bias input for the second amplifier stage in the SKY65111. Multiple bypass capacitors, C8–C10 have been utilized to ensure stability both in and out of the usable bandwidth of the device. C8 should be placed closely to L4 as shown in the application board layout.

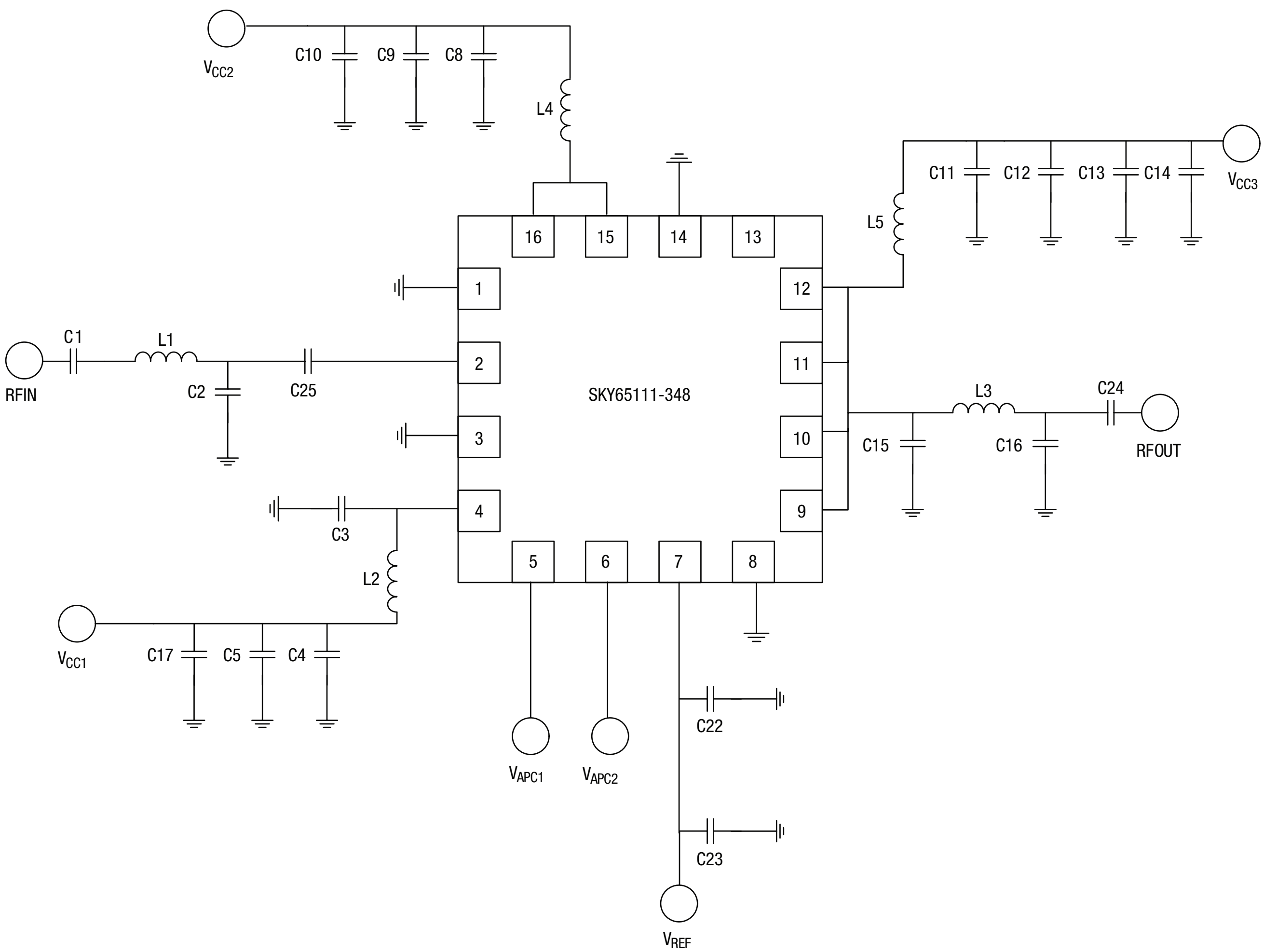

Figure 2. Application Circuit Schematic

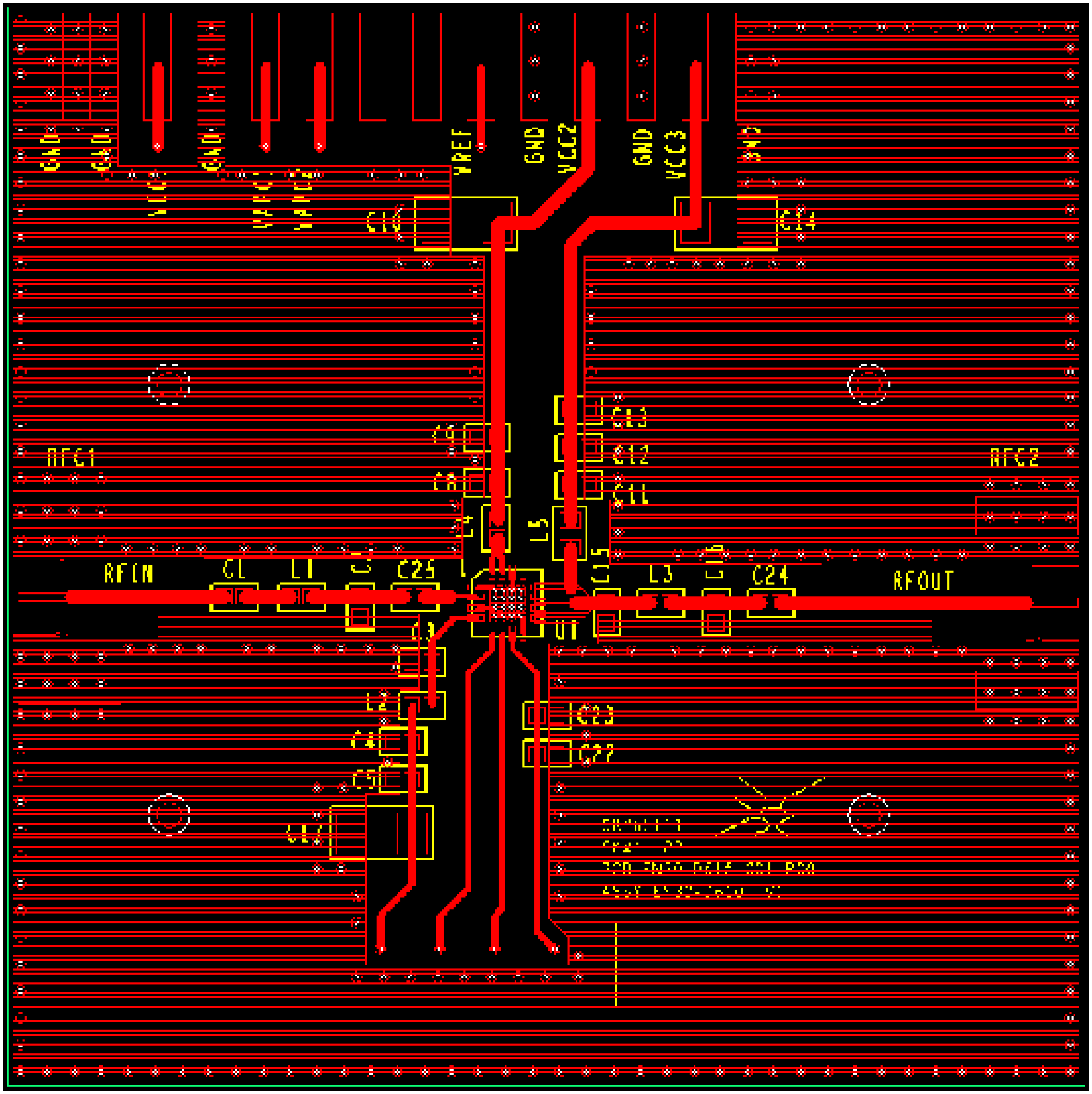

Figure 3. Application Board Layout

Table 1. SKY65111-348LF Recommended Evaluation Board Component Values

Component	Value	Size	Manufacturer	Part Number
C1	100 pF	0402	Murata	GRM1555C1H101JD83E
C2	0.5 pF	0402	Murata	GRM1555C1H0R5JZ35E
C3	4.7 pF	0402	Murata	GRM1555C1H4R7JZ35E
C4	100 pF	0402	Murata	GRM1555C1H101JD83E
C5	1000 pF	0402	Murata	GRM155R71H102KA01
C8	100 pF	0402	Murata	GRM1555C1H101JD83E
C9	1000 pF	0402	Murata	GRM155R71H102KA01
C10	10 μF	0402	AVX	TAJA106M006R
C11	100 pF	0402	Murata	GRM1555C1H101JD83E
C12	1000 pF	0402	Murata	GRM155R71H102KA01
C13	10 nF	0402	Murata	GRM155R71E103KA01
C14	10 μF	1206	AVX	TAJA106M006R
C15	15 pF	0402	Murata	GJM1555C1H150JB01E
C16	6.8 pF	0402	Murata	GJM1555C1H6R8CB01E
C17	10 μF	1206	AVX	TAJA106M006R
C22	1000 pF	0402	Murata	GRM155R71H102KA01
C23	100 pF	0402	Murata	GRM1555C1H101JD83E
C24	100 pF	0402	Murata	GRM1555C1H101JD83E
C25	27 pF	0402	Murata	GRM1555C270JZ35E
L1	1 nH	0402	Taiyo Yuden	HK1005-1N0S
L2	1.2 nH	0402	Taiyo Yuden	HK1005-1N2S
L3	1.8 nH	0402	Taiyo Yuden	HK1005-1N8S
L4	1 nH	0402	Taiyo Yuden	HK1005-1N0S
L5	10 nH	0603	Coilcraft	0603HC-10NXJB

Typical Performance Characteristics

$V_{CC1,2,3}$ = 3.5 V, V_{REF} = 3.5 V, $V_{APC1,2}$ = 2.7 V, F = 915 MHz, Z_0 = 50 Ω, T = 25 °C, unless otherwise noted

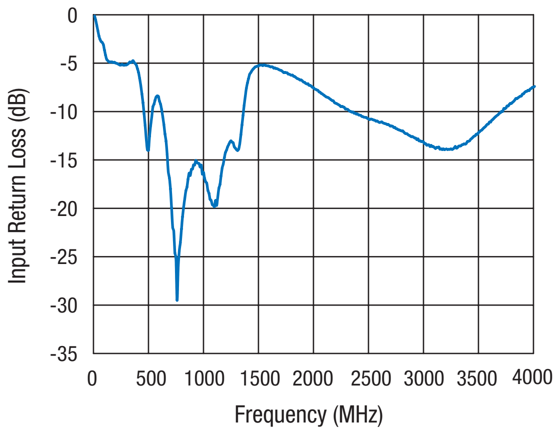

Figure 4. Input Return Loss vs. Frequency, P_{IN} = -30 dBm

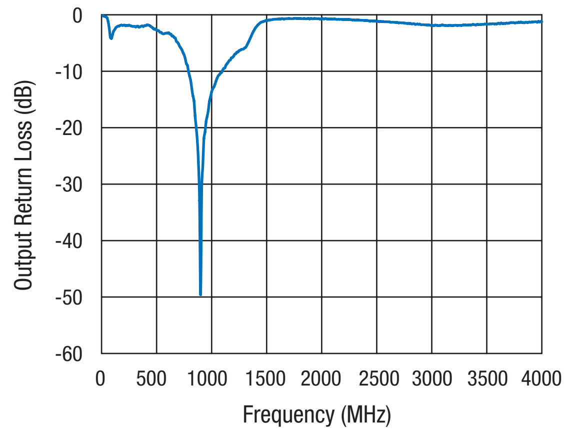

Figure 7. Output Return Loss vs. Frequency, P_{IN} = -30 dBm

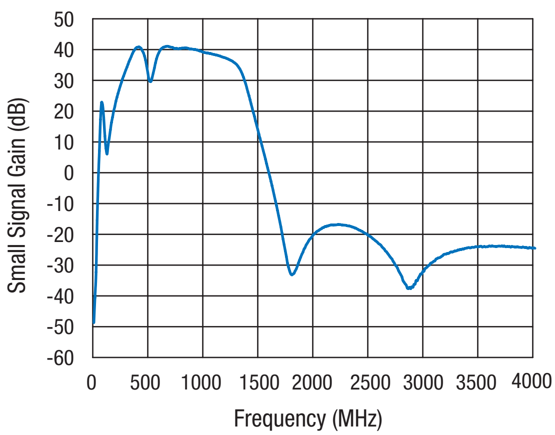

Figure 5. Small Signal Gain vs. Frequency, P_{IN} = -30 dBm

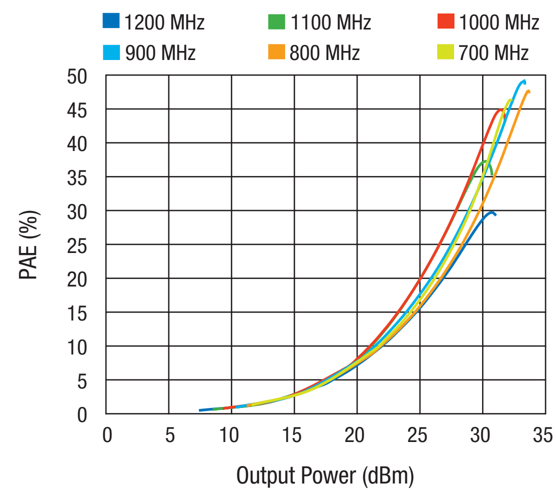

Figure 8. PAE vs. Output Power for Multiple Frequencies

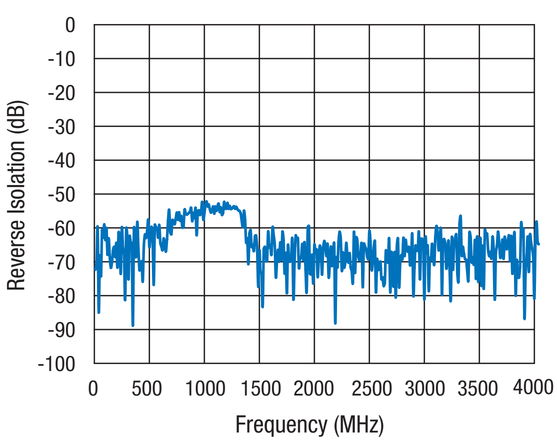

Figure 6. Reverse Isolation vs. Frequency, P_{IN} = -30 dBm

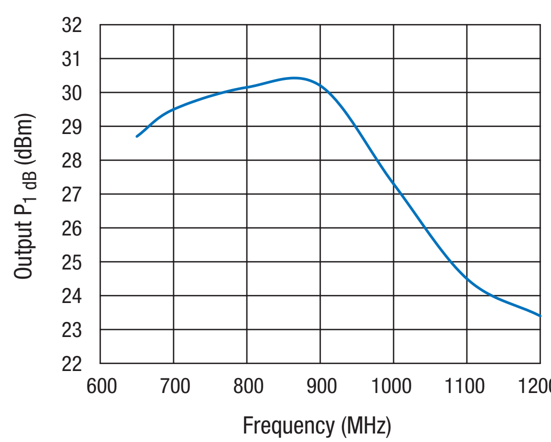

Figure 9. $OP_{1\ dB}$ vs. Frequency

Typical Performance Characteristics

$V_{CC1,2,3}$ = 3.5 V, V_{REF} = 3.5 V, $V_{APC1,2}$ = 2.7 V, F = 915 MHz, Z_0 = 50 Ω, T = 25 °C, unless otherwise noted

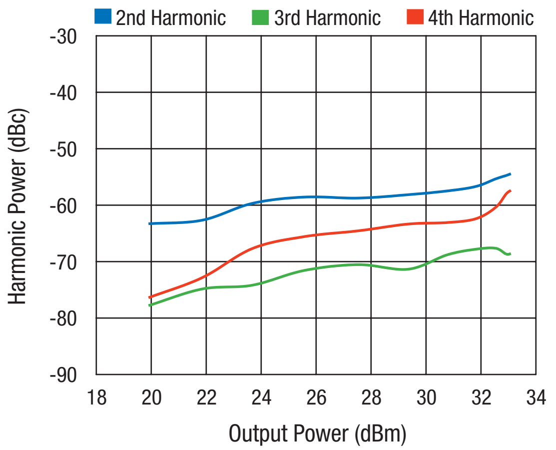

Figure 10. Harmonic Power vs. Output Power

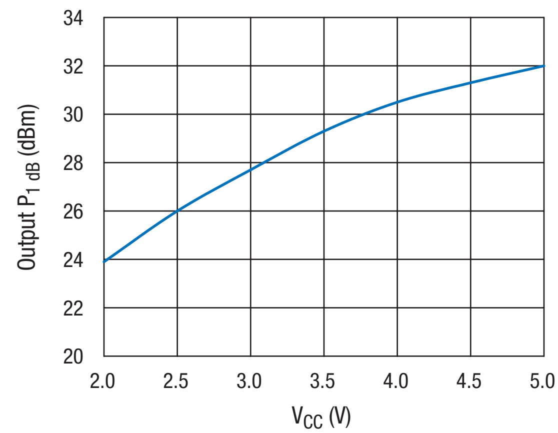

Figure 13. $OP_{1\ dB}$ vs. V_{CC}, V_{APC} = 2.7 V

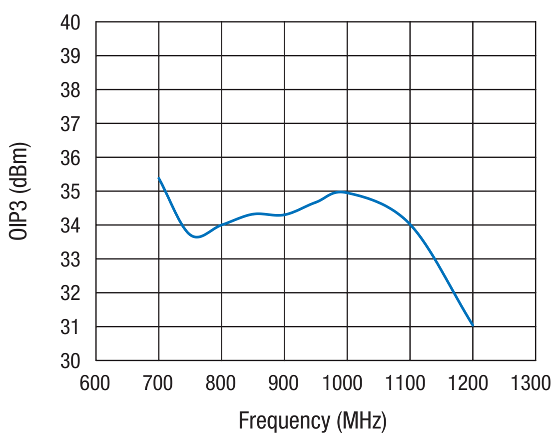

Figure 11. OIP3 vs. Frequency, P_{IN} = -20 dBm/Tone, ΔF = 5 MHz

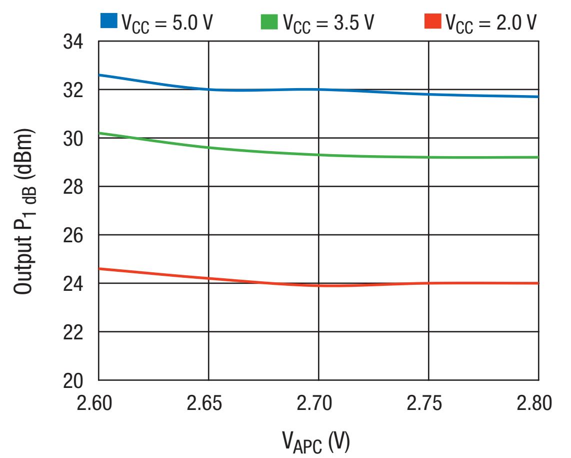

Figure 14. $OP_{1\ dB}$ vs. V_{APC}, V_{CC} = 5 V, 3.5 V, 2 V

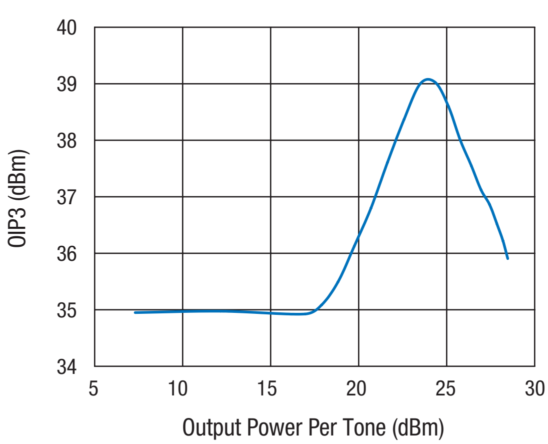

Figure 12. OIP3 vs. Output Power, ΔF = 5 MHz

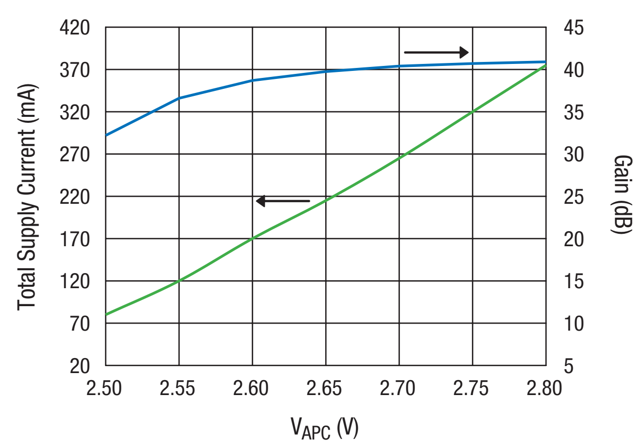

Figure 15. Supply Current and Small Signal Gain vs. V_{APC}, V_{CC} = 3.5 V

Device Bias Options

The SKY65111-348LF is capable of using a wide range of supply voltages while still maintaining good performance. V_{CC} is typically specified at 3.5 V, but can be as low as 2 V or as high as 5 V.

Changing V_{CC} will directly affect the output 1 dB compression point ($OP_{1\ dB}$) and gain of the device, but input and output return losses will only see small changes. Figure 13 describes the extent $OP_{1\ dB}$ is altered by varying the supply voltages.

Changing V_{APC} changes the bias point and quiescent current draw of the device. Lowering V_{APC} can actually increase $OP_{1\ dB}$ by introducing gain expansion at the compression point. Figure 14 describes the effects of varying V_{APC}.

915 MHz Harmonic Filter

The SKY65111-348LF has very good 2nd and 3rd harmonic performance, which minimizes interference at these frequency bands. To reduce these harmonics even more, external filtering may be used. Figure 16 shows a simple three component low-pass filter designed to improve harmonic rejection while maintaining low pass band insertion loss for 915 MHz operation. This filter should be placed immediately following the DC blocking capacitor, C24.

The filter improves rejection by approximately 13 dB and 34 dB at the 2nd and 3rd harmonics, respectively. Pass band insertion loss is approximately 0.3 dB.

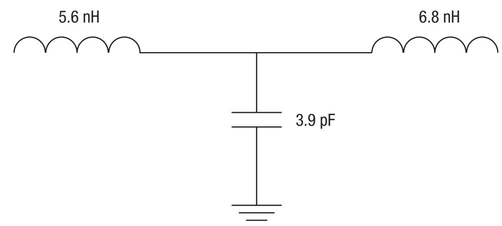

Figure 16. 915 MHz Harmonic Filter

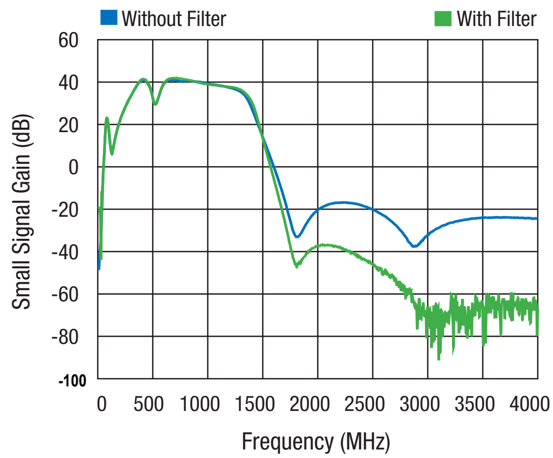

Figure 17. Small Signal Gain With and Without the 915 MHz Harmonic Filter