Design and Implementation of Low Power 32-bit Comparator

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ABSTRACT

Comparator plays a vital role in many IC applications, Microprocessors, computer systems etc. Hence it is desirable to design a comparator block with low power consumption and high-speed performance. In this paper a novel architecture of 32-bit comparator using Complementary metal-oxide semiconductor logic is proposed and computed its delay and power metrics. Further it is compared with the full adder based 32-bit comparator. From the analysis we derive the comparison between proposed and the conventional comparator. The complete designing of architectures and their result analysis was done in cadence virtuoso tool at 180 nm technology. Simulation results show that there is reduce in power consumption of 90% when compared to the conventional full adder-based comparator.

Keywords: CMOS, Comparator, Full Adder, GDI, Low power application.

1. Introduction

Designing low power circuits has evolved CMOS technology. Among all CMOS designs Comparator is one of them with enormous applications. Comparator usually of two types. An Equality comparator suggests whether the processed bits are equal or not. On the other hand, a Magnitude Comparator, as the name says that it compares magnitude of two bits and decides whether they are equal, greater or less than to each other. Since, it defines magnitude relation the comparator block can also be interpreted as magnitude decision module [1]-[6]. It also helps in suggesting the bigger value for ease of subtraction. It is used in numerous applications such as in digital communications, in Integrated circuits applications, digital electronics etc., A 32-bit comparator usually compares two 32 bit length operands and tells whether they are equal or less than or equal to each other [7]-[12]. The novel architecture of 32-bit comparator that was discussed in this paper was designed using CMOS logic with GDI logic [3]. The Gate diffusion input is a new technique applied for low power consumption and optimized delay of a given CMOS logic design [4]. In this technique, the pmos substrate is connected to the VCC terminal and the nmos substrate is connected to ground terminal. As GDI technique is popularly known for reducing power consumption, propagation delay of the design, the proposed design follows this technique [13]-[18].

This paper consists of 5 sections, in which the 2nd section deals with existing comparators so far. Section 3 includes proposed designs such as 2-bit, 4-bit, 10-bit and 32-bit comparator modules. Section 4 includes simulation results as well as comparative analysis of results. Section 5 includes conclusion and future scope of proposed design.

2. Existing Comparators

A Comparator usually performs subtraction operation in order to determine its operands relation. It can also be performed with help of carry look-ahead logic in which the relation between operands is defined by generate bits and propagate bits [19]-[25]. The existing designs include serial and parallel structured comparators [6]. The disadvantage with these comparators is that they provide less efficiency with respective to large inputs. The novel structure includes of 32-bit comparator is implemented by using lower range of comparators such as 10 and 4, 2 bit comparators respectively. The lower range 10-bit and 4-bit comparators are designed with help of cascading 4-bit and 2-bit comparators [26]-[33].

The 32-bit comparator is designed and implemented using Cadence virtuoso tool at 180 nm technology and is compared with the Raman's Full adder based 32-bit comparator architecture [34]-[39]. The Proposed architecture of Full adder based 32-bit comparator is as shown in the Fig. 1.

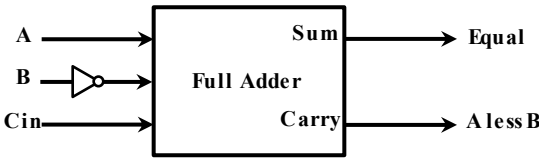


Fig. 1. (a) first picture; (b) second picture.

The above design works on the principle of adder. The results obtained with two inputs A, B are basis for generations of all the outputs. When A, B inputs generates, carry out generated is '1' and sum as non-zero then it is considered as A>B condition. Similarly, for equal than condition, carry out should be logic 1 and sum is equal to 0. For less than condition, carry out should be equal to 0.

The average power, delay and the power-delay product has been calculated. Usually these factors are mostly calculated as they define the optimal circuit performance. The major parameters in digital design are power, speed. If a design meets the requirements of speed it will not satisfy the requirement of power consumption and vice versa. The main aim of this the proposed design is to bring down the power metric down for usage of low power applications. Hence, in this paper a 32-bit comparator is designed using the 2,4,10 bit comparators focusing on less power consumption. Later on the calculated values of metrics are tabulated.

3. Proposed Model

The Proposed model which is a 32-bit comparator is designed from its lower order designs such as 2-bit, 4-bit, 10-bit modes respectively [8]. Therefore, these designs play an important role in power consumed by the 32-bit comparator.

3.1. 2-bit comparator

A 2-bit comparator as name suggests compares magnitude of two bit length variables [9]. It is realized using combinations of AND, OR gate combinations respectively as shown in the following Fig 2. The conventional 2-bit comparator equations are as follows [10].

(1) A= B (equal condition): A1, B1 A0, B0

Boolean expression: x_1x_0: $xi = A_iB_i + A_i'B_i'$

(2) A greater than B

Boolean expression: $A_1B_1' + x_1A_0B_0'$

(3) A less than B

Boolean expression: $A_1'B_1 + x_1A_0'B_0$

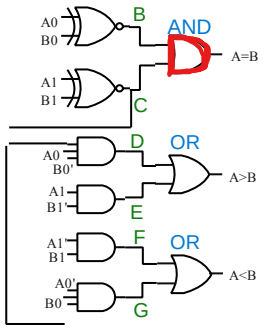


Fig. 2. Design of 2-bit Comparator

3.2. 4-bit comparator

The Comparator that is required to compare a length of 4-bit of each variable is a 4-bit comparator [11]. The 4-bit comparator is implemented irrespective of Boolean expressions. It is designed using three 2–bit comparators successively. For the succession comparators the less than and greater than outputs are rippled for generating the required logic as shown in Fig. 3.

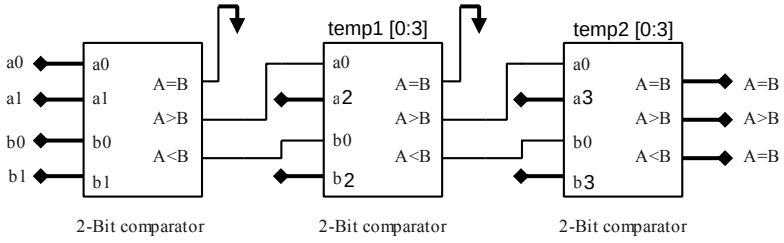


Fig. 3. Design of 4-bit Comparator

3.3. 10-bit comparator

The 10-bit comparator perform operation totally on 20 bits i.e. it compares two 10 bit length variables. It is usually generated using boolean expressions as that of 2-bit comparator. In this case, the design implementation is done using three 4-bit comparators [11] as shown in Fig. 3.

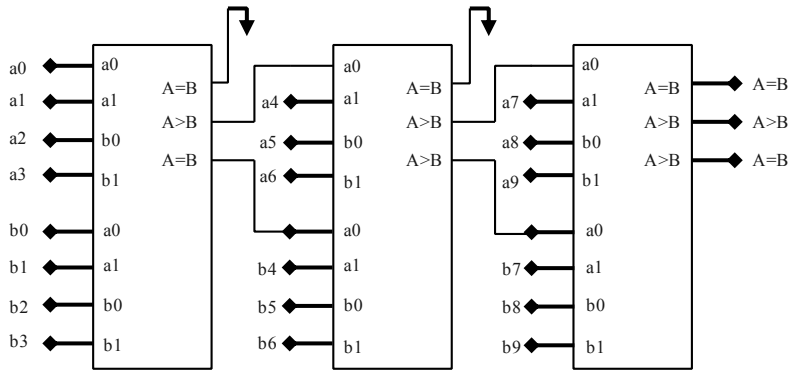


Fig. 4. Design of 10-bit Comparator

3.4. 32-bit comparator

The 32-bit comparator usually compares two 32 bit length variables. The design methodology proposed in this design is similar to N-bit parallel adder. A Parallel adder is designed using single bit full adder modules. In the same way, the proposed 32-bit comparator which is completely a novel architecture was implanted using low bit comparators such as 10, 4, 2 bit comparators which was seen in Fig. 3 and Fig. 4.

The only difference between a conventional comparator and the proposed one is that the conventional one designed through logic equations whereas the proposed one follows rippling of bits. In this design, the output bits of A>B (A greater than B), A<B (A less than B) that are generated at one comparator module is rippled to another [12]. In this design, the least significant bits are compared first and later the most significant bits are compared. So, the final comparison of bits depends on initial stages of compared bits [13].

The following figure 5 depicts the proposed 32-bit comparator.

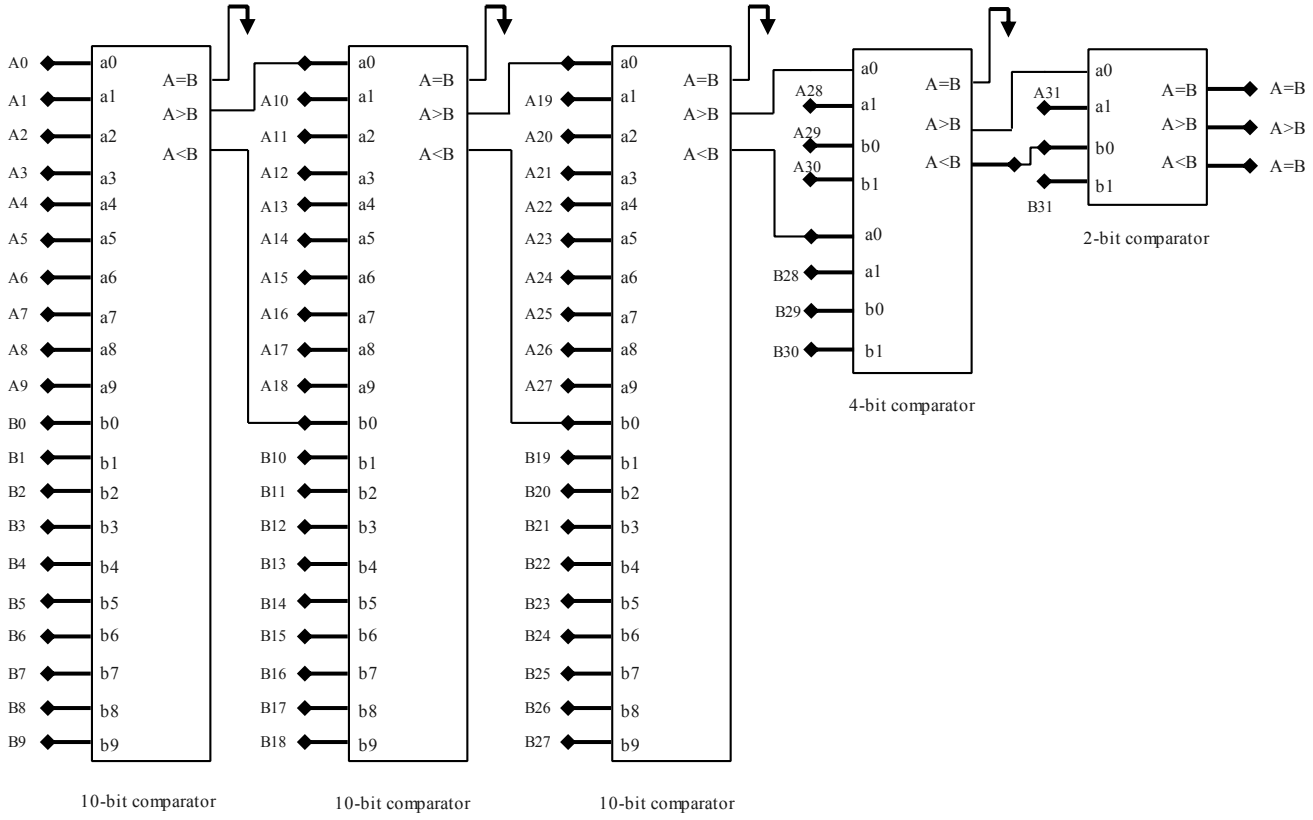


Fig. 5. Design of 32-bit Comparator

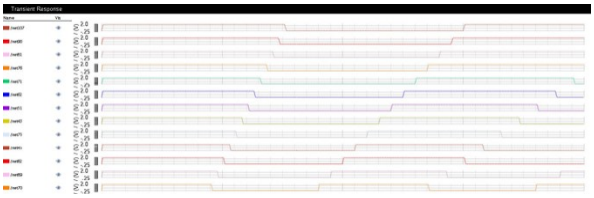
4. Results and Simulations

In this section, the Power and delay metrics [14] can be seen and compared with Raman's design of Full adder based 32-bit comparator using full adder which was implemented in Xilinx software.

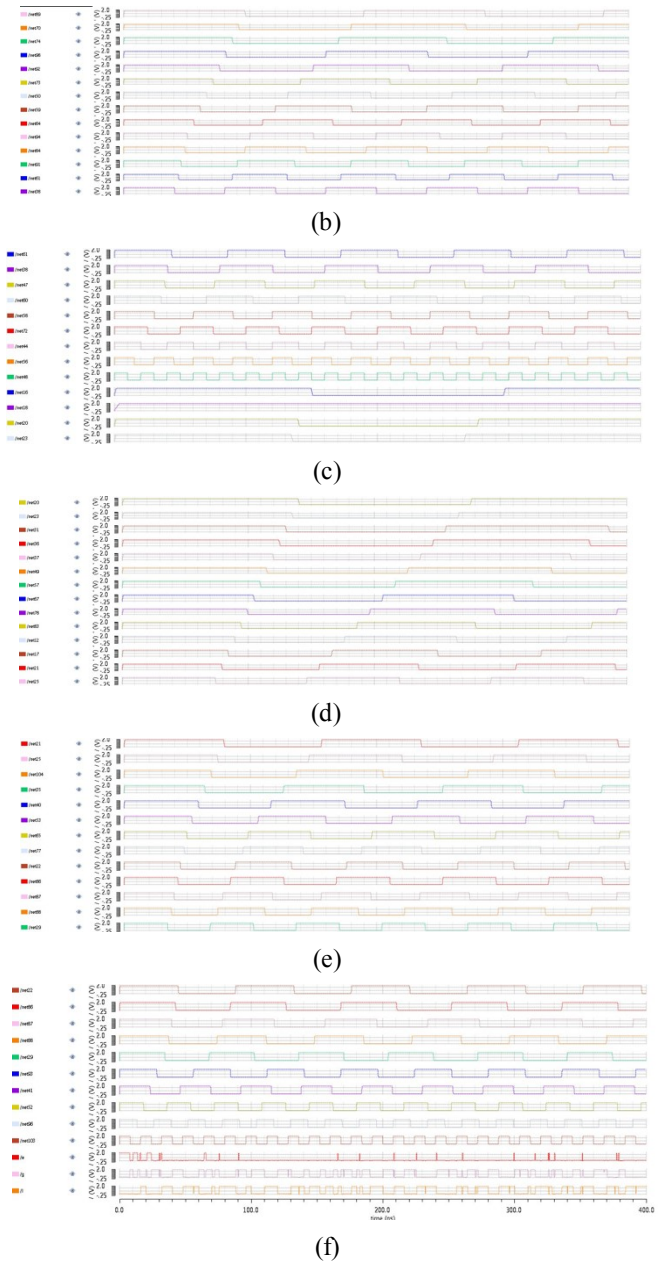
4.1. Simulation Results

The functionality of the proposed design is tested by providing pulse signal with logic 1 as 1.8 volts and logic 0 as 0 volts, respectively. The Variation of inputs is provided by giving different period and Pulse width to the signals.

The waveforms of 32-bit comparator are shown Fig. 6.



(a)



(b)

(c)

(d)

(e)

(f)

Fig. 6. Waveforms of 32-bit Comparator

The figures up to 6-e defines inputs from (A0-A31) and (B0-B31), respectively. The final results of A>B, A<B, A=B is simulated in Fig.6 (e).

4.2. Comparative analysis of results

The overall delay of 32-bit comparator is tabulated using Cadence virtuoso tool. The delay calculations specify the amount of time required for the output generation after the inputs has been applied. The delay between each and every input to generate the required output has been noted.

Table 1. Delay Of 32-Bit Comparator

INPUTS	*OUTPUTS*		
	A<B	***A=B***	***A>B***
A0	15.76E-9	7.42 E-9	7.341 E-9
A1	15.77 E-9	7.434 E-9	7.355 E-9
A2	15.78 E-9	7.448 E-9	7.369 E-9
A3	15.8 E-9	7.462 E-9	7.383 E-9
A4	15.81 E-9	7.476 E-9	7.397 E-9
A5	15.82 E-9	7.49 E-9	7.411 E-9
A6	1584 E-9	7.503 E-9	7.425 E-9
A7	15.83 E-9	7.517 E-9	7.439 E-9
A8	15.87 E-9	7.531 E-9	7.452 E-9
A9	15.88 E-9	7.545 E-9	7.466 E-9
A10	15.89 E-9	7.55 E-9	7.48 E-9
A11	15.91 E-9	7.573 E-9	7.494 E-9
A12	15.92 E-9	7.587 E-9	7.508 E-9
A13	15.94 E-9	7.601 E-9	7.522 E-9
A14	15.95 E-9	7.615 E-9	7.536 E-9
A15	15.96 E-9	7.628 E-9	7.55 E-9
A16	15.98 E-9	7.642 E-9	7.564 E-9
A17	15.99 E-9	7.656 E-9	7.577 E-9
A18	16.01 E-9	7.67 E-9	7.591 E-9
A19	16.02 E-9	7.684 E-9	7.605 E-9
A20	16.03 E-9	7.698 E-9	7.619 E-9
A21	16.04 E-9	7.703 E-9	7.625 E-9
A22	16.05 E-9	7.712 E-9	7.633 E-9
A23	16.05 E-9	7.717 E-9	7.639 E-9
A24	16.06 E-9	7.726 E-9	7.647 E-9
A25	16.07 E-9	7.731 E-9	7.652 E-9
A26	16.07 E-9	7.74 E-9	7.661 E-9
A27	16.09 E-9	7.753 E-9	7.675 E-9
A28	16.10 E-9	7.767 E-9	7.689 E-9
A29	16.12 E-9	7.781 E-9	7.702 E-9
A30	16.13 E-9	7.79 E-9	7.716 E-9
A31	16.14 E-9	7.809 E-9	7.73 E-9
B0	15.76 E-9	7.426 E-9	7.347 E-9
B1	14.78 E-9	6.448 E-9	6.369 E-9
B2	15.79 E-9	7.453 E-9	7.375 E-9
B3	15.80 E-9	7.467 E-9	7.389 E-9
B4	15.82 E-9	7.481 E-9	7.402 E-9
B5	15.83 E-9	7.495 E-9	7.416 E-9
B6	15.84 E-9	7.509 E-9	7.43 E-9
B7	15.86 E-9	7.523 E-9	7.444 E-9

B8	15.87 E-9	7.537 E-9	7.458 E-9
B9	15.89 E-9	7.551 E-9	7.472 E-9
B10	15.90 E-9	7.565 E-9	7.486 E-9
B11	15.91 E-9	7.578 E-9	7.50 E-9
B12	15.93 E-9	7.592 E-9	7.514 E-9
B13	15.94 E-9	7.606 E-9	7.527 E-9
B14	15.96 E-9	7.62 E-9	7.541 E-9
B15	15.97 E-9	7.634 E-9	7.555 E-9
B16	15.98 E-9	7.648 E-9	7.569 E-9
B17	16.0 E-9	7.662 E-9	7.583 E-9
B18	16.01 E-9	7.676 E-9	7.597 E-9
B19	16.02 E-9	7.69 E-9	7.611 E-9
B20	16.04 E-9	7.701 E-9	7.622 E-9
B21	16.04 E-9	7.706 E-9	7.627 E-9
B22	16.05 E-9	7.715 E-9	7.636 E-9
B23	16.06 E-9	7.72 E-9	7.641 E-9
B24	16.06 E-9	7.728 E-9	7.65 E-9
B25	16.07 E-9	7.734 E-9	7.655 E-9
B26	16.08 E-9	7.742 E-9	7.664 E-9
B27	16.09 E-9	7.759 E-9	7.68 E-9
B28	16.11 E-9	7.773 E-9	7.694 E-9
B29	16.12 E-9	7.787 E-9	7.708 E-9
B30	16.14 E-9	7.801 E-9	7.722 E-9
B31	16.15 E-9	7.815 E-9	7.736 E-9
	Average Delay		10.34ns

Power is an essential metric that is calculated for defining the performance of any logic circuitry [11]. The power consumption of the proposed 32-bit comparator is 90% lesser than the Raman's Full adder based comparator architecture which is tabulated in table 2.

The Power-delay product specifies the amount of energy consumption per performed or switching event. It is usually calculated by multiplying the power consumed with the average delay of the switching event.

The comparisons between proposed and full adder based 32-bit comparator has been laid as shown in table2.

Table 2. Comparison Between Proposed And Full Adder Based 32-Bit Comparator

Design	Power (mW)	Delay (nS)	Power-delay product (PJ)
Full adder based Comparator	151	5.23	789.73
Proposed Comparator	15.4	10.34	157.168

The Comparison table shows that there is reduce in power consumption nearly 90%, De lay has 50% increased. This shows the fact that for a circuit to be designed perfectly, it has to either bear disadvantages regarding power or delay. The power-delay product that ensures the efficiency and overall performance of proposed design is reduced nearly 80% with respective to the full based design.

5. Conclusion

In this paper, a novel architecture of 32-bit is proposed. The design of this architecture is implemented in Cadence virtuoso tool at 180 nm technology. The simulated results such as power, delay and power-delay product were produced with 1.8 volts supply. The Gate Diffusion Input technique enhances the simulation results by reducing power consumption [15]. The results depicts that the proposed design provides 90% less power consumption and some compatible delay. As in technology low power consumption became a vital factor, the proposed design enables that fact.

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