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A Low Power Area Efficient 4-bit Universal Shift Register

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ABSTRACT

This research proposes a method for designing a Universal Shift Register (USR) that consumes little power. The proposed 4-bit USR is split into two sections: Control activities include right shift, left shift, and parallel loading; D flip flips need a separate register. 4*1 MUX performs these USR operations. Since flip flops play such a crucial role in USR, the PIPO shift register incorporates various types of flip flops that have undergone extensive testing and development. Finally, the suggested 4-bit USR boosted speed while using little power. A 4-bit USR is designed and validated with the help of the Xilinx 14.7 simulation tool and the Verilog HDL programming language.

Keywords— Universal Shift Register, Multiplexer, Flip-flops, Xilinix 14.7 and Verilog HDL

1. INTRODUCTION

There are several different types of advanced systems, but the most frequent basic component is a flip flop. As a result of Moore's Law, CMOS innovation techniques have shrunk in size, enabling designers to fit more transistors onto a single chip [1]. The greater the number of transistors, the greater the amount of energy lost as heat or radiation. One of the most significant difficulties of low-power plan strategies and methodologies is the rising temperature. Due to the increasing importance of practical frameworks and the need to decrease control utilization (and thus warm dispersion) in high-thickness VLSI circuits, rapid and inventive improvements have been made in low-control design. Flip-flops are one of the most ubiquitous and fundamental computer components (FFs) [2]. Particularly sophisticated strategies these days sometimes include large pipelining systems [3] and the heavy reliance on feature-rich modules like enroll record, move enroll, and first in first out [4]. About half of the clock framework's total control's power consumption is expected to come from the clock itself. For this reason, FFs use a lot of resources from the chip. Consider the coordinated circuit's dependability together minimal power consumption. Higher levels of trading raise the potential for persistent quality issues since more normal current is discharged [5]. Tablets and other portable computing platforms are replacing laptops. Because of the persistence of this trend and the lack of any obvious solution in the near future of batteries, low power issues need a lot more attention. Future integrated circuits' energy consumption patterns may be coordinated based on the current trends because of the computerization of low-power plans. To achieve low power consumption there are requirements to design and develop low power consumption devices. Due to the increment of portable system and rapid

development in electronic sector a low power and less area and speed improved device is necessary to archives this goal. Therefore, the research goal of this paper is to propose a design of a low power, speed improved 4-bit universal shift register using D flip flops and multiplexers.

2. LITERATURE REVIEW

Significant and new improvements in low-power design have emerged from the need for portable devices and the necessity to minimize power consumption in VLSI processors [6]. Battery life, speed, power consumption, and size all need to be optimized for small silicon areas in order to make portable devices viable. There is widespread usage of synchronous circuits in digital circuits because of their ability to reduce design complexity. Flip-flops are a crucial timing element in digital circuits [7], but they have a significant impact on the circuit's speed, size, and power consumption.The most recent data input signal is kept in the flip-flop when a clock signal is present.DFFs are a major source of the heat generated by VLSI systems. Recording of the value of the D input occurs once per clock cycle. Captured values are used to calculate the Q output. These flip-flops provide the basis of the shift registers used in many electrical devices. The D FF behaves like a D-type transparent latch in that it retains the status of the signal on its D input pin when it is clocked but ignores any changes made to that input until it is clocked again [6,7]. The research in this paper looked at both double-edge triggered flip-flops (DEFFs) and clocked pair sharing (CPSFF) flip-flops. Single-ended conditional energy recovery (SCCER) and double-ended (DETFF) and triple-ended (CDMFF) flip-flops (MTCMOS) were also tested and rated. A PIPO shift register makes use of the studied flip flops. The two top flip-flops were chosen based on their power ratings. One may use a clock pulse sense latch in a number of different ways to create a 4-bit universal shift register [8]

2.1 Unversal Shift Register

With the help of a clock pulse, data is transferred from the register's storage location to the output device at regular intervals in digital electronics. The information may be moved to the right or left in serial or parallel modes. Shift registers may also be utilized in serial-in-parallel-out, serial-in-serial-out, parallel-in-parallel-out, and parallel-in-serial-out configurations [9].Shift registers may be either universal or bidirectional, depending on the direction of data flow. All the steps required to build a standard shift register are described in this article.

2.2 Existed Universal Shift Register

Using a shift register, data may be stored, moved, and loaded all at once. Both serial and parallel data processing are supported. Combining shift registers of a hexagonal shape. What we have here is a shift register that can take in data from several sources simultaneously. It's possible for universal shift registers to carry out the aforementioned three operations. **Parallel load operation –** All data is saved and stored instantly. **Shift left operation –** All of the data is stored and transmitted via a left-shifting serial channel. **Shift right operation –** When using a serial connection, information is stored and sent by shifting one step to the right [10].

This allows serial and parallel data to be processed using Universal shift registers.

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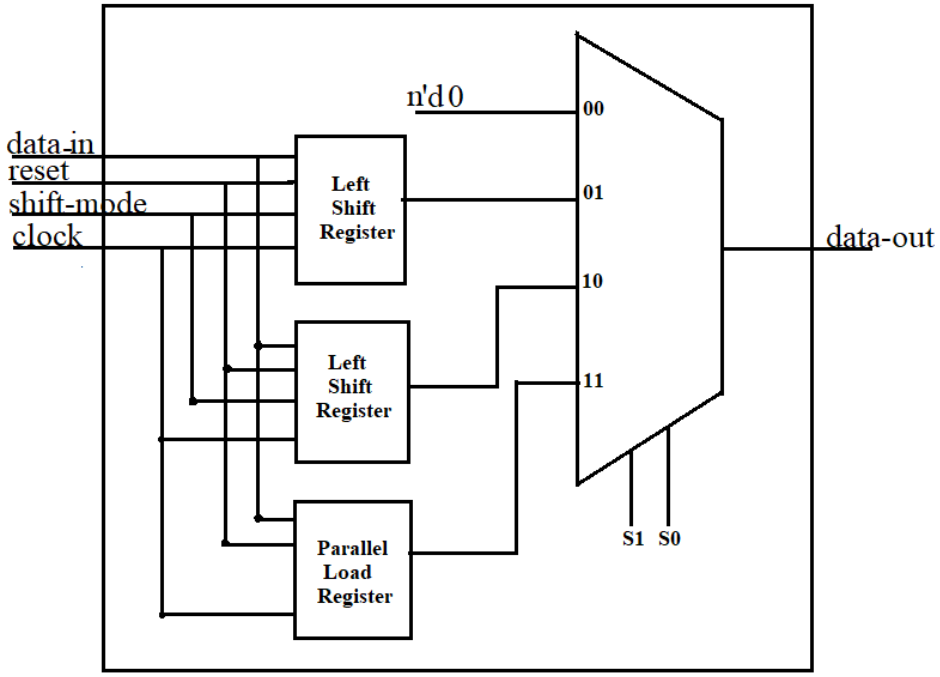

Fig 1:existed Universal Shift Register

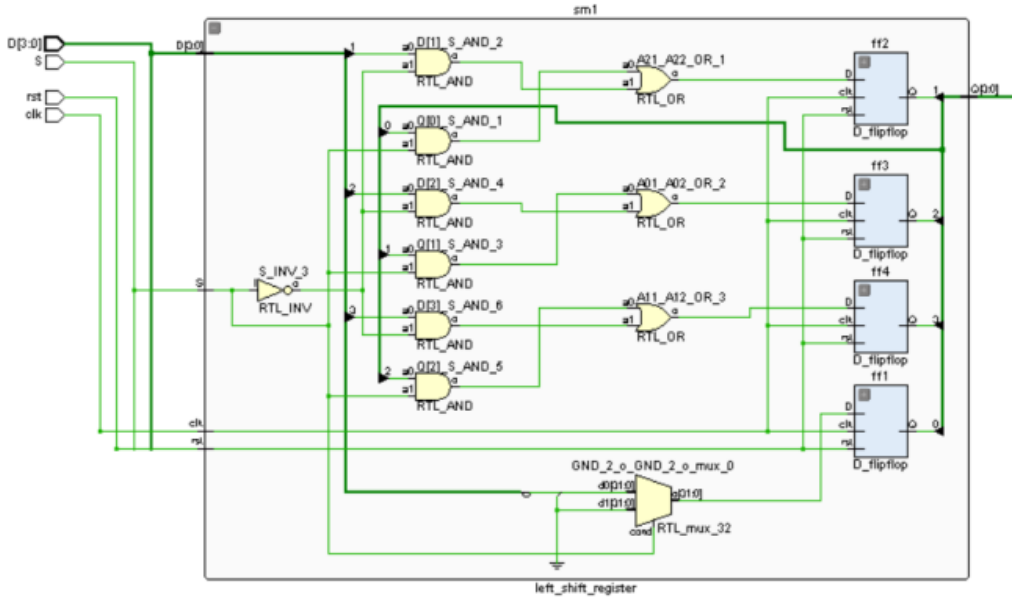

Fig2: 4-bitleft-to-right Shift register

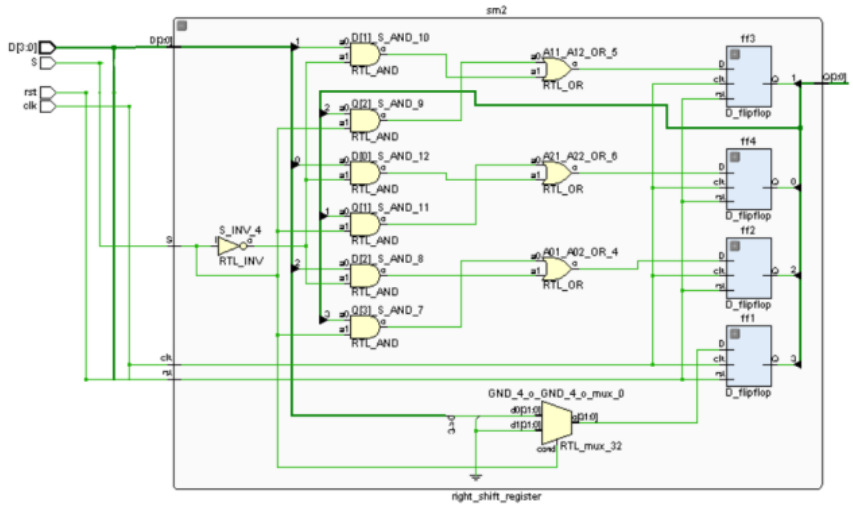

Fig3: This is a 4-bit right shift register.

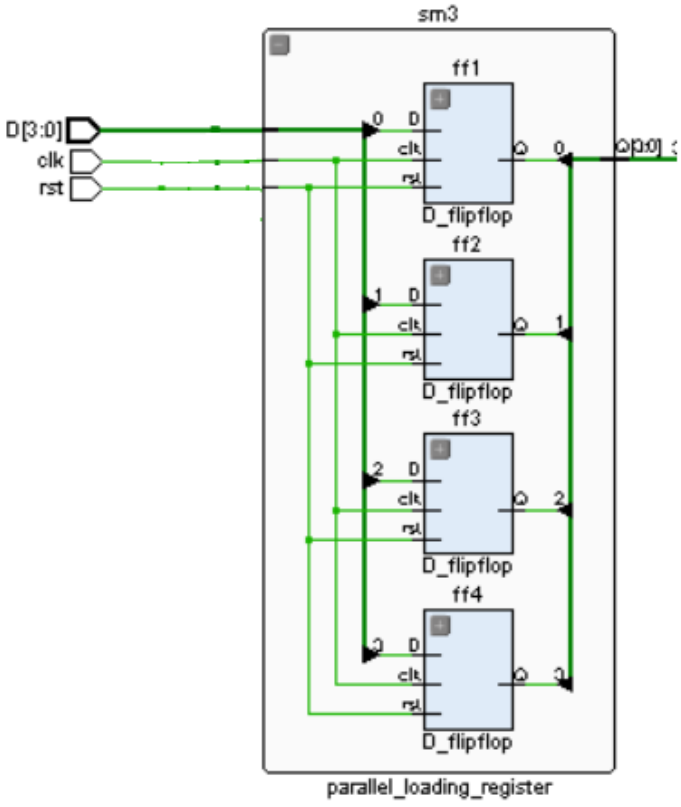

Fig4: Parallel loading shift register

Table1:Operating modes of existed universal shift register

OPREATING MODE	S1	S0	Shift mode
Locked	0	0	x
Shift right	0	1	1
Shift left	1	0	1
Parallel loading	1	1	x

3. PROPOSED UNIVERSAL SHIFT REGISTER

Each time the clock ticks over, the data in a shift register may be sent to an output device. In data transmission, either serial or parallel modalities may be utilized. Different input/output procedures may cause shift registers to function in different modes. For instance, shift registers may have several input/output modes. Bidirectional shift registers are used by all cultures. The universal shift register is well explained here.Data may be stored and shifted to the right or left at the same time using a universal shift register.It's possible to process data in either a sequential or parallel fashion. It's like a cross between unidirectional and bidirectional shift registers. Shift register with parallel input/output.

The following are three possible applications for universal shift registers.

- **Parallel load operation -** When data is saved concurrently, it is also retained in this way.
- **Shift left operation –** The data is stored and sent on a serial channel that often switches between the right and left sides of the connection.
- **Shift right operation**-Along the way to the right, serial data transfer and storage take place.

Thus, parallel and serial loads may both be handled by universal shift registers.

The image below illustrates how multiplexers and flip-flops may be used to build a four-bit universal shift register.

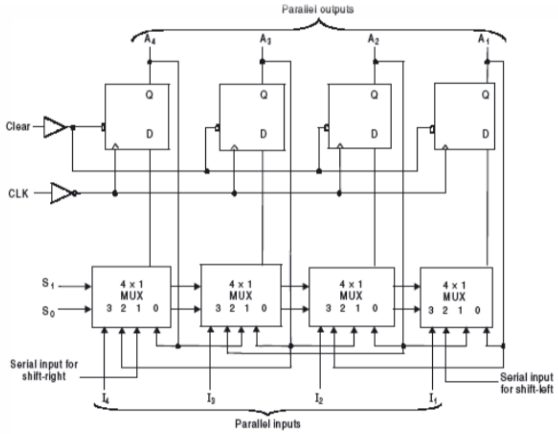

Fig5:a schematic for a universal 4-bit shift register

- This register's mode of operation is selected via the S0 and S1 pins. The parallel mode, the shift left operation, and the shift right operation are all viable alternatives.

- Pin 0 of the first 4x1 multiplexer is linked to the output of the first flip-flop. Please keep in mind the connections in this graphic.
- Shift-right serial input is connected to the first 4X1 MUX's Pin-1. Information is "right-shifted" by the register in this configuration.
- Like the serial input for shift-right, it is connected to pin-2 of the 4X1 MUX. The universal shift register moves all data one place to the left while in this mode.
- In order to facilitate parallel mode operation, the initial 4x1 MUX requires data to be fed to its third pin (I2), which then saves the information in a register.

The third input pin of the 4X1MUX is used to load the remaining data bits from the parallel input.

The parallel outputs of the flip-flops connected to the 41 MUX are designated by the letters Q1, Q2, Q3, and Q4.

Table2: Applications of the Universal Shift Register

OPREATING MODE	S1	S0
Locked	0	0
Shift right	0	1
Shift left	1	0
Parallel loading	1	1

If data may be shifted both to the right and the left under a parallel load, the register is acting as a universal shift register.

4. RESULTS

A RTL SCHEMATIC: The register transfer level (RTL) diagram, often known as the "blueprint of the architecture," is used to compare the actual architecture under development with the ideal architecture that was originally envisioned. The hdl language is used in conjunction with a coding language (such as verilog or vhdl) to transform an architectural description or overview into a functional overview. In order to facilitate analysis, the RTL schematic includes details on the internal connection blocks. See below for a representation in register transfer level (RTL) format of the proposed architecture.

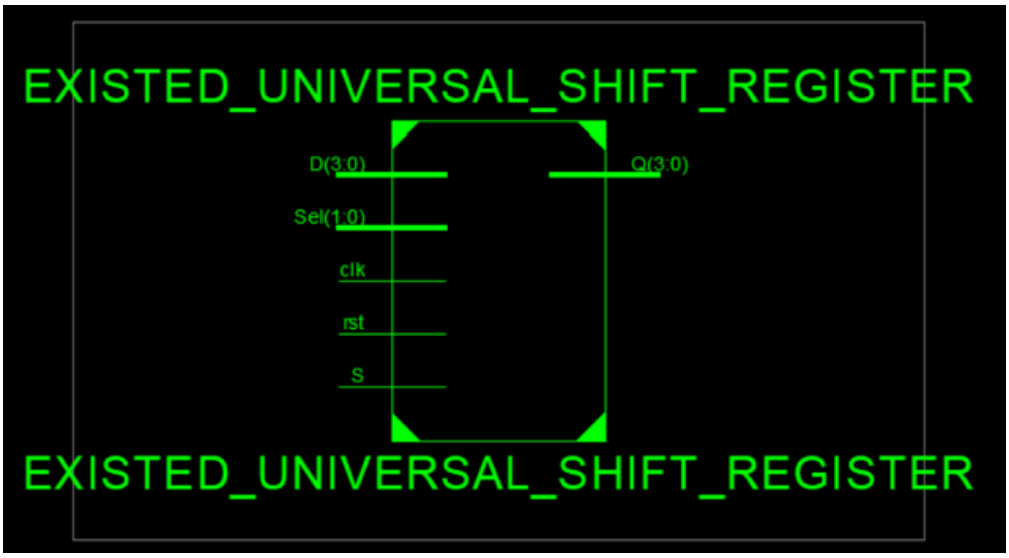

Fig 6: Existing universal shift register RTL schematic

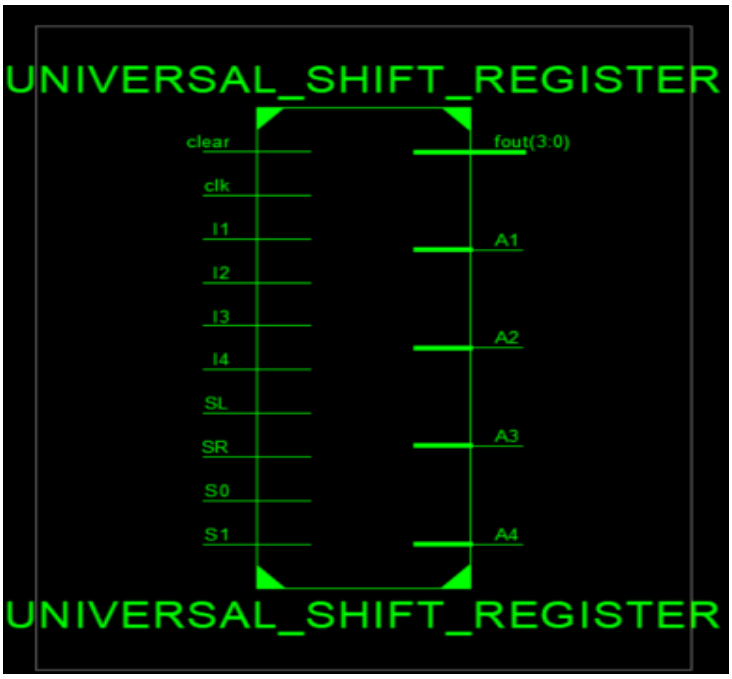

Fig 7: Designed universalshift register RTL diagram

SCHEMATICS IN TECHNOLOGY: The technological schematic provides a representation of the architecture in LUT format, where LUT is an area metric used in VLSI to assess architectural design. The FPGA's lookup tables (LUTs) are where the code's memory allocation is stored.

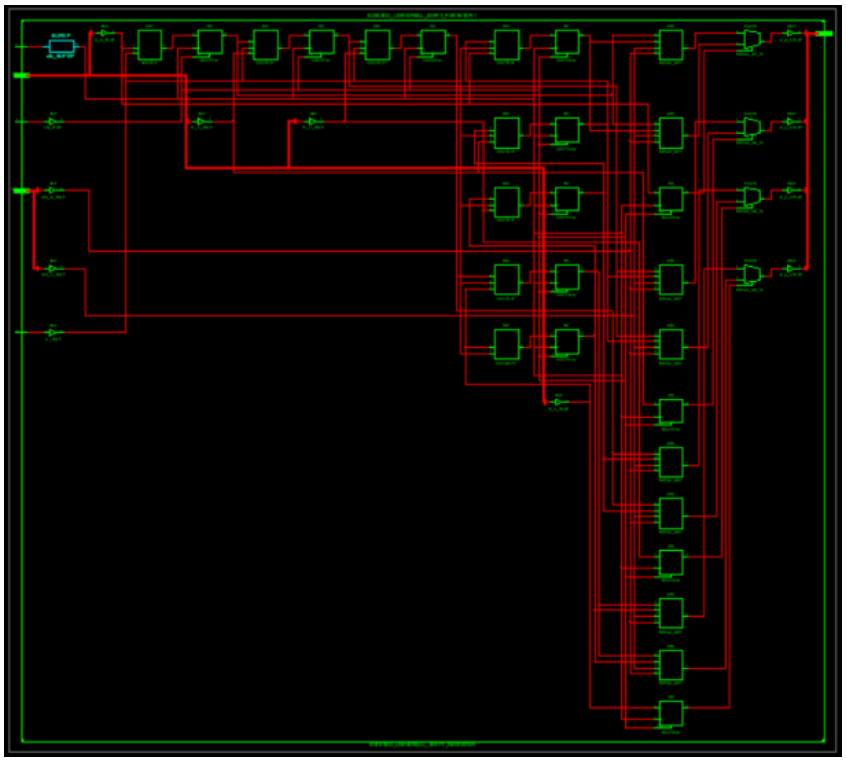

Fig 8: See the current universal shift register technology diagram

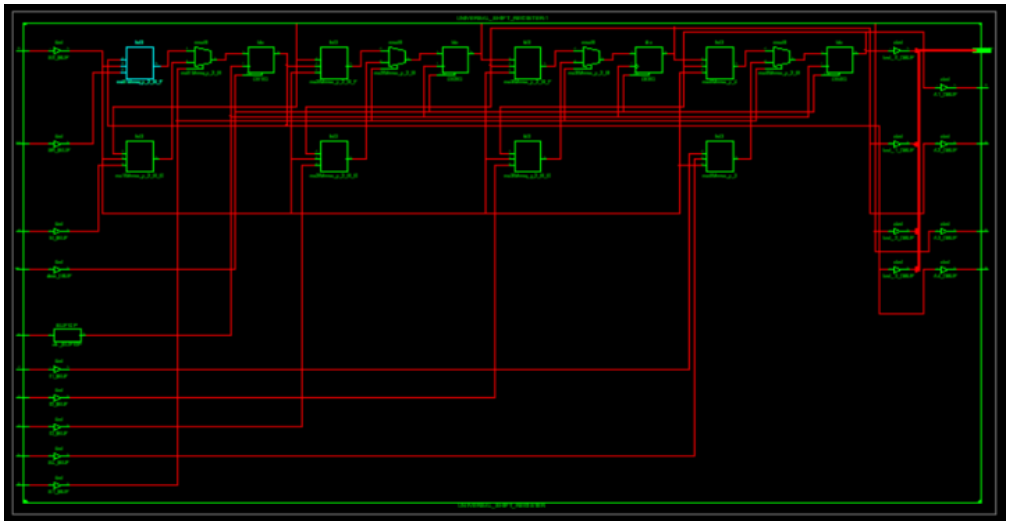

Fig 9:Check out the conceptual diagram for the universal shift register.

SIMULATION:When validating a system, simulation is used, but when validating individual components, schematics are used. You may switch to the simulation view by making the main screen of the tool anything other than an implantation view. Many radix number systems may be provided in this case.

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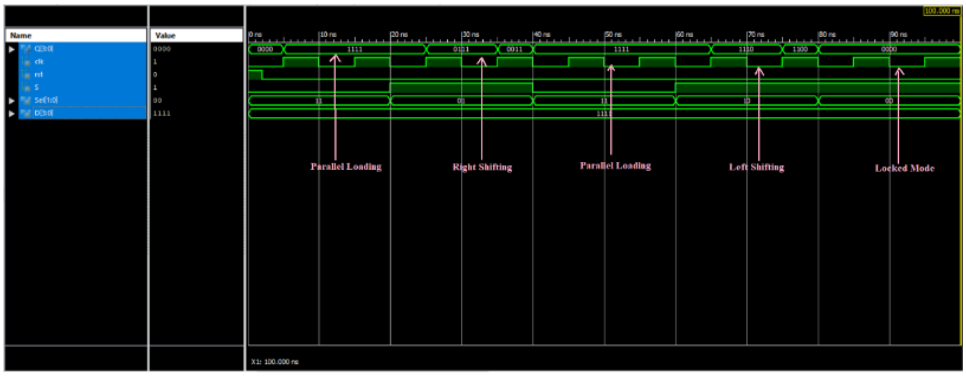

Fig10:Simulated Waveforms of existed universal shift register

Fig 11:Waveforms generated by the proposed universal shift register simulator

PARAMETERS:Think about the area, delay, and power that are mentioned in VLSI. These measures may be used to evaluate various designs. Parameters are determined with the use of the XILINX 14.7 software package and the verilog HDL language.

Table 3:parameter comparaison

PARAMETR	EXISTED UNIVERSAL SHIFT REGISTER DESIGN	PROPOSED UNIVERSAL SHIFT REGISTER DESIGN
NO.OF LUTS	16	8
DELAY (ns)	6.317	4.221
POWER (m.watt)	0.2833	0.1416

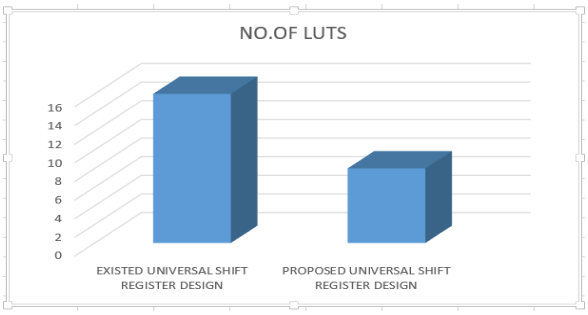

Fig12:LUT comparison bar graph

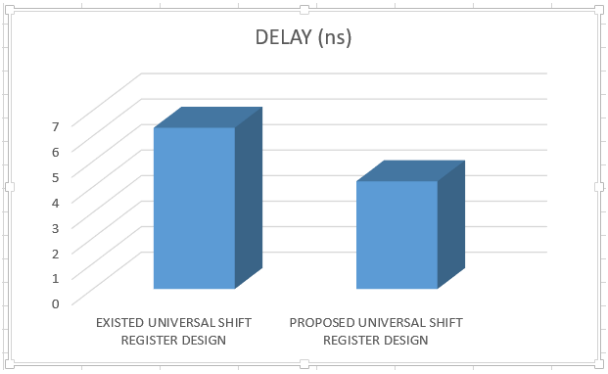

Fig13: Delay comparison bar graph

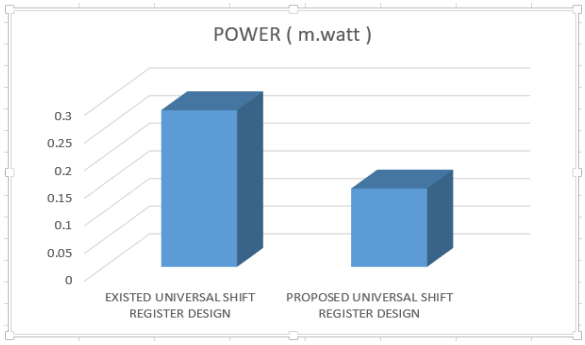

Fig14: power comparison bar graph

5. CONCLUSION

The parameter comparison table demonstrates that the proposed universal shift register improves upon the baseline USR used in this study. The experimental results demonstrate that the proposed universal shift register significantly improves speed with just a marginal increase in footprint and power consumption. Synthesis using the Xilinx ise 14.7 synthesiser is required, as is the creation of an RTL for the structures and verification of their functionality. The area (LUT'S), power, and delay are compared between the existing and planned systems. To reduce power consumption, we may be able to refine the concept of the global shift register by using logic gates that can operate in both directions.

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