Version

.9

DIGITAL RTL DESIGN PROJECT

PLL FUNCTION

Senior Project Validation and Test Plan

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Primary Owner: Ketan Ramani

04/08/2023

Revision History Block

Table 1: Revision History Block

Revision Number	Date MM/DD/YYYY	Revision Changes	Changes made by
0.1	10/23/2022	Document was created. Document only holds the headlines we expect to use throughout this project.	Ketan
0.2	10/29/2022	Added a “Changes made by” section to Revision History Added the first draft of the Introduction	Dylan
0.2	10/30/2022	Edited document by moving Revision History on the second page. Wrote minor details into Derivables, Schedule and Team Roles.	Ketan
0.3	11/13/2022	Wrote Configurations To Be Tested Section	Zachary
0.3	11/13/2022	Wrote minor details into Test items and Testing pass fail criteria.	Ketan
0.4	1/14/2023	Adding to Testing Pass/Fail Criteria, Testing Procedures, Schedule, and Team Roles Added tables to Team Roles and Schedule. Rewrote the Deliverables section and added in our new system architecture.	Dylan
0.5	2/19/2023	Edited: *Configurations to be tested* Edited: *Test/Fail Criteria* Added to: *Testing Procedure* Added to: *Team Roles* Added to: *Schedule*	Zachary Weiss
0.5	2/19/2023	Added : Team Roles Edited : Test Items- explains which items need to be tested.(I haven't finished explaining each module and register.)	Jisu Park

		Added : Testing pass/Fail Added : Testing Procedure. Added : Deliverables (haven't finished yet.)	
0.6	04/09/2023	Reformatted Document to be same style as Design Spec Updated my Section of Team roles Updated Schedule Removed unnecessary details such as mentions of I2C as well as any redundant or unimportant information.	Dylan Iverson
0.9	05/19/2023	Updated Document with peer review feedback. Revamped sections.	Jisu Park

Table of Contents

1. Introduction

Overview

Phase locked loops or PLL's are used for many applications. The current implementation uses mostly analog components. While the Analog version works, it is far from ideal. They take up a lot of physical space as the components used are relatively large, They aren't very intuitive to use, and finally adjusting the design requires making physical changes to the circuit rather than a software update. For these reasons, our team has been tasked with designing a purely digital PLL system. This will solve the previously mentioned problems, as well as hopefully be a more financially viable solution.

The purpose of this document is to explain procedures to test our all digital phase-locked loop(ADPLL) design.

Simulation and emulation

Each module has to be simulated with a testbench in Systemverilog before we emulate it on a FPGA. Simulation output is near perfect. On the other hand, emulation outputs are phasing off due to propagation delay.

2. Test Configuration

For simulation, each module continuously needed to be simulated to see if it returns the value we expected. Each module needed a testbench for simulation.

For emulation, we were familiar with the Intel FPGA development environment, so we chose Terasic Cyclone V GX. On Cyclone V GX, GPIO was the port for the input/output port. The output frequency can be limited by the connection port. The maximum speed restriction of GPIO is 50 MHz. An additional verilog file was needed to connect the FPGA port and the design(button control, GPIO connection, crystal oscillator, HEX display). The FPGA manufacturer provided a user manual for GPIO layout, and System Builder software for the port connection.

3. Test Items

3.1 Simulation

Software

- Modelsim

Using Modelsim to check the design is working properly.

3.2 Emulation

Hardware

- Terasic Cyclone V GX FPGA

Software

- Quartus
- Terasic System Builder

Test Equipment

- Oscilloscope

Using Oscilloscope to check the design is working properly.

3.3 Jittering

Jittering test was not able to be done. TI had equipment to measure jittering, but the output frequency needed to be sent via I2C, which we did not have.

4. Testing Pass/Fail Criteria

Inaccurate Output

Our sponsor has dictated that our system should work with a 2% margin for error. Each output period can be shorter or longer on purpose.The average of the output frequency is within 2% error. This means if our target output is 3 Mhz then our average output should be within the range of 2.94-3.06 Mhz, but there can be a frequency faster than 3.06 or slower than 2.94. Average output frequency within this range will be considered a pass, and anything outside of it would be considered a fail.

Slower Ring Oscillator Frequency

Our design can only take slower input frequency than the ring oscillator. The output frequency is based on the ring oscillator. The ring oscillator needs to be faster than the target output. If the ring oscillator frequency cannot exceed 4 Mhz or the target frequency, it is a failure.

Variable Input Frequency

Our design can only take slower input frequency than the ring oscillator. The output frequency is based on the ring oscillator. The ring oscillator needs to be faster than the target output. When an input frequency is changed, if the output frequency does not change to responding target frequency, it is a failure.

Calculation Error

If the calculation for the control signal is not correct, it is a failure.

Phase Shifting

During simulation, if the output has a different phase than the input, it is a failure.

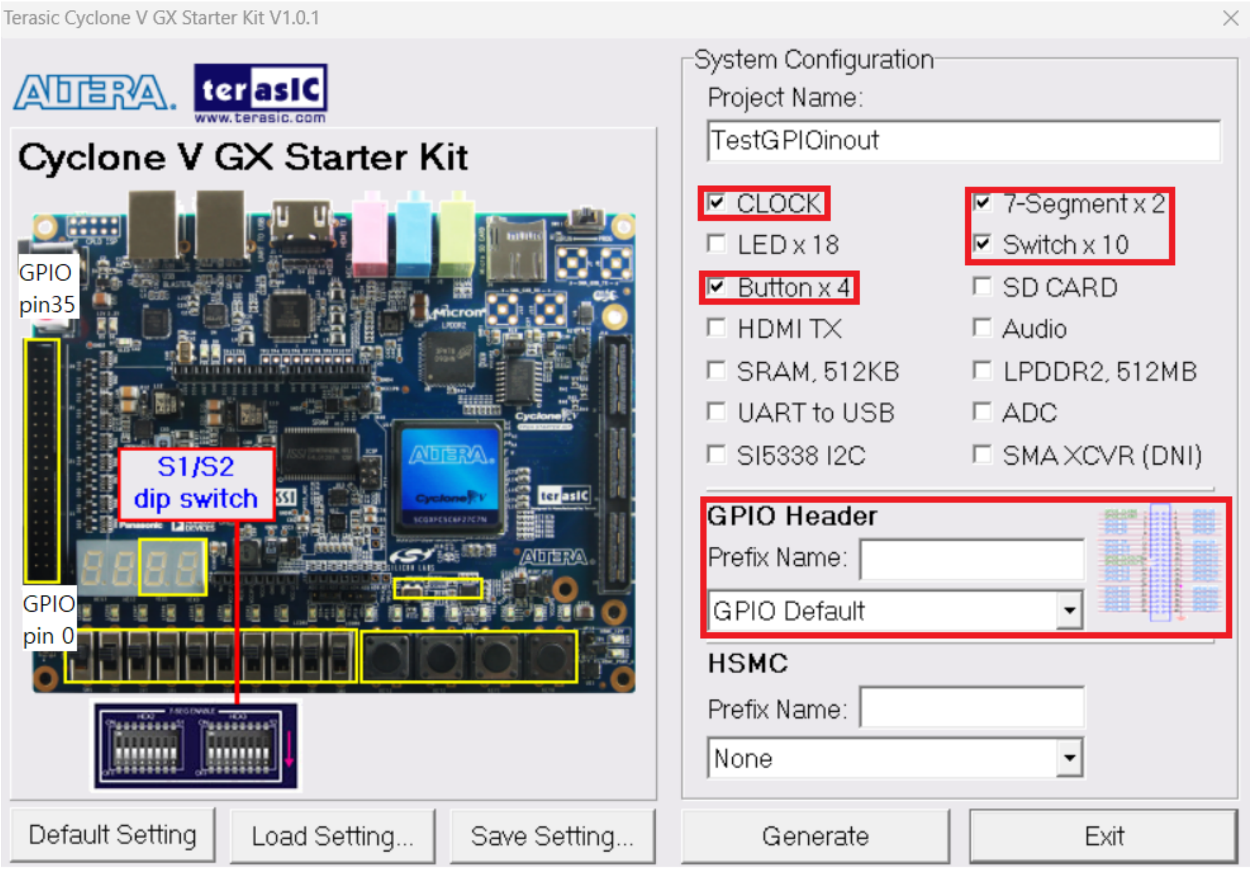
5. Testing Procedures

5.1 Simulation

Individual modules will be tested before the upper level module is built. Each module needs to be tested to make sure it behaves and generates expected output.The upper level testing will be conducted in a similar fashion.

5.2 Emulation

5.2.1 Top level module



Terasic Cyclone V GX Starter Kit V1.0.1

System Configuration

Project Name: TestGPIOinout

☑ CLOCK
☐ LED x 18
☑ Button x 4
☐ HDMI TX
☐ SRAM, 512KB
☐ UART to USB
☐ SI5338 I2C

☑ 7-Segment x 2
☑ Switch x 10
☐ SD CARD
☐ Audio
☐ LPDDR2, 512MB
☐ ADC
☐ SMA XCVR (DNI)

GPIO Header
Prefix Name:
GPIO Default

HSMC
Prefix Name:
None

Figure 1. Terasic System Builder program to select ports.

Terasic System Builder to build the top level entity. Select red boxes in Figure 1. Click the Generate button to create the file. The top level entity needs codes to assign FPGA ports,crystal oscillator frequency, hex display and switches to ADPLL ports. After creating the file, import it in the ADPLL Quartus project. Compilation and upload it on the FPGA.

5.2.2 FPGA and Oscilloscope

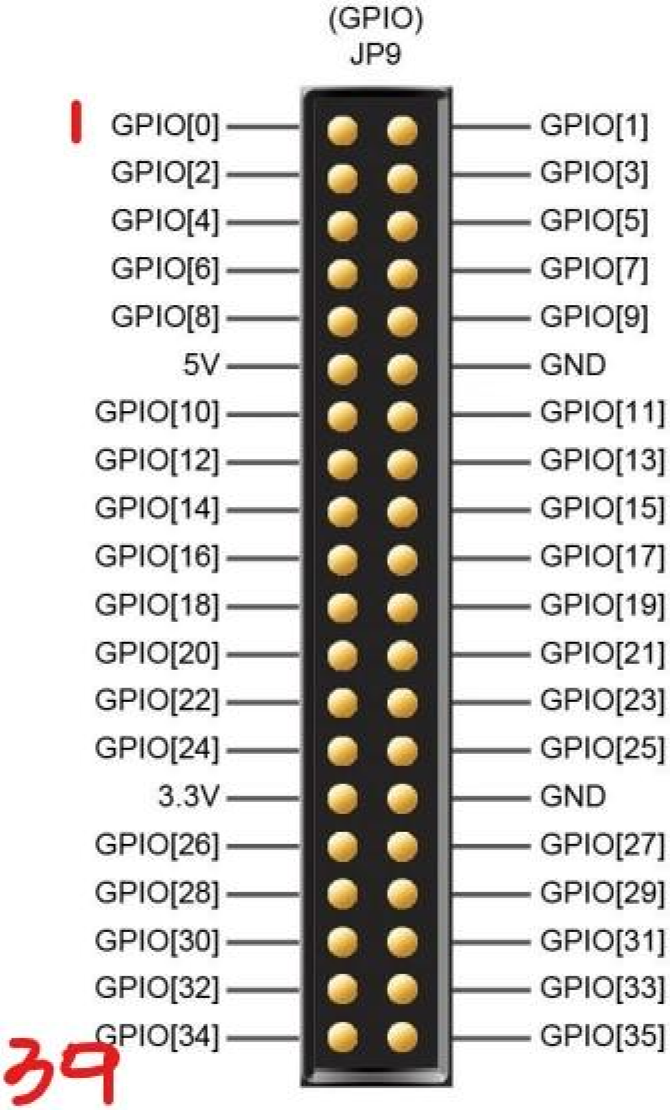
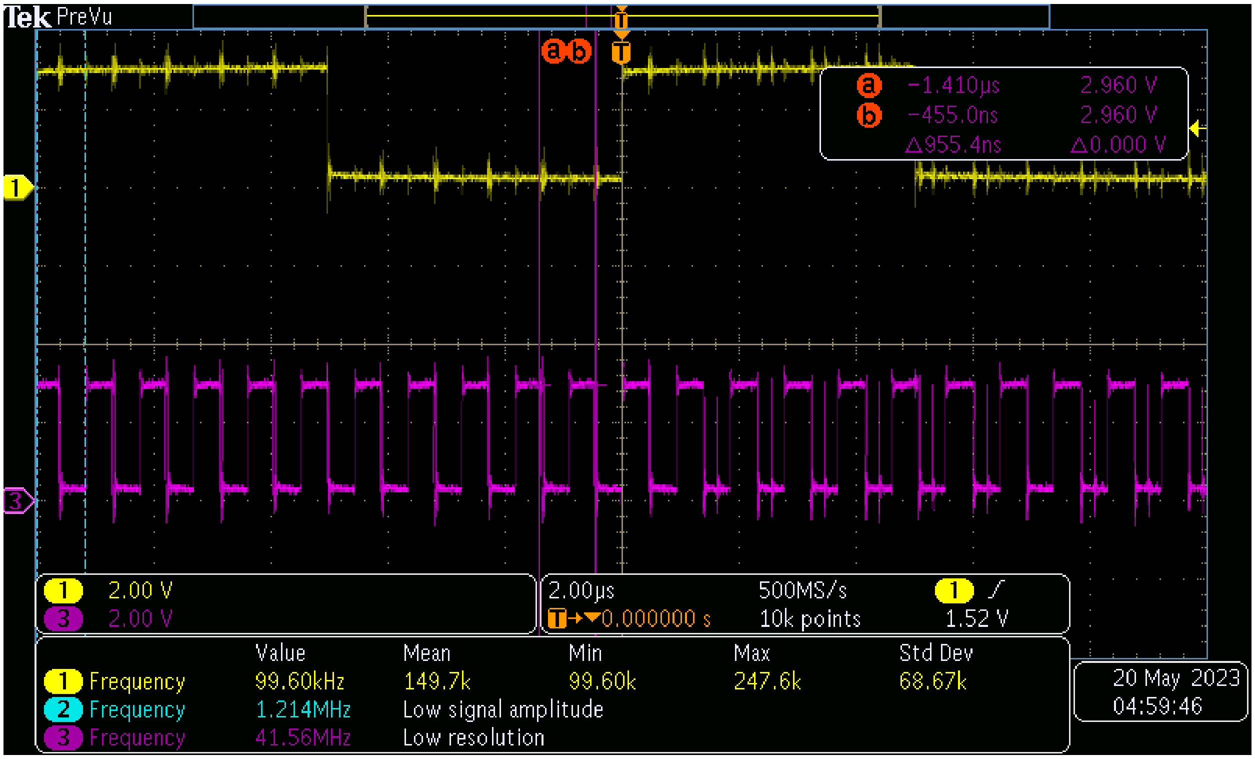


Figure 3-25 GPIO Pin Arrangement

Figure 2. GPIO pin layout.

Connect GPIO pins with the Oscilloscope. Check Figure 2 and the top level entity to connect ports.

5.2.3 Reading Oscilloscope



a −1.410µs 2.960 V
b −455.0ns 2.960 V
Δ955.4ns Δ0.000 V

1 2.00 V
3 2.00 V

2.00µs 500MS/s
T→0.000000 s 10k points
1 1.52 V

20 May 2023
04:59:46

	Value	Mean	Min	Max	Std Dev
1 Frequency	99.60kHz	149.7k	99.60k	247.6k	68.67k
2 Frequency	1.214MHz	Low signal amplitude			
3 Frequency	41.56MHz	Low resolution			

Figure 3. Oscilloscope(MSO 2024). Yellow line is the input frequency. Purple is the output frequency

Use the buttons and switches on FPGA to change configurations. Capture a frame, measure the frequency of a period, and calculate the frequency. Put different configurations and follow the previous steps

5.2.4 Jittering test.

Measure multiple periods and use a software to generate a histogram. It would tell the accuracy of ADPLL output.

6. Deliverables

The simulation has 0% error.

The emulation on the FPGA, due to the propagation delay, the output has phase shift. The ring oscillator frequency is 200Mhz. Even if the input is disconnected, the output creates a target frequency. There are some periods that have a 10~20% error range.

According to TI, our sponsor, our ADPLL design reduces size compared to “Analog PLL in about 12% of the area, or an 86% savings in silicon real estate”. Our design is a feed-forward system, it cannot be perfectly synchronised in the real world. The sponsor said “While never truly locked as a function of the architecture, their approach allows a reasonable approximation with an expected phase lag of roughly 20 ps – 40 ps in a 65 nm CMOS process”.

7. Team Roles

While every part of this project wouldn’t have been possible without a great deal of collaboration, each module and document had a specific member responsible for developing and maintaining. Below is a chart outlining these responsibilities.

Member	Responsibilities and Key roles.
Dylan	Weekly Updates, Controller Module, Multiple_Calculator, Divider Module
Jisu	PRD, Frequency Ratio Module, Top Level Module
Ketan	
Zach	Specification Document, Road Map & Schedule, Ring Oscillator Module

Table 1. Team Roles

8. Schedule

Task	Date to be completed	Current Status
Architecture chosen	11/18/22	Complete
Frequency Ratio Module	02/14/22	Complete
Controller Module	02/14/22	Complete
Divider Module	02/14/22	Complete
Ring Oscillator Module	02/14/22	Complete
RTL Completed	02/14/22	Complete
Order FPGA Board	02/28/22	Complete
Load Solution into FPGA	03/21/22	Complete
Demo Prepared	04/30/22	
Jitter Testing at TI	05/14/23	N/A

Table 2. Schedule

9. Risks and Mitigation

Risks:

- Output and input have different phases.
- Output frequency is stretching out.
- Output is not what is expected.

Risk mitigation:

- The chip could be overheated. If the phase difference or output is getting longer, cool down the chip.

10. Approvals

11. References

BOOKS

S. Brown, Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design(3rd edition),*McGraw Hill, 2014

WEBSITES

Terasic,"C5G_User_Manual"[Online].Available:https://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=830&FID=17219f04ba333c8a2ee2066deab991e5 Accessed on: April 13, 2023

Teledyne Lecroy, "A Robust Method for Measuring Clock Jitter" [Online] Available:https://www.teledynelecroy.com/doc/measuring-clock-jitter-tutorial#:~:text=Test the Oscilloscope Intrinsic Sample Clock Jitter 1,%28Df%2Ff%29 in PPM as %28Df%2Ff%29%2A10%5E6. ... More items Accessed on: May 19,2023

SOFTWARE & HARDWARE

ModelSim-Intel® FPGAs Standard Edition Software Version 20.1.1

Intel® Quartus® Prime Lite Edition Design Software Version 22.1 for Windows

Terasic - All FPGA Boards - Cyclone V - Cyclone V GX Starter Kit

Terasic - Cyclone V GS System Builder

MSO2024B Tektronix | Mouser