Power Efficient Comparator using Adiabatic Logic

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Abstract

The goal of this project for the course ENCS 3330 is to design a 16-bit comparator, aiming to master the techniques of schematic and layout design with less power. The details of designing a 16-bit comparator are given in this paper we use a process of 0.6u. It involves the methodology, circuit implementation, schematic simulation, layout. We start from circuit level and then draw the layout in the environment of CMOS. Finally, we extract the layout as a symbol in the schematic for re-simulation to obtain the results of the performance measure 13 ns and the power is 0.31m Watt. In designing, propagation delay, Area and power are considered. All parameters of circuit are decided and the circuit plot and waveform are produced, and we would test and verify every part of the CMOS circuit developed. The test results from simulation can meet the requirement. It means that the logic design, schematic and layout are correct, and our project can satisfy the requirements.

1 INTRODUCTION

Magnitude Comparator is a combinational circuit which compares the two n-bit numbers and it gives the output in form of the three status variables. That is A=B, A>B, A<B .and depending on the inputs, at any given time, only one of the output is high.

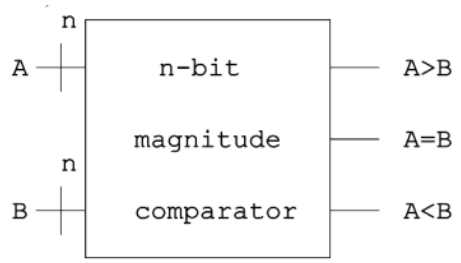

Figure 1: block diagram of n-bit magnitude[1]

1-bit comparator:

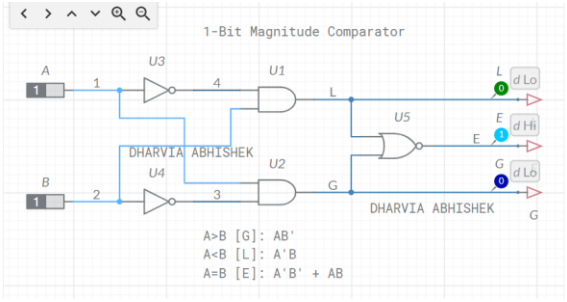

Figure 2 : 1-bit magnitude comparator using logic gates[2]

when we are comparing the two 1-bit numbers, then for the two bits we have total four different combinations. And this is the truth table of the 1-bit comparator, So as you can see when both the bits are same then we can say A=B that means whenever both A and B are 0 or both are 1 so A=B, the logical expression is equivalent to Output = A-B-+AB, similarly this A>B, when the number A is >B .and that is only happening, when the number SA=1 and B=0, So if we see the logical expression for this (A>B) = AB-Similarly A <B, when the number A is equal to 0 and B equal to 1 so the logical expression is (A<B) = A-B

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Figure 3 : 1-bit magnitude comparator truth table[3]

The circuit magnitude comparator, for comparing two n-Bit numbers, has 2n inputs and 2n entries in the truth table, for 1-Bit numbers, 2-inputs and 4-rows in the truth table. similarly for 16-Bit numbers 16-inputs and 216-rows in the truth table. style of the logic gates we used influences the size, power dissipation, speed, and the wiring complexity of a circuit. the size of the circuit depends on the number of transistors and their sizes, all of these characteristics vary from one logic style to another, choosing the best choice of logic style is the most important thing for circuit performance, good cost benefit.

2 DESIGN AND IMPLEMENTATION

We use Diode-Free Adiabatic Logic (DFAL) it is a logic design methodology aimed at minimizing energy dissipation in digital circuits. Unlike traditional CMOS logic, which consumes significant power due to the charging and discharging of capacitive loads, adiabatic logic techniques focus on energy recovery and reducing power loss during the switching of transistors. In order to build 16-bit Comparator using an Adiabatic technique, we build many components that are required in order to design the 16-bit Comparator the required components we used are as follows :

2.1 Inverter Gate

A Diode-Free Adiabatic Logic (DFAL) inverter is an essential component in adiabatic logic circuits, designed to minimize energy dissipation by eliminating diodes and focusing on energy recovery during the switching process. The inverter, being a fundamental building block, is critical in implementing more complex logic functions while maintaining the energy efficiency goals of adiabatic logic.

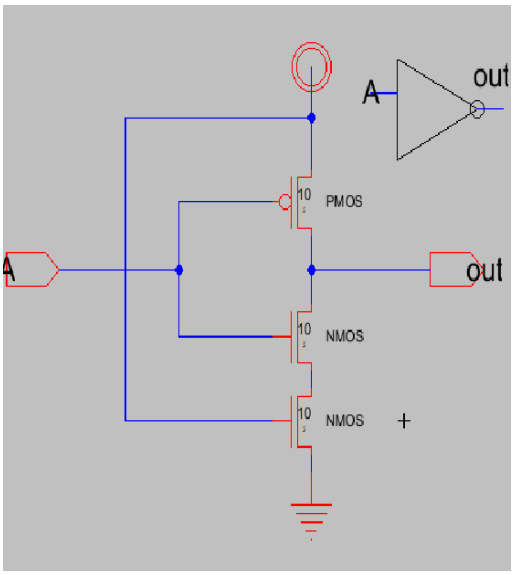

Figure 4 : inverter gate schematic

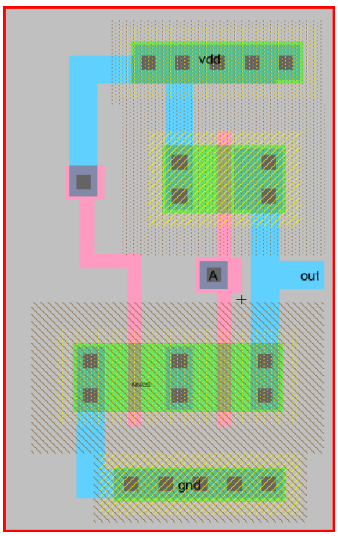

Figure 5 : inverter gate layout.

inverter Sizing : FIRST WE SET THE WIDTH OF PMOS DEVICES → WP =10 AND LENGTH =2

AND THE WN = WP/2 = 5 ,LENGTH =2

AREA = NUM OF PMOS *(Wn*Ln)+ NUM OF NMOS *(Wp*Lp)

AREA = (10*2)+2(10*2)=20+40=60 micrometer

2.2 NAND GATE

It has two p-channel MOSFETs (M1 and M2 connected in parallel) and two nMOS transistors (M3 and M4 connected in series). Output load capacitance is discharged through nMOS transistors M3, M4 and a discharging transistor M5 whose gate is directly connected with VDD .Gates of M2 and M3 are tied together with an input A and M1 and M4 with another input B.

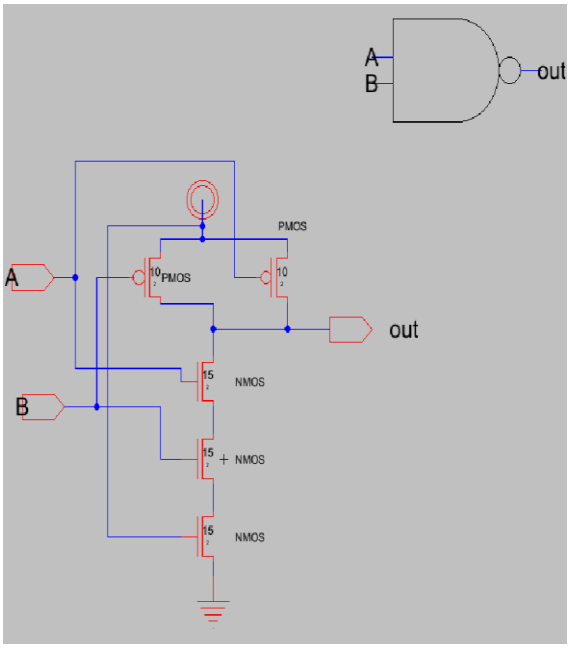

Figure 6 : 2-inputs NAND gate schematic

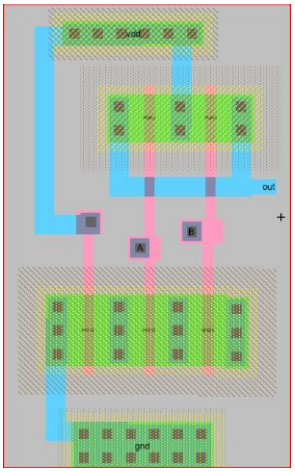

Figure 7 : 2-inputs NAND gate layout

NAND GATE SIZING : FIRST WE SET THE WIDTH OF PMOS DEVICES → WP =10 AND LENGTH =2

AND THE WN = WP/2 = 5 LENGTH =2

AREA = 2*(20*2)+3(15*2)=80+90=170 micrometer

2.3 NOR GATE

It has two p-channel MOSFETs (M1 and M2) and two nMOS transistors (M3 and M5) and a discharging nMOS transistor M4 whose gate is directly connected with VDD .Gates of M1 and M5 are connected with an input A and M2 and M3 with another input B.

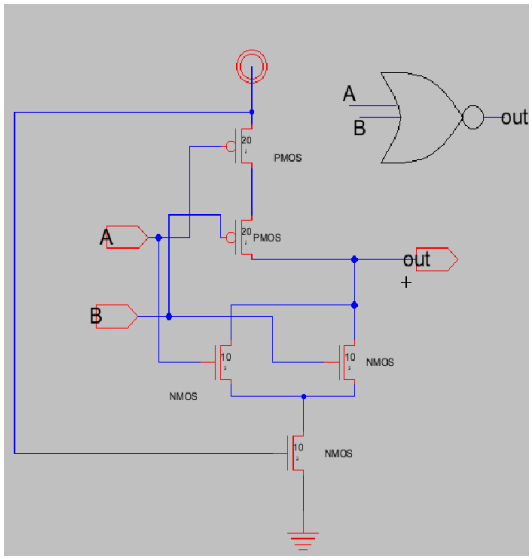

Figure 8 : 2-inputs NOR gate schematic

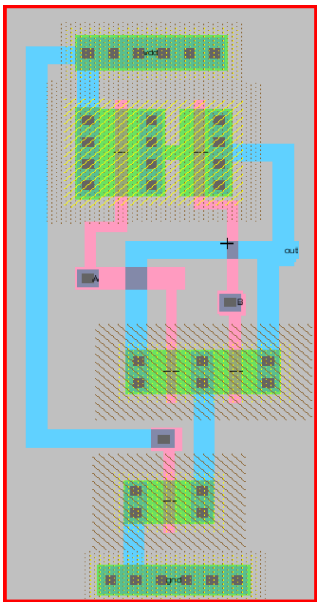

Figure 9 : 2-inputs NOR gate layout

NOR GATE SIZING: FIRST WE SET THE WIDTH OF PMOS DEVICES → WP =10 AND LENGTH =2

AND THE WN = WP/2 = 5 LENGTH =2

AREA = 2*(20*2)+3(10*2)=80+60=140 micrometer

2.4 AND GATE

In order to get and gate we concert and gate with inverter

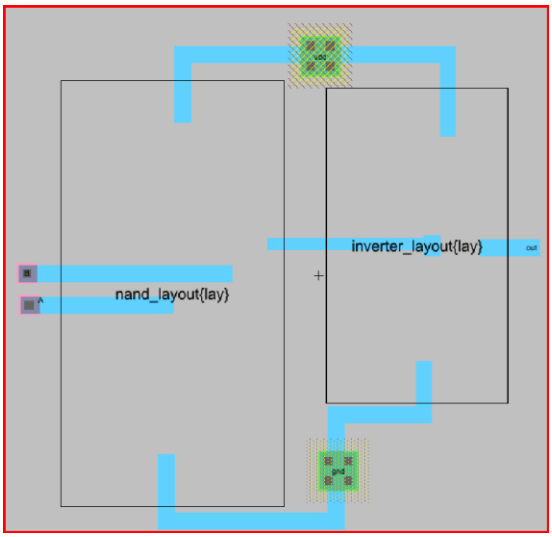

Figure 10: 2-inputs AND gate layput

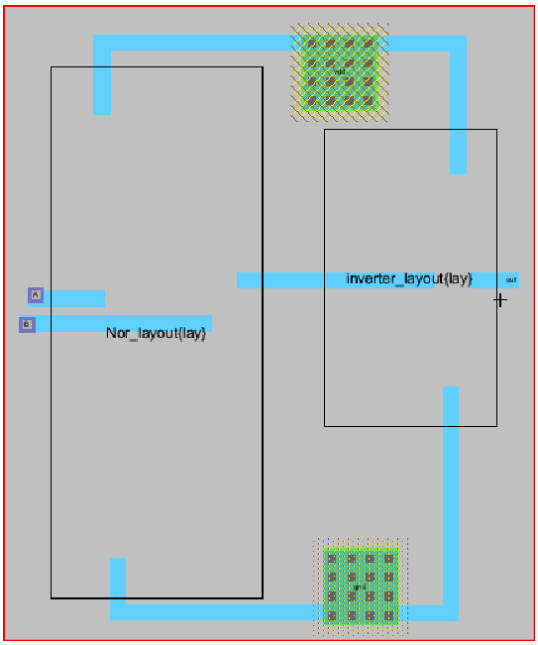

Figure 11 : 2-inputs OR gate Sechmtic &layput

2.5 1-BIT COMPARATOR

The circuit of the 1-bit Comparator was implemented using invertors, nand and NOR as shown in the following figure :

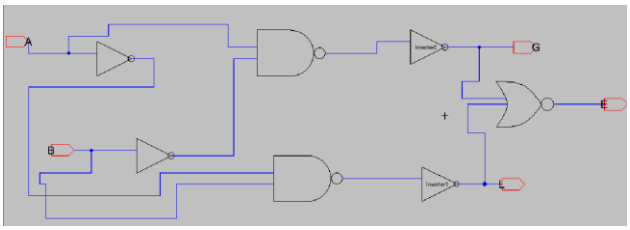

Figure 12 : ONE BIT COMPARATOR SCHEMATIC

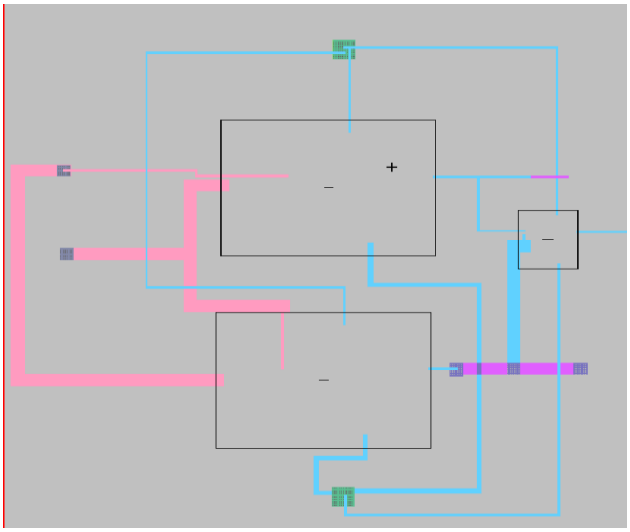

Figure 13 : ONE BIT COMPARATOR LAYOUT

AREA = 2* AREA inverters + 2* AREA NANDS+ AREA NOR

AREA = 2 * 60 + 2 * + 130 = 430 micrometer

2.6 2-BIT COMPARATOR

The circuit of the 2-bit Comparator was implemented using 2 of 1-Bit comparator circuit, invertors, nand and NOR as shown in the following figure :

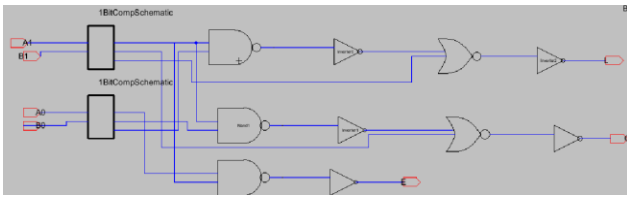

Figure 14 : TWO BIT COMPARATOR SCHEMATIC

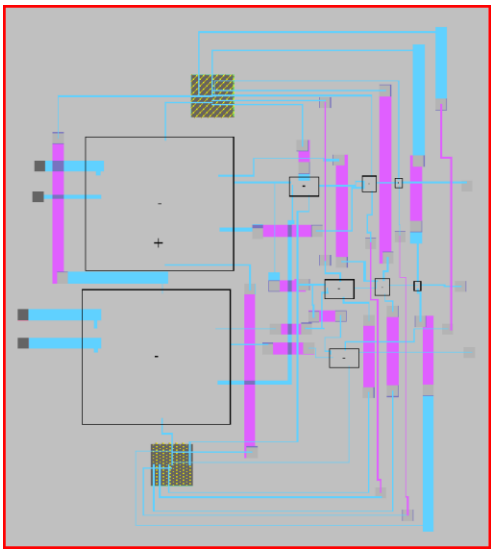

Figure 15 : TWO BIT COMPARATOR LAYOUT

AREA = 2* AREA 1-Bit Comparator+ 3 ands (Nand + inverter) + 2 NORS

AREA= 430 * 2 + 3(140 + 60) + 2*(140) = 1740 micrometers

2.7 4-BIT COMPARATOR

The circuit of the 4-bit Comparator was implemented using 2 of 2-Bit comparator circuit, invertors, nand and NOR as shown in the following figure :

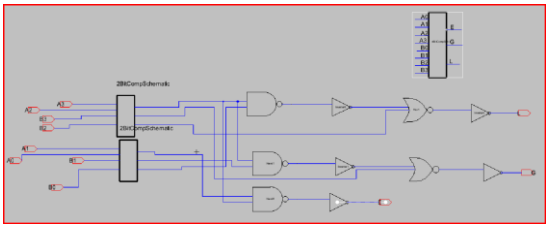

Figure 16 : FOUR BIT COMPARATOR SCHEMATIC

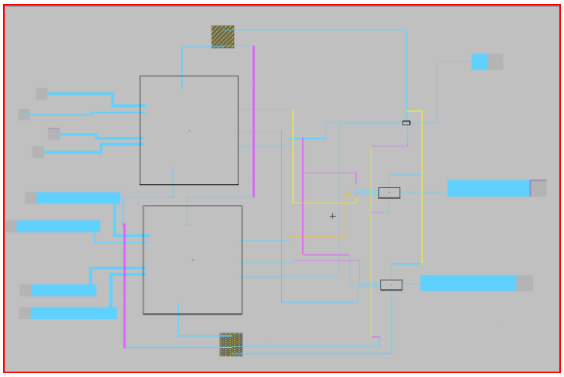

Figure 17 : FOUR BIT COMPARATOR LAYOUT

AREA = 2* AREA 2-Bit Comparator+ 3 ands (Nand + inverter) + 2 NORS

AREA = 1740 * 2 + 3(140+60) + 2(140) = 4360 micrometer

2.8 8- BIT COMPARATOR

The circuit of the 8-bit Comparator was implemented using 2 of 2-Bit comparator circuit, invertors, nand and NOR as shown in the following figure :

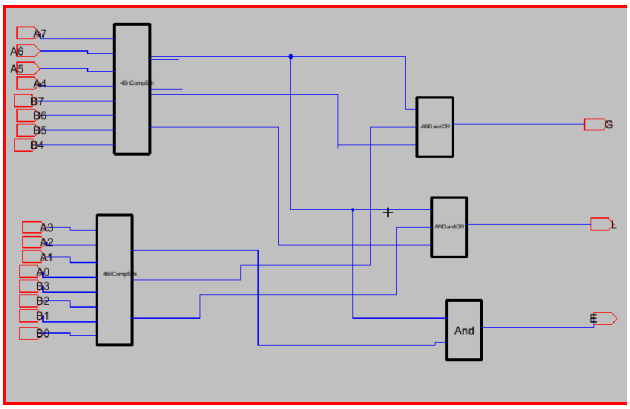

Figure 18 : EIGHT BIT COMPARATOR SCHEMATIC

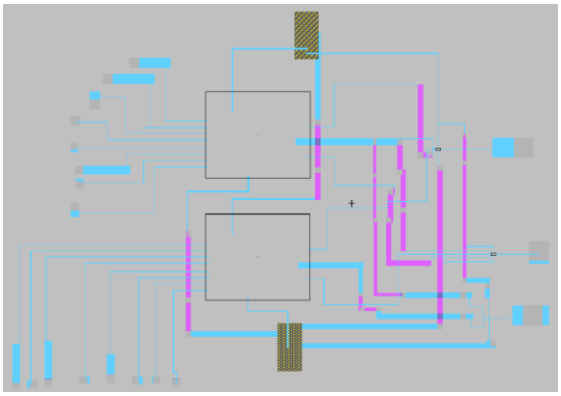

Figure 19 : EIGHT BIT COMPARATOR LAYOUT

AREA = 2* AREA 4-Bit Comparator+ 3 ands (Nand + inverter) + 2 NORS

AREA = 4360 * 2 + 3(140+60) + 2(140) = 9600 micrometer

2.9 16-BIT COMPARATOR

The circuit of the 16-bit Comparator was implemented using 2 of 8-Bit comparator circuit, invertors, nand and NOR as shown in the following figure :

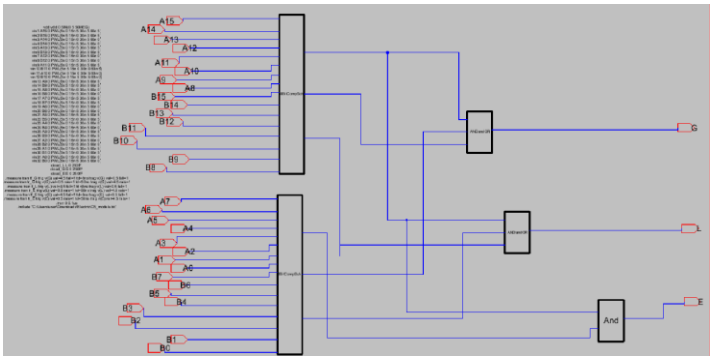

Figure 20 : 16 BIT COMPARATOR SCHEMATIC

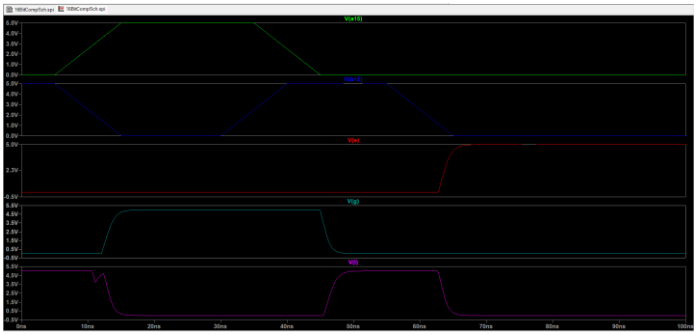

Figure 21 : 16 BIT COMPARATOR SCHEMATIC simulation

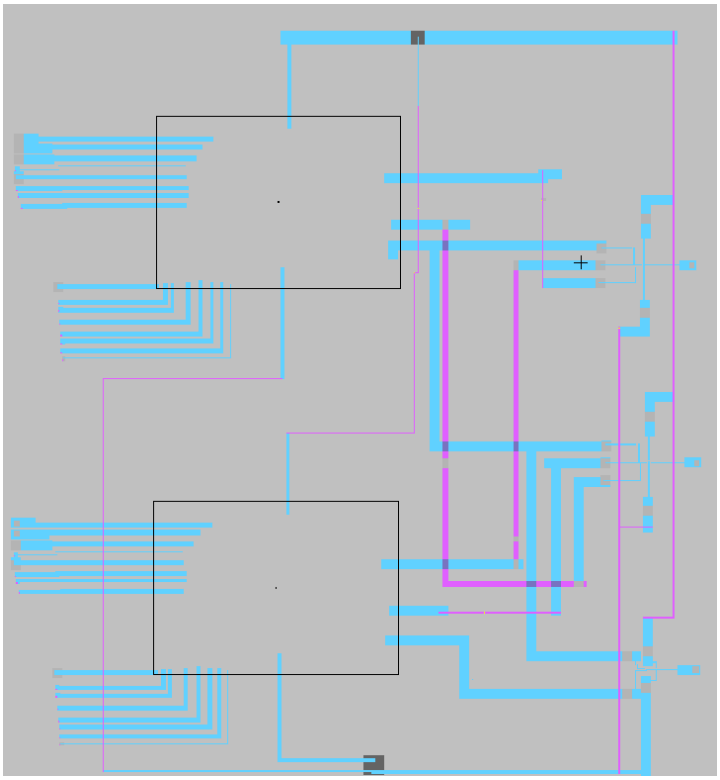

Figure 22 : 16 BIT COMPARATOR LAYOUT

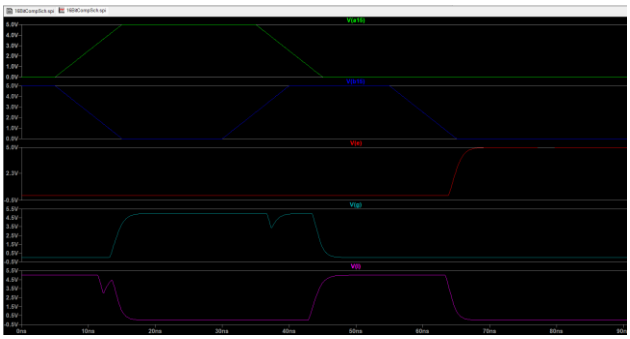

Figure 23 :16 BIT COMPARATOR layout simulation

AREA = 2* AREA 8-Bit Comparator+ 3 ands (Nand + inverter) + 2 NORS

AREA = 9600 * 2 + 3(140+60) + 2(140) = 20080 micrometer

3 16x16 bit magnitude comparator power and delay

3.1 16 BIT COMPARATOR TOTAL POWER

In order to calculate the power we use this code :

.measure tran Vout_L FIND V(L) AT=60n

.measure tran Vout_G FIND V(G) AT=60n

.measure tran Vout_E FIND V(E) AT=60n

.measure tran Pstatic_L PARAM='Iout_L*Vout_L'

.measure tran Pstatic_G PARAM='Iout_G*Vout_G'

.measure tran Pstatic_E PARAM='Iout_E*Vout_E'

The result was :

```
iout_l: i(cload_l)=-1.42812e-005 at 6e-008
iout_g: i(cload_g)=1.73255e-005 at 6e-008
iout_e: i(cload_e)=-2.62371e-005 at 6e-008
vout_l: v(l)=9.63508e-007 at 6e-008
vout_g: v(g)=1.22889e-008 at 6e-008
vout_e: v(e)=5 at 6e-008
pstatic_l: (iout_l*vout_l)=-1.376e-011
pstatic_g: (iout_g*vout_g)=2.12911e-013
pstatic_e: (iout_e*vout_e)=-0.000131186
```

Figure 24 : calculated power from the code

From the figure above

Power for Less than (L) = -1.376×10^{-11} W

Power greater than (G) = 2.12911×10^{-13} W

Power equals (E) = -1.31186×10^{-4} W

total power = $(-1.376\times10^{-11})+(2.12911\times10^{-13})+(-1.31186\times10^{-4})$ $\approx -1.31186\times10^{-4}$ W

3.2 Speed

In order to calculate the speed, we have to find the time difference when the input (how chanced the outout) reaches 50% of its value means 5/2 = 2.5 and when the output reaches 50% of its value means 5/2 its nearly to 2.5 :

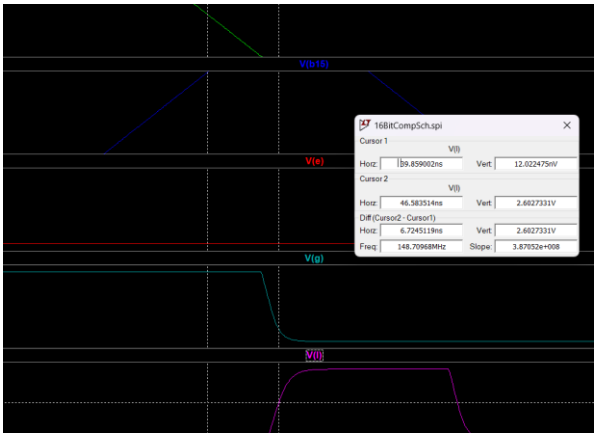

Figure 25 : delay when A<b

The figure above shows the time when the input reaches 50% of its value “2.5V” is almost 40ns, The figure above shows the time when the output equals reaches 50% of its value “2.5V” is almost 46ns, so the delay = 46-40 = 6ns .

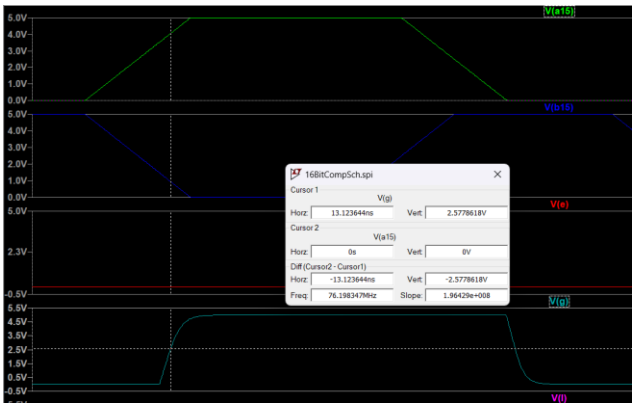

Figure 26 : delay when A>B

The figure above shows the time when the input reaches 50% of its value “2.5V” is almost Zero ns, The figure above shows the time when the output equals reaches 50% of its value “2.5V” is almost 13 ns, the delay = 13 - 0 = 13.

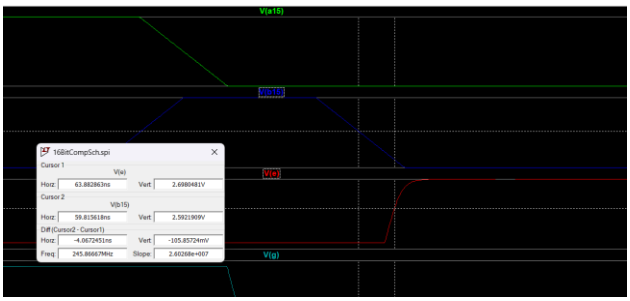

Figure 27 : delay when A= B

The figure above shows the time when the input reaches 50% of its value “2.5V” is almost 60ns, The figure above shows the time when the output equals reaches 50% of its value “2.5V” is almost 63ns, delay = 63 – 60 = 3ns.

Over all the delay will be the worst case which is 13ns it happened when A > B “greater than”

4 CONCLUSION

In this paper we build a 16-Bit Power Efficient Comparator using Adiabatic Logic Schematic and layout, starting with 1-bit Comparator then 2-bit Comparator then 4-bit Comparator them 8-bit Comparator then 16-bit Comparator we use 263 transistors, The proposed comparator has a maximum operating frequency, low-power dissipation and minimum delay. Our proposed low power we achieving performance measure 13 ns and the power is 0.31m Watt. These advantages of the proposed comparator make it suitable for various applications such as scientific computations, test circuits, memory addressing logic etc.

5 REFERENCES

[1]:

https://www.researchgate.net/figure/Architecture-of-4-Bit-special-adder-In-the-figure-3-A-B-C-D-are-four-inputsC0-and-C1_fig1_273058970

[2]:
https://www.multisim.com/content/CUbFk2UsbD2GSByTkbztUR/1-bit-magnitude-comparator/

[3]:

https://www.geeksforgeeks.org/magnitude-comparator-in-digital-logic/#:~:text=1%2DBit%20Magnitude%20Comparator,than%20between%20two%20binary%20numbers