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| **ELC363-02** |  | **FALL 2020** |

**ALU Design**

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**Instructor: Dr. Hernandez**

# General ALU Design

ALU’s have two inputs, one from registers and one from a multiplexer which determines if the second input comes from a register or from the instruction itself.

ALU’s also have a control input, ALUOp.

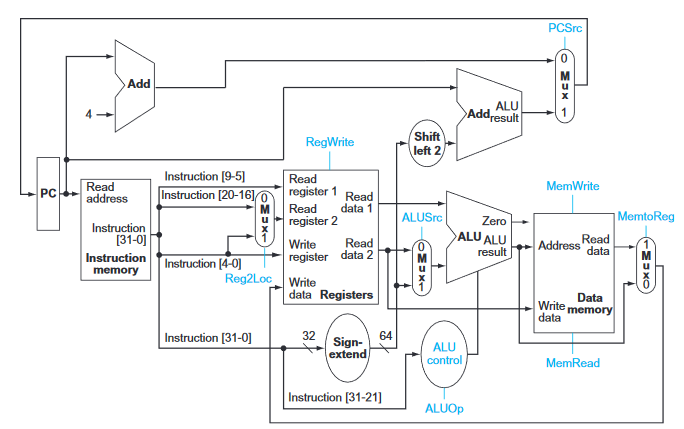


Figure 4.15: Processor datapath

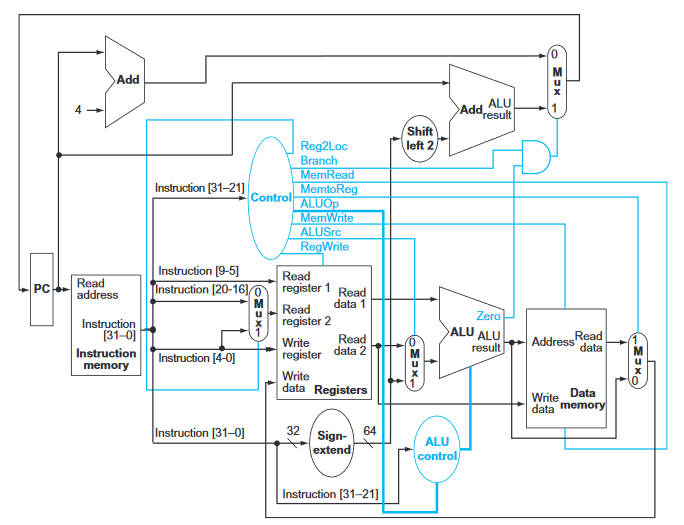


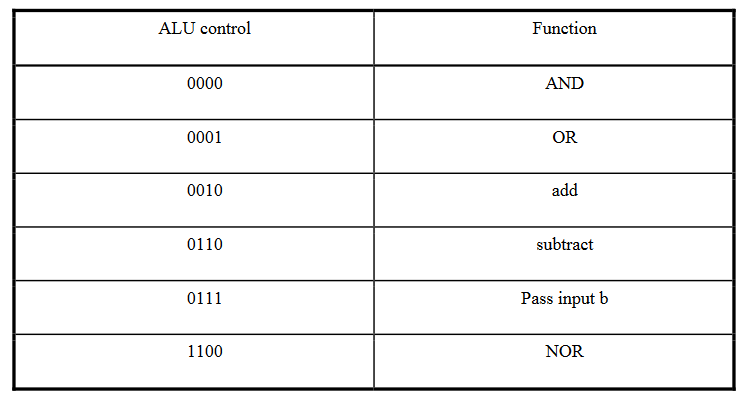
Figure 4.17: Datapath with control unit

The ALU control (ALUOp) is controlled by the instruction. This defines what operation to perform.

The ALU also has a zero output which tells us if the result is 0.

# Project ALU Design

This project calls for a 64 bit ALU. We can disregard overflow detection as stated in the lab document.



Additionally, the lab requires an “active high output that is asserted when the result is zero.” Which is exactly what the zero output of the ALU does. This statement is redundant.

## Desirables:

Verilog Code,

Waveforms that show that the ALU works for all functions.