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|  | School of Engineering |

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| **ENG 312** |  | **FALL 2019** |

**Processor Design Project 2 Behavior**

**Date: November 27th, 2020**

**Jeffrey Blanda, Alex Bolen**

**Instructor: Dr. Hernandez**

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| Instructions | | | | | |
| Name | Flags  [63:55] | OpCode  [54:44] | Rm  [20:16] | Rn  [9:5] | Rd  [4:0] |
| LDUR | X11110000 | XXXXXXXXXXX | XXXXX | Read Memory Address from This Register | Store value from memory into this register |
| STUR | 11X001000 | XXXXXXXXXXX | XXXXX | Adds the contents of this register to the full instruction to get the destination memory address | Store the value in this register |
| ADD | 000100010 | 10001011000 | Register with value 2 | Register with value 1 | Register data is stored |
| SUB | 000100010 | 11001011000 | Register with value 2 | Register with value 1 | Register data is stored |
| AND | 000100010 | 10001010000 | Register with value 2 | Register with value 1 | Register data is stored |
| ORR | 000100010 | 10101010000 | Register with value 2 | Register with value 1 | Register data is stored |
| CBZ | 10X000101 | XXXXXXXXXXX | XXXXX | XXXXX | Value to compare |
| B | 000000010 | 11001011000 | Same register as Rn | Any register | XXXXX |