Application Report
SLVA721A–February 2017–Revised August 2017

Basic Calculation of an Inverting Buck-Boost Power Stage

Ilona Weiss

ABSTRACT

This application note provides basic formulas that you need to design the power stage of an inverting buck-boost converter. The premise is that the power switch is integrated in the IC and the rectification is done by a diode (non-synchronous power stage). It provides all the formulas and considerations that you need to select the external power components such as the inductor, the diode, and the input and output capacitors. As the internal switch current capability is limited it will also provide an estimation to judge whether the load current can meet the IC specification.

Preconditions for the design:

- Basic understanding of the functionality, refer to this TI Training
- *Continous-Conduction-Mode* (CCM) consideration
- Large signal consideration
- Integrated switch
- Non-synchronous converter
- Basic understanding of the DC Bias Effect of Ceramic Capacitors

Trademarks

All trademarks are the property of their respective owners.

1 Basic Configuration of the Power Stage

Figure 1 shows the simplified schematic of an inverting buck-boost power stage. This topology is a so-called flyback topology where the energy is transferred to the output when switch S1 is open.

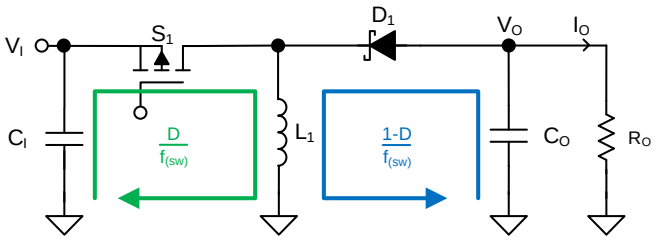

Figure 1. Simplified Schematic of an Inverting Buck-Boost Stage

Copyright © 2017, Texas Instruments Incorporated

The following waveforms describe the time characteristics of the necessary currents and voltages. These values are considered in this application note.

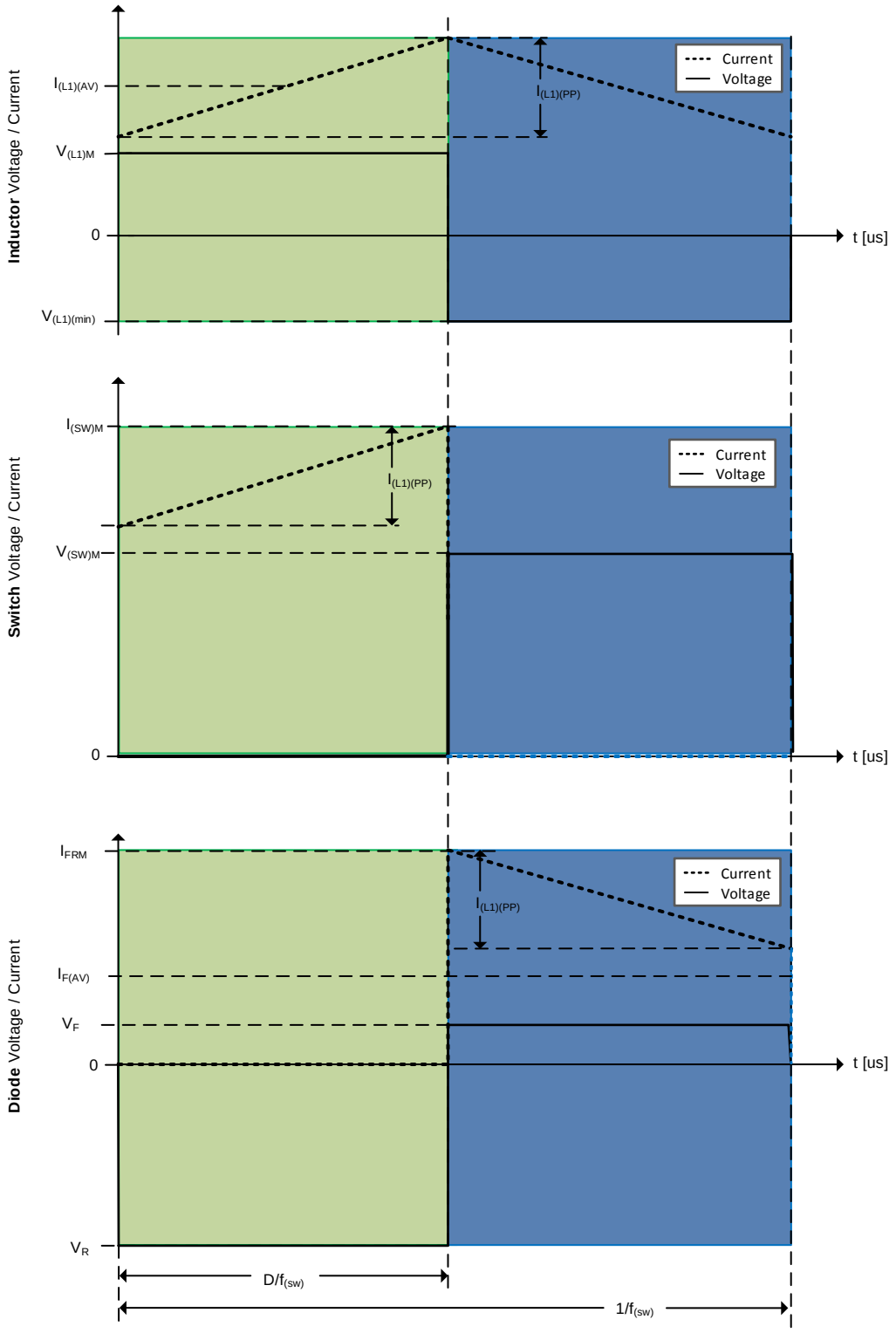

Figure 2. Simplified Waveforms of an Inverting Buck-Boost Stage

Copyright © 2017, Texas Instruments Incorporated

In order to design each external component and to analyze the IC capabilities, the following parameters must be prepared:

Table 1. Design Parameters

Description	Parameter	Unit
Input voltage range	$V_{I(min)}$ to V_{IM}	V
Output voltage	V_O	V
Maximum average output current	I_{OM}	A
Forward voltage drop of the rectifier diode	V_F	V
Allowed inductor current ripple	$I_{(L1)(PP)}$	mA
Recommended Inductance Range (data sheet)	L1	µH
Minimum switching current limit of internal switch S1 (data sheet)	$I_{(SW)(min)(lim)}$	A
Switching frequency of the internal switch S1 (data sheet)	$f_{(SW)}$	MHz

As for all inductive converters one of the essential formulas is the steady state duty cycle. This can be derived from the inductor volt-second balance and the capacitor charge balance. For a robust design it is recommended to calculate the worst-case scenario. For the inverting buck-boost this means the **maximum duty cycle D** present at the minimum input voltage. It is specified as:

$$D = \frac{-V_O + V_F}{-V_O + V_F + V_{I(min)}} \quad (1)$$

Rearranging Equation 1 provides the **DC conversion ratio V_O / V_I**:

$$\frac{V_O}{V_I} = \frac{-D}{1-D} \quad (2)$$

2 Check the Internal Switch S1

In the first step it is important to evaluate if the internal switch S1 can withstand the output current requirement of the application. The minimum switching current limit $I_{(SW)(min)(lim)}$ of the internal switch S1 of the chosen converter must be higher or equal to the **maximum switching current $I_{(SW)M}$** that is defined as:

$$I_{(SW)M} = \left(I_{OM} \times \frac{V_{I(min)} + V_F - V_O}{V_{I(min)}}\right) + \left(\frac{I_{(L1)(PP)}}{2}\right) \quad (3)$$

It is also possible to calculate the **maximum output current I_{OM}** that the converter can achieve by rearranging Equation 3, as:

$$I_{OM} = \left(I_{(SW)(min)(lim)} + \frac{I_{(L1)(PP)}}{2}\right)\left(\frac{V_{I(min)}}{V_{I(min)} + V_F - V_O}\right) \quad (4)$$

The **maximum voltage stress that the switch must withstand is $V_{(SW)M}$** and can be calculated with:

$$V_{(SW)M} = V_{IM} + V_F - V_O \quad (5)$$

3 Select the Inductor

The next step is to select the required inductance. If the inductance range is not limited by the IC you can estimate the required inductance based on the well-known differential equation:

$$L1 = \frac{V_I \, D}{I_{(L1)(PP)} \, f_{(SW)}} \quad (6)$$

The **average inductor current $I_{(L1)(AV)}$** is calculated by:

$$I_{(L1)(AV)} = \frac{I_O}{1-D} \quad (7)$$

Copyright © 2017, Texas Instruments Incorporated

However, most of the converters are already optimized for specific inductance ranges which are described in the data sheet. In this case, use the recommended value and calculate the **inductor current ripple $I_{(L1)(PP)}$** which is a rearrangement of Equation 6:

$$I_{(L1)(PP)} = \frac{V_{I(min)} D}{f_{(SW)} L1} \quad (8)$$

The **maximum inductor current $I_{(L1)M}$** is the sum of the average component and the half of the peak-to-peak inductor current ripple and is as well the maximum switch current shown in Equation 3.

$$I_{(L1)M} = I_{(SW)M} = I_{(L1)(AVG)} + \frac{I_{(L1)(PP)}}{2} \quad (9)$$

NOTE: The inductor must always have a higher current rating than Equation 3 as the inductance decreases with increased current. As a general guideline, the saturation current of the inductance shall be: $I_{(L1)(sat)} \geq 1.2 \times I_{(L1)M}$

As soon as switch S1 opens the energy is transferred to the output.

This means that the output voltage flies back to the switching node and the **voltage across the inductance $V_{(L1)}$** becomes the output voltage minus the voltage drop of the diode: $V_{(L1)M} = V_O - V_F$.

Vice versa, the **maximum voltage $V_{(L1)M}$** is defined as the maximum output voltage minus the voltage drop of the diode.

4 Select the Rectifier Diode

For selecting the appropriate diode, consider that it needs to withstand the following stress parameters:

1. Average current: $I_{F(AV)} = I_{OM}$
2. Maximum peak current: $I_{FRM} = I_{(SW)M}$
3. Maximum DC reverse voltage: $V_R = V_O - V_{I(min)}$
4. Power dissipation: $P_D = I_{OM} \times V_F$

Generally, TI recommends using Schottky diodes for inductive low- to middle-power DC/DC converters. This is due to the low forward voltage drop which leads to higher efficiency.

5 Select the Capacitors

In the inverting buck-boost topology, the input and the output currents are pulsed. The choice of the input and output capacitances is therefore crucial to ensure stable performance. When choosing capacitors, take into account that the capacitance of ceramic capacitors decreases with its applied voltage, also called the DC Bias Effect.

5.1 Input Capacitors

The input capacitance is required to hold up the input voltage during the time when the energy is decreasing in the inductor ((1 – D) / $f_{(SW)}$). If the input voltage drop shall not be bigger than $V_{I(PP)}$, the minimum effective value for this capacitor $C_{I(min)}$can be estimated with:

$$C_{I(min)} = \frac{I_{(L1)(AVG)} \times D}{f_{(SW)} \times [V_{I(PP)} - (I_{(L1)(PP)} \times ESR_{CI})]} \quad (10)$$

Be aware that most converters already provide the minimum input capacitance requirements in the data sheet.

Equation 10 implies that higher equivalent series resistance of the capacitor (ESR) increases the input voltage drop. TI recommends using low ESR capacitors (< 10 mΩ), also referenced in Section 5.2.

Copyright © 2017, Texas Instruments Incorporated

5.2 Output Capacitors

Since the output current is discontinuous as well, the output capacitor is required to supply the energy to the load during the time when energy is increasing in the inductor (D / $f_{(SW)}$). If the converter is internally compensated, use the recommended values of inductance and output capacitors in the data sheet.

Estimate the **output voltage ripple $V_{O(PP)}$** with the following equation:

$$V_{O(PP)} = \frac{I_O D}{f_{(SW)} C_O} + \left(\frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{CO} \tag{11}$$

If the converter is externally compensated, estimate the **minimum required capacitance $C_{O(min)}$** at an output voltage ripple requirement of $V_{O(PP)}$, given by:

$$C_{O(min)} = \frac{I_O \times D}{f_{(SW)} \times \left[V_{O(PP)} - \left(\frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{CO} \right]} \tag{12}$$

This formula implies that higher equivalent series resistance of the capacitor (ESR) increases the output voltage drop. TI recommends using low ESR capacitors (< 10 mΩ), also refer to the following NOTE.

NOTE: In general, TI recommends using ceramic capacitors due to their low ESR (< 10 mΩ).

However, ceramic capacitors have some disadvantages that must be considered thoroughly. The following list emphasizes these disadvantages, for detailed information refer to Murata:

- Capacitance decreases with increased voltage (DC bias effect)
- Capacitance decreases with decreased voltage rating
- Capacitance decreases with decreased package size
- Capacitance decreases with increased temperature

5.3 Note About Discontinuous Conduction Mode (DCM)

In the presented inverting buck-boost power stage, the converter could enter DCM operation due to the rectification diode D1 that only allows current to flow in one direction. If the load is so small that the inductor ripple current reaches zero, the switching node voltage becomes negative and the diode is in reverse direction. At this point for a certain time of the switching cycle, the converter will not provide current to the output which leads to different calculations and considerations.

This application note does not intend to provide the procedure to design a DCM converter.

However, be aware that such topology can enter DCM when the load is sufficiently small. The critical conduction current means the point when the converter enters DCM. This can be calculated by:

$$I_{O\,(DCM)} \leq \frac{I_{(L1)\,(PP)} \times (1-D)}{2} \tag{13}$$

or

$$I_{O\,(DCM)} \leq \frac{V_I^2 \times (V_F - V_O)}{(2 \times f_{SW} \times L1) \times (V_I + V_F - V_O)^2} \tag{14}$$

Copyright © 2017, Texas Instruments Incorporated

6 Summary of all Equations and an Application Example

The following chapter makes an exemplary calculation of the discussed formulas. The TPS65131 device is chosen for the consideration of the switch.

In the following tables all necessary parameters are shown as described in Table 1 and Table 2 will summarize all equations and exemplary calculations.

Table 2. Application Example - Parameters With TPS65131

Description	Parameter
Input voltage range	$V_{I(min)}$ = 2.7 V to V_{IM} = 5.5 V; V_I = 3.3 V
Output voltage	V_O = –10 V
Maximum average output current	I_{OM} = 100 mA
Forward voltage drop of the rectifier diode	V_F = 0.5 V
Allowed inductor current ripple	Use recommended inductance value L1 = 4.7 µH
Input voltage ripple	$V_{I(PP)}$ = 5% of V_{IM} = 275 mV
Output voltage ripple	$V_{O(PP)}$ = 0.1% of V_O = 10 mV
Equivalent Series Resistor (ESR)	ESR_{CI} = ESR_{CO} = 5 mΩ
Minimum switching current limit of internal switch S1 (datasheet)	$I_{(SW)(min)(lim)}$ = 1.8 A
Switching frequency of the internal switch S1 (datasheet)	$f_{(SW)}$ = 1.25 MHz

Table 3. Inverting Buck-Boost Calculations

Parameter Description [#]	Formula	Example with TPS65131
Maximum Duty Cycle	$D = \frac{-V_O + V_F}{-V_O + V_F + V_{I(min)}}$	$D = \frac{-(-10\ V) + 0.5\ V}{-(-10\ V) + 0.5\ V + 2.7\ V} = 0.795$
DC Conversion Ratio	$\frac{V_O}{V_I} = \frac{-D}{1-D}$	$\frac{V_O}{V_I} = \frac{-0.795}{1-0.795} = -3.878$
Maximum Peak Switch Current	$I_{(SW)M} = (I_{OM} \times \frac{V_{I(min)} + V_F - V_O}{V_{I(min)}}) + (\frac{I_{(L1)(PP)}}{2})$	$I_{(SW)M} = (0.1\ A \times \frac{2.7\ V + 0.5\ V - (-10\ V)}{2.7\ V}) + (\frac{365\ mA}{2}) = 671\ mA$
Maximum Output Current	$I_{OM} = (I_{(SW)(min)(lim)} + \frac{I_{(L1)(PP)}}{2})(\frac{V_{I(min)}}{V_{I(min)} + V_F - V_O})$	$I_{OM} = (1.8\ A + \frac{365\ mA}{2}) \times (\frac{2.7\ V}{2.7\ V + 0.5\ V - (-10\ V)}) = 405\ mA$
Maximum Peak Switch Voltage	$V_{(SW)M} = V_{IM} + V_F - V_O$	$V_{(SW)M}$ = 5.5 V + 0.5 V – (–10 V) = 16 V
Inductance	$L1 = \frac{V_I\ D}{I_{(L1)(PP)}\ f_{(SW)}}$	Data sheet Recommendation: L1 = 4.7 µH
Average Inductor Current	$I_{(L1)(AV)} = \frac{I_O}{1-D}$	$I_{(L1)(AV)} = \frac{0.1\ A}{1-0.795} = 0.488\ A$
Maximum Inductor Current	$I_{(L1)M} = I_{(SW)M} = I_{(L1)(AVG)} + \frac{I_{(L1)(PP)}}{2}$	$I_{(L1)M} = 488\ mA + \frac{365\ mA}{2} = 671\ mA$
Inductor Current Ripple	$I_{(L1)(PP)} = \frac{V_{I(min)}\ D}{f_{(SW)}\ L1}$	$I_{(L1)(PP)} = \frac{(2.7\ V) \times (0.795)}{1.25\ MHz \times 4.7\ \mu H} = 365\ mA$
Inductor Saturation Current	$I_{(L1)(sat)} > 1.2 \times I_{(SW)M}$	$I_{(L1)(sat)} > 805\ mA$
Diode Forward Current	$I_{F(AVG)} = I_{OM}$	$I_{F(AVG)}$ = 100 mA
Maximum Diode Peak Current	$I_{FRM} = I_{(SW)M}$	I_{FRM} = 671 mA

Copyright © 2017, Texas Instruments Incorporated

Table 3. Inverting Buck-Boost Calculations (continued)

Parameter Description [#]	Formula	Example with TPS65131
Maximum Diode DC Reverse Voltage	$V_{RM} = V_O - V_{IM}$	$V_{RM} = -15.5\ V$
Minimum Input Capacitance	$C_{I(min)} = \frac{I_{(L1)(AVG)} \times D}{f_{(SW)} \times [V_{I(PP)} - (I_{(L1)(PP)} \times ESR_{CI})]}$	$C_{I(min)} = \frac{(488\ mA) \times (0.795)}{1.25\ MHz \times [(0.05) \times (2.7\ V) - (365\ mA) \times (8\ m\Omega)]} = 2.3\ \mu F$
Minimum Output Capacitance	$C_{O(min)} = \frac{I_O \times D}{f_{(SW)} \times \left[V_{O(PP)} - \left(\frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{CO} \right]}$	$C_{O(min)} = \frac{(100\ mA) \times (0.795)}{1.25\ MHz \times [0.001 \times (-10\ V) - \frac{100\ mA}{1 - 0.795} + (\frac{365\ mA}{2} \times 5\ m\Omega)]} = 9.6\ \mu F$
Output Voltage Ripple	$V_{O(PP)} = \frac{I_O D}{f_{(SW)} C_O} + \left(\frac{I_O}{1-D} + \frac{I_{(L1)(PP)}}{2} \right) \times ESR_{CO}$	Requirement $V_{O(PP)} = 10\ mV$
Critical Conduction Current	$I_{O\,(DCM)} \le \frac{V_I^2 \times (V_F - V_O)}{(2 \times f_{SW} \times L1) \times (V_I + V_F - V_O)^2}$	$I_{O(DCM)} \le \frac{2.7\ V^2 \times (0.5\ V - (-10\ V))}{(2 \times 1.25\ MHz \times 4.7\ \mu H) \times (2.7\ V + 0.5\ V - (-10\ V))^2} = 37.4\ mA$

Copyright © 2017, Texas Instruments Incorporated

The presented calculations can be verified graphically with the Power Stage Designer Tool. The following cutouts of this tool will show the results of the given example from Table 2.

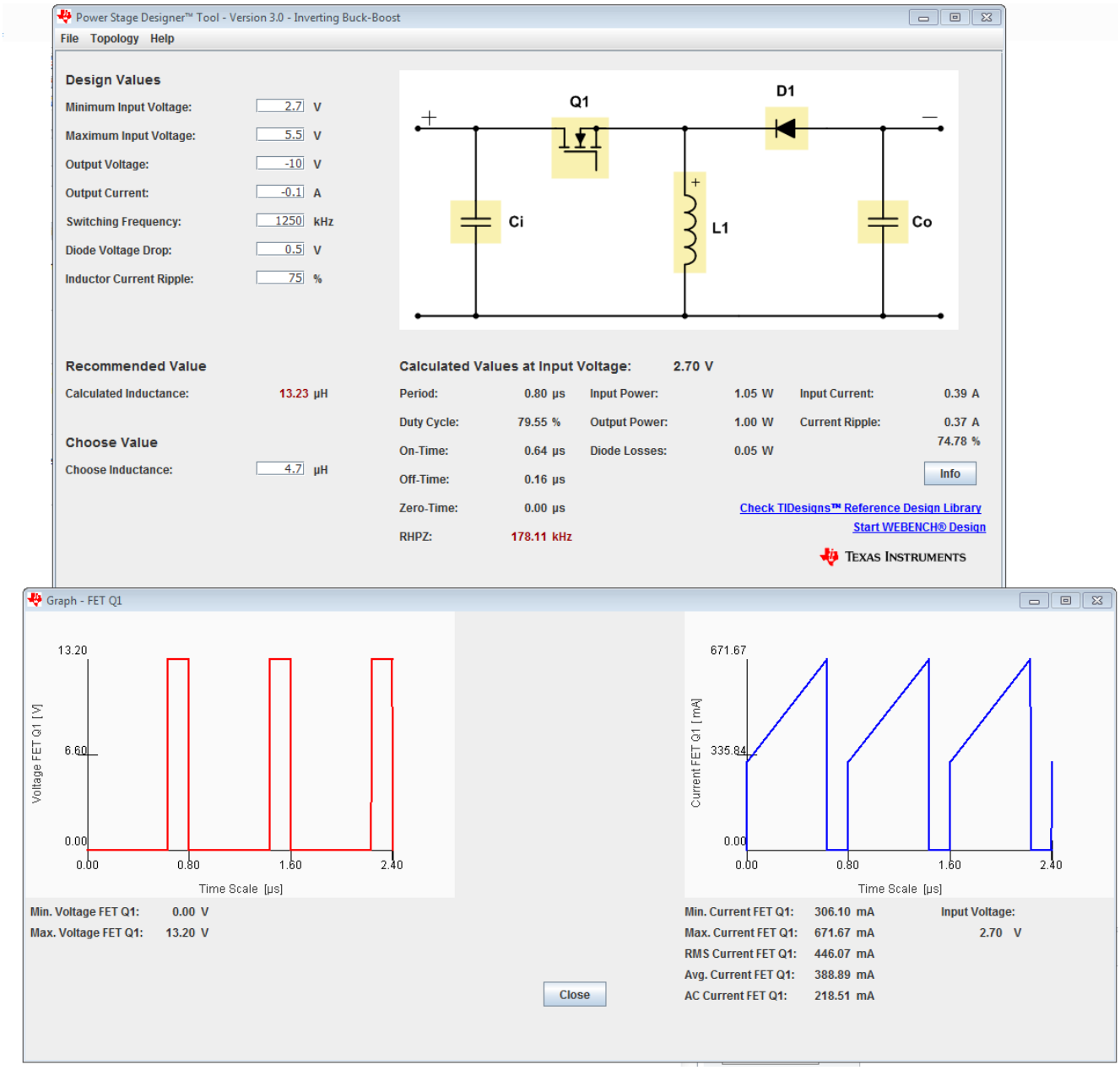

Figure 3. Screenshot of Power Stage Designer Tool (Version 3.0)

Copyright © 2017, Texas Instruments Incorporated

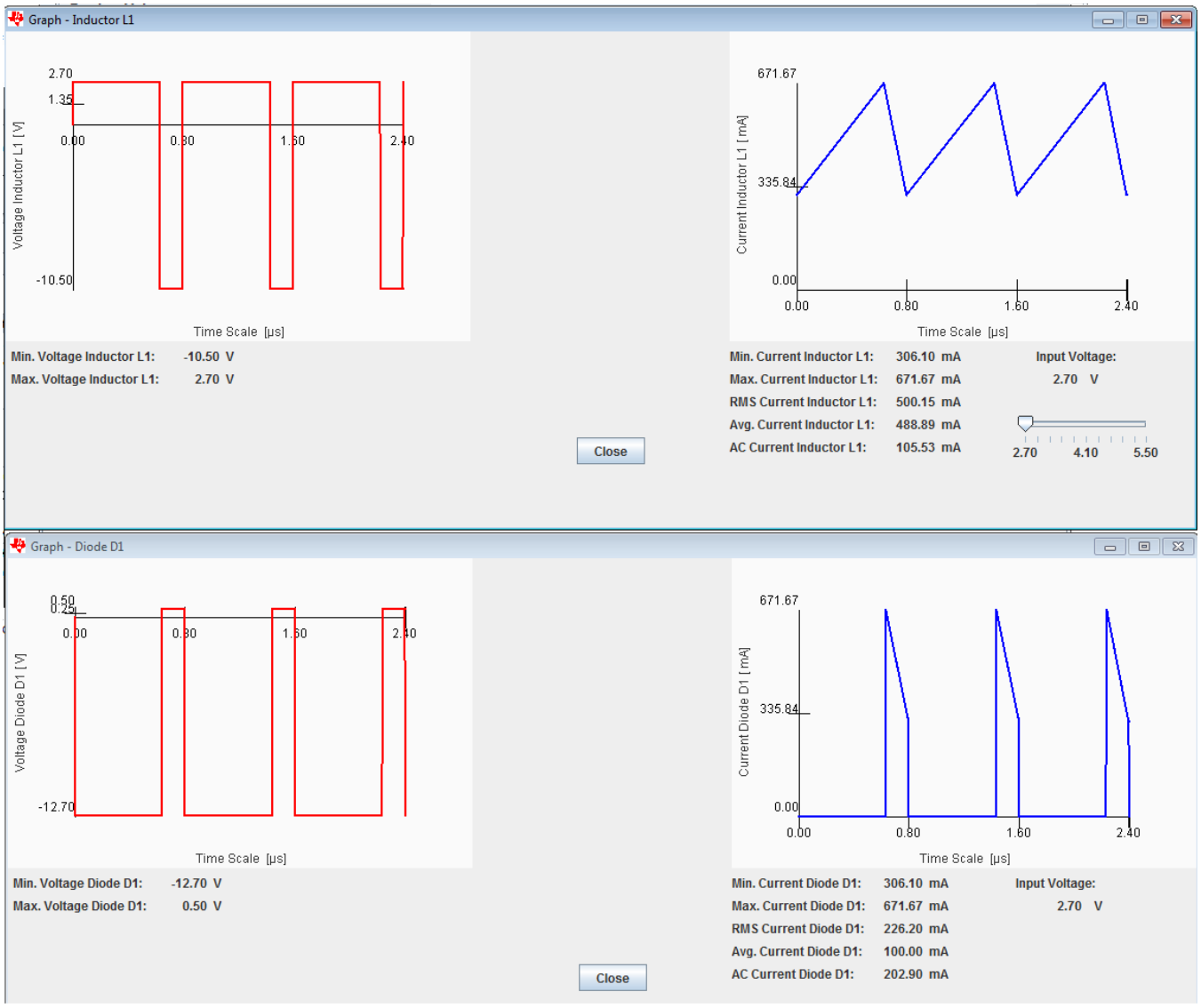

Figure 4. Screenshot of Power Stage Designer Tool (Version 3.0)

Copyright © 2017, Texas Instruments Incorporated

7 References

1. *Power Topologies Handbook* (Markus Zehendner, Matthias Ullmann), (SLYU036)
2. Power Stage Designer Tool – Version 3.0
3. *TPS6513x Positive and Negative Output DC-DC Converter* data sheet (SLVS493)
4. Writing Guidelines according to JESD99C
5. Basic Calculation of a Boost Converter's Power Stage (SLVA372)
6. Basic Calculation of a Buck Converter's Power Stage (SLVA477)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2017) to A Revision	Page
• Corrections made to equations 11 and 12.	5
• Corrections made to the *Minimum Output Capacitance* and *Output Voltage Ripple* formulas in the *Inverting Buck-Boost Calculations* table.	7

Copyright © 2017, Texas Instruments Incorporated

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated