

# Instability Analysis and Oscillation Suppression of Enhancement-Mode GaN Devices in Half-Bridge Circuits

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**Abstract**—This paper analyzes the problem of instability in enhancement-mode gallium nitride (GaN) transistors based half-bridge circuits. The instability may cause sustained oscillation, resulting in overvoltage, excessive electromagnetic interference (EMI), and even device breakdown. GaN devices operate in the saturation region when they conduct reversely during the dead time. Under the influence of parasitic parameters, the GaN-based half-bridge circuit exhibits positive feedback under certain conditions, thus, resulting in sustained oscillation. A small-signal model is proposed to study this positive feedback phenomenon. Like the second-order under-damped system, damping ratio is defined to determine the system's stability. Based on the model, the influence of circuit parameters on instability is investigated and guidelines to suppress the oscillation are given. Reducing the common-source inductance, increasing the gate resistance of the inactive switch or connecting a diode in parallel to the inactive switch are some effective ways to suppress the oscillation. Finally, the analyses are verified by both simulation and experiment.

**Index Terms**—Gallium nitride (GaN), parasitic, positive feedback, reverse conduction, sustained oscillation.

## I. INTRODUCTION

IN RECENT years, gallium nitride (GaN) transistors are gaining increased attention in high efficiency and high power density converters [1], [2]. Compared with silicon devices, GaN devices have a smaller figure of merit [3], and thus, are capable of working at a higher switching frequency while maintaining high efficiency. As the switching frequency increases, the power density of the converter can be increased due to the reduction in the size of the passive components [4]–[10]. However, higher

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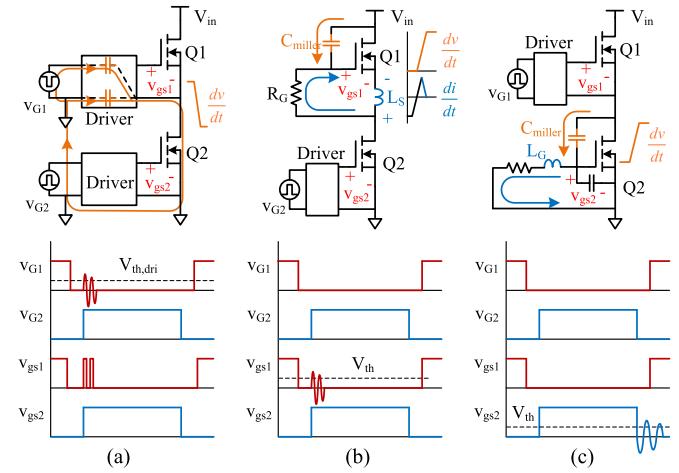


Fig. 1. Equivalent circuit and typical waveforms of the common instability problems.  $V_{G1}$  and  $V_{G2}$  are the PWM signals;  $V_{gs1}$  and  $V_{gs2}$  are the gate-source voltages. (a) PWM signal noise, related to high  $dv/dt$  and parasitic capacitance between power circuit and signal circuit. (b) Turn-on gate oscillation, related to high  $dv/dt$ , high  $di/dt$ , miller capacitance and common-source inductance. (c) Turn-off gate oscillation, related to high  $dv/dt$  and large gate inductance.

switching speed can lead to more serious overvoltage and parasitic ringing, and lower on-resistance and capacitances can result in a smaller damping ratio. This can lead to more severe instability problems for GaN-based power circuits [11]–[14].

Research work has been conducted to study the instability problem. Fig. 1 shows the three common problems of instability. One of the problems is the pulse width modulation (PWM) signal distortion caused by high  $dv/dt$  [11], [15]. High  $dv/dt$  can distort the PWM signal through the parasitic capacitance between signal circuit and power circuit. The distorted PWM signal may trigger the switch to falsely turn ON or turn OFF. The second common problem is the turn-on gate oscillation induced by high  $dv/dt$  and high  $di/dt$  [12], [16]–[18]. In a half-bridge circuit, when the active switch turns ON, the drain-source voltage of inactive device increases sharply. The displacement current flows through the miller capacitance of the inactive switch to its gate node, which may cause the gate-source voltage to exceed the threshold voltage. Meanwhile, a voltage is generated across the common-source inductance under the effect of  $di/dt$ . The voltage worsens the gate-source voltage of the inactive switch through the driver loop. In worse cases, this problem could lead

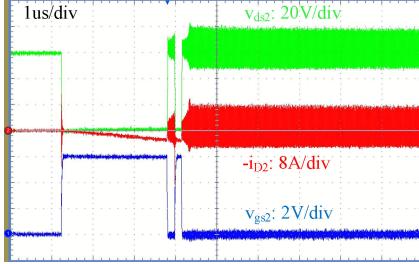


Fig. 2. Measured sustained oscillation waveforms in the GaN-based half-bridge circuit.

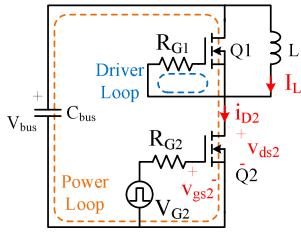


Fig. 3. Half-bridge circuit with inductive load. Q1 is the inactive device and Q2 is the active device.

to sustained oscillation. The third problem of the instability is turn-off gate oscillation caused by the large gate inductance and high  $dv/dt$ . During the active switch turn-off process, the current through miller capacitance caused by high  $dv/dt$  must be sunk through the gate inductance, and thus, energy is stored in gate inductance. Then under the effect of gate inductance and input capacitance, the gate voltage of active switch rings back and may exceed the threshold voltage, thus, resulting in false turn-on and even sustained oscillations. The papers [13], [19] established a model using negative resistance theory and successfully explained the instability of a SiC-based circuit. Another problem is observed in cascode GaN devices under high-current turn-off condition [14]. The cascode GaN device is normally off by using a low-voltage Si MOSFET connected in series with a depletion-mode GaN device. The capacitance mismatch between GaN device and Si MOSFET may result in the oscillation. Adding a proper capacitor in parallel with Si MOSFET can solve the problem.

Besides the above problems, there is another problem observed in enhancement-mode GaN devices based half-bridge circuit. Fig. 2 shows the measured waveforms and Fig. 3 is the GaN-based half-bridge circuit. The oscillation occurs when the active switch is OFF and the inactive switch conducts reversely. Note that the gate-source voltage of the active device is normal. The oscillations are related to the unique reverse conduction characteristics of the GaN devices, which does not occur in silicon or silicon carbide MOSFETs based circuit because of their different reverse conduction characteristics from GaN devices.

This paper presents a theoretical treatment of the sustained oscillation problem in enhancement-mode GaN devices based half-bridge circuits. The GaN devices work in the saturation region due to their unique reverse conduction characteristics when conducting reversely during dead time. And a feedback

TABLE I  
LIST OF SYMBOLS

Symbol	Description
$g_m$	Reverse transconductance
$R_{\text{loop}}$	High-frequency power loop resistance
$R_{G\text{int}}$	Internal gate resistance of Q1
$R_{G1}$	External added gate resistance of Q1
$R_G$	Total gate resistance, sum of $R_{G\text{int}}$ and $R_{G1}$
$L_S$	Common-source inductance of Q1
$L_G$	Gate inductance of Q1
$L_D$	Drain inductance
$C_{gs}$	Gate-source capacitance of Q1
$C_{ds}$	Drain-source capacitance of Q1
$C_{gd}$	Gate-drain capacitance of Q1
$C_{oss2}$	Output capacitance of Q2
$C_{ext}$	External capacitance paralleled with $C_{oss2}$
$i_{ch}$	Channel current of Q1
$i_{D2}$	Drain current of Q2
$v_{gd}$	Gate-drain voltage of Q1
$v_{ds2}$	Drain-source voltage of Q2
$v_{gs2}$	Gate-source voltage of Q2

system is formed if the parasitic parameters are considered. The feedback may become positive under some conditions, resulting in sustained oscillations. A small-signal model is proposed to describe the feedback system. Then the stability criterion is proposed to determine the stability of the system. Based on the stability criterion, the effect of circuit parameters on the oscillation is investigated and guidelines to suppress the oscillation are presented. Spice simulation is performed to verify the analysis and provides detailed insight into the problem. Finally, a GaN-based half-bridge prototype is built and the experiment results show a good agreement with the analyses.

The paper is organized as follows. Section II proposes a model to describe the problem of instability. Section III investigates the influence of circuit parameters on instability and presents guidelines to suppress the oscillation. Sections IV and V are simulation and experiment verifications. Section VI concludes the paper.

## II. CIRCUIT MODELING AND STABILITY CRITERION

A half-bridge circuit with an inductive load in Fig. 3 is chosen to study the instability problem. The top switch Q1 works as a synchronous device, which is called inactive device. The bottom switch Q2 is an active device driven by double pulse signals. The switching of the active switch causes current commutation with the external circuits, whereas the switching of the inactive switch only causes current commutation within the switch. The inactive switch is also called “synchronous FET.” After Q2 turns off, the inductor current  $I_L$  flows through Q1 from its source to drain. In this case, the sustained oscillation may occur due to the reverse conduction characteristics of GaN devices and parasitic parameters. Table I lists the symbols used in this paper.

### A. Reverse Conduction Characteristics of GaN Devices

The reverse conduction characteristics of GaN devices are quite different from that of Si or SiC MOSFETs. Si or SiC MOSFETs have body diodes to conduct the reverse current. As for

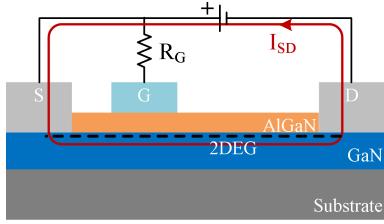


Fig. 4. Simplified structure of GaN devices when conducting reverse current. 2DEG in the channel starts to conduct when  $V_{gd} > V_{gd,\text{th}}$ .

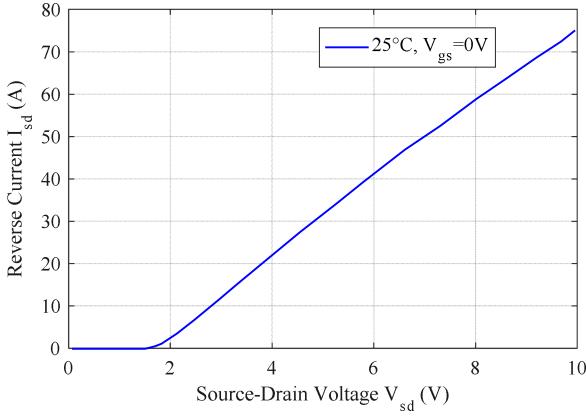


Fig. 5. Reverse conduction characteristics of a 650-V GaN device [21].

GaN devices, there is no body diode existing in them. When the gate-source voltage  $V_{gs}$  or gate-drain voltage  $V_{gd}$  is greater than the threshold voltage, the electrons are attracted to the aluminum gallium nitride (AlGaN) and GaN heterostructure interface so that the two-dimensional electron gas (2DEG) is re-established, and thus, the GaN devices can conduct current [3], [20]. The conditions that GaN devices can conduct current are

$$V_{gd} > V_{gd,\text{th}} \text{ or } V_{gs} > V_{gs,\text{th}} \quad (1)$$

where  $V_{gd,\text{th}}$  is gate-drain threshold voltage and  $V_{gs,\text{th}}$  is gate-source threshold voltage.

Fig. 4 shows a simplified structure of GaN devices when conducting reversely. The gate-source voltage  $V_{gs}$  equals 0 V because the gate leakage current is negligible. In other words,  $V_{gd} = V_{sd}$ . After Q2 turns off, inductor current charges the output capacitance of Q1 reversely, resulting in the increase of  $V_{sd}$ . Q1 starts to conduct until  $V_{sd}$  exceeds the threshold voltage  $V_{gd,\text{th}}$ . Q1 works in saturation region because

$$V_{sd} > V_{gd} - V_{gd,\text{th}}. \quad (2)$$

The channel current  $I_{ch}$  is now controlled primarily by the gate-drain voltage  $V_{gd}$ .

Fig. 5 shows the reverse conduction characteristics of a 650-V GaN device. The curve is measured at steady state, so the current  $I_{sd}$  equals the channel current  $I_{ch}$ . Meanwhile,  $V_{gd}$  equals  $V_{sd}$  when  $V_{gs}$  is 0 V. Therefore, the  $I_{sd}$ - $V_{sd}$  curve is also the  $I_{ch}$ - $V_{gd}$

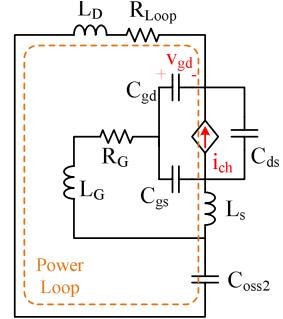


Fig. 6. Small-signal circuit of the half-bridge circuit.

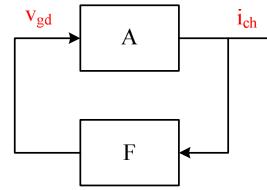


Fig. 7. Block diagram of the feedback system.

curve and the following relationship can be obtained:

$$I_{ch} = f(V_{gd}). \quad (3)$$

Equation (3) shows that the GaN device's channel can be equivalent to a voltage-controlled current source.

### B. Small-Signal Model

Because the transconductance and capacitance of switching device are nonlinear, it is difficult to directly establish a model to determine the stability of the circuits. With the linearized small-signal model, the stability theory of linear system can be used. The small-signal circuit in Fig. 6 is derived from the circuit in Fig. 3. The bus capacitor  $C_{bus}$  is shorted and the inductor  $L$  is opened. Q2 is replaced by its output capacitance  $C_{oss2}$  because it has been turned off. Q1 is replaced by a voltage-controlled current source combining with three capacitors. Gate resistance  $R_G$  consists of Q1's inner gate resistance  $R_{Gint}$  and external gate resistance  $R_{G1}$ . The common-source inductance  $L_S$  is the inductance shared by the driver loop and the power loop. The gate inductance  $L_G$  is defined as the driver loop inductance minus the common-source inductance. The drain inductance  $L_D$  is defined as the power loop inductance minus the common-source inductance.  $R_{loop}$  is the high-frequency power loop resistance.

The small-signal circuit can be described by a feedback system. Fig. 7 shows the block diagram of the feedback system. A is the amplified gain. F is the feedback transfer function.

According to (3), A is derived as

$$A(s) = \frac{i_{ch}(s)}{v_{gd}(s)} = g_m \quad (4)$$

where  $i_{ch}$  is a small change of the channel current,  $v_{gd}$  is a small change of gate-drain voltage, and  $g_m$  is the transconductance.

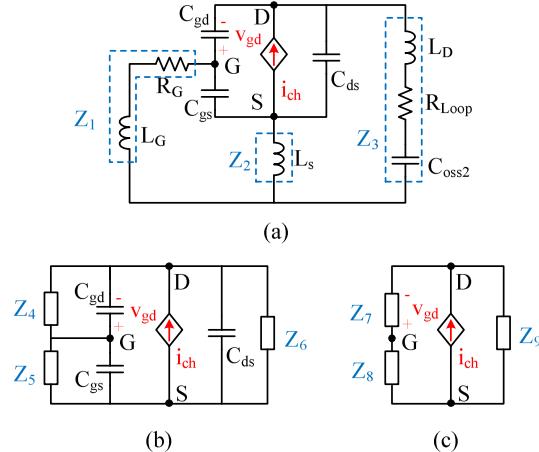


Fig. 8. Circuit simplification processes for deriving the feedback transfer function  $F$ .

Next is to derive the feedback transfer function  $F$ . Fig. 6 is redrawn as shown in Fig. 8(a). The impedances  $Z_1$ ,  $Z_2$ , and  $Z_3$  form a star connection. The star connection can be changed into delta connection by using the following formulas:

$$Z_4 = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}{Z_2} \quad (5)$$

$$Z_5 = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}{Z_3} \quad (6)$$

$$Z_6 = \frac{Z_1 Z_2 + Z_2 Z_3 + Z_1 Z_3}{Z_1} \quad (7)$$

where  $Z_1 = R_G + sL_G$ ,  $Z_2 = sL_S$ , and  $Z_3 = R_{\text{loop}} + sL_D + 1/sC_{\text{oss}2}$ . The circuit is further simplified in Fig. 8(c), where  $Z_7 = Z_4/(1/sC_{\text{gd}})$ ,  $Z_8 = Z_5/(1/sC_{\text{gs}})$ , and  $Z_9 = Z_6/(1/sC_{\text{ds}})$ . Then we could obtain the feedback transfer function

$$F(s) = \frac{v_{\text{gd}}(s)}{i_{\text{ch}}(s)} = -\frac{Z_7 Z_9}{Z_7 + Z_8 + Z_9}. \quad (8)$$

Then, the loop gain  $G$  is expressed as

$$\begin{aligned} G(s) &= A(s) \cdot F(s) \\ &= -\frac{g_m}{s} \frac{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \end{aligned} \quad (9)$$

where  $b_i$  and  $a_i$  ( $i = 0, 1, 2, 3, 4$ ) are coefficients listed in the appendix. It should be noted that this is a fifth-order system. There are seven dynamic elements, a loop formed by  $C_{\text{gd}}$ ,  $C_{\text{gs}}$ , and  $C_{\text{ds}}$ , and a cut set formed by  $L_S$ ,  $L_G$ , and  $L_D$ . The order of the system is the number that the dynamic elements minus the number of loops formed by capacitors and the number of cut sets formed by inductors.

The well-known Barkhausen stability criterion states that for any feedback system to attain stable oscillation, the loop gain is equal to unity [22]

$$G(j\omega_0) = 1 \quad (10)$$

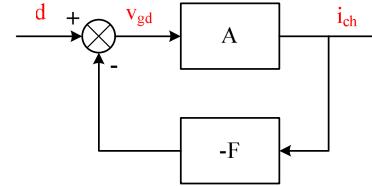


Fig. 9. Modified block diagram of the feedback system.  $d$  is the disturbance.

TABLE II  
CIRCUIT PARAMETERS

Symbol	Value	Symbol	Value
$g_m$	10 S	$L_D$	7 nH
$R_{\text{loop}}$	0.22 $\Omega$	$C_{\text{gs}}$	240 pF
$R_G$	1.3 $\Omega$	$C_{\text{ds}}$	440 pF
$L_S$	0.2 nH	$C_{\text{gd}}$	60 pF
$L_G$	5.2 nH	$C_{\text{oss}2}$	65–500 pF

where  $\omega_0$  is oscillation frequency. However, little information about the stability can be acquired from (10). In order to have a deeper insight into the system, the block diagram is modified by adding a disturbance signal  $d$ , as shown in Fig. 9.

According to Fig. 9, the closed-loop transfer function  $T(s)$  is derived as

$$T(s) = \frac{i_{\text{ch}}(s)}{d(s)} = \frac{A(s)}{1 - G(s)}. \quad (11)$$

Submitting (4) and (9) into (11), it yields

$$T(s) = \frac{g_m s (b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0)}{c_5 s^5 + c_4 s^4 + c_3 s^3 + c_2 s^2 + c_1 s + c_0}. \quad (12)$$

The poles of  $T(s)$  determine the stability of the system. The system is unstable if the real part of any pole is positive. All poles can be solved easily with the help of mathematical tools if the circuit parameters are known.

The circuit parameters are obtained based on the experimental prototype. Parasitic inductance is extracted through Ansys Q3D extractor software according to the printed circuit board (PCB) layout. The transconductance and capacitances are taken from the device's datasheet. Their values are chosen at the dc operating point, which is determined by inductor current and bus voltage. The dc operating point selected for linearization is when Q2 has turned off and Q1 is reversely conducting. At this operating condition,  $C_{\text{oss}2}$  is the value when Q2 is biased at the bus voltage and  $g_m$  is the slope of the  $I_{\text{sd}}-V_{\text{sd}}$  curve where the current equals the inductor current. The capacitance  $C_{\text{oss}2}$  varies from 500 to 65 pF when the bus voltage increases from 0 to 500 V. Table II lists the circuit parameters.

### C. Stability Criterion

With the purpose of illustrating the stability of the system, the pole-zero map of  $T(s)$  is plotted in Fig. 10(a). There are five poles, a real pole  $p_3$  and two pairs of complex conjugate poles  $p_1$  and  $p_2$ . The real pole  $p_3$  is negative and located far from the imaginary axis, therefore, has no effect on the instability of the system. Fig. 10(b) is the enlarged view and it shows that  $p_1$  is

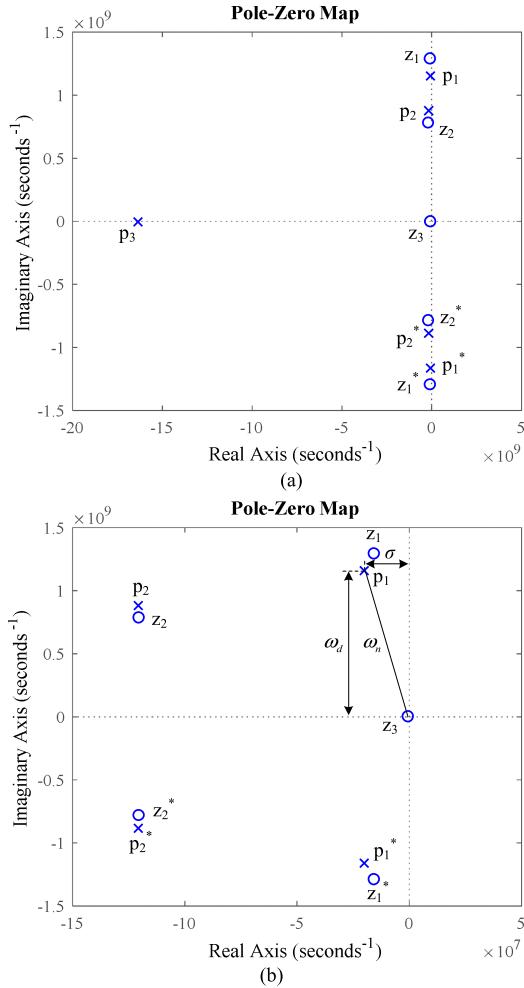


Fig. 10. (a) Pole-zero map of closed-loop transfer function  $T(s)$ . (b) Enlarged pole-zero map. ( $L_D = 7 \text{ nH}$ ;  $C_{oss2} = 100 \text{ pF}$ ;  $R_{loop} = 0.22 \Omega$ ;  $R_G = 1.3 \Omega$ ;  $L_G = 5.2 \text{ nH}$ ;  $C_{gs} = 240 \text{ pF}$ ;  $L_S = 0.2 \text{ nH}$ ;  $C_{ds} = 440 \text{ pF}$ ;  $g_m = 10 \text{ S}$ ;  $C_{gd} = 60 \text{ pF}$ ).

much closer to the imaginary axis than  $p_2$ . Therefore,  $p_1$  is the dominant pole and determines the system's stability.

The complex pole  $p_1$  can be defined in terms of their real and imaginary parts

$$p_1 = -\sigma + j\omega_d. \quad (13)$$

Similar to the second-order system, the damping ratio is defined as [23]

$$\zeta = \frac{\sigma}{|p_1|} = \frac{\sigma}{\sqrt{\sigma^2 + \omega_d^2}} = \frac{\sigma}{\omega_n}. \quad (14)$$

The damping ratio  $\zeta$  can be used to reflect the stability of the system. When  $\zeta = 0$ , the amplitude of the oscillation remains constant over time and the oscillation frequency is  $\omega_d$ . When  $\zeta > 0$ , the pole has a negative real part so the system is stable. The greater the damping ratio  $\zeta$  is, the faster the oscillation damps. When  $\zeta < 0$ , the pole has a positive real part so the system is unstable and the oscillation amplitude increases with time. Note that the oscillation will eventually turn into a steady state because of the nonlinearity of the switching devices. Fig. 2

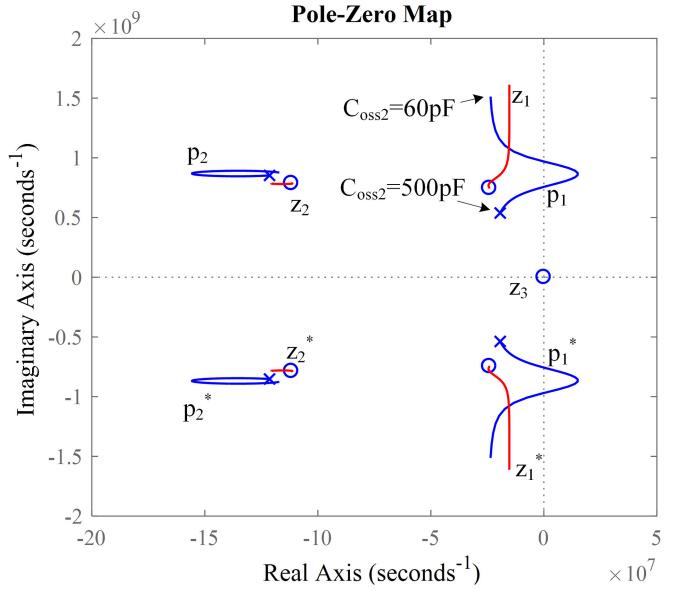


Fig. 11. Pole-zero locus of  $T(s)$  when  $C_{oss2}$  changes from 60 to 500 pF.

clearly shows the process that the oscillation changes from an increased state to a steady state.

Because  $p_1$  is very close to the imaginary axis, the oscillation frequency can be approximately calculated

$$f \approx \frac{\omega_d}{2\pi}. \quad (15)$$

Fig. 11 shows the pole-zero locus of  $T(s)$  when  $C_{oss2}$  changes from 60 to 500 pF. It is reasonable to use  $p_1$  as the dominant pole because  $p_1$  is always much closer to the imaginary axis than  $p_2$ . Fig. 11 also shows that  $p_1$  enters the right half plane when  $C_{oss2}$  is in a certain range. Because  $C_{oss2}$  is nonlinear and decreases as the drain-source voltage increases, the system is unstable in a certain range of bus voltage.

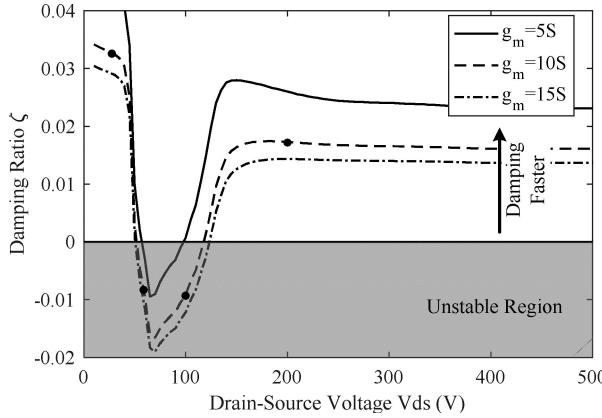
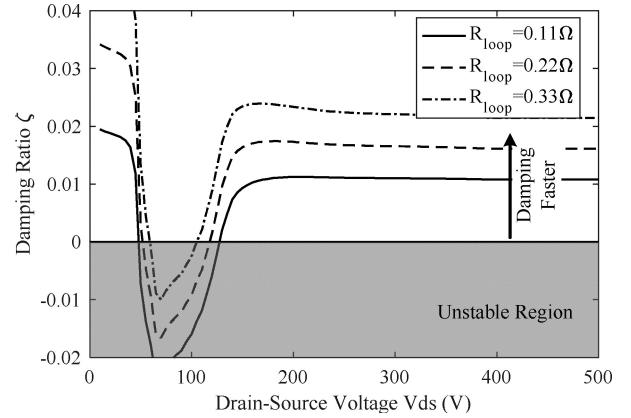
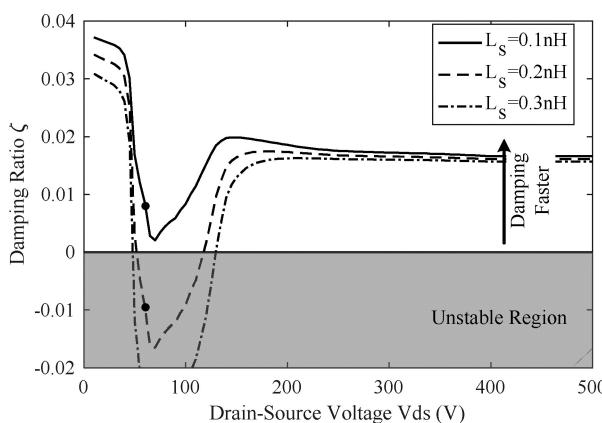
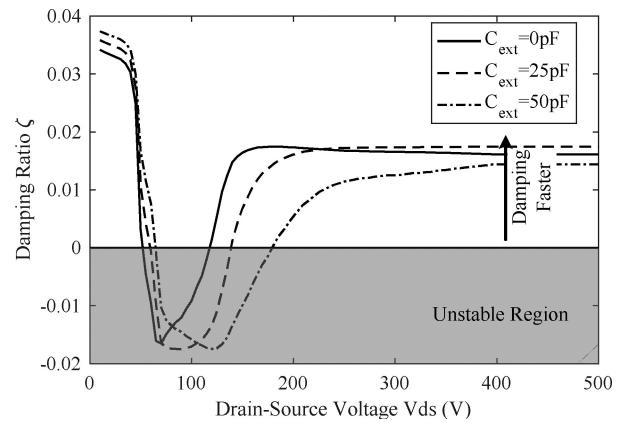
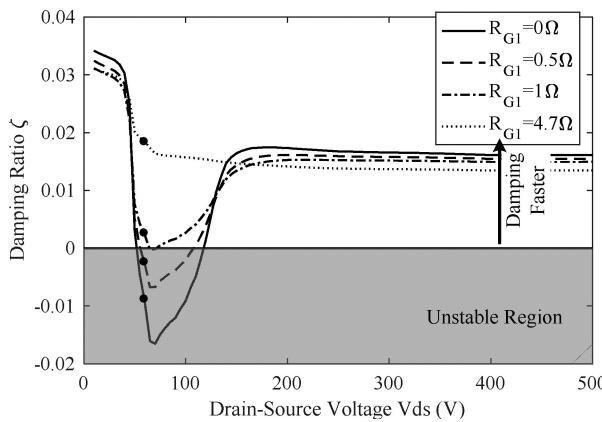
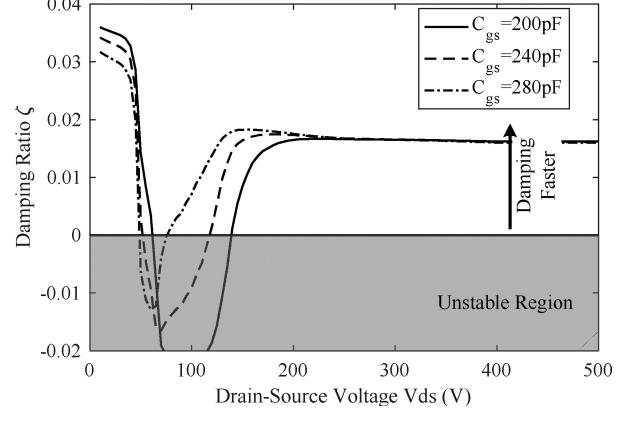
### III. INFLUENCE OF CIRCUIT PARAMETERS ON INSTABILITY

The oscillations can cause many problems: overvoltage, excessive electromagnetic interference (EMI), or even device breakdown. To avoid the sustained oscillation and suppress the oscillation rapidly, the influence of the parameters on the instability is studied and the guidelines are developed.

#### A. Influence of Circuit Parameters on Instability

Figs. 12–21 illustrate the damping ratio variation by sweeping different circuit parameters to investigate their influence on stability. The plotting procedures of each curve are as follows. First, the bus voltage is divided into a number of discrete values from 10 to 500 V and the value of  $C_{oss2}$  corresponding to each bus voltage is obtained according to the  $C_{oss}$ – $V_{ds}$  curve. Then, the poles are solved after substituting  $C_{oss2}$  and other parameter values into (12). Finally, the damping ratios at the corresponding bus voltage are obtained by using (14). The circuit parameters are listed in Table II.

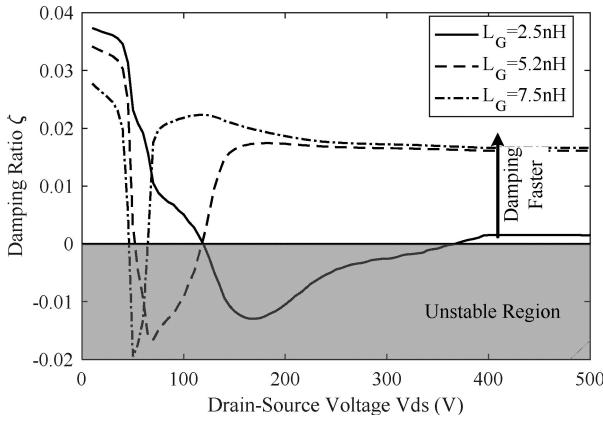
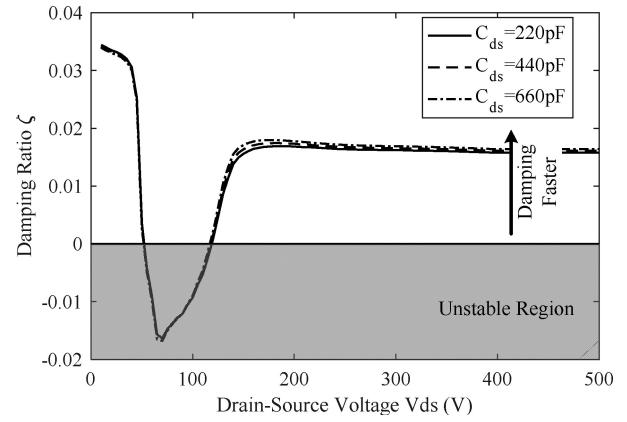
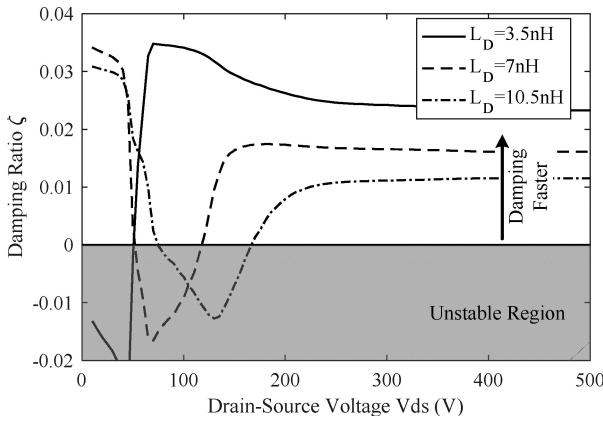
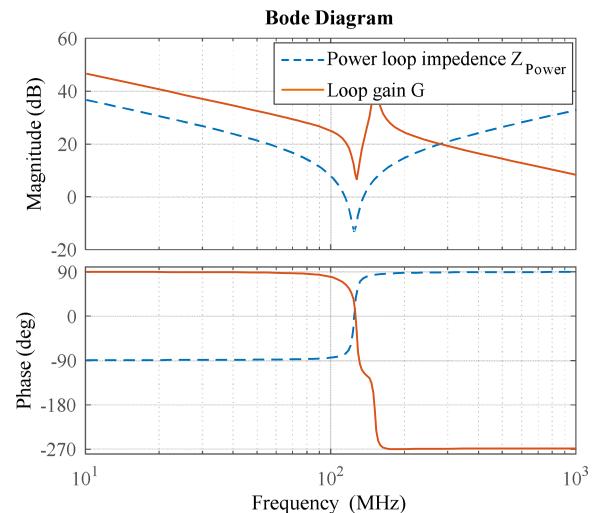
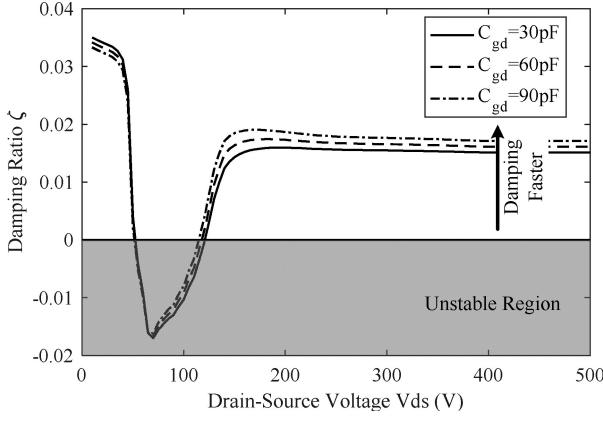
The damping ratio changes significantly when the bus voltage is below 200 V since  $C_{oss2}$  reduces rapidly with the increase

Fig. 12. Damping ratio  $\zeta$  versus transconductance  $g_m$ .Fig. 15. Damping ratio  $\zeta$  versus power loop resistance  $R_{loop}$ .Fig. 13. Damping ratio  $\zeta$  versus common-source inductance  $L_S$ .Fig. 16. Damping ratio  $\zeta$  versus external capacitance  $C_{ext}$  paralleled with  $C_{oss2}$ .Fig. 14. Damping ratio  $\zeta$  versus external gate resistance  $R_{G1}$ .Fig. 17. Damping ratio  $\zeta$  versus gate-source capacitance  $C_{gs}$ .

of the bus voltage. When the bus voltage is above 200 V, the damping ratio is nearly constant because the change of  $C_{oss2}$  is small. According to the figures, it can be concluded that: the damping ratio increases with an increase of  $R_{loop}$ , or increases with a decrease of  $g_m$  and  $L_S$ ; the system tends to be more stable with larger  $R_g$  and  $C_{gs}$ ; the unstable region moves to a lower voltage region with a decrease of  $L_D$  or an increase of

$L_G$ ; an increase in  $C_{oss2}$  enlarges the unstable region;  $C_{gd}$  and  $C_{ds}$  have little influence on the damping ratio.

Further analyses are conducted to gain a better understanding of the instability. Fig. 22 shows the bode diagram of power loop impedance  $Z_{Power}$  (defined as  $R_{loop} + s(L_D + L_S) + 1/sC_{oss2}$ ) and loop gain  $G$ . The oscillation frequency is located where the phase of the loop gain  $G$  is near zero, which is close to the resonant frequency of  $Z_{Power}$ . Since  $Z_{Power}$  is very

Fig. 18. Damping ratio  $\zeta$  versus gate inductance  $L_G$ .Fig. 21. Damping ratio  $\zeta$  versus drain-source capacitance  $C_{ds}$ .Fig. 19. Damping ratio  $\zeta$  versus drain inductance  $L_D$ .Fig. 22. Bode diagram of the power loop impedance  $Z_{\text{Power}}$  and loop gain  $G$ .Fig. 20. Damping ratio  $\zeta$  versus gate-drain capacitance  $C_{gd}$ .

low at the oscillation frequency, most of the oscillation current should flow through the power loop. When the large oscillation current flows through  $L_S$ , a large voltage is generated in  $L_S$ , and then could have a significant impact on  $v_{gd}$  through the driver circuit. The smaller  $L_G$  tends to allow more voltage generated in  $L_S$  to be fed back into  $v_{gd}$ , resulting in worse oscillation. Because  $L_S \ll L_G$ ,  $Z_6 \approx Z_{\text{Power}}$ . As shown in Fig. 8(b),  $C_{ds}$  is connected in parallel with  $Z_6$ . The impedance of  $C_{ds}$  is much

larger than  $Z_6$  at the oscillation frequency, which is satisfied in most cases, so the role of  $C_{ds}$  is negligible.

In addition, the junction temperature of the device also has an effect on the oscillation.  $R_{\text{loop}}$  increases as the junction temperature increases due to the increased on-resistance of the device. Meanwhile,  $g_m$  decreases as junction temperature increases. So the damping ratio increases and the system tends to be more stable at higher junction temperature.

### B. Guidelines to Suppress Oscillation

According to the above analysis, the guidelines to suppress the oscillation are summarized. The first option is to reduce the parasitic parameters such as  $L_D$ ,  $C_{\text{ext}}$ , and especially  $L_S$  by optimizing the layout. Another benefit of reducing  $L_D$ ,  $L_S$ , and  $C_{\text{ext}}$  is that the switching losses are reduced accordingly [24]–[26]. The second method is to increase the gate resistance  $R_G$ . This is the simplest and easiest way. However, larger  $R_G$  increases the risk of false turn-on problem [17]. In addition, paralleling a diode with Q1 is also an effective way. After Q2 turns off, the reverse current is bypassed by the diode and Q1 no

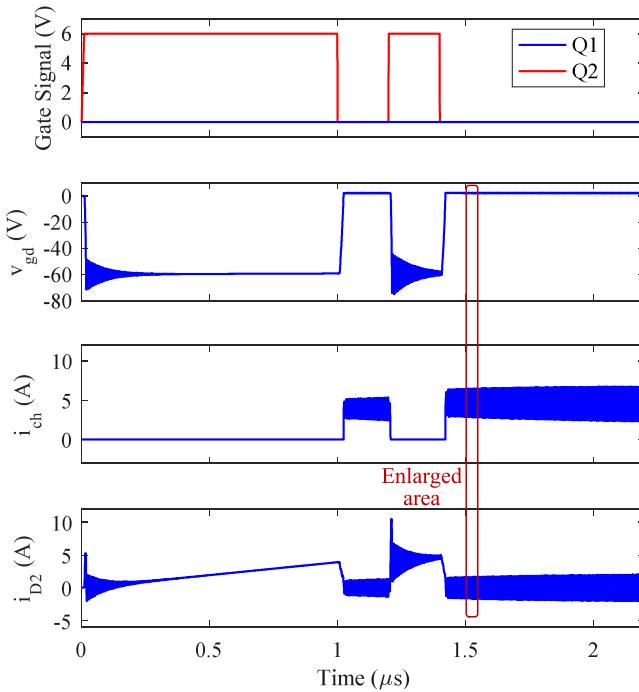


Fig. 23. Simulated waveforms.

longer operates in the saturation region. So the unstable phenomenon does not occur. Another benefit is that the reverse conduction loss can be reduced because the reverse conduction voltage of the diode is smaller than that of the GaN device [27]. The disadvantage is that the switching losses are increased due to the junction capacitance and the reverse recovery charge of the diode.

It is not recommended to improve the stability by increasing  $L_G$  because the large  $L_G$  will cause the gate voltage oscillation. Besides, an external paralleled  $C_{gs}$  may not be effective because of the presence of  $L_S$  and  $R_{Gint}$ . It should be noted that reducing the switching speed of the active device does not help to reduce the risk of sustained oscillation.

#### IV. SIMULATION VERIFICATIONS

Simulation is conducted to verify the analysis using LTspice software. The simulation circuit is a half-bridge circuit and parasitic parameters are taken into account. The GaN device uses a spice model provided by the manufacturer. The device model is modified so that we can observe the channel current and the gate-drain voltage inside the device. The bus voltage is 60 V and the current is about 5 A when Q2 turns off. Other circuit parameters are listed in Table II. Q2 is driven by a double pulse signal. Fig. 23 shows the simulated waveforms. The sustained oscillation is observed after Q2 turns off, which is predicted in Fig. 12.

The waveforms are zoomed in to present more details in Fig. 24. The waveforms of  $v_{gd}$  and  $i_{ch}$  have the same shape and the same phase, which confirms the relationship between  $i_{ch}$  and  $v_{gd}$  expressed in (4) and also indicates that Q1 works in the saturation region.

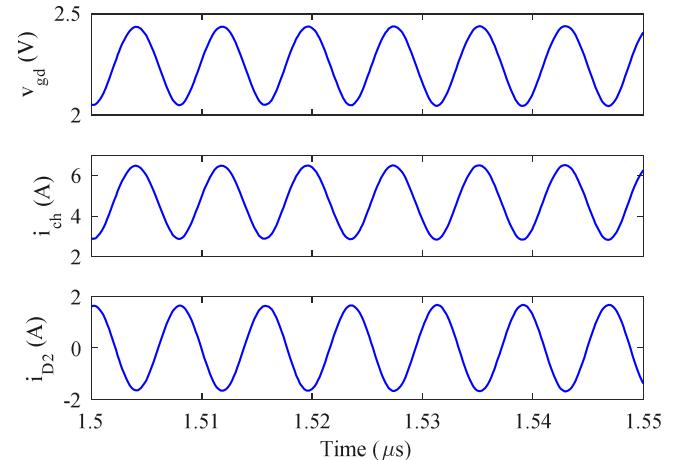


Fig. 24. Enlarged view of the simulated waveforms.

Fig. 25 shows the waveforms when gate signal of Q1 is added. When gate signal of Q1 is high, Q1 operates in the ohmic region instead of saturation region. The channel current is no longer controlled by  $v_{gd}$ . The circuit becomes stable because there exists no closed-loop system. The power loop inductance, output capacitance of Q2, and high-frequency power loop resistance form a second-order under-damped circuit, and thus, the oscillation damps down. After the Q1's drive signal changes from high to low, Q1 again works in the saturation region. The system is unstable and sustained oscillation occurs again. The oscillation is attenuated when the common-source inductance  $L_S$  is reduced to 0.1 nH as shown in Fig. 25(c). In Fig. 25(d), the oscillation damps when the Q1's external gate resistance  $R_{G1}$  increases to 4.7 Ω. Fig. 25(e) shows that paralleling a diode with Q1 also has a good effect on suppressing oscillation. The damping ratios calculated by (14) are highlighted in Fig. 13 and Fig. 14. The instability predicted by the damping ratios is consistent with the simulation results.

## V. EXPERIMENT RESULTS AND DISCUSSIONS

### A. Experimental Prototype

Fig. 26 shows a prototype of the half-bridge circuit with an inductive load. The switching devices are GS66508P (650 V enhancement-mode GaN devices) produced by GaN Systems Inc. The internal gate resistance  $R_{Gint}$  of GaN device is 1.3 Ω. The driver is LM5114. The current shunt is SSDN-414, which has a resistance of 0.1 Ω and a bandwidth of 2 GHz. The probe is P6139A with a bandwidth of 500 MHz. The parameters of the prototype are shown in Table III. The other parameters are listed in Table II.

### B. Experimental Verifications

1) *Influence of Bus Voltage on Stability:* Fig. 27 shows the measured waveforms under different bus voltages. When the bus voltage is 30 or 200 V, the oscillation is damped quickly. When the bus voltage is 60 or 100 V, the oscillation is undamped. The instability is also predicted by the damping ratios highlighted

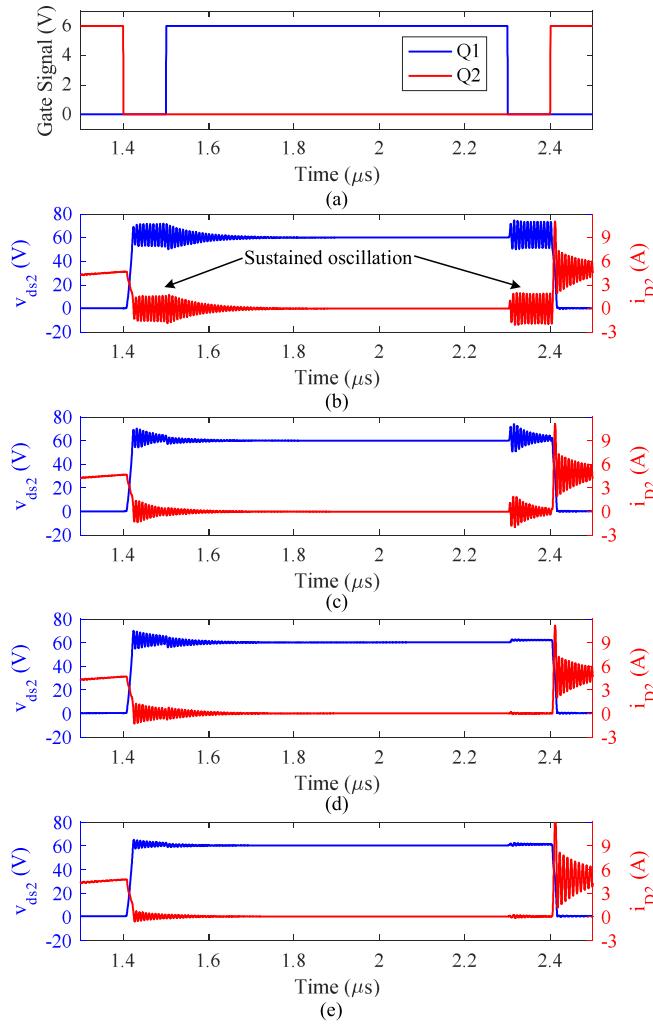


Fig. 25. Simulated waveforms. (a) Gate signals. (b)  $R_{G1} = 0 \Omega$  and  $L_S = 0.2 \text{ nH}$ . (c)  $R_{G1} = 0 \Omega$  and  $L_S = 0.1 \text{ nH}$ . (d)  $R_{G1} = 4.7 \Omega$  and  $L_S = 0.2 \text{ nH}$ . (e)  $R_{G1} = 0 \Omega$ ,  $L_S = 0.2 \text{ nH}$ , and Q1 is paralleled with a diode.

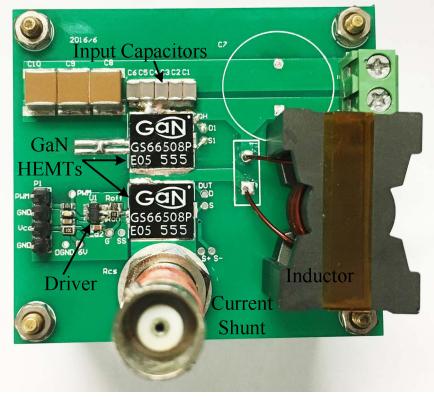


Fig. 26. Experimental prototype of the half-bridge circuit with inductive load.

in Fig. 12. When the bus voltage is 60 or 100 V, the damping ratio is less than zero, thus, predicting the system is unstable; when the bus voltage is 30 or 200 V, the damping ratio is greater than zero, thus, predicting the system is stable. The experiment results show a good agreement with the predicted results.

TABLE III  
PROTOTYPE PARAMETERS

Symbol	Description	Value
$V_{bus}$	Bus voltage	30–200 V
$I_L$	Inductor current	5 A
$R_S$	Current shunt resistance	0.1 Ω
$R_{Gint}$	Internal gate resistance of GaN devices	1.3 Ω
$V_G$	Driver voltage	6 V
$R_{G2}$	Q2's gate on (off) resistor	20 Ω (10 Ω)

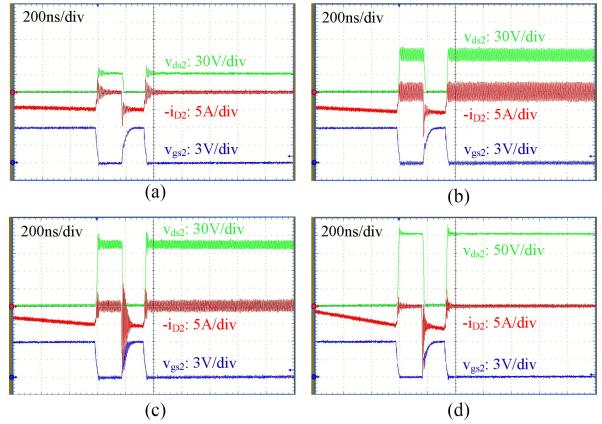


Fig. 27. Measured waveforms under different bus voltages where  $R_{G1} = 0 \Omega$ . (a)  $V_{bus} = 30 \text{ V}$ . (b)  $V_{bus} = 60 \text{ V}$ . (c)  $V_{bus} = 100 \text{ V}$ . (d)  $V_{bus} = 200 \text{ V}$ .

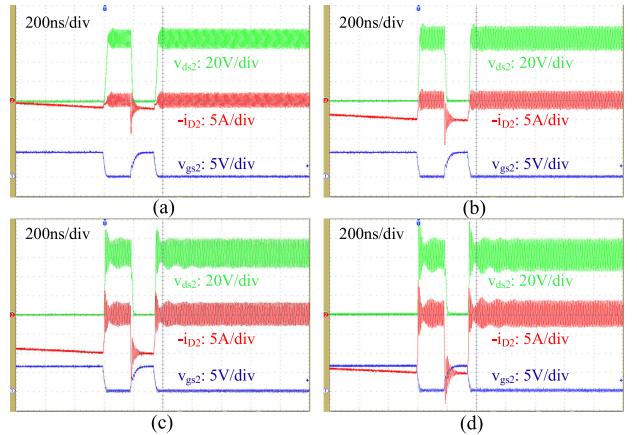


Fig. 28. Measured waveforms under different inductor currents. (a)  $I_L = 2 \text{ A}$ . (b)  $I_L = 5 \text{ A}$ . (c)  $I_L = 10 \text{ A}$ . (d)  $I_L = 15 \text{ A}$ .

2) *Influence of Inductor Current on Stability:* Fig. 28 shows the measured waveforms with different inductor current. The inductor current has little influence on the stability due to its small impact on the circuit parameters when it changes from 2 to 15 A. In addition, the switching speed varies with inductor current, which indicates that the switching speed has no effect on such instability to some extent.

3) *Oscillation Frequency:* The predicted oscillation frequency is calculated using (15). The oscillation frequency varies with  $V_{bus}$  since the output capacitance  $C_{oss2}$  is a function of the drain-source voltage. Fig. 29 shows that the measured results agree well with the predicted results. In addition,

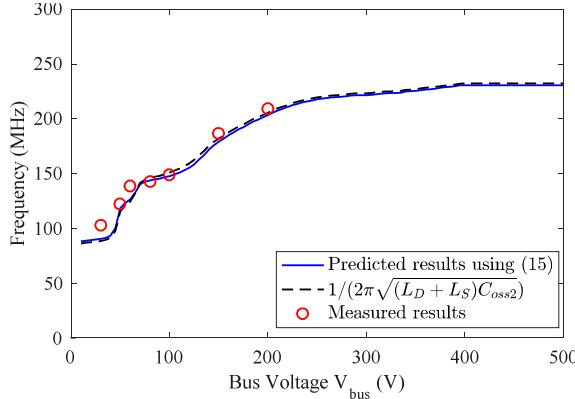
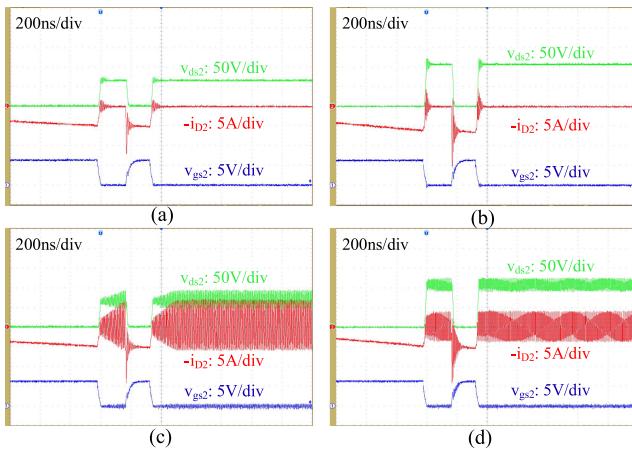


Fig. 29. Oscillation frequency.

Fig. 30. Measured waveforms under different common-source inductance where  $R_{G1} = 1 \Omega$ . (a)  $L_S = 0.2 \text{ nH}$  at  $V_{bus} = 60 \text{ V}$ . (b)  $L_S = 0.2 \text{ nH}$  at  $V_{bus} = 100 \text{ V}$ . (c)  $L_S = 0.5 \text{ nH}$  at  $V_{bus} = 60 \text{ V}$ . (d)  $L_S = 0.5 \text{ nH}$  at  $V_{bus} = 100 \text{ V}$ .

resonant frequency of the power loop impedance  $Z_{loop}$ , namely  $1/(2\pi((L_D + L_S)C_{oss2})^{0.5})$ , is close to the predicted and experimental results, which can be used to easily estimate the oscillation frequency.

### C. Guidelines to Suppress Oscillation

**1) Reducing Common-Source Inductance to Suppress Oscillation:** Two experiments with different  $L_S$  are performed. The GaN device GS66508P has a source sense pin connected with the source inside the package in order to reduce  $L_S$ . At the first experiment, the driver ground of inactive device is connected to the source sense pin and the resulted  $L_S$  is about 0.2 nH. The circuit is stable when bus voltage is 60 or 100 V by increasing  $R_{G1}$  to 1  $\Omega$  as shown in Fig. 30(a) and (b). At the second experiment, the driver ground is disconnected from the source sense pin and then connected to the source.  $L_S$  is, thus, increased to about 0.5 nH. It is a reasonable approach to connect the driver ground to the source because some GaN devices do not have the source sense pin. Under the experimental conditions, sustained oscillations are observed as shown in Fig. 30(c) and (d). The experimental results show that reducing  $L_S$  can effectively suppress the oscillation.

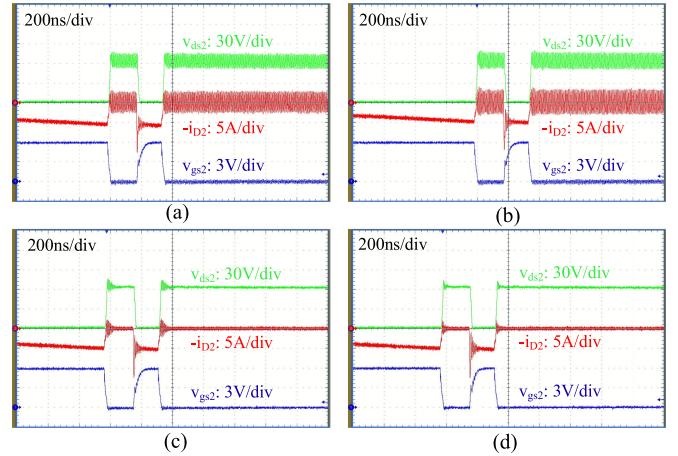
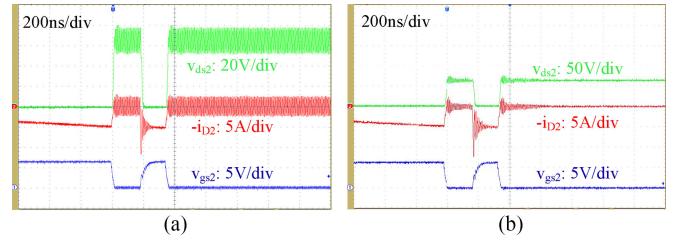
Fig. 31. Measured waveforms under different external gate resistors at  $V_{bus} = 60 \text{ V}$ . (a)  $R_{G1} = 0 \Omega$ . (b)  $R_{G1} = 0.5 \Omega$ . (c)  $R_{G1} = 1 \Omega$ . (d)  $R_{G1} = 4.7 \Omega$ .

Fig. 32. Measured waveforms. (a) Without diode. (b) SiC diode is paralleled across the drain and source of the inactive switch.

### 2) Increasing Gate Resistance to Suppress Oscillation:

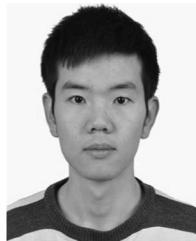
Fig. 31 shows the measured waveforms under different external gate resistors  $R_{G1}$  at  $V_{bus} = 60 \text{ V}$ . When  $R_{G1}$  is very small, such as 0 and 0.5  $\Omega$ , the oscillation is undamped. When  $R_{G1} = 1 \Omega$ , the oscillation is damped slowly. When  $R_{G1}$  is increased to 4.7  $\Omega$ , the oscillation is damped quickly. The experimental results show that increasing the gate resistance can significantly suppress the oscillation.

The instability is also predicted by the damping ratios highlighted in Fig. 14. The damping ratio increases with the increase of  $R_{G1}$ . When  $R_{G1}$  is 0 and 0.5  $\Omega$ , the damping ratio is less than zero, thus, predicting the system is unstable. When  $R_{G1}$  is 1 and 4.7  $\Omega$ , the damping ratio is greater than zero, thus, predicting the system is unstable. Because the damping ratio at  $R_{G1} = 1 \Omega$  is smaller than that at  $R_{G1} = 4.7 \Omega$ , the oscillation decays more slowly at  $R_{G1} = 1 \Omega$ . The predicted results obtained from the proposed model are consistent with the experiment results.

**3) Paralleling a Diode Across the Drain and Source of the Inactive Switch to Suppress Oscillation:** A 600-V SiC diode [28] is paralleled across the drain and source of the inactive switch to suppress the oscillation. The junction capacitance of the SiC diode leads to increase in  $C_{ds}$ , which has little effect on the stability because the increased  $C_{ds}$  has little effect on the damping ratio, as shown in Fig. 21. As a comparison, the circuit works in an unstable state without the diode, and sustained oscillation is observed in Fig. 32(a). After the diode is paralleled, the sustained oscillation is suppressed as shown in Fig. 32(b). However, the oscillation does not decay quickly at the beginning



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Dr. Jain received the Queen's Prize for Excellence in Research, the IEEE William Newell Power Electronics Award, the Engineering Medal of the Professional Engineers of Ontario, the IEEE IAS Distinguished Lecturer, Fellow of the Royal Society of Canada, Fellow of the Engineering Institute of Canada, and Fellow of the Canadian Academy of Engineering.