EE 212

Semiconductor Devices and Modeling

Lecture Notes

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Middle East Technical University
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NOTICE

Course Description: Basic semiconductor concepts. Conduction mechanisms in semiconductors and physical electronics. Physics of p-n junction diodes, bipolar junction transistors (BJTs) and field-effect transistors (FETs). Modes of operation and characteristics. Transistor biasing and small-signal models for BJTs and FETs. Secondary effects in transistors. Dynamic models for diodes and transistors. Modeling concepts for computer-aided design.

Grading

Midterm Examination 1 : 25%

Midterm Examination 2 : 25%

Final Examination : 30%

Short Examinations, Attendance, Homework: 20%

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Course Rules-I

In order to take the final and/or resit examination student must meet the following condition:

A minimum PRE score of 30.00 calculated as follows:

$$\text{PRE Score} = \frac{\text{Midterm 1 Score} + \text{Midterm 2 Score}}{2} x0.5 + \text{Average Short Examination Score} x0.2 + \text{Attendance Rate(\%)} x0.1$$

Students who fail to meet the above condition will be assigned the NA grade.

- Midterm 1, Midterm 2 and Short Examination scores will be assigned out of 100.
- Attendance rate will be calculated using the student attendance recorded during the semester.
- A single make up examination will be offered for the midterm examinations in the case of presentation of an approved medical report or legal (documented) excuse acceptable by the Department .

Course Rules-II

- Attend the lectures.
  Good attendance rate : 100%
  Any attendance rate below 100% is not desirable.

Course topics are stongly related to each other. Therefore, if you must miss a lecture, make sure you review the material covered in this lecture before coming to class for the next one.

- Study and review the course material regularly.

- Participate in the class discussions.

- Come on time to class for the lectures. Please be aware of the fact that students arriving late greatly disturb the presentation of the lecture. Such disturbances will not be allowed by the instructors if they occur repeatedly.

Course Rules-III

- Academic dishonesty will absolutely not be tolerated and disciplinary action will be initiated in case unethical conduct is suspected.

- Do not hesitate to contact your instructor during the semester (before it is too late) if you do not feel that you are comprehending the course material well enough even though you study regularly and have a good attendance rate. Your instructor will help you figure out the problem.

- Do not attempt to contact any of the instructors with the intention of raising your grade during the letter grade assignment phase.

- You will be allowed to inspect your corrected examination booklets on the dates announced at least one week in advance. Do not attempt to make a reservation at another date for this purpose unless you have an approved legal (documented) excuse.

Course Rules-IV

- Do not forget to bring your calculator to the examinations. You will not be allowed to share a calculator with a classmate during the examinations.
- Access to mobile phones, tablet PCs and having any stored/recorded course related information on the calculators, desks, armlet chairs etc during the examinations will be considered as unethical conduct.
- Midterm and final examinations will be started exactly at the time announced by the Department. Make sure you arrive at least 20 minutes before the examinations start.
- Short examinations will be given during the lecture hours. Students coming late to class will not be allowed to take the short examination and will not be given a make up for this examination.

GOOD LUCK!

EE 212-Semiconductor Devices and Modeling

Preface

The miracles of electronics and optoelectronics building the information age could not have been possible without an important class of materials called semiconductors. The ingenuity of the mankind combined with the generosity of the Nature has led to the invention of devices implementing important functions such as amplification, sensing, switching and processing which have greatly changed our daily life. The majority of these devices relies on the exceptional properties of the semiconductors.

Solid state device technology is a very wide and interdisciplinary field covering disciplines such as physics, electrical engineering, material science, chemistry and mechanical engineering. Therefore, it is not an easy task to teach the fundamentals of this technology especially at an introductory level assuming no background other than freshman physics, calculus and preliminary circuit theory. With the objective of providing the students with a background on the most essential fundamentals of semiconductors and solid state devices at an introductory level, the material presented in this course is carefully selected to include the topics which every electrical engineer, independent of specialization area, should be familiar with.

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With discussions far from being advanced, we will first get familiar with the basic properties of semiconductors and then utilize these properties to construct and study electronic/photonic devices that find wide application areas in the field of electrical engineering. Our motivation will be toward understanding the basic principles and predict/model the behavior of these devices in circuit applications with the main objective of acquiring substantial background for junior year courses on analog and digital electronics (EE 311 and EE 312) as well as some senior level courses.

In summary, while you will not be a solid state engineering expert after taking this course, you will be ahead of understanding semiconductor devices at a black-box level. Note that successful implementation of many circuit/system applications relies on this background which will allow you perform your job as an electrical engineer in a more efficient and productive manner. If you choose to specialize in this important area of Electrical Engineering, you will have a chance to be exposed to much wider and detailed coverage of the related topics in our senior level course EE419-*Solid State Devices*.

After taking this course you will

- understand the fundamentals of semiconductors and solid-state electronics at a depth sufficient to understand the principles of p-n junction diodes and transistors,
- understand the preliminary device models utilized by circuit simulators,
- predict the behaviour of diodes and transistors in analog and digital circuits,
- learn how transistors are utilized for amplification of signals,
- learn how optical devices such as photodetectors, solar cells and LEDs work,
- acquire substantial background for junior year courses on analog and digital electronics (EE 311 and EE 312) as well as the senior level course EE 419.

A BRIEF GUIDE TO USE THIS DOCUMENT

This document is intended to be self-sufficient for a student regularly attending the lectures and reviewing the course material. However, some of the references that you may wish to consult for further discussion/material are given on the selected slides with the corresponding sections of the edition listed on the chapter cover page (you can also find related discussions in the other reference books). Please note that section numbers may change in a different edition and be aware that you will be responsible for the topics covered in this document. Targeting 100% attendance rate will minimize the need to consult multiple reference books to comprehend the course material.

The Lecture Notes will be available for download from METU CLASS Web Site in pdf format. Please download and have it printed and bound (to bring to class) as soon as possible.

CHAPTER I

INTRODUCTION TO SEMICONDUCTOR FUNDAMENTALS

References

1) B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th Edition, Prentice Hall, 2006.

2) R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.

3) J. Singh, *Semiconductor Devices An Introduction*, McGraw-Hill, 1994.

4) R. F. Pierret, *Advanced Semiconductor Fundamentals*, Modular Series on Solid State Devices, Volume VI, Addison-Wesley, 2003.

5) M. Shur, *Introduction to Electronic Devices*, John Wiley, 1996.

6) R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*, Mc Graw Hill, 2nd Edition, 2004

The Role of This Chapter

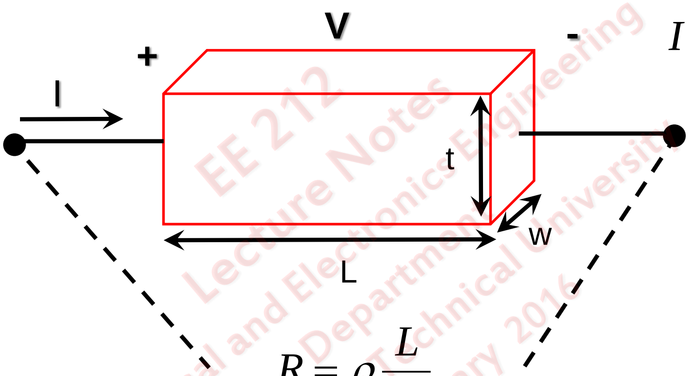
The characteristics of a semiconductor device strongly depend on the physical properties of the material used for device fabrication. The operational principles of a device constructed with a particular combination of semiconductor structures are established through the behavior of charge carriers in the material based on these physical properties and the operating conditions.

The objective of this chapter is to introduce the basic properties of semiconductors and the action of the charge carriers inside semiconductors at a depth sufficient to understand the operation of devices such as diodes and transistors at a preliminary level.

We will start with a qualitative description of the formation of energy bands in solids and classification of materials based on their electrical conductivity. The next topic of discussion will be the doping of semiconductors to control their conductivity through creation of charge carriers free for conduction. We will then discuss the action of charge carriers in response to Electric-field and carrier density gradients as well as to optical excitation creating excess carriers in the material.

It is a must to comprehend the material in this chapter in order to be able to understand the operational principles of diodes and transistors.

Resistance, Resistivity and Conductivity



$$I = \frac{V}{R}$$

$$R = \rho \frac{L}{wt}$$

$\rho = \frac{1}{\sigma}$, ρ: resistivity ($\Omega - cm$), σ: conductivity $(\Omega\text{-cm})^{-1}$, R: resistance (Ω)

L ↑⇒R↑, wt (cross sectional area) ↑⇒R ↓

Solid State Electronic Materials

Ref.6: 2.1

Classification	ρ	σ	Typical ρ (Ω-cm)	Example
Insulator	Large	Small	> 10^5	**Diamond**
Semiconductor	Moderate (Controllable)	Moderate (Controllable)	10^{-3}-10^5	**Silicon**
Conductor	Small	Large	< 10^{-3}	**Copper**

Q: What makes semiconductors so important for electronics?

S: The ability to modify the resistivity (conductivity) in a very wide range by adding impurities to the material (as we will see later).

The most widely used semiconductor is Silicon (Si) which is a column IV element in the periodic table. Since it (ideally) contains only one type of atom (Si), it is called elemental semiconductor.

Bonding Types

Ref.1: 3.1.1

Ionic Bonding: Electron exchange between the atoms resulting in formation of ions. Example: Na ($1s^2 2s^2 2p^6 3s^1$) and Cl ($1s^2 2s^2 2p^6 3s^2 3p^5$). $3s^1$ electron of Na atom $\rightarrow$ Cl atom.

The atoms are held together by the coulombic forces between the Na^+ and Cl^- ions.

Q: Is NaCl a conductor or insulator?

S: The outer orbits of all atoms are completely filled and there are no electrons loosely bound to the atoms constructing the crystal. This is equivalent to saying that there are no free electrons to contribute to current (no free charge carriers).Therefore, NaCl is an insulator.

Bonding Types

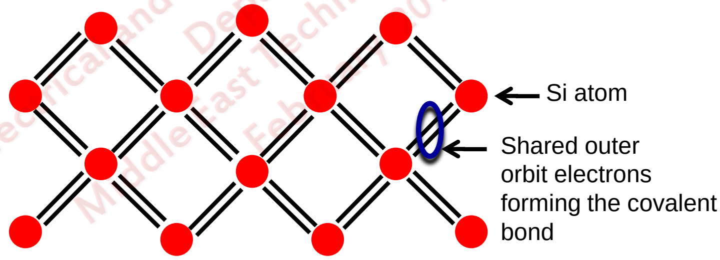
Ref.1: 3.1.1

Metallic Bonding: The outer electrons (such as $3s^1$ in Na) belong to the whole lattice and the crystal is held together by the forces between the positive ions and the free electrons. Note that a huge number of electrons is available for conduction $\rightarrow$ high conductivity.

Covalent Bonding: This is the type of bonding occuring in most semiconductors. Consider Si atoms with the electronic structure:

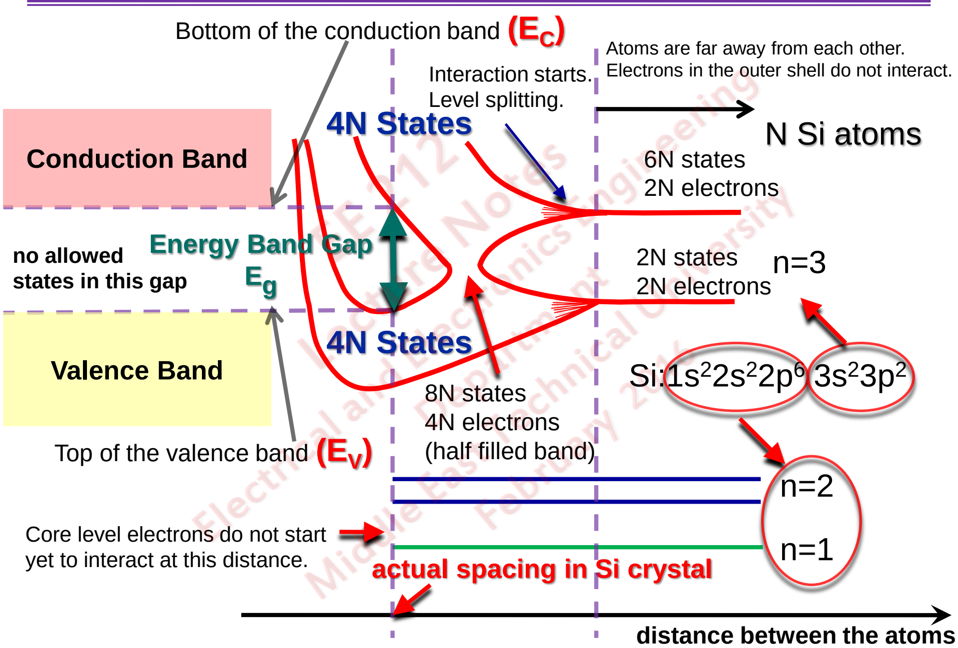
$1s^2 2s^2 2p^6 3s^2 3p^2$

In Si crystal each silicon atom shares its four outer orbit electrons with the neighboring Si atoms. The bonding forces result from quantum mechanical interactions between the electrons.



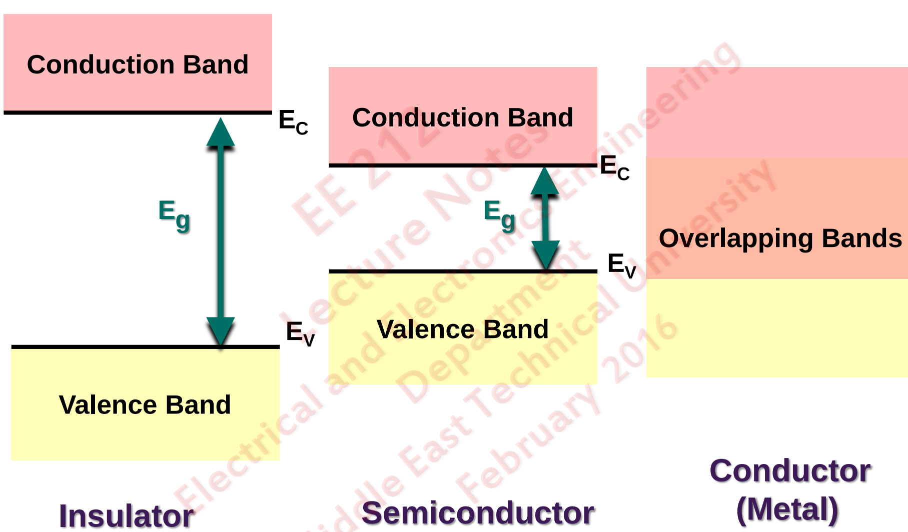
Energy Bands

Ref.1: 3.1.2, Ref. 2: 2.2.2



Energy Bands

Ref.1: 3.1.3, Ref. 2: 2.2.4

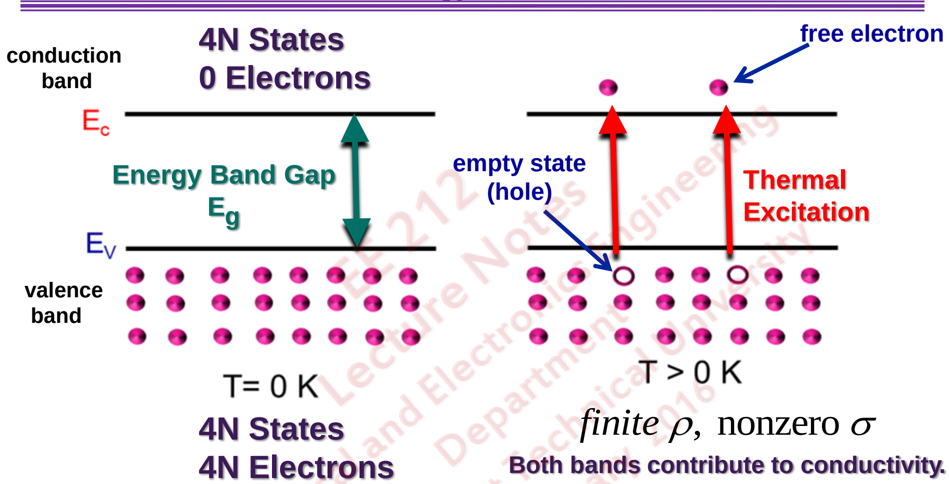


Q: What is the difference between the energy states of isolated atoms and those in a solid?

S: Electrons in isolated atoms occupy discrete energy states. On the other hand, energy bands (allowed and forbidden) form in a solid when we bring the atoms together to construct the crystal.

Q: Comment on the energy difference between the states in an energy band of a typical crystal.

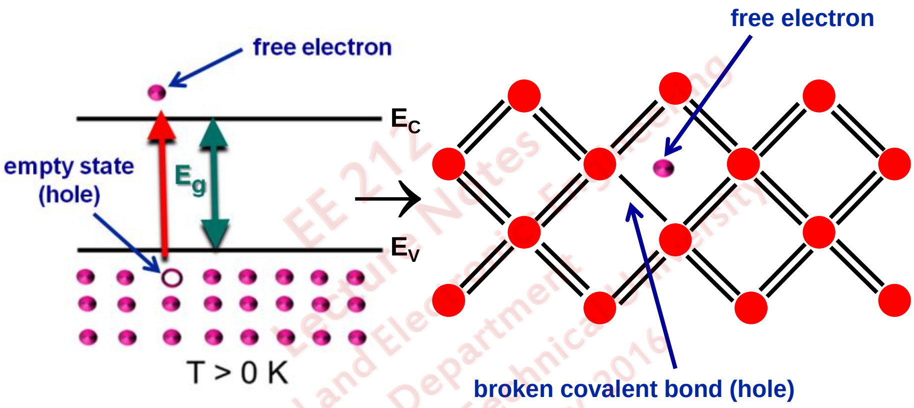
S: Since N in a typical crystal is a huge number, the energy difference between the states in a band is very small. Therefore, the conduction and valence bands can be considered to be continuous bands of energies.



Perfect insulator at 0 K. Conduction band does not contribute to conduction since there are no charge carriers. All the states in the valence band are filled $\Rightarrow$ no contribution of the valence band to current.

$$\rho = \infty, \ \ \sigma = 0$$

Carriers



Thermal excitation generates electron hole pairs (EHPs).

Q: What is the energy required to break a covalent bond (excite an electron from the valence to the conduction band)?
S: E_g.

Carriers

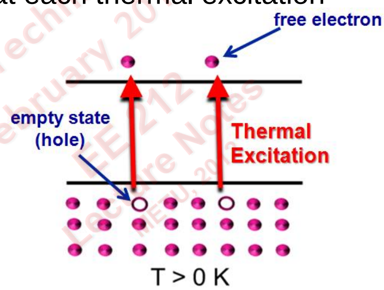
Intrinsic Semiconductor: perfectly pure semiconductor (intrinsic Si contains only Si atoms).

Carrier density in intrinsic semiconductor is called intrinsic carrier concentration (**n_i**).

Q: What is the relation between the conduction band electron density (**n**) and valence band hole density (**p**) in an intrinsic semiconductor?
S: The free carriers are generated by thermal excitation in an intrinsic semiconductor under equilibrium. Note that each thermal excitation creates

- one electron in the conduction band
- one hole in the valence band

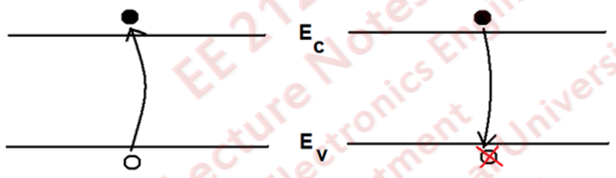
Therefore $n=p=n_i$



Carriers

Ref.1: 3.2.3

Note that there should be an inverse process balancing the thermal generation in order to achieve time independent electron and hole concentrations in a semiconductor (otherwise n and p continuously increase with time). The inverse process is called recombination.



Generation (creation of an electron-hole pair)

Recombination (annihilation of an electron-hole pair)

An electron is excited from the valence band to conduction band resulting in a filled state in the conduction band and an empty state (hole) in the valence band.

An electron makes a transition from the conduction band to an empty state in the valence band resulting in loss of an EHP.

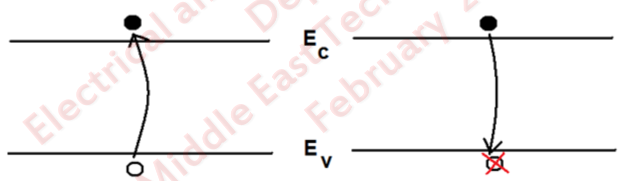
$$\boxed{np = n_i^2}$$

Carriers

Ref.1: 3.2.3

Q: How do the carrier concentrations (n and p) change with temperature in an intrinsic (pure) semiconductor?

S: When the temperature is increased the thermal generation rate becomes higher leading to a larger generation rate for EHPs. Due to the larger densities of electrons in the conduction band and holes in the valence band, the recombination rate is also increased. Obviously, we still need to have a balance between the generation and recombination rates. However, at a higher temperature this balance occurs at higher n and p resulting in n_i increasing with temperature.



Important Semiconductors

The characteristics of a semiconductor device strongly depend on the physical properties of the material used for device fabrication. Different applications requiring different physical properties call for the availability of a wide group of semiconductors for device fabrication. Among these materials, Si and GaAs are the most well known semiconductors with the most mature technologies.

Si is a material which is abundant in nature offering the lowest cost solution for the manufacturer. It is one of the most extensively studied semiconductors with very well known properties and characteristics. However, there exist electron device applications where the physical properties of Si do not meet the requirements. At the same time, Si does not work well for optical devices (such as lasers) while some other semiconductors (such as GaAs) do.

The following table lists the energy bandgaps of some semiconductors. Some of these materials are elemental semiconductors (Si and Ge), while the others are compound semiconductors formed by combining elements from different columns (mostly III and V) of the periodic table.

Important Semiconductors

We see that energy bandgaps varying in a wide range are available for fabricating devices to operate with different characteristics. The other physical properties of these materials also change in a wide scale offering devices with different

- operation frequencies
- operation conditions (biasing voltage, temperature etc)
- radiation emission characteristics
- radiation detection characteristics
- ....

The discussion in this course will mostly focus on Si based devices while the semiconductor fundamentals presented in this chapter are, of course, applicable to all semiconductors.

Semiconductor	Energy Gap (300 K)
Si	1.11
Ge	0.74
GaAs	1.42
InP	1.35
InSb	0.17
InAs	0.36
GaP	2.26
GaN	3.2

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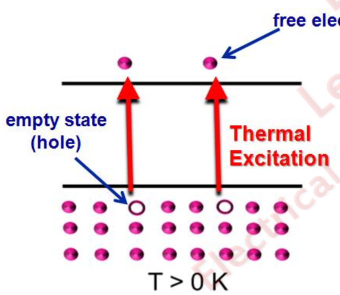
Intrinsic Carrier Concentration

Ref.1: 3.2.3, Ref. 6: 2.2

Q: List the possible parameters governing the intrinsic carrier concentration in a semiconductor.

S:

- Temperature, T↑⇒thermal excitation rate ↑⇒ EHP generation rate↑
- E_g, Bandgap ↓ ⇒ thermal excitation rate ↑⇒ EHP generation rate↑



$$n_i = \sqrt{BT^3 e^{-\frac{E_g}{kT}}}$$

Bandgap Energy in eV (1.12 eV for Si)

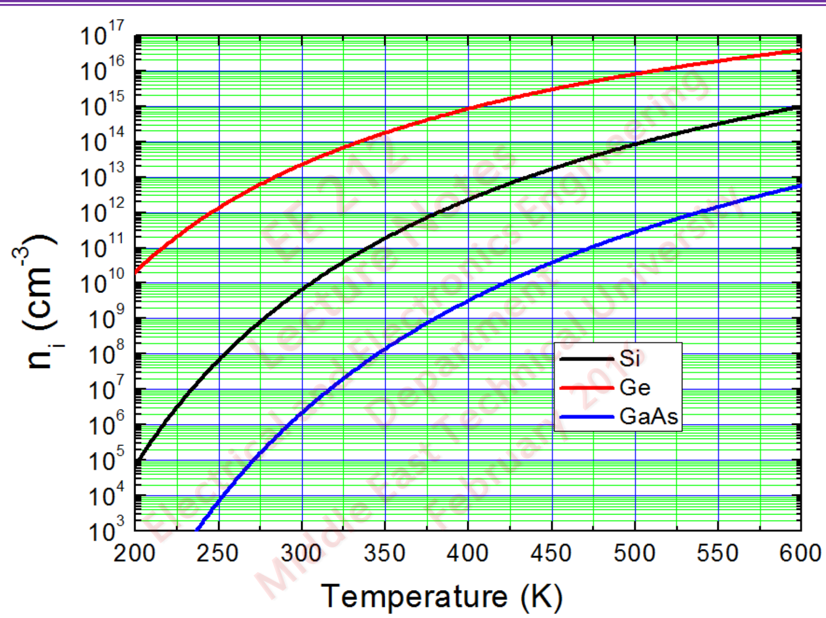
T in K

Boltzmann Constant (8.62×10^{-5} eV/K)

T in K

material dependent parameter (1.08×10^{31} K^{-3}-cm^{-6} for Si)

Intrinsic Carrier Concentration



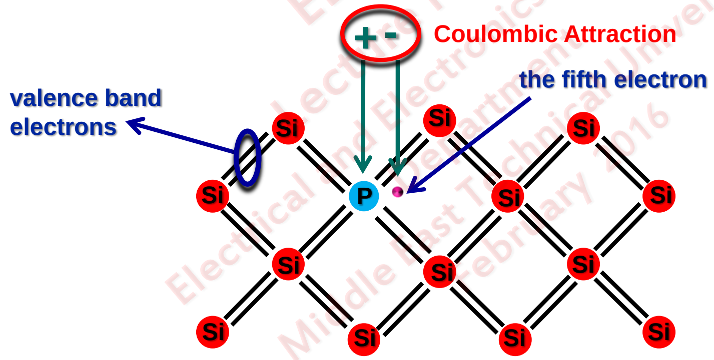
The most important property of a semiconductor for electronic device applications is the ability to control the resistivity of the material by **introducing impurities at controlled amounts**.

This process is called **doping**. An intrinsic (pure) semiconductor can be doped to make **n>p (n-type)** or **p>n (p-type)**.

Formation of contacts between **n** and **p** type semiconductors results in devices performing useful functions such as rectification and amplification of signals as well as switching which establish the basis for analog and digital electronics.

Q: What happens if a Column V impurity such as P is added to Si which is a Column IV element?

S: When a P atom replaces a Si atom in the crystal, four of the (five) outer shell electrons of P are used to form bonding with the neighboring Si atoms. We have one electron left out of this bonding structure. This electron is loosely bound to the P atom and can easily be set free for conduction.

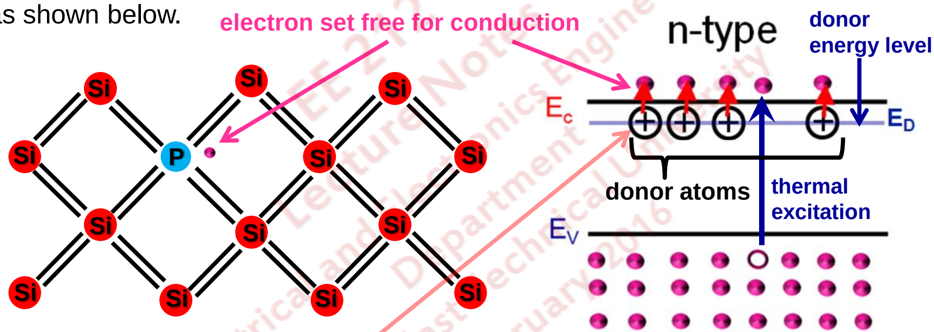


Doping-n type

Ref.1: 3.2.4, Ref. 2: 2.3.4

Since Column V impurity P donates an electron free for conduction to Si, it is called **donor** atom.

This type of doping process can be represented using the energy band diagram as shown below.



Note that the donor atom is charge neutral when it is introduced to the crystal. If you take one electron away from this atom (set the electron free for conduction), the donor atom becomes positively charged (called donor ionization).

Q: What is the (thermal) energy required to ionize the donor atom (ionization energy)?

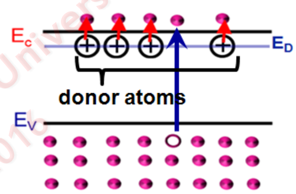
S: E_C-E_D.

Doping-n type

Q: Consider an intrinsic (pure) semiconductor. Mark the correct answer for this semiconductor.

○ **$n=p=n_i$** ○ **$n>p$, $n>n_i$** ○ **$n<p$, $n<n_i$**

Q: Now dope this semiconductor with donors. Mark the correct answer for the doped semiconductor.



○ **$n=p=n_i$** ○ **$n>p$, $n>n_i$** ○ **$n<p$, $n<n_i$**

Q: Compare the hole density in an intrinsic semiconductor ($p=n_i$) with that in a donor doped semiconductor.

○ **$p_{donor\text{-}doped}>n_i$** ○ **$p_{donor\text{-}doped}< n_i$**

?

Doping-n type

S: In order to answer this question, remember that the product of the electron and hole concentrations is constant at a given temperature or

$$n_{doped}\, p_{doped} = n_i^2$$

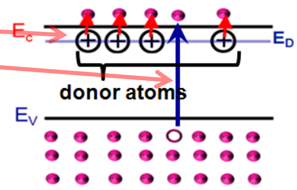
We have increased n over n_i by doping the semiconductor with donor impurities ($n_{doped} > n_i$). Then

$$p_{donor-doped} = \frac{n_i^2}{n_{donor-doped}} < n_i$$

Q: Find the expression for the electron concentration in a donor doped semiconductor if the donor doping density is N_D donors per cm^3. Assume that all the donors are ionized (donate electrons to the conduction band).

S: The sources of electrons in a donor doped semiconductor are

- donor ionization
- thermal generation



However,

$$n \neq N_D + n_i$$

Doping-n type

In order to find the required expression we need to use the following relations:

1) The charge neutrality of the semiconductor is not disturbed through thermal generation (an EHP is created) or recombination (an EHP is destroyed).
   Donor ionization does not disturb the charge neutrality either. Hence, a negatively charged electron is created for each positively charged ionized donor.
   Then total negative charge must be equal to total positive charge in the material or

volume

$$qVn = qV(N_D^+ + p) \Rightarrow n = N_D^+ + p$$

$$\text{Assuming complete ionization, } N_D^+ = N_D,$$

$$n = N_D + p$$

2) $np = n_i^2$

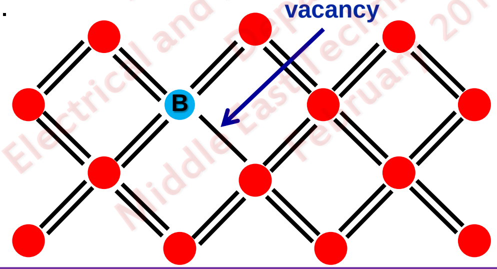
$$n = \frac{N_D + \sqrt{N_D^2 + 4n_i^2}}{2}$$

Doping-p type

Ref.1: 3.2.4, Ref. 2: 2.3.4

Q: What happens if a Column III impurity such as B is added to Si which is a Column IV element?

S: When a B atom replaces a Si atom in the crystal, four valence electrons are needed to complete the covalent bond with the neighboring Si atoms. However, since B atom has three outer shell electrons, an incomplete bond is constructed with a vacancy. This incomplete bond (vacany) does not need to be fixed in position. Note that electrons from Si-Si bonds (if provided with necessary energy) can fill this vacancy (completing the bond) and transfer the incomplete bond to another atom. This is considered as the impurity taking an electron from the valence band which includes the electrons of the Si-Si bonds. Once this happens, the B atom becomes negatively charged (with one extra electron).

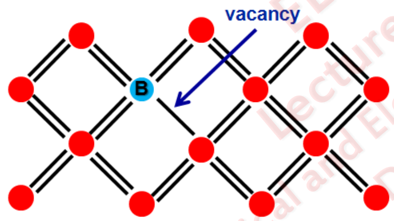


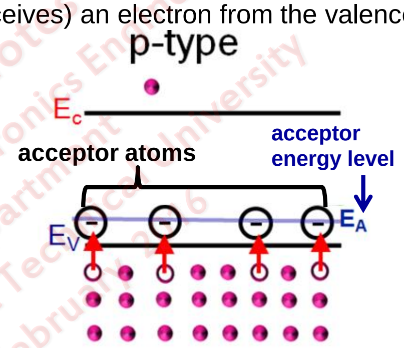
Doping-p type

Ref.1: 3.2.4, Ref. 2: 2.3.4

This type of doping process can be represented using the energy band diagram as follows. The above described process can be visualized as B atoms accepting electrons from the valence band and creating empty states (holes) in this band.

Since Column III impurity B accepts (receives) an electron from the valence band, it is called **acceptor** atom.





Q: What is the (thermal) energy required to ionize the acceptor atom (ionization energy)?

S: E_A-E_V.

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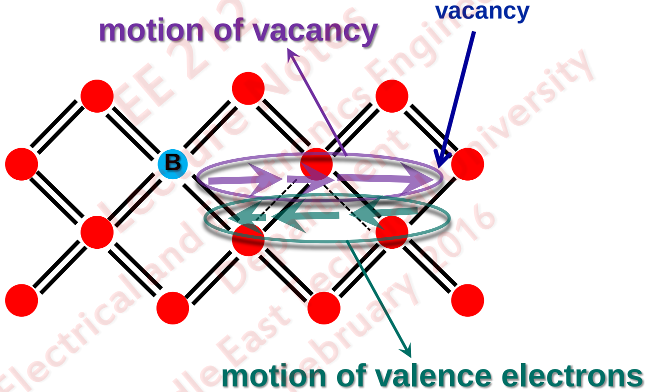
Doping-p type

As the valence electrons move from atom to atom filling vacancies, the vacancies also move through the crystal. However, note that the direction of motion of the vacancy (as a result of the motion of the electrons) will be opposite to that of the electrons.



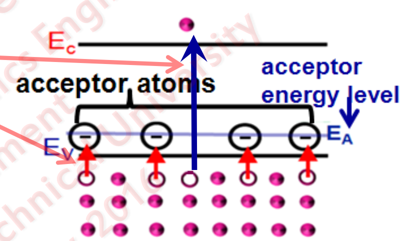
The contribution of the valence band to conduction (motion of valence band electrons) can be described using the motion of the vacancies. However, note that the vacancy (hole) should be treated as a positively charged particle.

Doping-p type

Q: Find the expression for the hole concentration in an acceptor doped semiconductor if the acceptor doping density is N_A acceptors per cm^3. Assume that all the acceptors are ionized (accept electrons from the valence band).

S: The sources of holes in an acceptor doped semiconductor are

- acceptor ionization
- thermal generation



However,

$$p \neq N_A + n_i$$

Use charge neutrality equation:

$$qVp = qV(N_A^- + n) \Rightarrow p = N_A^- + n$$

Assuming complete ionization, $N_A^- = N_A$,

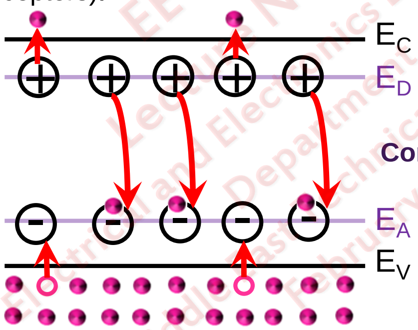
$$\left.\begin{aligned} p &= N_A + n \\ np &= n_i^2 \end{aligned}\right\} \quad p = \frac{N_A + \sqrt{N_A^2 + 4n_i^2}}{2}$$

Compensation

Ref.1: 3.3.4

Q: What happens if I dope a semiconductor with both donors and acceptors?

S: This process is called compensation. The electrons of the donor atoms fill the vacancies created by the acceptors. This is not a desirable process and it should be avoided unless absolutely necessary, since it degrades the transport properties of the material due to high concentration of impurity atoms (both donors and acceptors).



The above pictured process is equivalent to the annihilation of a valence band hole created by an acceptor by a conduction band electron created by a donor.

Carrier Concentrations

Ref. 2: 2.5.4, 2.5.5

Q: How do I find the electron and hole concentrations in a compensated semiconductor?

S:

ionized impurity densities

Charge Neutrality Equation: $n + N_A^- = p + N_D^+$

Assuming complete ionization: $N_D^+ = N_D, N_A^- = N_A \rightarrow n + N_A = p + N_D$

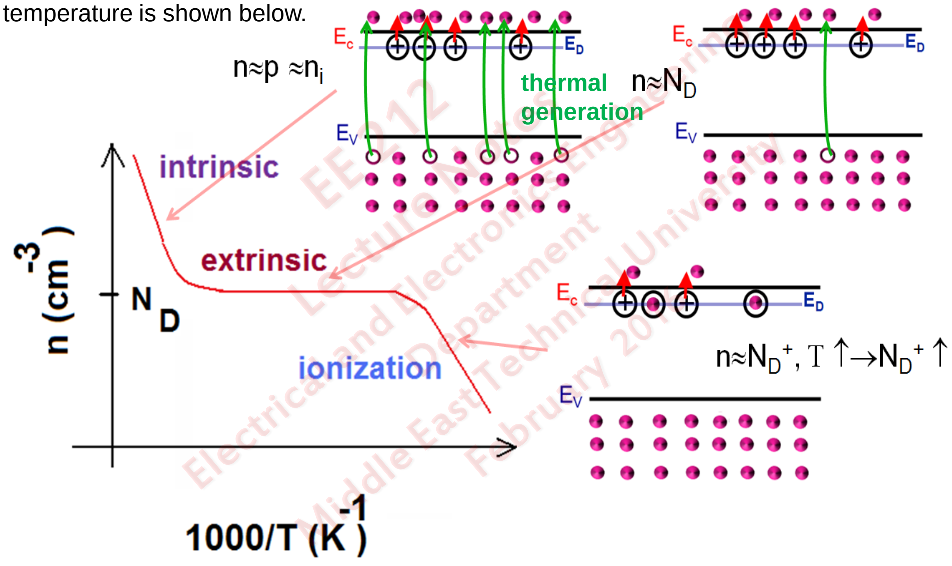
$$pn = n_i^2 \rightarrow n = \frac{N_D - N_A + \sqrt{(N_D - N_A)^2 + 4n_i^2}}{2},$$

$$p = \frac{N_A - N_D + \sqrt{(N_A - N_D)^2 + 4n_i^2}}{2}$$

Carrier Concentrations

Ref. 2: 2.5.7

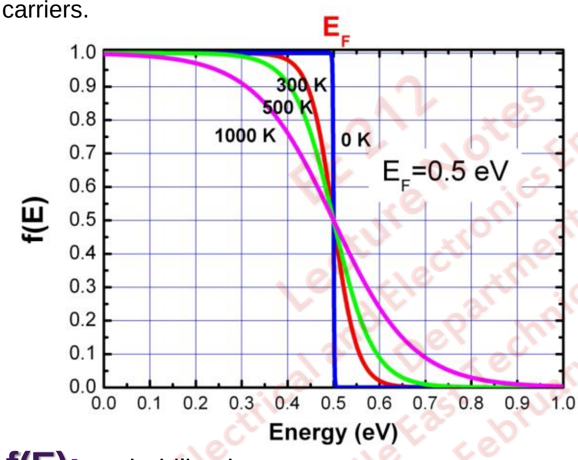
The variation of the electron concentration in a donor doped semiconductor with temperature is shown below.



Fermi Dirac Distribution Function

Ref.1: 3.3.1, Ref. 2: 2.4.2

Fermi-Dirac Function governs the occupancy of the available energy states by the carriers.



$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}}$$

f(E): probability that an energy state at an energy E is occupied by an electron at temperature T.

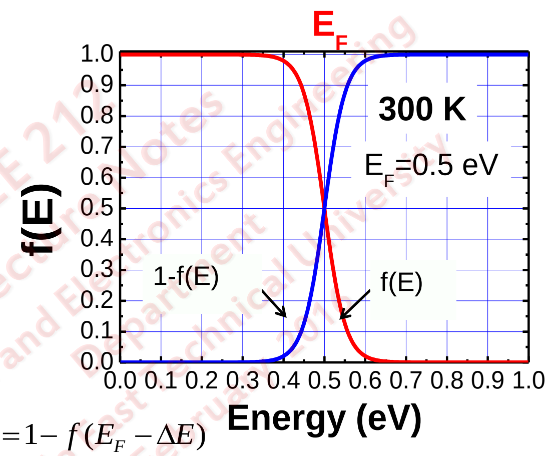
E_F: reference energy level (**Fermi Level**).

Fermi Dirac Distribution Function

Ref.1: 3.3.1, Ref. 2: 2.4.2

Fermi Function is symmetrical around the Fermi Level.

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT}}}$$



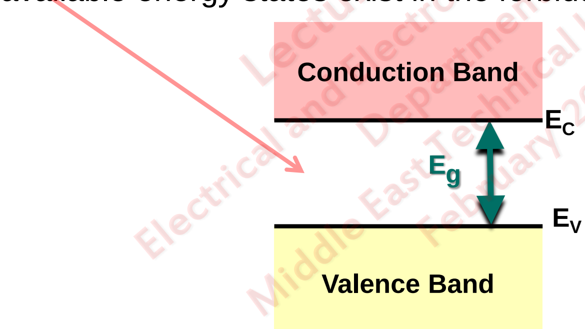
$$\underbrace{f(E_F + \Delta E)}_{\text{Probability that the energy state at } E_F+\Delta E \text{ is occupied}} = 1 - \underbrace{f(E_F - \Delta E)}_{\text{Probability that the energy state at } E_F-\Delta E \text{ is empty}}$$

Fermi Dirac Distribution Function

Ref.1: 3.3.1, Ref. 2: 2.4.2

Fermi-Dirac Function yields the occupancy probability of a state at energy E assuming that there exists an available energy state at this energy.

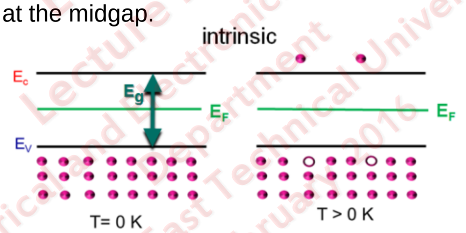
Note that no electron can occupy an energy level in a forbidden gap even though f(E) may not be zero in this energy interval, since no available energy states exist in the forbidden energy gaps.



Fermi Dirac Distribution Function

Q: Where is the Fermi level located in an intrinsic semiconductor?

S: n=p in an intrinsic semiconductor. Assuming that the density of the available energy states in the conduction band is identical to that in the valence band, E_F should be located at the midgap position to make n=p. In other words, the probability that a state is occupied (an electron exists) at an energy ΔE above Ec should be equal to the probability that a state ΔE below Ev is empty (a hole exists) in order to have n=p. The symmetry of the Fermi function around the Fermi level satisfies this requirement if the Fermi level is positioned at the midgap.



$$E_F = E_V + \frac{E_g}{2} = E_V + \frac{E_C - E_V}{2} = \frac{E_C + E_V}{2}$$

$$n = p = n_i$$

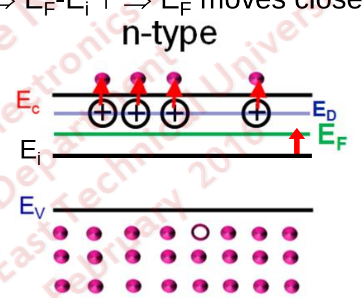
$E_F=(E_C+E_V)/2=$**E_i (intrinsic level)** in intrinsic semiconductor

Fermi Dirac Distribution Function

$$n = n_i e^{\frac{E_F - E_i}{kT}} \quad , \quad p = n_i e^{\frac{E_i - E_F}{kT}}$$

Q: How does E_F-E_i change when an intrinsic semiconductor is doped with donors?

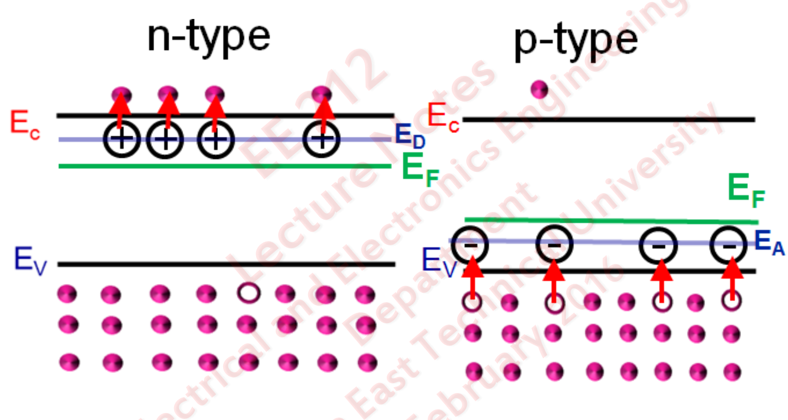
S: $N_D \uparrow$ (initially N_D=0) $\Rightarrow$ n $\uparrow \Rightarrow$ E_F-E_i $\uparrow$ $\Rightarrow$ E_F moves closer to the conduction band edge (E_C).



Q: How does E_i-E_F change when an intrinsic semiconductor is doped with acceptors?

S: write

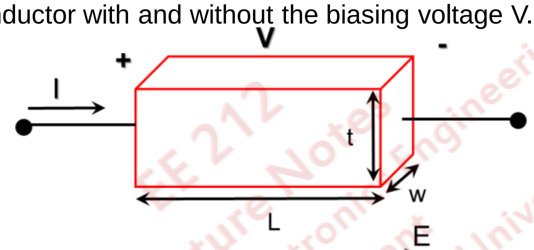
Fermi Dirac Distribution Function



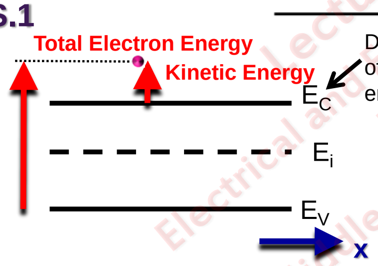
Exercise Questions

Ref. 2: 3.1.5

Q.1 Consider the following semiconductor. Plot the energy band diagram of this semiconductor with and without the biasing voltage V.



S.1



Displays the variation of the electron potential energy with position

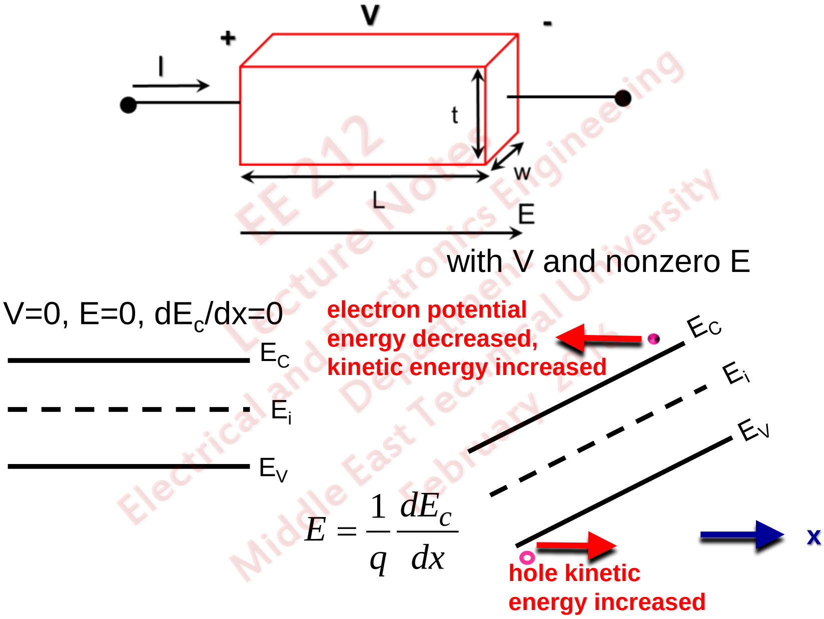
$$Potential\ Energy = -q\ x\ electrostatic\ potential\ (V)$$

$$Then\ \frac{dV}{dx} = -\frac{1}{q}\frac{dE_C}{dx} = -E\ (E-field)\ \text{ or}$$

$$E = \frac{1}{q}\frac{dE_C}{dx}$$

Exercise Questions

Ref. 2: 3.1.5



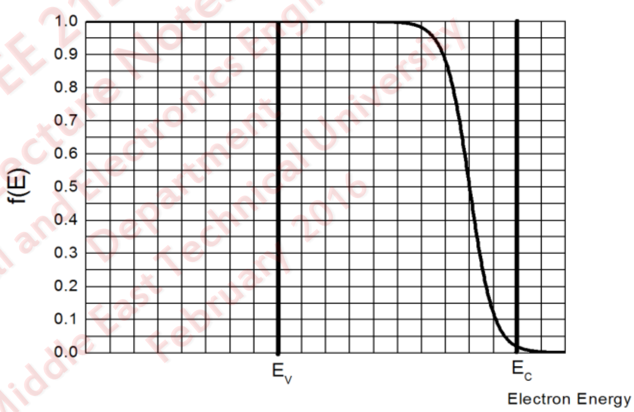
$$E = \frac{1}{q}\frac{dE_c}{dx}$$

Exercise Questions

Q.2 (to be solved on white board)

The occupation probability of a semiconductor with E_g=1 eV, n_i=10^{10} cm^{-3} (300 K) is shown below. Find the electron concentration in the conduction band at 300 K. kT= 25 meV.

S.2 write



Exercise Questions

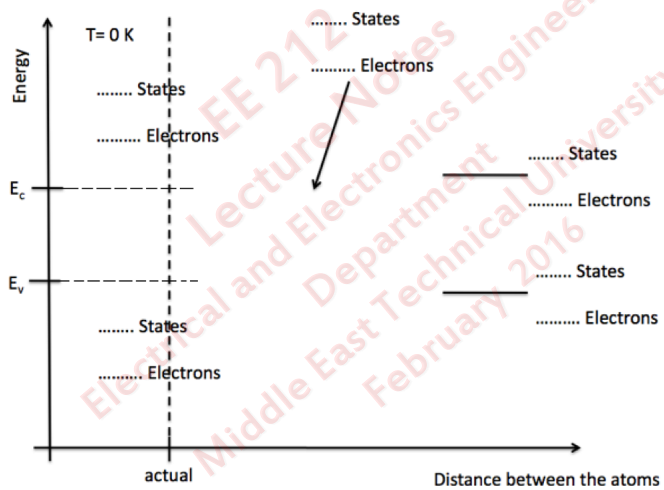
Q.3 (to be solved on white board)

Find the location of the Fermi level with respect to the intrinsic level in GaAs at 300 K if it is doped with donor atoms at a density of 10^{14} cm^{-3}. The intrinsic carrier concentration of GaAs is approximately 2×10^{6} cm^{-3} at 300 K.

S.3 write

Q.1 Homework 1 (Estimated Time To Complete < 150 min.)

Show the formation of the energy bands in a solid constructed by bringing N atoms with electronic structure $1s^2 2s^2 2p^6 3s^2 3p^2$ together. Show only the bands forming through the outer shell (3s-3p) states.



EE 212 Lecture Notes
Electrical and Electronics Engineering Department
Middle East Technical University
February 2016

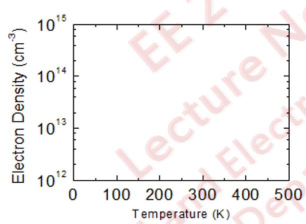
Q.2 Homework 1

Fill in the blanks.

- ………………………… are materials with resistivities smaller than the resistivity of …………………… and larger than the resistivity of ………………………
- Fermi-Dirac function is symmetrical around the Fermi Level. This means that the probability of finding a filled state ΔE ……………………………………………………….is equal to the probability of ………………………………………………………. …………………………………
- In an intrinsic semiconductor (in equilibrium) the ……………………….. density is equal to the ………………………… density and these are created by ……………………………………………
- An intrinsic Si sample can be converted to n-type Si by introducing impurities from …………………………………. of the periodic table. These impurities are called ………………………….. and they increase the ………………………………… in the ………………………… band.
- Charge neutrality in a semiconductor means that the sum of the densities of the ……………………………………. and ………………………………………. is equal to the sum of the densities of ………………………………………. and …………………..
- An intrinsic semiconductor may be regarded as a perfect insulator at 0 K since at this temperature the …………………………… band is completely ……………………… and the ………………………………… band is completely ……………………………

Q.3 Homework 1

- At room temperature, the Fermi-Dirac distribution function has non-zero values for the energy levels between E_v and E_C. Does this imply that an electron can occupy an energy state in the bandgap? Explain your reasoning.
- Find $E_f - E_i$ in intrinsic Si when it is heated to 400 K. Provide only the numerical answer.
- Plot (roughly) the electron concentration versus temperature in an n-type Si (N_D=10^{14} cm^{-3}) doped with hypothetical donors with zero ionization energy.



- Why do Column V impurities in Si increase the electron concentration in the conduction band? Explain qualitatively in sufficient detail.
- Find the location of the Fermi level with respect to intrinsic level if the probability that a state filled at the conduction band edge is equal to the probability that a state is empty at valence band edge.
- You have an n-type Si sample and an intrinsic Si sample. You heat (only) the intrinsic Si sample until the electron concentration equals that of the n-type sample. Is the energy difference between the conduction band and Fermi Level (E_c-E_F) in the intrinsic sample greater than, about the same as, or less than that in the n-type sample at this temperature? Explain your reasoning.

Q.4 Homework 1

Determine the equilibrium electron and hole concentrations inside a uniformly doped sample of Si under the following conditions. For each of the conditions, determine E_F-E_i, and draw the energy band diagram for the Si sample. Assume that the bandgap energy (E_G) does not change with temperature.

i) T = 300 K, $N_A \ll N_D$, $N_D = 10^{15}/cm^3$.

ii) T = 300 K, $N_D \ll N_A$, $N_A = 10^{16}/cm^3$.

iii) T = 300 K, $N_A = 9x10^{15}/cm^3$, $N_D = 10^{16}/cm^3$.

iv) T = 450 K, $N_A = 0$, $N_D = 10^{14}/cm^3$, $n_i = 5x10^{13}/cm^3$

Q.5 Homework 1

i) Given a sample of Silicon doped with acceptor impurities, describe two ways to make the equilibrium carrier concentrations approximately equal.

ii) In the table below, compare the quantities in the left column to the quantities in the right column by writing one of the following symbols in the provided spaces: **<, >, =**. If there is insufficient information to make a comparison, write: **NC**.

Electron density in the conduction band of intrinsic silicon at T=0K		Hole density in the valence band of Germanium at T=0 K doped with a donor atom concentration of $N_D=10^{16}$ cm^{-3}.
(E_F-E_V) in silicon doped with $N_D=10^{16}$ cm^{-3} donor impurities and $N_A=10^{18}$ cm^{-3} acceptor impurities at T=300K.		(E_F-E_V) in intrinsic silicon at T=400K.
Thermal generation rate of EHPs in a sample of intrinsic silicon at T=300K.		Recombination rate of EHPs in the same sample at T=200 K.

Q.6 Homework 1

Circle the correct answer for the following 17 questions.

- Consider a Si crytal with N Si atoms. Which of the following statements is **wrong**?
  a) There are 4N available energy states in the conduction band
  b) There are 4N available energy states in the valence band
  c) There are no allowed energy states between the bottom of the conduction and top of the valence bands
  d) There are 4N electrons in the valence band at 0 K
  e) All of the above statements are correct

- The conductivity of an intrinsic semiconductor at very low temperatures will be low since
  a) there are no electrons in the valence band and the conduction band is filled
  b) the mobility of the electrons in the conduction band will be low
  c) the impurity ionization energy is large
  d) thermal excitation rate from valence to conduction band will be low
  e) None of the above

- The conductivity of an intrinsic semiconductor at temperature T will depend on
  i) T ii) energy band gap iii) dimensions of the material
  a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

- The electron concentration in intrinsic Si at 300 K is
  a) 0 b) 1×10^{20} cm^{-3} c) 1×10^{10} cm^{-3} d) 5×10^{9} cm^{-3} e) None of the above

- The intrinsic carrier concentration in Si at 400 K is
  a) $> 1 \times 10^{10}$ cm^{-3} b) $< 1 \times 10^{10}$ cm^{-3} c) 1×10^{10} cm^{-3} d) 0 e) ∞

Q.6 Homework 1

- When N Si atoms are brought together and perfectly pure Si crystal is formed,

a) There exist 8N total energy states in the conduction band
b) The crystal conducts even at 0 K due to half filled conduction band
c) Energy bands form due to the interaction of core level electrons
d) Electron concentration in conduction band is equal to the hole concentration in valence band
e) All of the above are correct

- The energy difference between the allowed states in the conduction band of Si is small since

a) There is a huge number of atoms in a typical Si crystal
b) The energy bandgap of Si is not large
c) The conduction band of Si is half filled at any temperature
d) There exist thermal excitation of electrons from the valence to the conduction band
e) None of the above is correct

- The intrinsic carrier concentration in a semiconductor is 1×10^{14} cm^{-3} at 300 K. What is the electron concentration in this semiconductor (at 300 K) if it is doped with (only) acceptors at a concentration of 1×10^{14} cm^{-3}? All the acceptors are ionized at 300 K.

a) 1.6×10^{14} cm^{-3}
b) 6.2×10^{13} cm^{-3}
c) 1×10^{14} cm^{-3}
d) 0
e) can not be determined with the provided information.

- If an intrinsic semiconductor is doped with donor atoms to make it n-type

a) Electron concentration is much larger than the hole concentration at any temperature
b) Each donor atom donates one electron to the valence band
c) Electron concentration is decreased
d) Conductivity of the semiconductor is increased
e) All of the above are correct

Q.6 Homework 1

- When the temperature of an intrinsic semiconductor is increased
  i) the thermal generation rate is increased
  ii) the recombination rate is increased
  iii) a balance between thermal generation and recombination rate will occur at higher carrier concentrations in the conduction and valence bands
  a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

- When Column V impurities are introduced into intrinsic Si and they are ionized
  i) the hole concentration is decreased
  ii) the Fermi level approaches the conduction band
  iii) the resistivity of the material is decreased
  a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

- When Column III impurities (completely ionized at T=300 K) are introduced into intrinsic Si at a density comparable to intrinsic carrier concentration at 300 K
  i) the hole concentration increases considerably if the temperature is increased to 350 K
  ii) contribution of thermal generation to hole concentration becomes negligibly small
  iii) the Fermi level deviates from the intrinsic level
  a) only iii b) i and ii c) i and iii d) ii and iii e) i, ii and iii

Q.6 Homework 1

- Consider two Si samples with different donor impurities. $(E_C\text{-}E_D)_{\text{sample 1}} > (E_C\text{-}E_D)_{\text{sample 2}}$
  i) sample 2 starts to show extrinsic behavior at lower temperatures
  ii) sample 2 starts to show intrinsic behavior at lower temperatures
  iii) sample 1 is more compensated
  a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

- If an intrinsic semiconductor with intrinsic carrier concentration of $1\text{x}10^{14}$ cm^{-3} is doped with donors at a density of $1\text{x}10^{14}$ cm^{-3}, the hole concentration under complete ionization is
  a) $1.62\text{x}10^{14}$ cm^{-3} b) $1\text{x}10^{14}$ cm^{-3} c) $1\text{x}10^{28}$ cm^{-3} d) $6.2\text{x}10^{13}$ cm^{-3} e) None of the above

- If the probability of occupancy for an energy state 50 meV above the Fermi level is 0.1, the probability of occupancy for an energy state 50 meV below the Fermi level is
  a) 0.1 b) 0.9 c) 0 d) 1 e) None of the above

- E_C-E_F in Si doped with $N_D=1\text{x}10^{16}$ cm^{-3} (300 K, complete ionization) is
  a)345 meV b) 550 meV c) 205 meV d) 25 meV e) 895 meV

- If a built in E-field exists in a semiconductor, E_C and E_V change with position since
  i) the electron potential energy is changing with position
  ii) the energy band gap is changing with position
  iii) the Fermi Level is changing with position
  a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

Homework 1

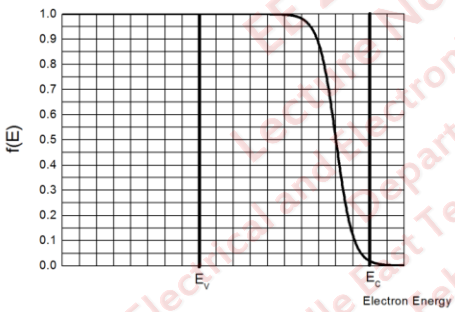
Consider a semiconductor with the following properties at 300 K:

Temperature independent bandgap of E_g= 1 eV,

Donor Doping Density=$1x10^{15}$ cm^{-3} ,

Acceptor Doping Density=0 .

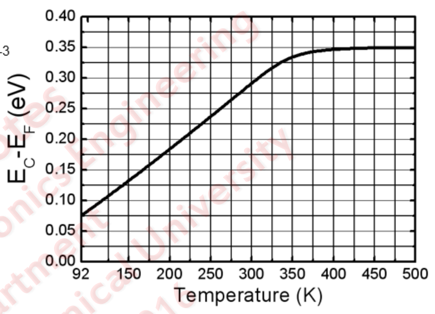
The occupancy probability (f(E)) in this semiconductor at 300 K is shown below.



Find the intrinsic carrier concentration of this semiconductor at **320 K**.

Homework 1

- E_C-E_F versus T (in the range 92-500 K) is shown below for a doped semiconductor with
  . temperature independent bandgap energy
  . E_F=E_i in intrinsic material
  . only one type of impurity at a density of $1x10^{14}$ cm^{-3}
  . complete ionization of impurities for T> 90 K.

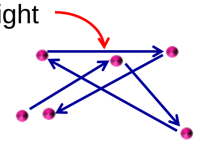


i) Find the energy bandgap of the semiconductor by explaining your reasoning.
ii) Is the material n- or p-type doped? Briefly explain your reasoning.
iii) E_C-E_F = 237 meV at 250 K. Use this data to find the intrinsic carrier concentration of the semiconductor at 250 K.
iv) Use your answer to part (iii) to find the electron concentration in the semiconductor at 400 K.

Carrier Transport-Drift

Ref. 2: 3.1

Motion of a single electron in the absence of Electric Field is shown below.



Electron is scattered at the end of each free flight. The scattering may be due to the disturbance by the impurities,defects, lattice vibrations etc.

The instantaneous velocity of the electron is not zero (even when E-field=0) and the motion arises from the nonzero thermal energy of the electron. **This motion is random**.

Q: What is the average velocity of an electron with thermal motion if you follow its trajectory in momentum space for a sufficiently large duration, Δt?

S:

Carrier Transport-Drift

Ref. 2: 3.1

Q: What is the average velocity of a very large number of electrons with thermal motion at any instant, t ?

S:

Q: What is the current, I ?

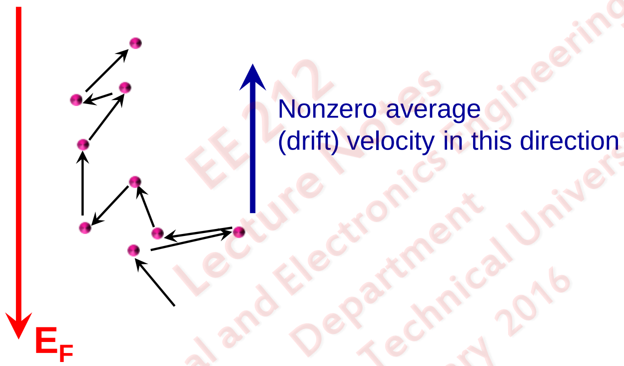
S:

Carrier Transport-Drift

Ref. 2: 3.1

Q: How do the electrons move in the presence of an E-field?

S:



Drift motion due to the Electric Field is superimposed on the random thermal motion.

Drift: motion of the charge carriers under the force of Electric Field.

The resulting current is called **drift current**.

Carrier Transport-Drift

Ref. 2: 3.1

Q: How do I describe the current resulting from this complicated motion of the electrons?

S: It is not too difficult (at least under steady-state conditions).

We will be interested only in the average (drift) velocity in response to an E-field which establishes the current flowing through material.

Note that the thermal motion (due to random nature) will have no effect on the current. If we know the average (drift) velocity (v_d) of the electrons under an applied E-field:

electron drift velocity(cm/sec)

Electron drift current density $\rightarrow$ $$J_n = -\underbrace{qn}_{\text{charge density (C/cm}^3\text{)}} v_{dn}$$

(A/cm²)=C/(sec-cm²)

Similarly,

hole drift velocity(cm/sec)

Hole drift current density $\longrightarrow$ $J_p = qpv_{dp}$

Q: How do I establish the relation between the drift current density and E-field (E)?

S: The electron and hole drift velocities can be expressed as

$\mathbf{v_{dn}=-\mu_n E}$ and $\mathbf{v_{dp}=\mu_p E}$ under low enough E-fields.

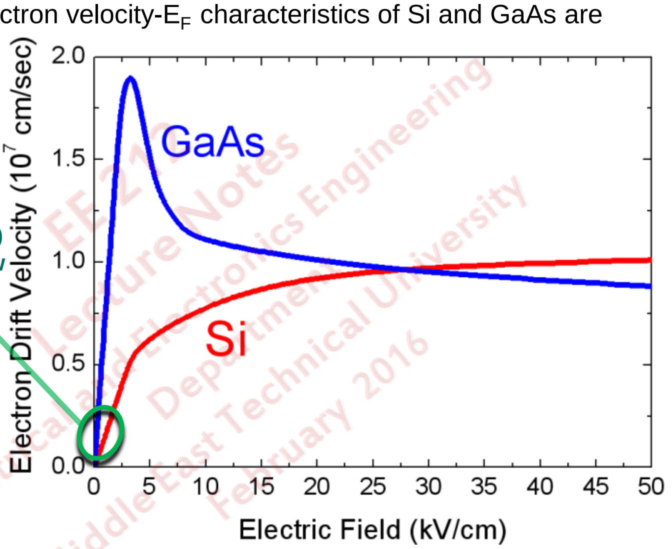
μ_n: electron mobility ($cm^2/V\text{-}sec$)

μ_p: hole mobility ($cm^2/V\text{-}sec$)

Under high fields above relations lose validity, and the drift velocity does not depend linearly on the E-field.

The steady-state electron velocity-E_F characteristics of Si and GaAs are shown below.

v=μE approximation (with constant mobility) is acceptable under low E-fields.



Electron mobility in GaAs is larger than that in Si resulting in higher speed of operation (GaAs devices may operate under higher frequencies).

Carrier Transport-Drift

Ref. 2: 3.1

Mobility is a material dependent parameter determined by the combined effects of various scattering mechanisms in the material.

If the carrier motion is frequently disturbed by scattering mechanisms, this results in a low carrier mobility meaning that the carriers can not acquire large drift velocities under E-field.

Typically, electron mobility is larger than the hole mobility.

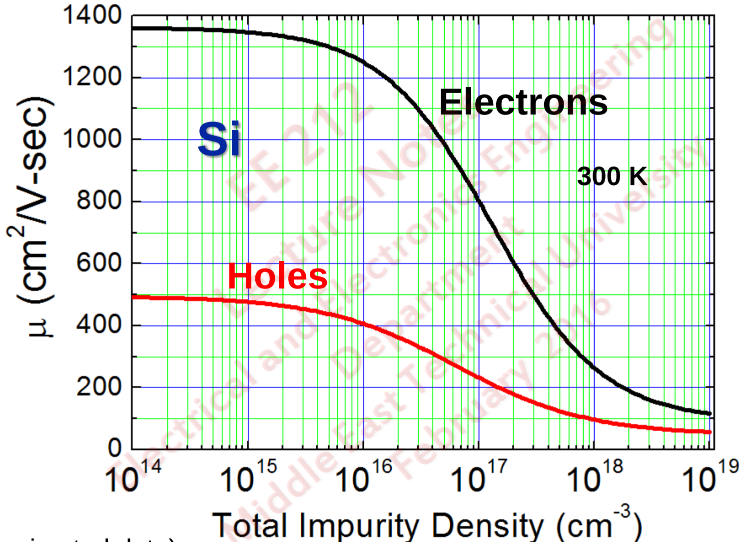
Q: Write the expressions for the electron and hole drift current densities in terms of carrier mobilities.

S:
$$J_n = -qnv_{dn} = -qn(-\mu_n E) = qn\mu_n E$$
$$J_p = qpv_{dp} = qp\mu_p E$$

Note that both drift currents are in the direction of the E-field.

Carrier Transport-Drift

Ref. 2: 3.1, Ref. 6: 2.7



(approximated data)

Q: How do I describe the conductivity of a material in terms of mobility?

S: Remember that Ohm's Law relates the current density to E-field by

$$J = \sigma E$$

Then,

$$J = J_n + J_p = q(n\mu_n + p\mu_p)E = \sigma E \Rightarrow \sigma = q(n\mu_n + p\mu_p)$$

Note that conductivity depends on both mobility and carrier (electron and hole) densities.

Q: Write the approximate expression for the conductivity of an n-type semiconductor in terms of donor doping density ($N_D >> n_i$, $N_A=0$).

S: If $N_D >> n_i$, $n \approx N_D$, $p = n_i^2/n \approx n_i^2/N_D$ << n. Then

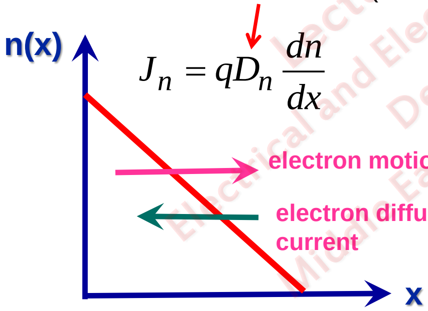
$$\sigma \cong qn\mu_n \cong qN_D\mu_n$$

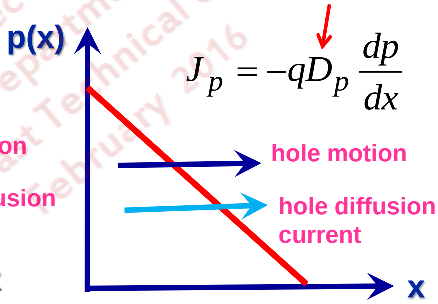
The second basic transport mechanism is diffusion which takes place when there exist carrier density gradients. Electrons and holes (like particles) tend to diffuse from regions of high concentration toward regions of low concentration.

The motion of carriers due to diffusion establish currents called **diffusion currents**.

electron diffusion coefficient (cm²/sec) hole diffusion coefficient (cm²/sec)

$$J_n = qD_n \frac{dn}{dx} \qquad J_p = -qD_p \frac{dp}{dx}$$





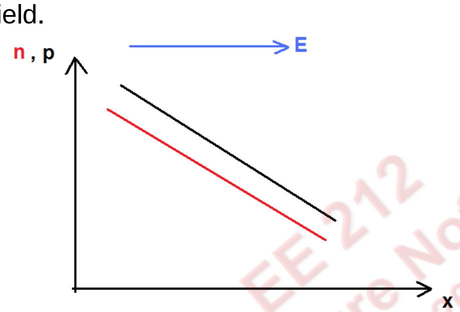
The diffusion coefficient is related to the mobility through the following expression

$$D_n = \frac{kT}{q}\mu_n, \quad D_p = \frac{kT}{q}\mu_p \quad \text{(Einstein Relation)}$$

$$\frac{kT}{q} = V_T\,(thermal\ \ voltage)$$

$$V_T \cong 25\ meV\ \ at\ \ 300\ K$$

Let's consider the following case where we have both carrier density gradients and E-field.



$$\boxed{\begin{aligned} J_{ndrift} &= qnv_{nd} = qn\mu_n E \\ J_{pdrift} &= qpv_{pd} = qp\mu_p E \\ J_{ndiff} &= qD_n\frac{\partial n}{\partial x} \\ J_{pdiff} &= -qD_p\frac{\partial p}{\partial x} \end{aligned}}$$

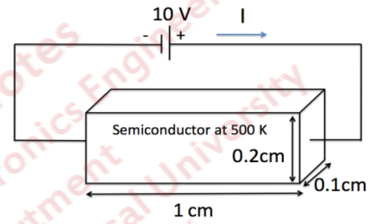
→ e-flow (diffusion)
← e-current (diffusion)
← e-flow (drift)
→ e-current (drift)

→ hole flow (diffusion)
→ hole current (diffusion)
→ hole flow (drift)
→ hole current (drift)

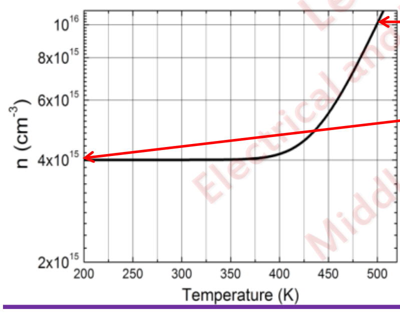
$$\boxed{J_{n_{total}} = q\mu_n nE + qD_n\frac{\partial n}{\partial x}, \quad J_{p_{total}} = q\mu_p pE - qD_p\frac{\partial p}{\partial x}}$$

Exercise Questions

Q.4 The temperature dependence of the electron concentration in a semiconductor (doped with donors only) is given below. A bias voltage is applied to a sample of this semiconductor as shown below. Find the current flowing through the sample at 500 K. The electron and hole mobilities in this semiconductor at 500 K are 3000 and 2000 cm^2/V-sec, respectively.



S.4



n=1x10^{16} cm^{-3}

N_D=4x10^{15} cm^{-3}

$$n + N_A = p + N_D \ (complete\ ionization)$$

$$1x10^{16} + 0 = p + 4x10^{15} cm^{-3} \rightarrow p = 6x10^{15} cm^{-3}$$

$$I = JA = \sigma EA = q(n\mu_n + p\mu_p)\frac{10V}{1cm}0.2x0.1cm^2 = 269mA$$

Exercise Questions

Q.5 (to be solved on white board)

A semiconductor sample is doped with 10^{14} donor atoms/cm^3 and 7x10^{13} acceptor atoms/cm^3. At the temperature of the sample, the resistivity of the intrinsic semiconductor is 60 ohm-cm., the electron mobility is 3800 cm^2/V-sec and the hole mobility is 1800 cm^2/V-sec. Find the total current density through the sample if an electric field of 2 V/cm is applied.

S.5 write

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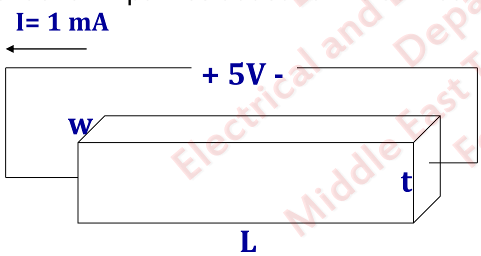
Middle East Technical University, EE 212-Semiconductor Devices and Modeling, Lecture Notes

Exercise Questions

Q.6 (to be solved on white board)

The following bar (at 300 K) is made of an n-type semiconductor doped with donors only. The semiconductor properties are given below.
Electron Mobility = 1250 $cm^2/V\text{-}sec$, E_g(bandgap)=1.43 eV , $n_i=2\times10^6\ cm^{-3}$,
E_C-E_D= 188 meV
The ionized donor concentration in the bar is given as $N_D^+ = \dfrac{N_D}{1+2e^{\frac{E_F-E_D}{kT}}}$

where N_D is the total donor concentration and E_D is the donor level.
Ignore the contribution of holes to conductivity and find the total concentration of donor impurities added to this semiconductor.



T= 300 K,
kT=0.0259 eV
w=10 μm
t= 10 μm
L=100 μm

Exercise Questions

S.6 write

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Exercise Questions

Ref. 1: 4.4.2

Q.7 Show that $\dfrac{D}{\mu}=\dfrac{kT}{q}$

S.7 Under equilibrium $I_{drift}+I_{diffusion}=I_{total}=0$ for both electrons and holes.

$$(qn\mu_n E+qD_n\frac{dn}{dx})A=0\rightarrow E\neq 0 \text{ if } \frac{dn}{dx}\neq 0,$$

$$E=-\frac{D_n}{\mu_n}\frac{1}{n}\frac{dn}{dx},\quad n=n_i e^{\frac{E_F-E_i}{kT}}$$

$$\frac{dn}{dx}=\frac{d}{dx}\left(\frac{E_F-E_i}{kT}\right)n\Rightarrow$$

$$E=-\frac{D_n}{\mu_n}\frac{d}{dx}\left(\frac{E_F-E_i}{kT}\right)=\frac{D_n}{\mu_n}\frac{1}{kT}\frac{dE_i}{dx} \text{ since } \frac{dE_F}{dx}=0 \text{ under equilibrium}$$

$$E=\frac{1}{q}\frac{dE_C}{dx}=\frac{1}{q}\frac{dE_i}{dx} \text{ as we have shown before. Then}$$

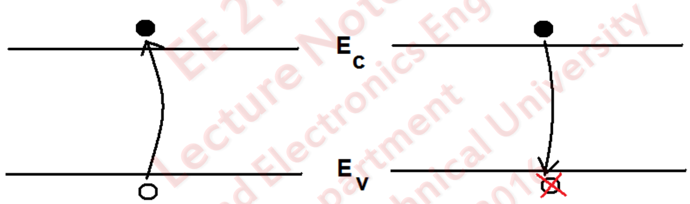
$$E=\frac{1}{q}\frac{dE_i}{dx}=\frac{D_n}{\mu_n}\frac{1}{kT}\frac{dE_i}{dx}\Rightarrow\frac{D_n}{\mu_n}=\frac{kT}{q}$$

Recombination-Generation Processes

Ref. 1: 4.3.1, Ref. 2: 3.3.1

Recombination: a process through which free **carriers** are **lost**

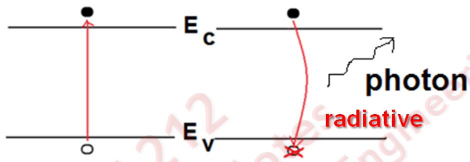
Generation : a process through which free **carriers** are **generated**



Generation
(creation of an electron-hole pair)

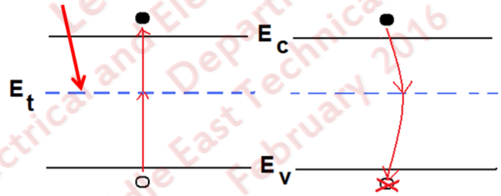
Recombination
(annihilation of an electron-hole pair)

Recombination-Generation Processes Ref. 1: 4.3.1, Ref. 2: 3.3.1



Direct (band to band)
generation and recombination

introduced by impurities and/or defects



Indirect (through state(s) in the bandgap)
generation and recombination

Recombination-Generation Processes Ref. 1: 4.3.1

Thermal Equilibrium-No Excitation

The recombination rate must be equal to the generation rate in order to achieve time independent carrier concentrations.

Since both electrons and holes are needed in a recombination process, recombination rate can be expressed as

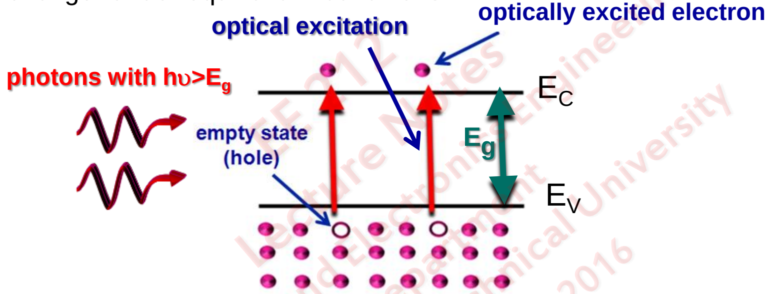
$$r_{eq} = \alpha_r n_o p_o$$

where n_o and p_o stand for the equilibrium carrier densities and α_r is the proportionality (recombination) constant.

Q: Find the thermal generation rate expression at equilibrium.

S: $g_{thermal} = r_{eq} = \alpha_r n_o p_o = \alpha_r n_i^2$

Now let’s illuminate a semiconductor with light having a photon energy larger than the bendgap (E_g). We are now optically exciting the semiconductor and we are no longer under equilibrium conditions.



Interaction of the photons with the valence band electrons create electron hole pairs as a result of electron transitions from the valence to the conduction band.

Since we have optical generation in addition to thermal generation, the electron and hole concentrations are now larger than equilibrium densities.

If we keep the light on, we eventually reach steady state with

$$n = n_o + \delta n, \quad p = p_o + \delta p$$

total electron concentration excess electron concentration

At steady-state we should have time independent carrier concentrations which requires a balance between the recombination and total (thermal + optical) generation rate.

$$\cancel{g_{thermal}} + g_{optical} = \text{total generation rate} = \alpha_r np = \text{recombination rate}$$

$$= \alpha_r (n_o + \delta n)(p_o + \partial p) = \cancel{\alpha_r n_o p_o} + \alpha_r \delta n p_o + \alpha_r n_o \delta_p + \alpha_r \delta_n \delta_p$$

$$g_{optical} = \alpha_r \delta n p_o + \alpha_r n_o \delta_p + \alpha_r \delta_n \delta_p$$

In a semiconductor the carrier with a larger concentration is called majority carrier. The other carrier type is the minority carrier.

Electrons are majority carriers in **n-type** material.
Holes are minority carriers in **n-type** material.
Electrons are minority carriers in **p-type** material.
Holes are majority carriers in **p-type** material.

Recombination-Generation Processes

Ref. 1: 4.3.3

$$g_{optical} = \alpha_r \delta n p_o + \alpha_r n_o \delta_p + \alpha_r \delta_n \delta_p$$

If the optically generated (steady-state) excess carrier concentration is much smaller than the equilibrium majority carrier density, the excitation level is considered to be low. Then,

$$g_{optical} = \alpha_r \delta p (p_o + n_o) + \cancel{\alpha_r \delta_p^2} \quad (\delta_n = \delta_p)$$

ignore if low level excitation, $\delta n << n_o$ in n-type
$\delta p << p_o$ in p-type

$$\delta p = \frac{g_{optical}}{\alpha_r (n_o + p_o)}$$

$$\text{Define} \quad \tau = \frac{1}{\alpha_r (n_o + p_o)} \Rightarrow \delta p = g_{optical} \tau$$

recombination lifetime

steady-state excess carrier concentration with the light on

Recombination-Generation Processes

Q: A semiconductor sample (N_D=10^{16} cm^{-3}, n_i=2x10^6 cm^{-3}, τ=1x10^{-6} sec) is illuminated continuously (and uniformly) with g_{op}=10^{16} EHP/(cm^3-sec). Find the electron and hole densities in the sample under illumination.

S:

$$Since\ N_D >> n_i,\ n_o \cong N_D$$

$$\delta n = \delta p = g_{op} \tau = 10^{16} EHP/(cm^3 - \sec) x 10^{-6} \sec = 10^{10} cm^{-3}$$

$$Note\ that\ \delta n = \delta p << n_o\ as\ required\ by\ the\ low\ level\ excitation\ condition.$$

$$n = n_o + \delta_n \cong n_o = 1x10^{16}\ cm^{-3}$$

$$p = p_o + \delta_p = \frac{n_i^2}{n_o} + \delta p = 4x10^{-4} + 10^{10} \cong 1x10^{10}\ cm^{-3}$$

Note that low level excitation does not considerably change the majority carrier density, however the change in the minority carrier concentration is huge.

Q: A p-type semiconductor sample is continously illuminated with light (low level excitation) and the light is turned off at t=0. Find the expression for the excess electron density, δ_n (t) for t>0.

S:

- rate at which n is changed = generation rate -recombination rate
- It takes some time to reach the steady-state. During this time interval, n and p are time dependent.
- recombination rate = $\alpha_r n(t)p(t)$
- generation rate = $\alpha_r n_0 p_0 = \alpha_r n_i^2$

Then

$$\frac{dn}{dt} = \alpha_r n_i^2 - \alpha_r n(t)p(t)$$

$$n(t) = n_0 + \delta n(t)$$

$$p(t) = p_0 + \delta p(t)$$

Electrons and holes are annihilated in pairs. Thus,

$$\delta n(t) = \delta p(t)$$

$$\frac{dn}{dt} = \frac{d}{dt}(\delta n) = \alpha_r n_i^2 - \alpha_r \left(n_0 + \delta n(t)\right)\left(p_0 + \delta p(t)\right)$$

$$= \alpha_r \cancel{n_i^2} - \cancel{\alpha_r} n_0 p_0 - \alpha_r (n_0 + p_0)\delta n(t) - \cancel{\delta n^2}$$

$$\frac{d}{dt}(\delta n) = \alpha_r (n_0 + p_0)\delta n(t)$$

$$\delta n(t) = \delta n(0) e^{-\alpha_r (n_0 + p_0)t}$$

$$\tau_n = \frac{1}{\alpha_r (n_0 + p_0)}$$

$$\boxed{\delta n(t) = \Delta n e^{-t/\tau_n}}$$

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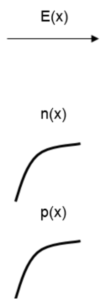
Homework 2 (Estimated Time To Complete < 100 min.)

Q.1

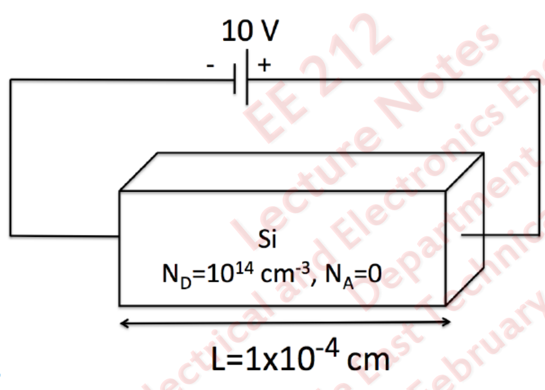
Circle the correct directions of the electron and hole flow directions and currents in the presence of an electric field and concentration gradients as shown below.



- Hole Flow(diffusion) ...... → ←
- Hole Flow (drift) ...... → ←
- Hole Current(diffusion) ... → ←
- Hole Current (drift) .... → ←
- Electron Flow (diffusion)... → ←
- Electron Flow (drift) .... → ←
- Electron Current (diffusion) → ←
- Electron Current (drift) ..... → ←

Q.2 Homework 2

Find the current density flowing through the following Si bar at 300 K.



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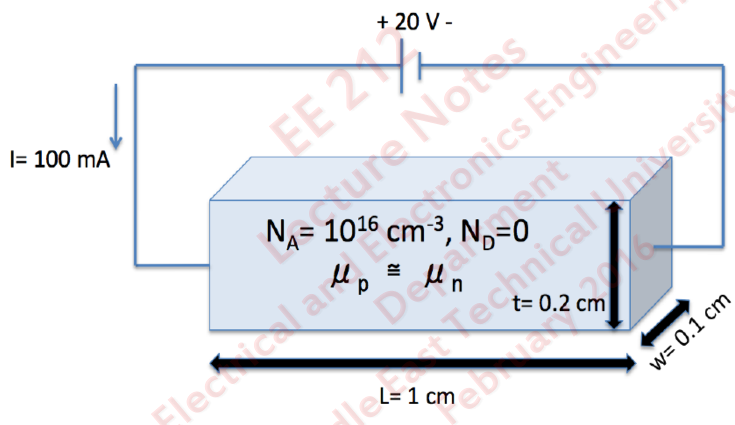
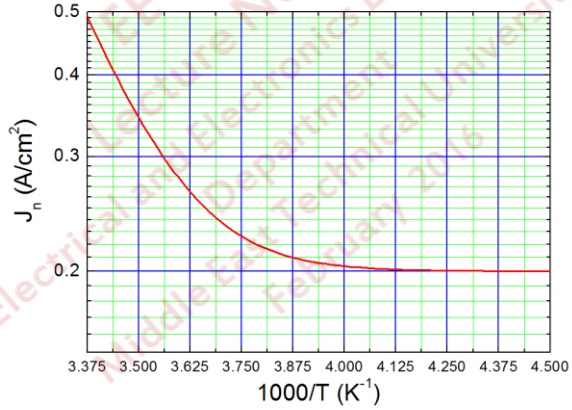
Q.3 Homework 2

Estimate the hole mobility in the following semiconductor sample. n_i=1x10^9 cm^{-3}, q=1.6x10^{-19} C



Q.4 Homework 2

Consider the following figure showing the electron drift current density under an E-field of 100 V/cm in an n-type semiconductor (N_A=0) versus 1000/T where T is the temperature. The electron mobility in the semiconductor is equal to 1250 cm^2/V-sec and it is independent of temperature in the temperature range 220-300 K. The energy bandgap is also independent of temperature in this range. Find the energy bandgap of this semiconductor as precisely as possible.



Hint: Note that J_n=0.49 A/cm^2 at T=296 K and J_n=0.3 A/cm^2 at T=281 K

Q.5 Homework 2

Circle the correct answer.

- Which of the following statements is/are **correct** for a semiconductor in equilibrium?
  i) the recombination rate depends on temperature
  ii) the minority carrier recombination lifetime depends on majority carrier density
  iii) the minority carrier concentration decreases with increasing temperature
  a) ii and iii b) all of them c) only ii d) i and ii e) i and iii

- Which of the following statements is/are **correct**, if an n-type semiconductor with N_D>>n_i is exposed to low level optical excitation with photon energy larger than the energy bandgap?
  i) the product of the electron and hole concentrations will not change
  ii) the intrinsic carrier concentration will increase
  iii) the minority carrier concentration will significantly change
  a) ii and iii b) all of them c) only iii d) i and ii e) i and iii

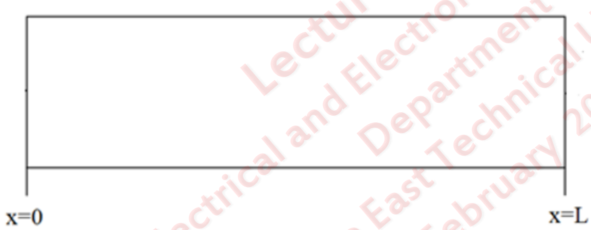
- Which of the following statements is/are **correct** for an n-type Si sample?
  i) drift current is directly proportional to electric field under very large electric field
  ii) drift current is directly proportional to the carrier concentration
  iii) the equilibrium hole concentration depends on the temperature of the sample
  a) ii and iii b) all of them c) only ii d) i and ii e) i and iii

Q.6 Homework 2

The n-type doping density in a Si semiconductor bar (N_A=0, n_i=10^{10} cm^{-3}, T=300 K) is given as

$$N_D = 10^{15}(1-\frac{x}{L}) + 10^{13}\ \mathbf{cm}^{-3}$$

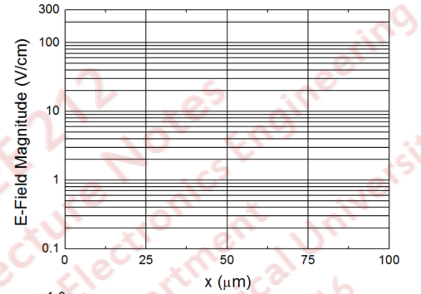
where L=100 μm is the length of the bar with uniform cross sectional area.

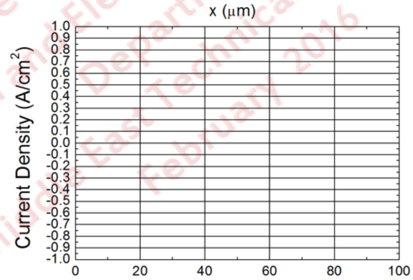


Ignore the dependence of the electron mobility on the doping density and assume complete ionization of impurities.

Q.6 Homework 2

i) Find the expression for the built-in E-field in the bar and plot it by calculating its magnitude at x=0, 25, 50, 75 and 100 μm. Also find and plot the drift and diffusion current densities (J_{drift} and J_{diff}). Note that no bias voltage is applied to the bar.

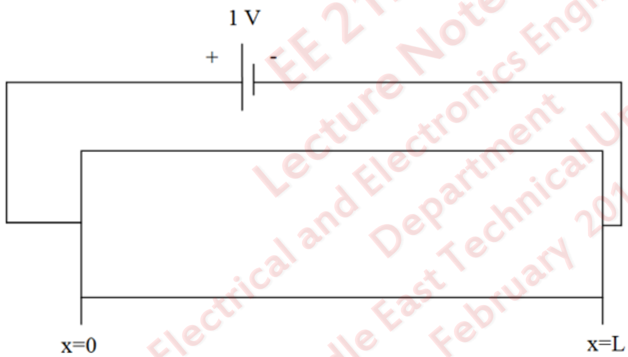




Q.6 Homework 2

ii) Does the E-field depend linearly on x in the above question. Why or Why not? Explain

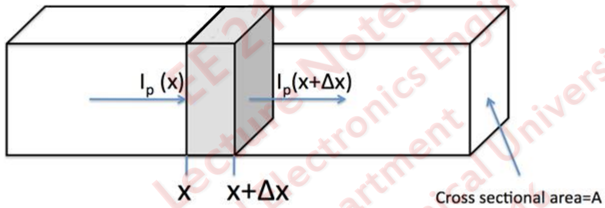
iii) Find the current density flowing through the bar if it is biased as shown below. Show and clearly explain your complete work.



Continuity Equation

Ref. 1: 4.4.3

Consider the highlighted volume in the following n-type semiconductor bar. The hole generation rate is equal to the hole recombination rate in this volume. Find the rate of change of hole density in the volume.



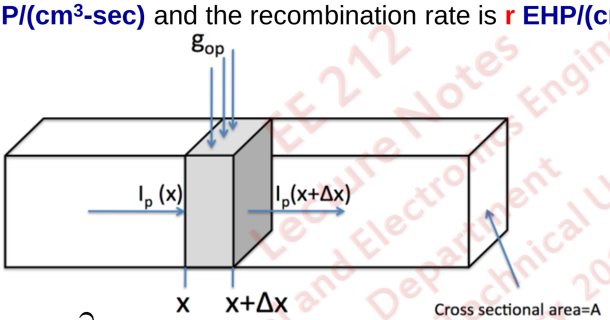
$$\underbrace{q\underbrace{A\Delta x}_{\text{volume}}\frac{\partial p}{\partial t}}_{\text{rate of hole charge build up in the volume}} = I_p(x) - I_p(x+\Delta x) \Rightarrow \frac{\partial p}{\partial t} = \frac{1}{qA\Delta x}\left[I_p(x) - I_p(x+\Delta x)\right]$$

$I_p(x)$=q x number of holes entering/unit time

$I_p(x+\Delta x)$=q x number of holes leaving/unit time

Continuity Equation

Now, consider the highlighted volume in the following n-type semiconductor bar. This volume is optically excited (low level) with a rate of g_{op} **EHP/(cm^3-sec)**. The thermal generation rate of electron hole pairs in this volume is g_T **EHP/(cm^3-sec)** and the recombination rate is **r** **EHP/(cm^3-sec)**.



$$\underbrace{q\underbrace{A\Delta x}_{\text{volume}}\frac{\partial p}{\partial t}}_{\text{rate of hole charge build up in the volume}} = \underbrace{I_p(x) - I_p(x+\Delta x)}_{\substack{\text{rate of hole charge build up}\\ \text{in the volume due to the difference}\\ \text{between entering and leaving currents}}} + \underbrace{qA\Delta x(g_{op} + g_T)}_{\substack{\text{rate of hole charge generation}\\ \text{in the volume due to optical}\\ \text{and thermal generation}}} - \overbrace{qA\Delta x r}^{\substack{\text{rate of hole charge loss}\\ \text{in the volume}\\ \text{due to recombination}}}$$

Continuity Equation

$$\frac{\partial p}{\partial t}=\frac{I_p(x)-I_p(x+\Delta x)}{qA\Delta x}+(g_{op}+g_T-r) \;\Rightarrow\; \frac{\partial p}{\partial t}=-\frac{1}{q}\frac{\partial J_p}{\partial x}+g_{op}-(r-g_T)$$

Define r-g_T : net recombination rate (recombination – thermal generation rate)

$$r-g_T=\underbrace{\alpha_r(n_o+\delta n)(p_o+\delta p)}_{r}-\underbrace{\alpha_r n_o p_o}_{g_T}=\alpha_r\delta n p_o+\alpha_r n_o\delta n+\alpha_r\delta n\delta p$$

Under low level excitation,

$$r-g_T=\alpha_r\delta n p_o+\alpha_r n_o\delta p=\alpha_r(n_o+p_o)\delta p=\frac{\delta p}{\tau_p}$$

Then,

$$\frac{\partial p}{\partial t}=-\frac{1}{q}\frac{\partial J_p}{\partial x}-\frac{\delta p}{\tau_p}+g_{op} \text{ under low level excitation.}$$

If there is no optical excitation (g_{op}=0), $\boxed{\frac{\partial p}{\partial t}=-\frac{1}{q}\frac{\partial J_p}{\partial x}-\frac{\delta p}{\tau_p}}$

This equation is known as the **hole continuity equation**.

Continuity Equation

Ref. 1: 4.4.3, Ref. 2: 3.4.1

A similar derivation for electrons yields

$$\boxed{\frac{\partial n}{\partial t}=\frac{1}{q}\frac{\partial J_n}{\partial x}-\frac{\delta n}{\tau_n}}$$

which is the **electron continuity equation**.

Remember that

$$n(t)=n_0+\delta n(t)$$
$$p(t)=p_0+\delta p(t)$$

Equilibrium carrier concentrations are time independent. Then

$$\frac{\partial \delta p}{\partial t}=-\frac{1}{q}\frac{\partial J_p}{\partial x}-\frac{\delta p}{\tau_p} \qquad \frac{\partial \delta n}{\partial t}=\frac{1}{q}\frac{\partial J_n}{\partial x}-\frac{\delta n}{\tau_n}$$

Diffusion Equation

Ref. 1: 4.4.3, Ref. 2: 3.4.2

Remember that

$$\boxed{J_{n_{total}} = q\mu_n nE + qD_n \frac{\partial n}{\partial x}, \quad J_{p_{total}} = q\mu_p pE - qD_p \frac{\partial p}{\partial x}}$$

If E=0 (zero E-field),

$$\boxed{J_{n_{total}} = qD_n \frac{\partial n}{\partial x}, \quad J_{p_{total}} = -qD_p \frac{\partial p}{\partial x}}$$

If the above equations are inserted into the continuity equations to represent J_n and J_p,

$$\boxed{\frac{\partial(\delta p)}{\partial t} = D_p \frac{\partial^2 \delta p}{\partial x^2} - \frac{\delta p}{\tau_p}} \quad \boxed{\frac{\partial(\delta n)}{\partial t} = D_n \frac{\partial^2 \delta n}{\partial x^2} - \frac{\delta n}{\tau_n}}$$

The above equations are known as hole and electron **diffusion equations** since they are applicable under zero E-field (no drift, diffusion only).

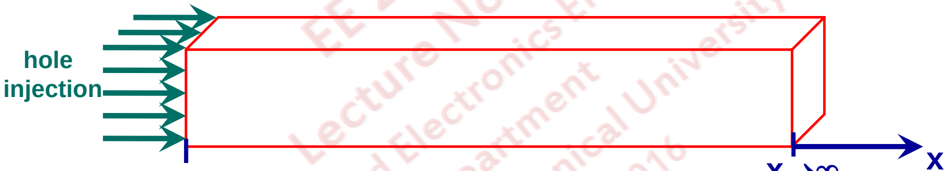
Exercise Questions

Q.8 (to be solved on white board)

Consider a uniformly donor doped silicon sample in **equilibrium** . This sample is uniformly illuminated for t ≥ 0 (low level excitation). Find the expression for the excess hole concentration, $\delta_p(t)$, in the sample for t>0 in terms of hole recombination lifetime, τ_p, optical generation rate, g_{op}, and the other necessary parameters.

S.8 write

Q.9 (to be solved on white board)
Excess holes are continuously injected into a semi-infinite n-type semiconductor bar at x=0. E=0 inside the bar. Excess hole concentration (δp) at the injection point (x=0) is Δp. Find the expression for the steady-state excess hole concentration throughout the bar in terms of Δp, hole diffusion coefficient, D_p, and hole recombination lifetime, τ_p. Plot $\delta p(x)$. Assume low level injection.



S.9 write

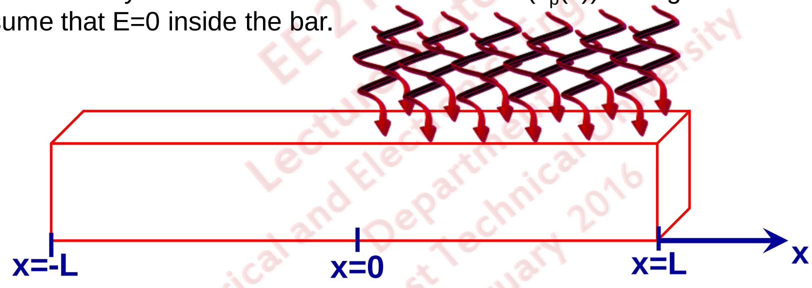
S.9 continued write

Exercise Questions

Ref. 2

Q.10 (to be solved on white board)

Consider an n-type semiconductor bar with $N_D=10^{16}$ cm^{-3}, $\mu_p=500$ cm^2/V-sec and very large L. Hole recombination lifetime (τ_p) in the bar is 10^{-7} sec. Half of this bar (x>0) is illuminated with $g_{op}= 10^{20}$ EHP/(cm^{3}-sec) as shown below. Find and plot the steady-state excess hole concentration ($\delta_p(x)$) throughout the bar. Assume that E=0 inside the bar.



Exercise Questions

S.10 write

Q.1 Homework 3 (Estimated Time To Complete < 120 min.)

The following differential equation governs the behavior of the free electron concentration (n_p) in a p-type material, assuming possible optical excitation:

$$\frac{\partial \delta n_p}{\partial t} = D_N \frac{\partial^2 \delta n_p}{\partial x^2} - \frac{\delta n_p}{\tau_n} + g_{op}$$

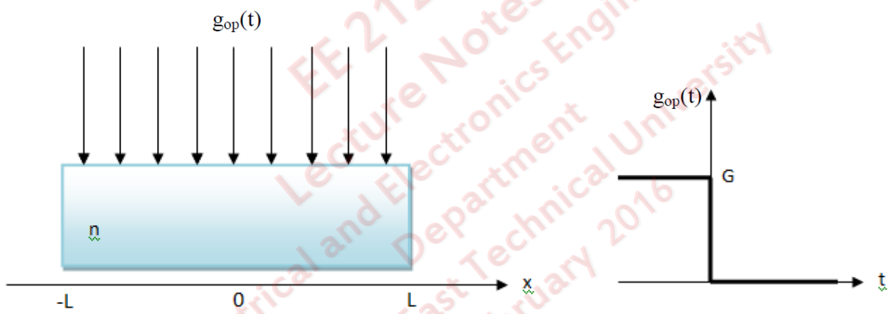
where D_N is the diffusion constant of electrons and g_{op} is the optical generation rate (electrons/cm^3.s). Write different forms and solutions of this equation for the following special cases (You may assume general boundary conditions).

a) Steady state, no light
b) Uniform illumination is turned off at t=0, find equation and solution for t > 0 (no concentration gradient, no light for t>0)
c) Uniform steady-state illumination (no concentration gradient)

Q.2 Homework 3

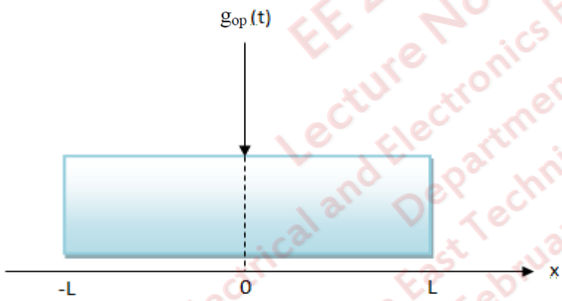
Consider a uniformly doped n-type semiconductor bar.

(a) The bar is uniformly illuminated by $g_{op}(t)$. Find and sketch the excess minority carrier concentration as a function of time. Assume low-level injection and zero electric field inside the bar.



Q.2 Homework 3

(b) The illumination produces a constant excess-carrier generation rate g_{op} at x=0 so that an excess hole density of Δp is maintained at that point. Find and sketch the excess minority carrier concentration as a function of x. Assume that the minority carrier life time is infinite, and assume the excess minority carrier concentration is zero at x=-L and x=L.



Q.3 Homework 3

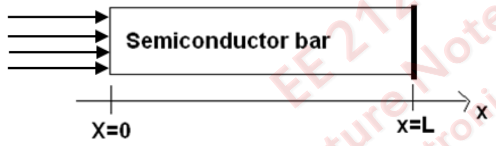
Consider a uniformly donor doped silicon sample in **equilibrium** at 300°K. This sample is uniformly illuminated, continuously in time starting at t=0. Assume that $N_D=10^{15}$ /cm^3, $\tau_p=10^{-5}$ sec and the optical generation rate, $g_{op}=10^{14}$ EHP /cm^3 per second.

i) Starting from the balance between the generation and recombination rates, derive the expression for the **steady state** excess hole concentration, δp, in terms of optical generation rate and recombination lifetime. Indicate all your assumptions.

ii) Use the continuity equation to derive the expression for $\delta p(t)$ for t>0 under continuous illumination (light **is not** turned off) and sketch $\delta p(t)$ versus time.

Q.4 Homework 3

Assume that the following n-type semiconductor bar is continuously illuminated from one side as shown below. L is much smaller than the hole diffusion length in the bar. There is an ohmic contact at x=L where the excess minority carrier concentration is zero. The excess hole concentration at x=0 is Δp and the excitation level is low.



Assume that the E-field in the bar is negligibly small. Start from the continuity equation and derive the expression for the average time required for an excess hole created at x=0 to reach the boundary at x=L in terms of hole diffusion coefficient and other necessary parameters.

Q.5 Homework 3

A hole current of 10^{-4}A/cm^2 is **continuously** injected into the side (x=0) of a long n-type Si bar . Assume that the holes flow only by diffusion, and that at very large values of x, the density of excess holes decays to zero.

Given : $\mu_p = 400\text{cm}^2/\text{V}-\text{s}$; $\mu_n = 1600\text{cm}^2/\text{V}-\text{s}$; $\tau_p = 25\text{x}10^{-6}\text{s}$.

i) Determine the steady-state excess hole density at x=0.
ii) If the bar has $N_D=10^{15}$ cm^{-3}, determine the rates of generation and recombination of electron-hole pairs at x=100 μm.

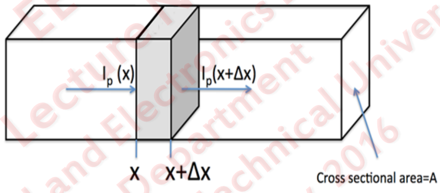
Q.6 Homework 3

Circle the correct answer.

- What does the $\delta p/\tau_p$ term represent in the hole continuity equation?
  a) recombination rate – (thermal+optical) generation rate
  b) recombination rate – thermal generation rate
  c) $\alpha_r np$
  d) recombination life time
  e) none of the above

- If the recombination rate is equal to thermal generation rate, $I_p(x+\Delta x)-I_p(x)$ in the following figure is

  a) $-q\dfrac{1}{A\Delta x}\dfrac{\partial p}{\partial t}$
  b) $q\dfrac{1}{A\Delta x}\dfrac{\delta p}{\partial t}$
  c) $q\dfrac{1}{A\Delta x}\dfrac{\partial p}{\partial t}$
  d) $-qA\Delta x\dfrac{\partial p}{\partial t}$
  e) none of the above



- If the excess hole concentration in an n-type semiconductor under illumination is expressed as $g_{op}\tau_p$, then the semiconductor is
  i) at steady-state
  ii) under low level optical excitation
  iii) exposed to light with photon energy smaller than the band gap energy
  a) ii and iii b) all of them c) only i d) only ii e) i and ii

Q.7 Homework 3

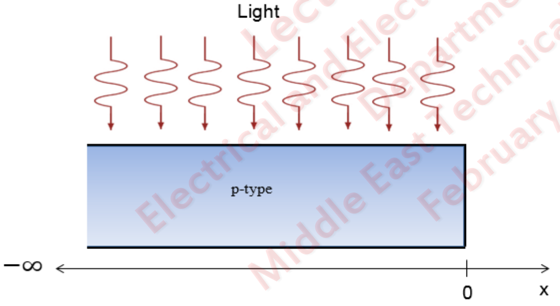
Two experiments are conducted on a uniformly doped, semi-infinite p-type bar. In the first experiment, the bar is uniformly illuminated as shown in the following figure. When the excess carrier concentration reaches its steady-state value, the light is turned off and the excess free electron density decays as follows:

$$\delta n(t) = 10^{10} e^{-t/10^{-6}}\ cm^{-3}$$

where *t* is in seconds.

In another experiment, the semiconductor bar is again uniformly illuminated with the same optical generation rate, but for this case, carriers are simultaneously extracted at $x = 0$ making $\delta n(x = 0) = 0$.

Determine the steady-state excess free electron concentration $\delta n(x)$ for $x < 0$. You may assume 1) low-level injection condition, and 2) negligible electric field inside the bar.



T = 300 K
μ_n =1500 cm^2/V.sec

CHAPTER II

p-n Junction Diodes

References

1) B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th Edition, Prentice Hall, 2006.

2) J. Singh, *Semiconductor Devices An Introduction*, McGraw-Hill, 1994.

3) R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.

4) M. Shur, *Introduction to Electronic Devices*, John Wiley, 1996.

5) R. C. Jaeger and T. N. Blalock, Microelectronic Circuit Design, Mc Graw Hill, 2nd Edition, 2004 .

p-n Junction Diodes

The Role of This Chapter

- Semiconductor devices (such as transistors) performing different functions in electronic circuits include p-n junctions in their internal structures. p-n junction is one of the most important building parts utilized in the construction of these devices.

- You should be familiar (through an earlier course) with the utilization of a p-n junction diode in simple circuits. While the p-n junction by itself is able to perform some important functions in electronics and optoelectronics such as rectification, waveform shaping, radiation detection and light emission, it allows the configuration of devices with more complicated structures to implement important signal processing functions.

- Due to the above reasons, the characteristics of important semiconductor devices can not be understood even at an introductory level without an understanding of the principles of p-n junction operation. The main objective of this chapter is to provide this primary background in order to form the basis for our discussions in the following chapters on transistors.

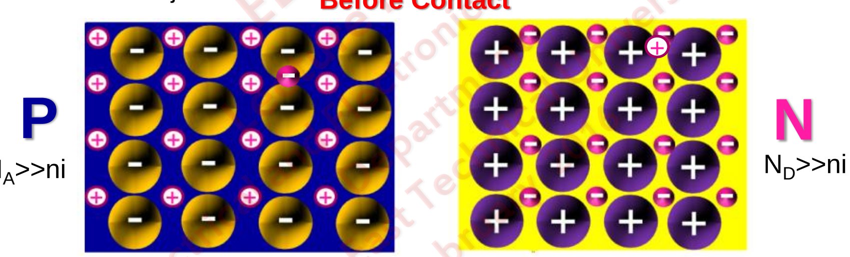
It is a must to comprehend the material in this chapter in order to be able to follow the discussions in the subsequent chapters.

p-n Junction Diodes-Junction Formation

Ref. 1: 5.2.1

When a p type semiconductor is brought into contact with an n-type semiconductor, large electron and hole density gradients arise since the hole concentration in the p-side is much larger than that in the n-side, and the electron concentration in the n-side is much larger than that in the p-side. Carrier concentration gradients call for diffusion of carriers (holes start to diffuse from the p to the n-side, and the electrons diffuse from the n to the p-side). Diffusing carriers leave behind the charge of the immobile ionized impurity atoms (donors in the n-side and acceptors in the p-side). The uncompensated charge creates a built-in E-field at the junction.

Before Contact

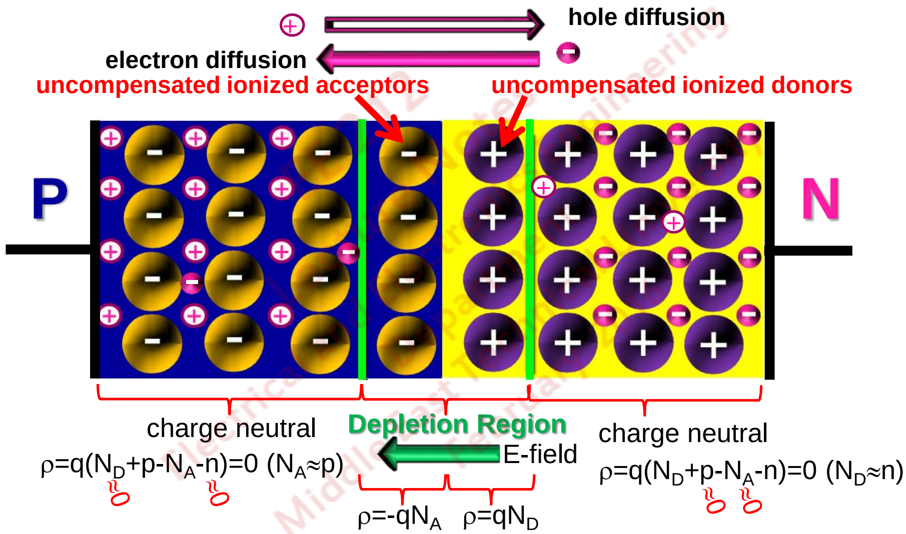


$N_A >> n_i$ $\quad$ $N_D >> n_i$

$\rho = q(\underbrace{N_D}_{\approx 0} + p - N_A - \underbrace{n}_{\approx 0}) = 0 \ (N_A \approx p)$ $\quad$ $\rho = q(N_D + \underbrace{p}_{\approx 0} - N_A - \underbrace{n}_{})$ ...

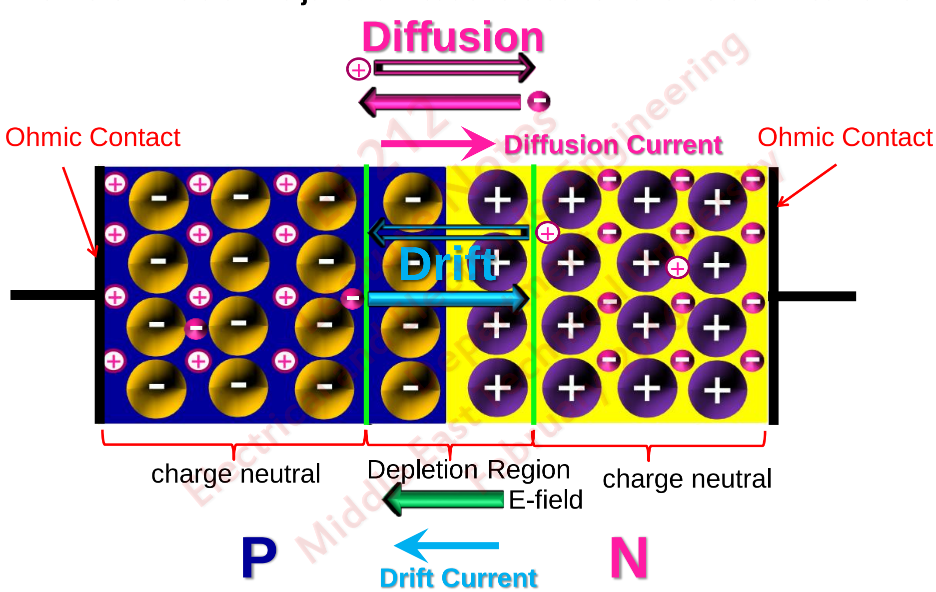
p-n Junction Diode at Equilibrium (no Biasing Voltage)

Creation of the depletion region and built-in E-field

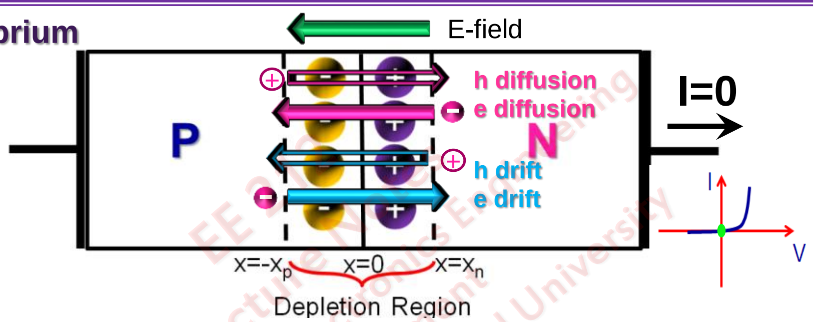


There exists uncompensated (nonzero) charge inside the depletion region resulting in the creation of an E-field at the junction. .

Nonzero E-field at the junction leads to electron and hole drift currents.



Equilibrium



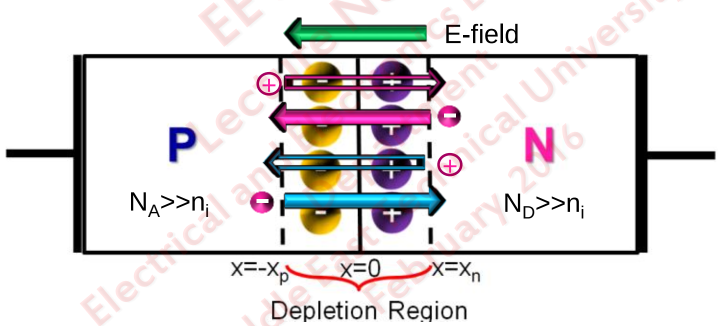
The net current flowing through the junction should be zero under equilibrium conditions.

h diffusion current →
h drift current ←

e diffusion current →
e drift current ←

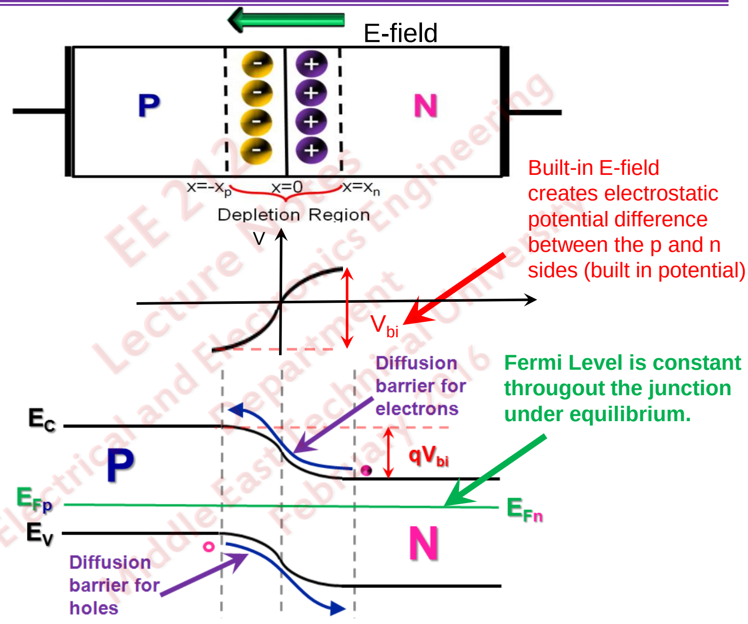
Based on the requirements of equilibrium, the sum of the hole drift and diffusion currents is zero as well as that of the electrons. This results in zero net current flowing through the junction.

In summary, formation of the contact between p and n type materials calls for diffusion currents due to carrier density gradients. However, the diffusion of the carriers from one side to the other also generates drift currents due to a built in E-field created at the juction. Electron and hole diffusion currents are canceled by electron and hole drift currents, and no current flows through the junction under equilibrium (zero bias).

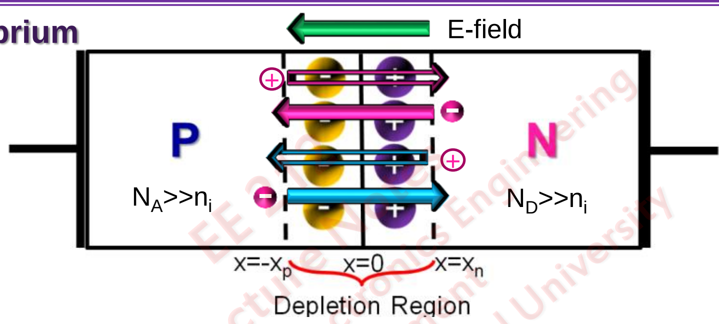


$$I_n = qA(\mu_n nE + D_n \frac{dn}{dx}) = 0 \qquad I_p = qA(\mu_p pE - D_p \frac{dp}{dx}) = 0$$

Equilibrium



Equilibrium



$$I_n = qA(\mu_n nE + D_n \frac{dn}{dx}) = 0 \qquad I_p = qA(\mu_p pE - D_p \frac{dp}{dx}) = 0$$

p_p:equilibrium hole concentration in the p-side≈N_A

n_p:equilibrium electron concentration in the p-side≈n_i^2/N_A

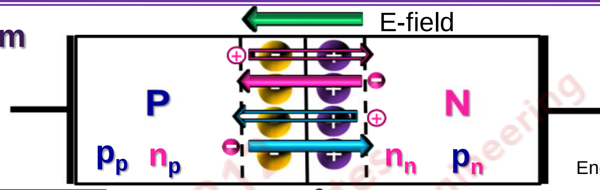
n_n:equilibrium electron concentration in the n-side ≈N_D

p_n:equilibrium hole concentration in the n-side≈ n_i^2/N_D

p-n Junction Diodes-Junction Formation

Ref. 1: 5.2.1, 5.2.2, 5.2.3

Equilibrium



$$\frac{\mu_p kT}{q}$$

$$I_p = q(\mu_p pE - D_p \frac{dp}{dx}) = 0$$

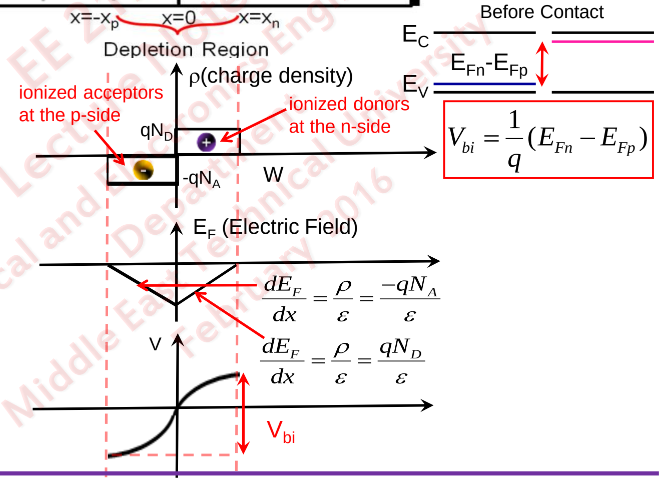
$$= pE - \frac{kT}{q}\frac{dp}{dx} = 0$$

$$E = -\frac{kT}{qp}\frac{dp}{dx} = -\frac{dV}{dx}$$

$$\int_{V_p}^{V_n} dV = -\frac{kT}{q}\int_{p_p}^{p_n}\frac{dp}{p}$$

$$V_n - V_p = V_{bi} = -\frac{kT}{q}\ln(\frac{p_n}{p_p})$$

$$V_{bi} = \frac{kT}{q}\ln(\frac{N_A N_D}{n_i^2})$$



$$\frac{dE_F}{dx} = \frac{\rho}{\varepsilon} = \frac{-qN_A}{\varepsilon}$$

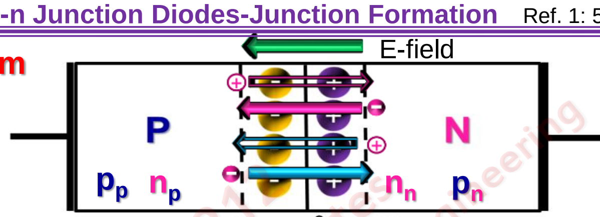
$$\frac{dE_F}{dx} = \frac{\rho}{\varepsilon} = \frac{qN_D}{\varepsilon}$$

$$V_{bi} = \frac{1}{q}(E_{Fn} - E_{Fp})$$

p-n Junction Diodes-Junction Formation

Ref. 1: 5.2.1, 5.2.2, 5.2.3

Equilibrium



$$qAx_n N_D = qAx_p N_A$$

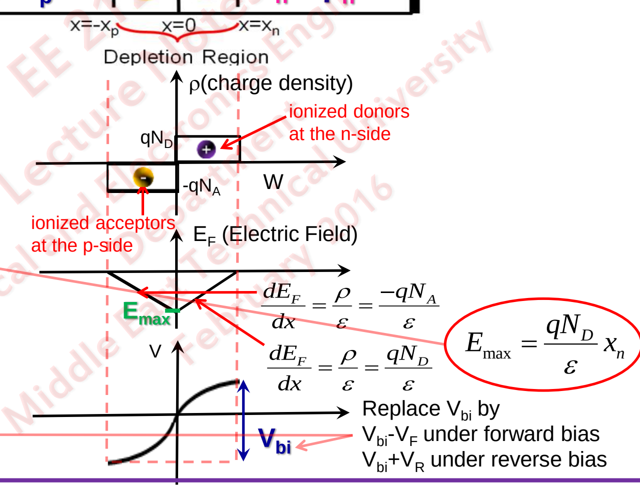
$$W = x_n + x_p = x_n(1 + \frac{N_D}{N_A})$$

$$V_{bi} = -\int_{-x_p}^{x_n} E dx = \frac{1}{2} W E_{\max}$$

$$V_{bi} = \frac{1}{2} W \frac{qN_D}{\varepsilon} x_n$$

$$= \frac{1}{2} W \frac{qN_D}{\varepsilon}\frac{W}{1 + \frac{N_D}{N_A}}$$

$$W = \sqrt{\frac{2\varepsilon}{q}\frac{N_A + N_D}{N_A N_D} V_{bi}}$$



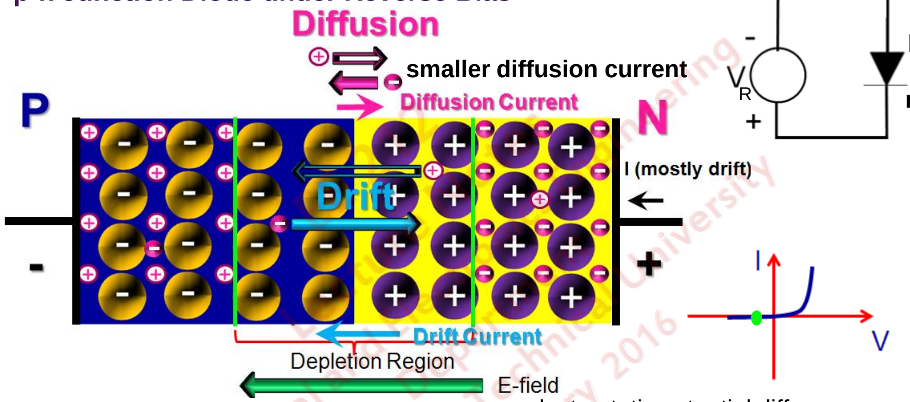
$$\frac{dE_F}{dx} = \frac{\rho}{\varepsilon} = \frac{-qN_A}{\varepsilon}$$

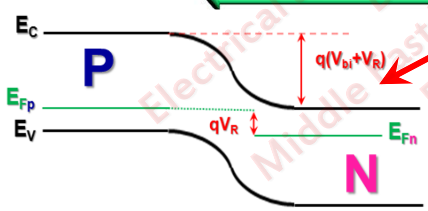
$$\frac{dE_F}{dx} = \frac{\rho}{\varepsilon} = \frac{qN_D}{\varepsilon}$$

$$E_{\max} = \frac{qN_D}{\varepsilon} x_n$$

Replace V_{bi} by
$V_{bi}-V_F$ under forward bias
$V_{bi}+V_R$ under reverse bias

p-n Junction Diode under Reverse Bias

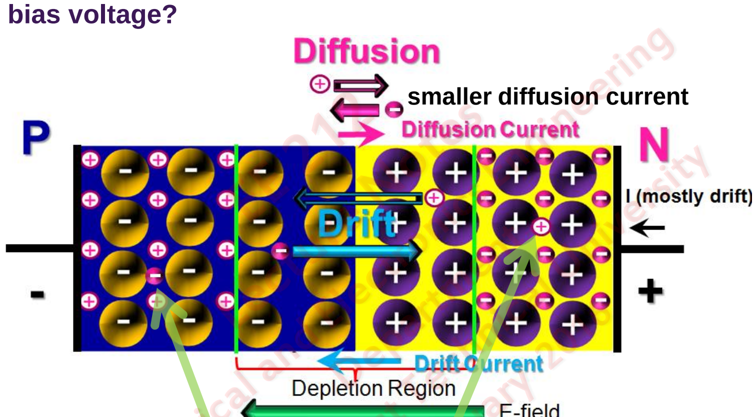




electrostatic potential difference and the diffusion barrier are increased. The balance between drift and diffusion is disturbed.

Due to the larger diffusion barrier, the diffusion current should obviously be smaller than that under equilibrium.

What about the drift current? Does the drift current considerably change with bias voltage?

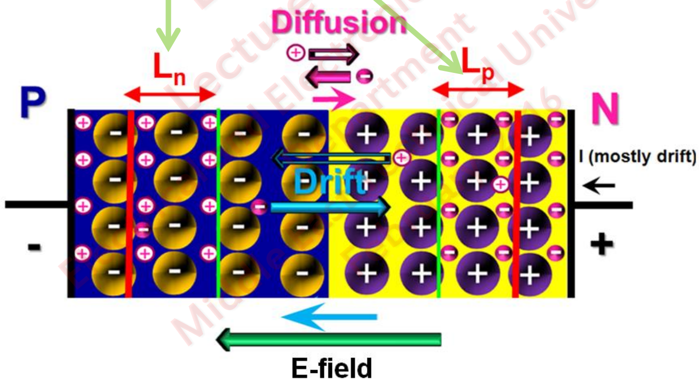


Note that the drift current is generated by the minority carriers entering (or generated at) the depletion region (electrons in the p-side, holes in the n-side). In the absence of optical excitation, these minority carriers are created by thermal generation. The thermal generation rate depends on temperature and the bandgap of the semiconductor. Unless the bandgap of the semiconductor is small, the minority carrier density will be low at room temperature resulting in a very small drift current (as is the case in a Si diode).

p-n Junction Diodes-Operation Modes

Ref. 1: 5.3.1

A minority carrier (electron on the p-side or hole on the n-side) must be created in a volume within a diffusion length from the edge of the depletion region in order to contribute to the drift current. Remember that the diffusion length is defined as the average distance a carrier can diffuse before being annihilated by recombination. Hence, the minority carriers generated outside the above described region can not reach the depletion region (and contribute to drift current) since they are annihilated by recombination.

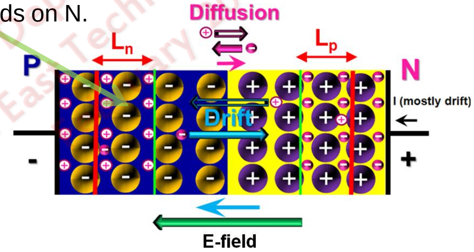


p-n Junction Diodes-Operation Modes

Ref. 1: 5.3.1

Now, let's go back to our question. Does the drift current depend on the bias voltage?

The bias voltage changes the depletion region width and the E-field magnitude inside the depletion region. A larger reverse bias results in a stronger E-field at the junction. One can think that this leads to a larger drift current due to larger minority carrier velocity (if the carrier velocity is not saturated). However, it can be shown that the drift current does not depend on the velocity of the minority carriers as they transit the depletion region since this current is limited by the generation rate of the minority carriers. In order to make this statement more clear, let's suppose that N electrons are generated per second in this volume. If the E-field in the depletion region is large enough (it is) to result in a sufficiently large velocity (even under zero bias), then N electrons/second are collected at the n side independent of the biasing voltage. In other words, the number of the electrons passing to the n side (electron component of the drift current) is limited by the electron generation rate and depends on N.



In summary,

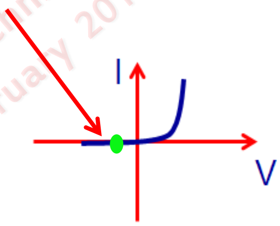
Equilibrium diffusion current= Equilibrium drift current

Reverse bias diffusion current << Equilibrium diffusion current

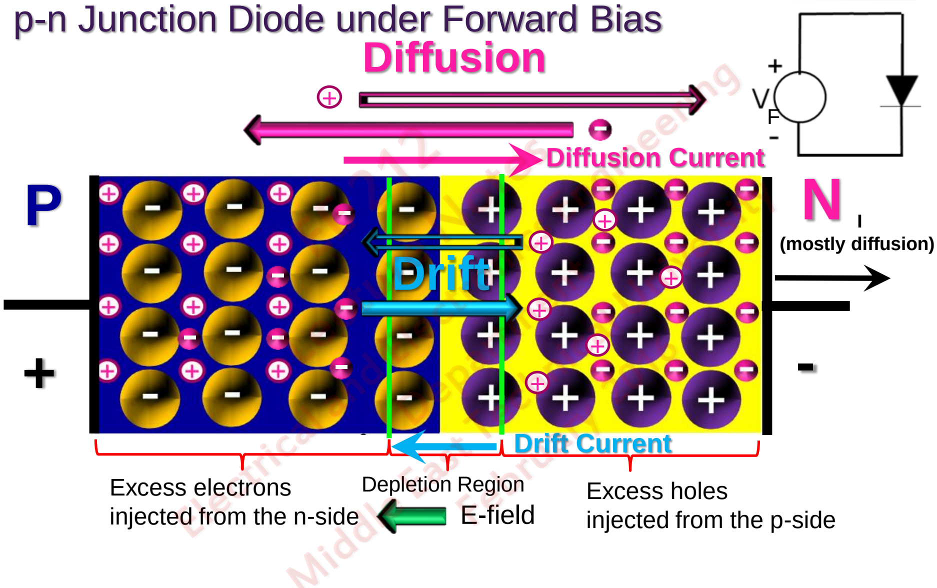
Reverse bias drift current ≈ Equilibrium drift current

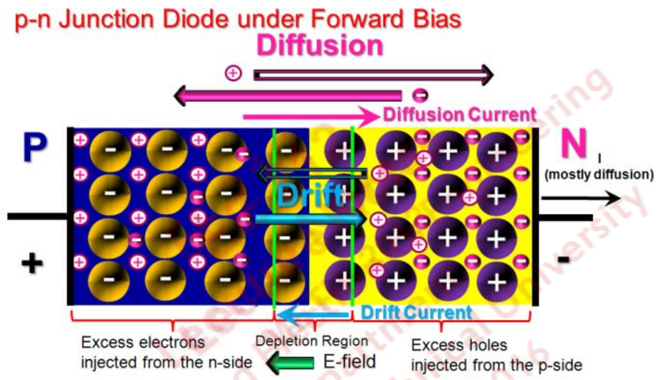
⇒ the current is dominated by drift under reverse bias.

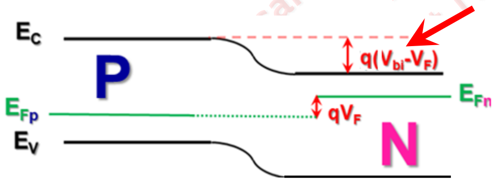
⇒ reverse bias current is bias independent.



p-n Junction Diode under Forward Bias







Electrostatic potential difference and the diffusion barrier are decreased.

Due to the smaller diffusion barrier, the diffusion current should be larger than that under equilibrium.

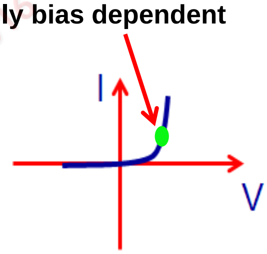
Equilibrium diffusion current= Equilibrium drift current

Forward bias diffusion current >> Equilibrium diffusion current

Forward bias drift current ≈ Equilibrium drift current

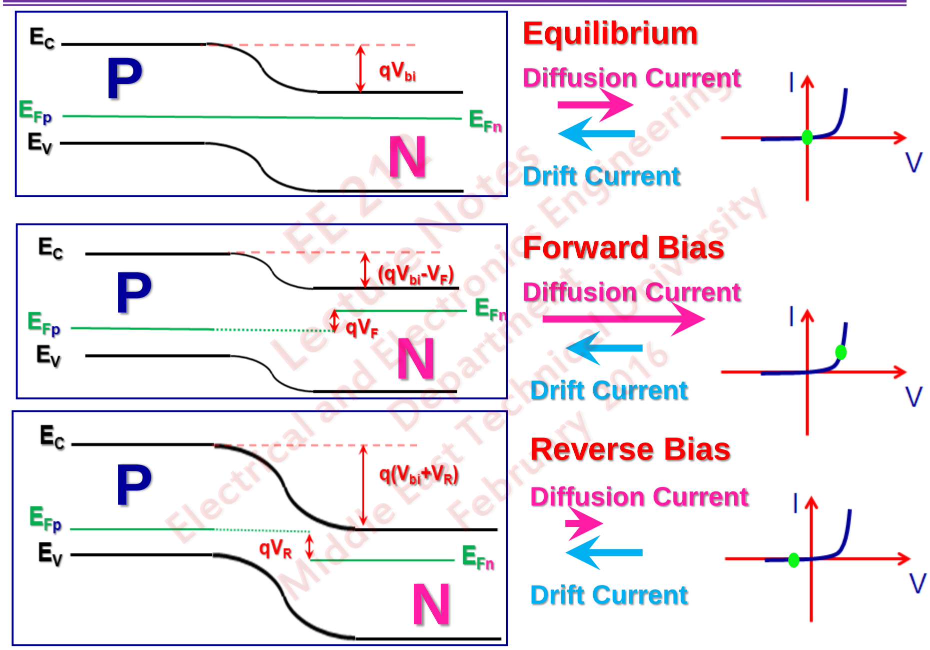
⇒ the current is dominated by diffusion under forward bias.

Since the barrier for diffusion depends strongly on the biasing voltage, forward bias (diffusion) current is strongly bias dependent (increases exponentially with forward bias).



p-n Junction Diodes-Operation Modes

Ref. 1: 5.3.1



p-n Junction Diodes-Exercise Questions

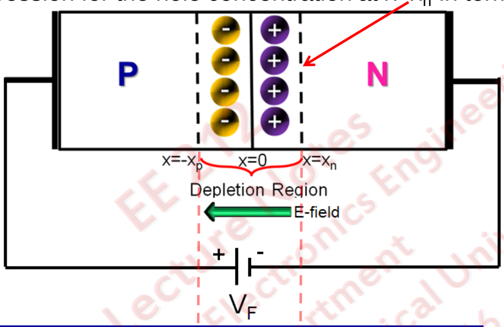
Q.1 (to be solved on white board)

You form a p-n junction between p-type (N_A= 1x10^{16} cm^{-3}) and n-type (N_A= 1x10^{18} cm^{-3}) Si. Calculate the depletion layer width and draw the energy band diagram of the junction in equilibrium. Show and label the Fermi level and the (calculated) junction potential on the diagram.

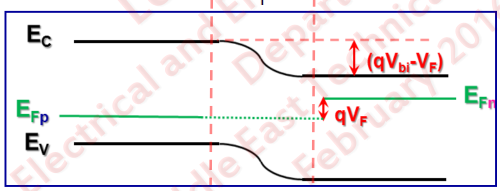
S.1 write

p-n Junction Diodes-Current

Q: Find the expression for the hole concentration at $x=x_n$ in terms of p_n.



S:

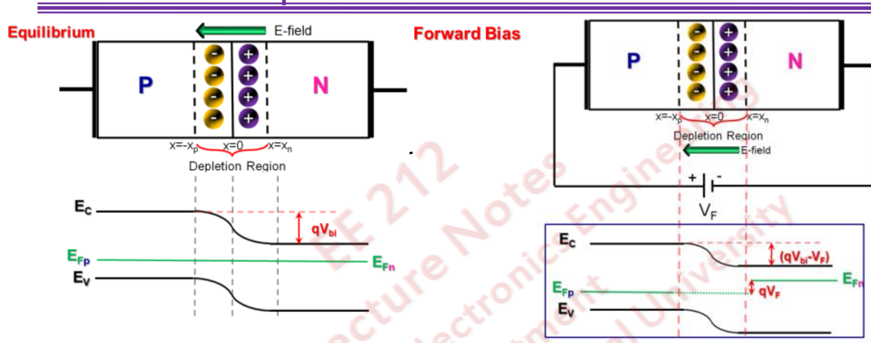


Under equilibrium conditions:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{p_p}{p_n}\right) \text{ or } p_n = p_p e^{-\frac{qV_{Bi}}{kT}} \text{ or } \overset{p_n}{p(x_n)} = \overset{p_p}{p(-x_p)} e^{-\frac{qV_{Bi}}{kT}}$$

p-n Junction Diodes-Current

Ref.1: 5.3.2



Under equilibrium conditions:

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{p_p}{p_n}\right) \text{ or } p_n = p_p e^{-\frac{qV_{Bi}}{kT}} \text{ or } \overset{p_n}{p(x_n)} = \overset{p_p}{p(-x_p)} e^{-\frac{qV_{Bi}}{kT}} \qquad \frac{p(x_n)}{p(-x_p)} = \frac{p_n}{p_p} = e^{-\frac{qV_{Bi}}{kT}}$$

Note that the built-in potential (V_{bi}) arises from the E-field forming at the junction to create drift currents opposing the diffusion currents in order to meet the requirements of equilibrium (I=0). A hole in the p-side has to overcome a potential barrier of qV_{Bi} in order to diffuse to the n-side under equilibrium conditions. This potential barrier will be reduced by qV_F if a forward bias of V_F is applied. Therefore, it is reasonable to assume that $p(x_n)$ will be increased (above the equilibrium value) by a factor of $e^{qV_F/kT}$ with the application of the forward bias, V_F, since the occupancy of an energy state decreases exponentially with increasing energy.

Then under forward bias:

$$\frac{p(x_n)}{p(-x_p)} = e^{-\frac{q(V_{Bi}-V_F)}{kT}} \quad or \; p(x_n) = p(-x_p)e^{-\frac{q(V_{Bi}-V_F)}{kT}} \cong p_p e^{-\frac{q(V_{Bi}-V_F)}{kT}}$$

where we have assumed that the majority carrier concentrations do not considerably change with forward bias (low level injection) such that $p(-x_p)$ is still equal to the equilibrium hole (majority carrier) density in the p-side (p_p). Then, the ratio of the hole concentration at $x=x_n$ to $\mathbf{p_n}$ is expressed as

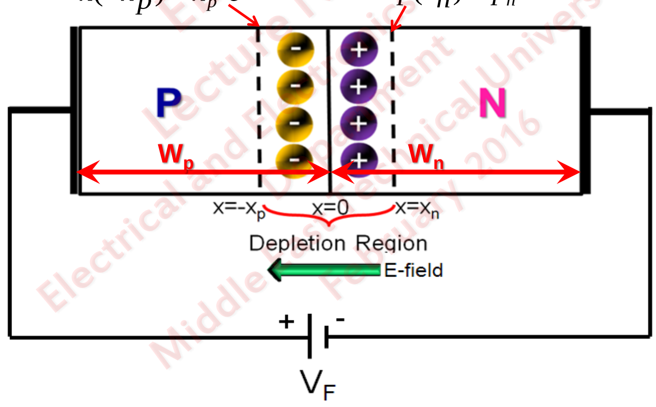
$$\frac{p(x_n)}{p_p}\cdot\frac{p_p}{p_n} = \frac{p(x_n)}{p_n} = e^{-\frac{q(V_{Bi}-V_F)}{kT}} \cdot e^{\frac{qV_{Bi}}{kT}} = e^{\frac{qV_F}{kT}} \quad \text{or} \quad \boxed{p(x_n) = p_n\, e^{\frac{qV_F}{kT}}}$$

Similarly, $\boxed{n(-x_p) = n_p\, e^{\frac{qV_F}{kT}}}$

Q: Find the expressions for the the excess carrier concentrations in the following diode for $x>x_n$ and $x<-x_p$. Assume that

- $W_n>>L_p$ and $W_p>>L_n$ where L_p and L_n are the diffusion lengths of the injected holes and electrons in the n and p sides, respectively,
- the injection level is low enough not to change the majority carrier concentrations,
- Electric Field outside the depletion region is zero.

$n(-x_p) = n_p\, e^{\frac{qV_F}{kT}}$ $\quad$ $p(x_n) = p_n\, e^{\frac{qV_F}{kT}}$



S: Let's first try to guess the distributions of the excess holes in the n-side and the excess electrons in the p-side before starting the quantitative analysis.

Since E-Field is zero outside the depletion region, the injected carriers move by diffusion in the charge neutral regions. The diffusion length is defined as the average distance a (injected or generated) carrier can diffuse before it is annihilated (by recombination).

Since $W_n >> L_p$ and $W_p >> L_n$, the injected excess carriers will not be able to reach the ohmic contacts meaning that $\delta p(W_n)=\delta n(-W_p)=0$. The injected excess carrier densities on both sides decrease with distance between the depletion layer edges and the ohmic contacts.

Do they decrease linearly? I don't think so since a linear decrease in the carrier concentration corresponds to a constant difffusion current. Consider the electron diffusion current in the p-side.

$$\boxed{J_{ndiff} = qD_n \frac{\partial n}{\partial x} = qD_n \frac{\partial \delta n}{\partial x}}$$

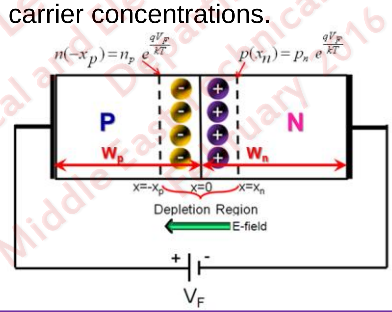
p-n Junction Diodes-Current

Ref.1: 5.3.2

$$\boxed{J_{ndiff} = qD_n \frac{\partial n}{\partial x} = qD_n \frac{\partial \delta n}{\partial x}}$$

A constant electron diffusion current requires zero recombination (and no electron loss) since constant (position independent) electron current means that the number of electrons passing through a location per unit time must be uniform throughout the charge neutral n-side.

Since there exists recombination in the n- and p-sides, diffusion currents must change (decrease) with position which is in conflict with linear decrease in the excess carrier concentrations.



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p-n Junction Diodes-Current

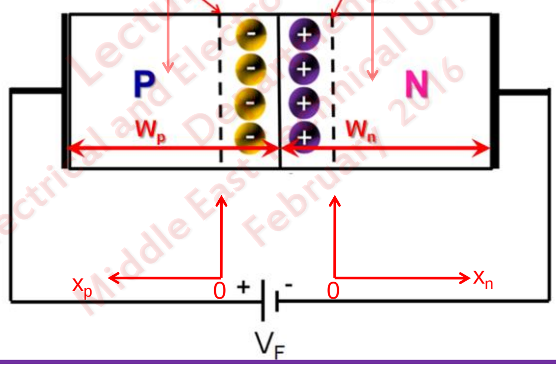
Ref.1: 5.3.2

In order to derive the expression for the excess carrier concentrations in the charge neutral regions (with zero E-field) the diffusion equations must be solved.

$$\boxed{\frac{\partial(\delta n)}{\partial t} = D_n \frac{\partial^2 \delta n}{\partial x^2} - \frac{\delta n}{\tau_n}} \qquad \boxed{\frac{\partial(\delta p)}{\partial t} = D_p \frac{\partial^2 \delta p}{\partial x^2} - \frac{\delta p}{\tau_p}}$$

At steady-state, $\dfrac{\partial^2 \delta n}{\partial x^2} = \dfrac{\delta n}{D_n \tau_n}$ $\quad \dfrac{\partial^2 \delta p}{\partial x^2} = \dfrac{\delta p}{D_p \tau_p}$

$n = n_p\, e^{\frac{qV_F}{kT}}$ $\qquad p = p_n\, e^{\frac{qV_F}{kT}}$



p-n Junction Diodes-Current

Ref.1: 5.3.2

The general solutions of the above equations are:

$$\delta p(x) = C_1 e^{\frac{x_n}{L_p}} + C_2 e^{-\frac{x_n}{L_p}} \quad \text{for } x_n \geq 0 \qquad L_p = \sqrt{D_p \tau_p}, \ \textit{hole diffusion length in the n-side}$$

$$\delta n(x) = C_3 e^{\frac{x_p}{L_n}} + C_4 e^{-\frac{x_p}{L_n}} \quad \text{for } x_p \geq 0 \qquad L_n = \sqrt{D_n \tau_n}, \ \textit{electron diffusion length in the p-side}$$

Applying the boundary conditions,

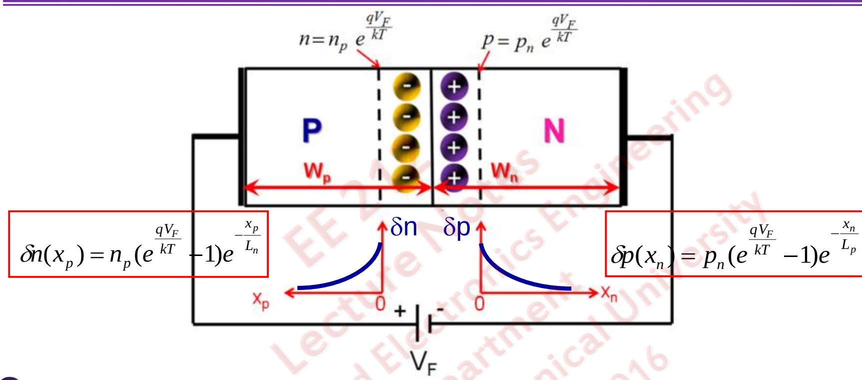
$$\delta p(x_n = 0) = p_n e^{\frac{qV_F}{kT}} - p_n = p_n(e^{\frac{qV_F}{kT}} - 1) \Rightarrow C_1 + C_2 = p_n(e^{\frac{qV_F}{kT}} - 1),$$

$$x_n \to \infty, \delta p \to 0 \Rightarrow C_1 = 0, C_2 = p_n(e^{\frac{qV_F}{kT}} - 1)$$

$$\delta n(x_p = 0) = n_p e^{\frac{qV_F}{kT}} - n_p = n_p(e^{\frac{qV_F}{kT}} - 1) \Rightarrow C_3 + C_4 = n_p(e^{\frac{qV_F}{kT}} - 1),$$

$$x_p \to \infty, \delta n \to 0 \Rightarrow C_3 = 0, C_4 = n_p(e^{\frac{qV_F}{kT}} - 1)$$

$$\boxed{\textit{Then } \ \delta p(x_n) = p_n(e^{\frac{qV_F}{kT}} - 1)e^{-\frac{x_n}{L_p}}, x_n \geq 0 \ , \ \delta n(x_p) = n_p(e^{\frac{qV_F}{kT}} - 1)e^{-\frac{x_p}{L_n}}, x_p \geq 0}$$



Q: Find the current flowing through the diode under above conditions.

S: For $x_n \geq 0$, $\quad I_p\big|_{x_n=0} = -qAD_p \dfrac{d\delta p}{dx_n} = qA\dfrac{D_p}{L_p} p_n(e^{\frac{qV_F}{kT}} - 1)$

For $x_p \geq 0$, $\quad I_n\big|_{x_p=0} = qAD_n \dfrac{d\delta n}{dx_p} = -qA\dfrac{D_n}{L_n} n_p(e^{\frac{qV_F}{kT}} - 1)$

Note that both currents are indeed in the same direction. The difference in the sign arises from the definition of the x_n and x_p coordinates in opposite directions.

If we assume that there is no recombination in the depletion region, then the electron current at x_p=0 should be equal to that at x_n=0. Therefore, we obtain the total current as the sum of the electron current at x_p=0 and the hole current at x_n=0.

$$I = qA(\frac{D_p}{L_p} p_n + \frac{D_n}{L_n} n_p)(e^{\frac{qV_F}{kT}} - 1) = I_s(e^{\frac{qV_F}{kT}} - 1)$$

Shockley Equation

I_s: reverse saturation current

Remember that we have initially assumed $W_n >> L_p$ and $W_p >> L_n$. Therefore, the above equation is applicable only for those diodes with the p-and n-side lengths much longer than the minority carrier diffusion lengths.

$L_p = \sqrt{D_p \tau_p}, \quad$ *hole diffusion length in the n-side*

$L_n = \sqrt{D_n \tau_n}, \quad$ *electron diffusion length in the p – side*

$$\boxed{I = qA(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p)(e^{\frac{qV_F}{kT}} - 1)}$$

Strong temperature dependence

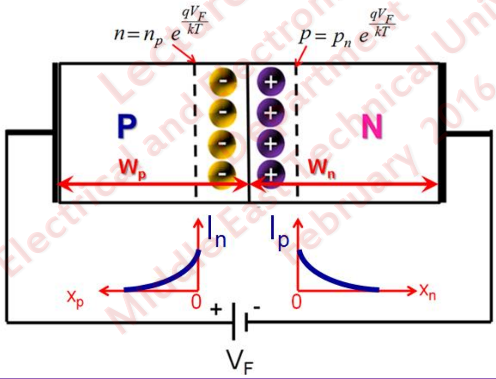
Under reverse bias (V<0) with |V |>>kT/q,

$$\boxed{I = -qA(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p) = -qA(\frac{L_p}{\tau_p}\frac{n_i^2}{N_D} + \frac{L_n}{\tau_n}\frac{n_i^2}{N_A})}$$

Let's now plot the electron and hole diffusion currents through the device.

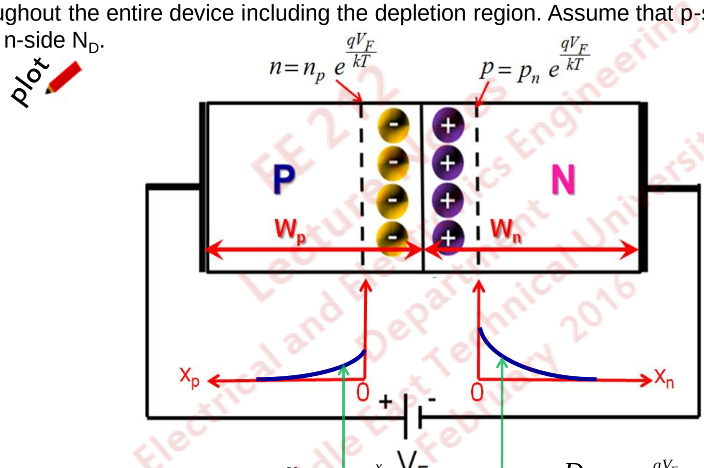
$$I_p(x_n) = -qAD_p \frac{d\delta p}{dx_n} = qA\frac{D_p}{L_p} p_n(e^{\frac{qV_F}{kT}} - 1)e^{-\frac{x_n}{L_p}} \quad \text{for } x_n \geq 0$$

$$I_n(x_p) = qAD_n \frac{d\delta n}{dx_p} = qA\frac{D_n}{L_n} n_p(e^{\frac{qV_F}{kT}} - 1)e^{-\frac{x_p}{L_n}} \quad \text{for } x_p \geq 0$$



Q: The total current (I_p+I_n) flowing through the device must be constant (position independent). Complete the following figure by including all the current components throughout the entire device including the depletion region. Assume that p-side N_A is larger than n-side N_D.

S:



$$I_{np} = qA\frac{D_n}{L_n} n_p(e^{\frac{qV_F}{kT}} - 1)e^{-\frac{x_p}{L_n}} \qquad I_{pn} = qA\frac{D_p}{L_p} p_n(e^{\frac{qV_F}{kT}} - 1)e^{-\frac{x_n}{L_p}}$$

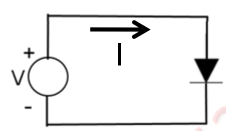
p-n Junction Diodes-Current

Ref.1: 5.3.2

Q: Now explain the plot you have obtained (majority carrier currents).

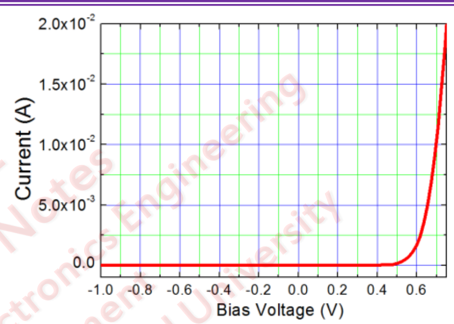
S: In the charge neutral regions away from the depletion region edges, the current is carried by majority carriers. This is expected since the majority carriers lost by recombination with the injected minority carriers and injection to the other side must be supplied by the majority carrier (drift) currents. Note that even a small E-field in the bulk regions is sufficient to have a large enough current due to the large concentration of majority carriers

p-n Junction Diodes-I-V Characteristic



$$I = I_s(e^{\frac{qV}{kT}} - 1)$$

I_s: reverse saturation current



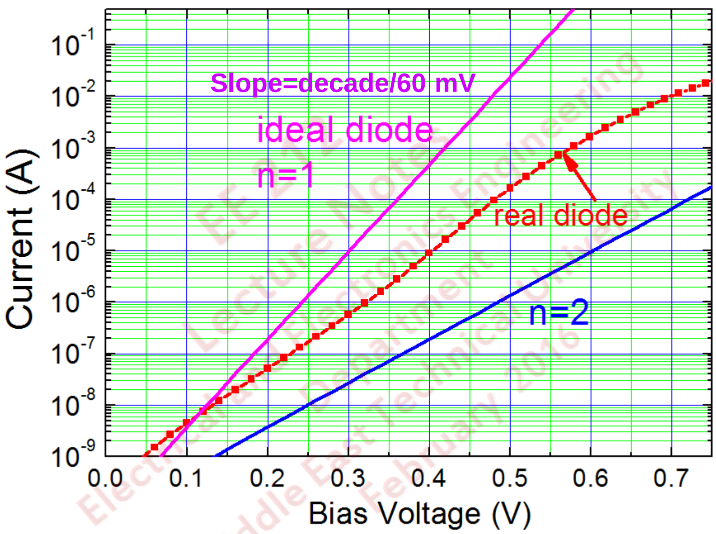
The above equation may not accurately describe the dependence of the diode current on the biasing voltage V in real diodes due to nonideal effects. A more accurate expression includes a nonideality factor n .

$$I = I_s(e^{\frac{qV}{nkT}} - 1)$$

Nonideal effects may become dominant under low and high injection levels (forward bias). n may approach 2 under low and high forward bias voltages while it is close to 1 in a good diode under moderate forward bias.

Another nonideal effect is the increase in the reverse bias current of a diode with increasing reverse bias voltage due to widening depletion region. The reverse current increases approximately in proportion to $(V_{bi}+V_R)^{1/2}$.

p-n Junction Diodes-I-V Characteristic



Temperature Coefficient: It can be shown that the voltage drop across a forward biased Si diode decreases by ~1.8 mV for every 1 ^{o}C increase in the diode temperature.

p-n Junction Diodes-Capacitances

Ref.1: 5.5.4

Junction (Depletion) Capacitance

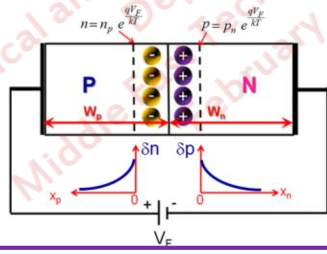
$$C_{DEP} = \frac{dQ_{depletion}}{dV} = A\sqrt{q\frac{\varepsilon}{2(V_{bi}-V)}\frac{N_A N_D}{N_A+N_D}} = \frac{\varepsilon A}{W_{DEP}},$$

for a p$^+$-n diode ($N_A >> N_D$) $\quad C_{DEP} = A\sqrt{\frac{q\varepsilon N_D}{2(V_{bi}-V)}}$

This capacitance is dominant under reverse and low forward bias where the minority carrier injection is not at considerable level.

Diffusion Capacitance

Diffusion capacitance arises from the minority carrier charge stored in the n and p sides during forward bias. The bias dependency of the minority carrier charge results in a capacitance effect.



p-n Junction Diodes-Capacitances

Ref.1: 5.5.4

Let's consider a long p^+-n junction diode with $N_A >> N_D$ and $W_n >> L_p$.

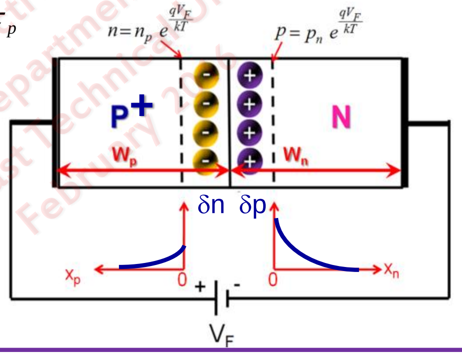
$$I = qA\left(\frac{D_p}{L_p}p_n + \frac{D_n}{L_n}n_p\right)\left(e^{\frac{qV_F}{kT}} - 1\right) \cong qA\frac{D_p}{L_p}p_n e^{\frac{qV_F}{kT}} \quad \text{since } p_n >> n_p$$

Charge stored under the excess hole distribution (in the n-side) is

$$Q_p = qA\int p_n e^{\frac{qV_F}{kT}} e^{-\frac{x_n}{L_p}} dx_n = qAL_p p_n e^{\frac{qV_F}{kT}}$$

$$C_{diff} = \frac{dQ_p}{dV_F} = \frac{q^2 A}{kT} L_p p_n e^{\frac{qV_F}{kT}} = \frac{q}{kT} I\tau_p$$

Diffusion capacitance dominates under forward bias.

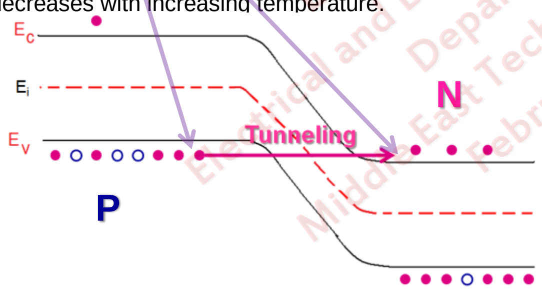


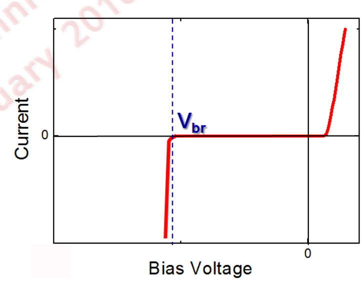
p-n Junction Diodes-Zener Breakdown

Ref.1: 5.4.1

In a p-n junction with both sides heavily doped (large N_A on the p-side and large N_D on the n-side), reverse bias breakdown occurs at relatively low bias voltages due to tunnelling. This breakdown mechanism is called **Zener Breakdown**.

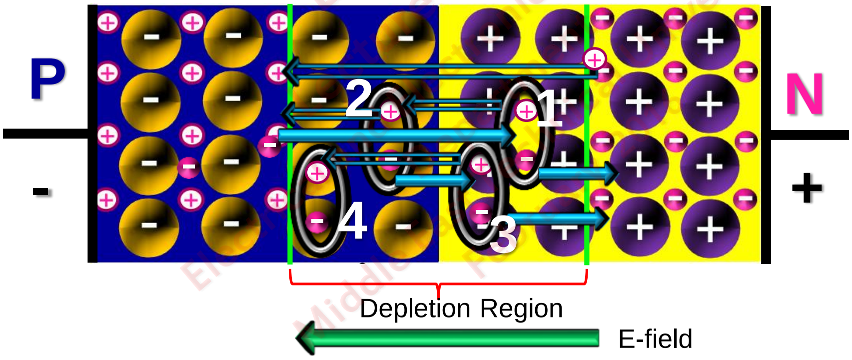
With increasing reverse bias voltage, conduction band edge on the n-side eventually goes below the valence band edge on the p-side. Once this occurs, a large number of filled states in the p-side valence band is aligned in energy with a large number of empty states in the n-side conduction band. Significant tunneling starts if both sides are heavily doped due to a small depletion layer width and a low barrier for tunneling. Note that electron tunneling from p to n side results in reverse current in the opposite direction (from n to p). If at least one side is lightly doped, large depletion region width results in a large tunneling barrier and avalanche breakdown occurs instead of Zener breakdown. Zener breakdown voltage decreases with increasing temperature.





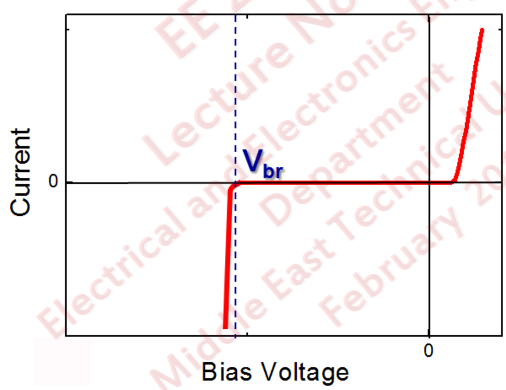
p-n Junction Diodes-Avalanche Breakdown
Ref.1: 5.4.2

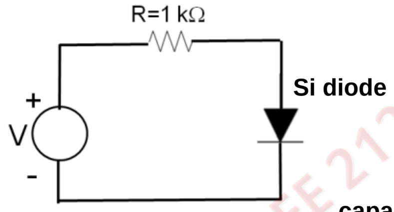
If the reverse bias voltage across the diode is increased to a large magnitude, a very large E-field exists in the depletion region. Under this condition, the minority carriers may acquire large kinetic energy sufficient to break a covalent bond by colliding with the atoms (impact ionization) while passing through the depletion region. The EHPs created by this process may also create new EHPs resulting in the EHP generation and the reverse current through the junction growing like an avalanche (processes 1→2→3→4...). This type of breakdown mechanism is called **avalanche breakdown**.

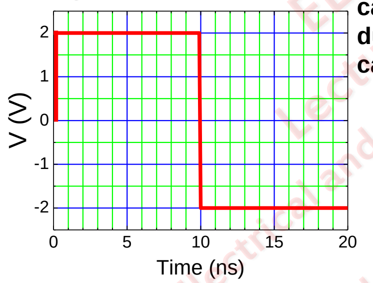


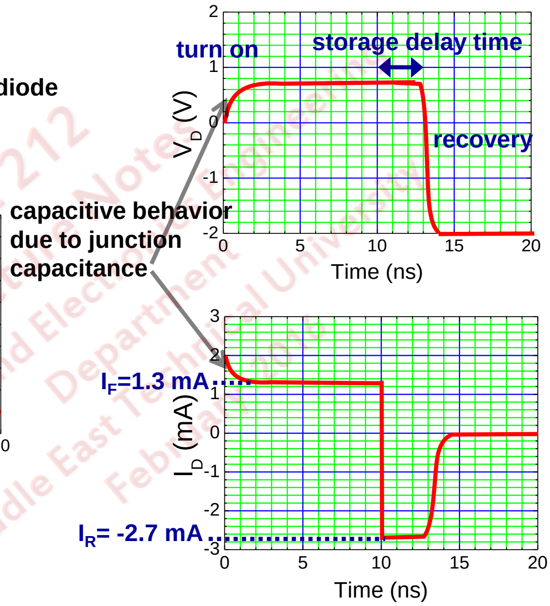
p-n Junction Diodes-Avalanche Breakdown
Ref.1: 5.4.2

Avalanche breakdown voltage increases with temperature. In order to have avalanche breakdown, at least one side of the diode must be lightly/moderately doped, otherwise Zener breakdown occurs due to tunneling.









$$I_F = \frac{2V - 0.7V}{1K\Omega} = 1.3\ mA$$

$$I_R = \frac{-2V - 0.7V}{1K\Omega} = -2.7\ mA$$

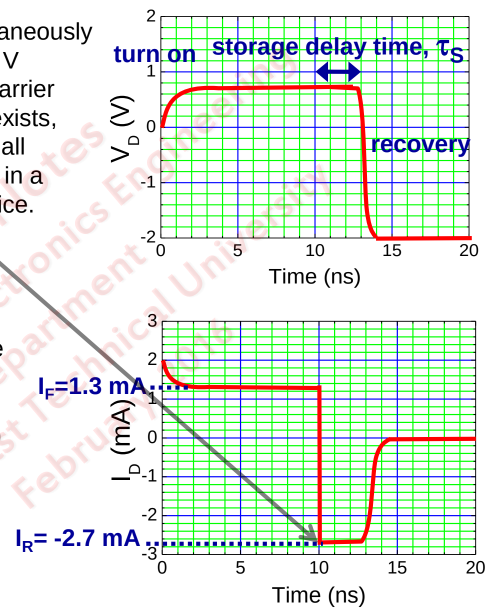
Diode voltage can not be reversed instantaneously when the biasing voltage is switched to -2 V reverse bias. As long as excess minority carrier charge (injected during the forward bias) exists, the diode voltage remains positive and small during the storage delay time. This results in a large reverse current flow through the device.

$$I_R = \frac{-2V - 0.7V}{1K\Omega} = -2.7\ mA$$

After the excess charge is removed by recombination (long diode) or reaching the contact (short diode), large reverse bias voltage starts to develop across the diode and eventually reaches -2 V (bias voltage) with the diode current = $-I_S$ (very small).

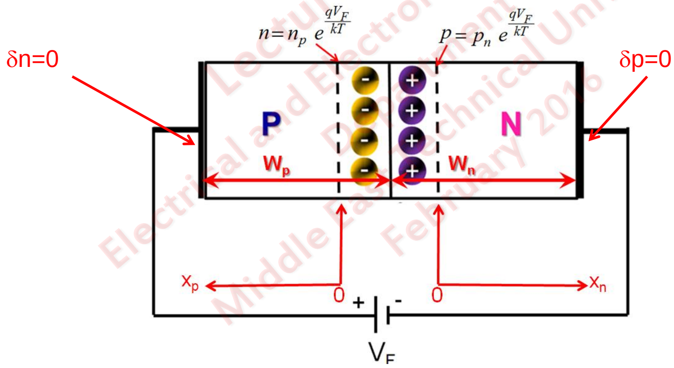
$$\tau_S = \tau_T \ln\left(1 - \frac{I_F}{I_R}\right)$$

for a short diode.



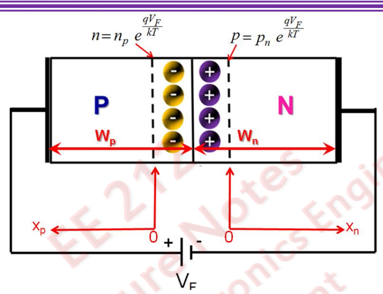
Q.2 (to be solved on white board)

In the previous section, we have worked on a **long diode**. Let's now see how we should express the diode current in the case of a **short diode** with p- and n-side lengths much shorter than the diffusion lengths of the minority carriers. Note that there will exist negligible recombination of the injected minority carriers under this condition meaning that the diffusion currents arising from minority carrier injection should not change with position. In addition to this information, we need the boundary conditions at the ohmic contacts to find the excess carrier distributions throughout the diode. The excess carrier concentration at the ohmic contacts is zero.



p-n Junction Diodes-Exercise Questions

S.2 write



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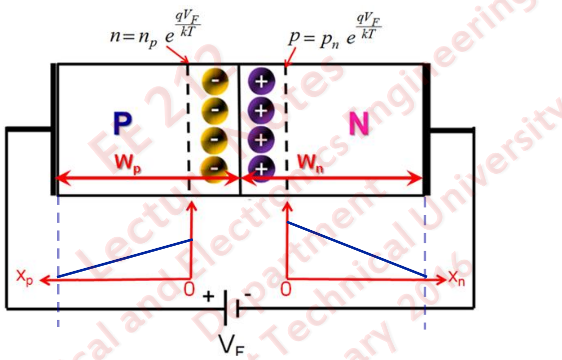
Q.3 Find the expression for transit time of the holes (τ_T) in a short p^+-n junction diode in terms of the length of the n-side (ignore depletion layer width).

S.3:



$$I_p = -qAD_p \frac{d\delta p}{dx_n} \cong qAD_p \frac{p_n(e^{\frac{qV_F}{kT}} - 1)}{W_n} = \frac{Q_p}{\tau_T} \cong \frac{qAW_n p_n(e^{\frac{qV_F}{kT}} - 1)/2}{\tau_T}$$

$$\tau_T = \frac{W_n^2}{2D_p}$$

Q.4 (to be solved on white board)

Find the expression for the diffusion capacitance of a short p^+-n diode.

S.4 write

Q.5 (to be solved on white board)

Consider the following silicon p^+-n junction diode.

n side doping density = $1x10^{16}$ cm^{-3},

d=$2x10^{-6}$ m

contact (built-in) potential of the diode = 0.840 V ,

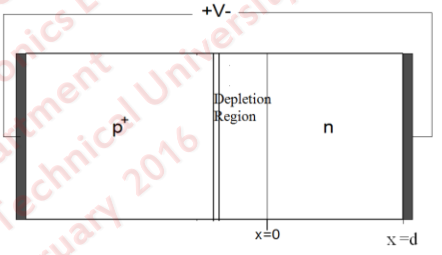
hole mobility in the n-side = 250 cm^2/V-sec

τ_p in the n-side = $5x10^{-11}$ seconds,

p-n junction cross sectional area: 10^{-4} cm^2

V= 0.640 V, Electric-field=0 for 0<x<d

The diode is under steady-state conditions.



i) Calculate the total charge due to the excess holes in the side

ii) Ignore the contribution of electrons to current and calculate the diode current by using the excess hole charge found in the previous step.

iii) Calculate the diffusion capacitance of the diode..

S.5 write

CHAPTER III

Photonic Devices-

Photodetectors, Solar Cells and Light Emitting Diodes

References

1) B. G. Streetman, S. K. Banerjee, *Solid State Electronic Devices*, 6^{th} Edition, Prentice Hall, 2006.

2) J. Singh, *Semiconductor Devices An Introduction*, McGraw-Hill, 1994.

3) R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.

4) http://en.wikipedia.org/wiki/Solar_cell

The Role of This Chapter

Optoelectronic devices detecting electromagnetic radition have found a wide application area both as discrete sensors and integrated sensor arrays. Photodetectors sensing in various wavelenght bands such as x-ray, UV, visible and infrared are enjoying enlarging markets for a wide range of applications.

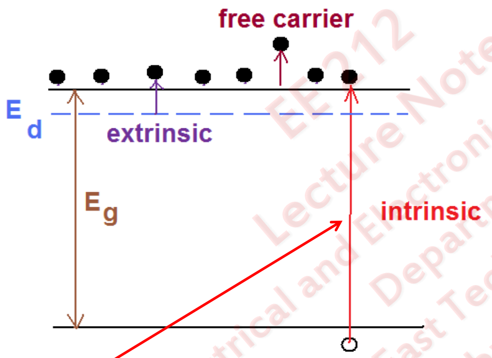
Particular applications which have significantly increased the demand to photodetectors are optical communication, signal processing and data storage. Utilization of photons with very desirable properties for this purpose is realized through devices emitting and detecting light at a wavelength proper for the application.

Imaging is another area where photodetector technology has a huge market. Due to the wide electromagnetic spectrum covering the operation of various sensors, many different semiconductors and detector technologies are employed for imaging in different bands.

Due to the increasing energy demand, the importance of solar cell technology converting solar energy into electricity should be obvious, The Sun is sourcing an enormous amount of energy. The utilization of this huge energy source properly depends (at least) partly on the development of the solar cell technology.

Since the focus of this course is on the electron devices, we will present a very brief introduction to optical devices at a preliminary level by leaving a very important type of optical device, the LASER, out of discussion. Optical devices are discussed with much wider coverage in the senior level course EE *419-Solid State Devices*.

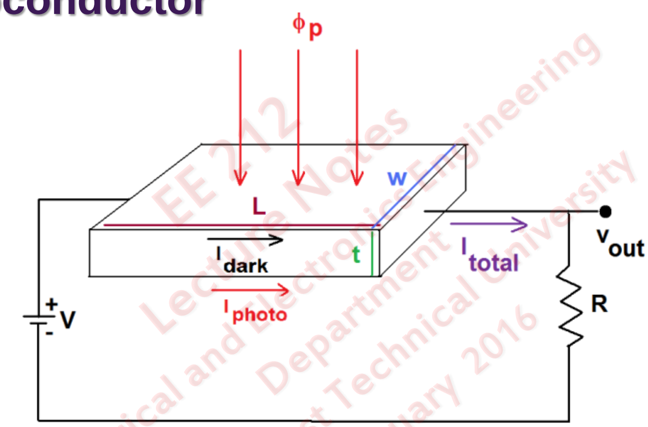
Optical Absorption Processes in Semiconductors



Semiconductor	λ_c (μm)
Si	1.1
GaAs	0.89
InP	0.92
$In_{0.53}Ga_{0.47}As$	1.7
InSb	5.5
$Hg_xCd_{1-x}Te$	1-25

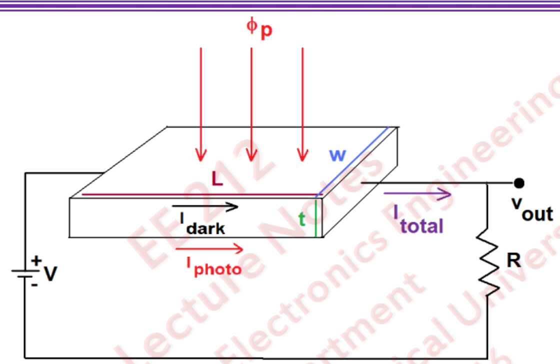
$$\boxed{\lambda_c = \frac{hc}{E_g} = \frac{1.24}{E_g} \text{ where } E_g \text{ is in eV and } \lambda \text{ in } \mu m}$$

Photoconductor



$$\boxed{\frac{dn}{dt} = \phi_p\left(\frac{photons}{cm^2 - \sec}\right).wL(cm^2).\eta(electrons/photons)}$$

electron photo-generation rate **quantum efficiency**



$$I_{total} = JA = \sigma Ewt = (\sigma_{dark} + \Delta\sigma)Ewt = \sigma_p Ewt$$

$$I_{dark} = \sigma_{dark} Ewt, \quad \sigma_{dark} = q(\mu_n n_o + \mu_p p_o)$$

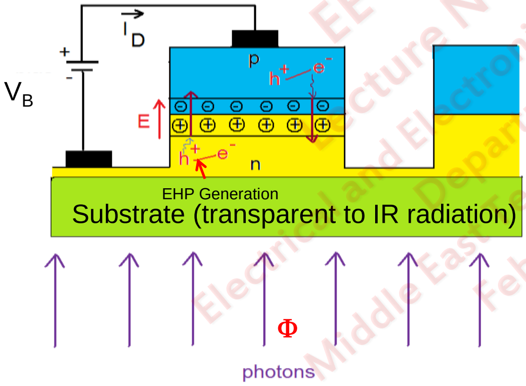
$$\sigma_p = q[\mu_n(n_o + \delta n) + \mu_p(p_o + \delta_p)] \text{ where } \delta_n = \delta_p = g_{op}\tau_p$$

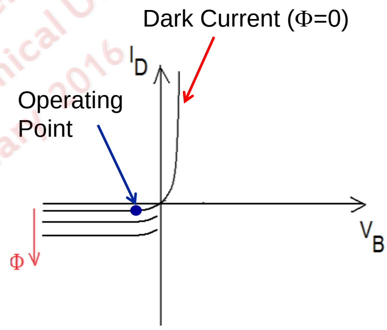
$$\Delta\sigma = q(\mu_n + \mu_p)\delta n$$

$$I_{photo} = \Delta\sigma Ewt = q(\mu_n + \mu_p)\delta_n Ewt = q(\mu_n + \mu_p) g_{op}\tau_n Ewt$$

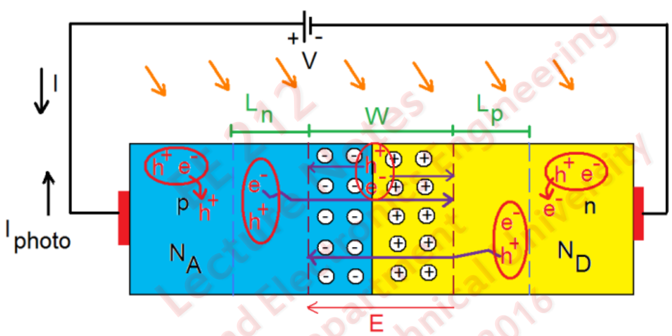
Photovoltaic Detectors

Photoconductors are not suitable devices for large format imaging arrays including many pixels with small dimensions since a photoconductor needs a large enough biasing voltage to create a sufficiently large E-field for the collection of photo-generated carriers. A reverse biased p-n junction, on the other hand, does not need a large biasing voltage and it operates with a very small current level being compatible with dense arrays for high resolution imaging.





Photocurrent Generation



EHP/(cm³-sec)

$$I_{photo} = \underbrace{qAg_{op}L_n}_{} + \underbrace{qAg_{op}W}_{} + \underbrace{qAg_{op}L_p}_{} = qAg_{op}(L_p + L_n + W)$$

charge generated per second in diffusion region in p-side

charge generated per second in depletion region

charge generated per second in diffusion region in n-side

Photodetectors- Photovoltaic Detectors

Ref. 1: 8.1.1

For a long diode,

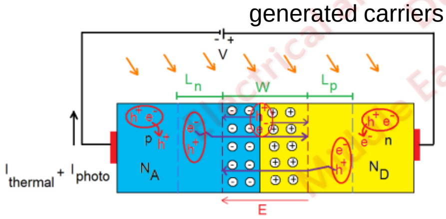
$$\boxed{I_{total} = qA\left(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p\right)\left(e^{\frac{qV}{kT}} - 1\right) - qAg_{op}(L_p + L_n + W)}$$

Under reverse bias (V<0) with |V |>>kT/q,

Strong temperature dependence

$$\begin{aligned} I_{total} &= -qA\left(\frac{L_p}{\tau_p} p_n + \frac{L_n}{\tau_n} n_p\right) - qAg_{op}(L_p + L_n + W)] \\ &= \underbrace{-qA\left(\frac{L_p}{\tau_p}\frac{n_i^2}{N_D} + \frac{L_n}{\tau_n}\frac{n_i^2}{N_A}\right)}_{\text{current due to thermally generated carriers } (I_{dark})} - \underbrace{qAg_{op}(L_p + L_n + W)}_{\text{current due to optically generated carriers } (I_{photo})} \end{aligned}$$

current due to thermally generated carriers (I_{dark}) << current due to optically generated carriers (I_{photo})



must hold to have large S/N

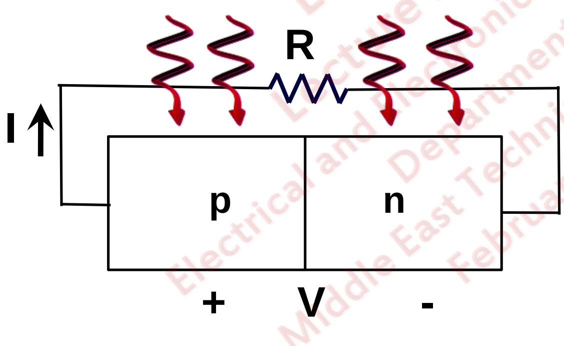
cool down the diode if you are dealing with low band semiconductors (large n_i).
As an example infrared sensors for thermal imagers operate with cooling.

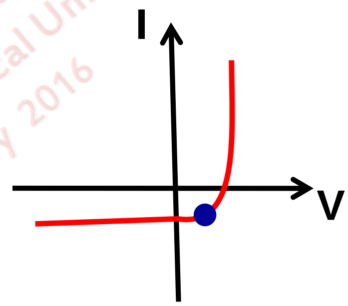
Solar Cells

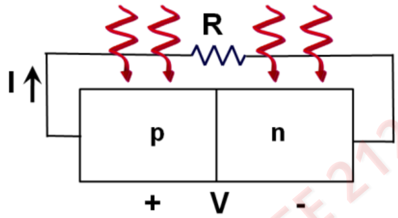
Ref. 1: 8.1.1, 8.1.2, Ref. 2: 10.3.1

Solar Cell is a device used to convert radiation energy to electricity. The most powerful source of radiation is, of course, the Sun which is expected to continue to provide huge energy output for billions of years.

The conventional solar cell is a large area p-n junction. As shown below, in the fourth quadrant of its I-V characteristic, an illuminated p-n junction delivers power to a resistor connected between its terminals.







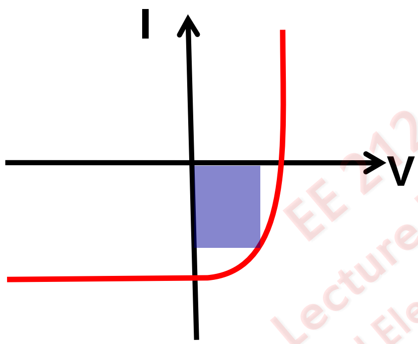
The total current through an illuminated p-n junction is

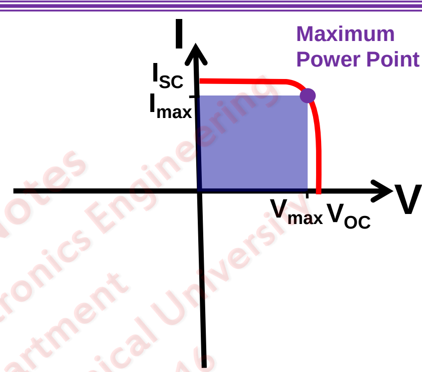
$$I_{total} = I_S(e^{\frac{qV}{nkT}} - 1) - I_{photo}$$

In the case R→∞ (open circuit) the voltage developing on the p-n junction is called open circuit voltage, V_{OC}. For Si solar cells, $V_{OC} \approx 0.7$ V.

$$V_{OC} = \frac{nkT}{q}\ln\left(1 + \frac{I_{photo}}{I_S}\right)$$

In the case R=0 (short circuit) the current through the the p-n junction is called short circuit current, $I_{SC}=I_{photo}$.





$$\eta_{ce} = \frac{P_{max}}{P_{input}} x100 = \frac{I_{max}V_{max}}{P_{input}} x100$$

conversion efficiency

optical power

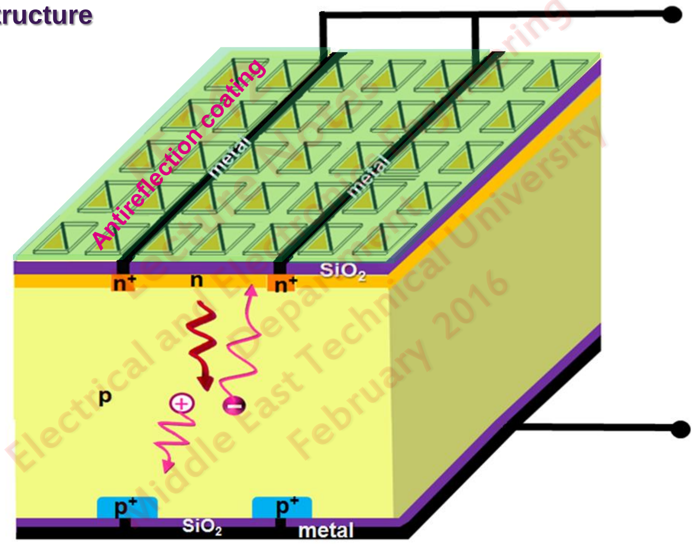
$$F_f = \frac{I_{max}V_{max}}{I_{SC}V_{OC}}$$

fill factor

$$\eta_{ce} = \frac{F_f I_{SC} V_{OC}}{P_{input}} x100$$

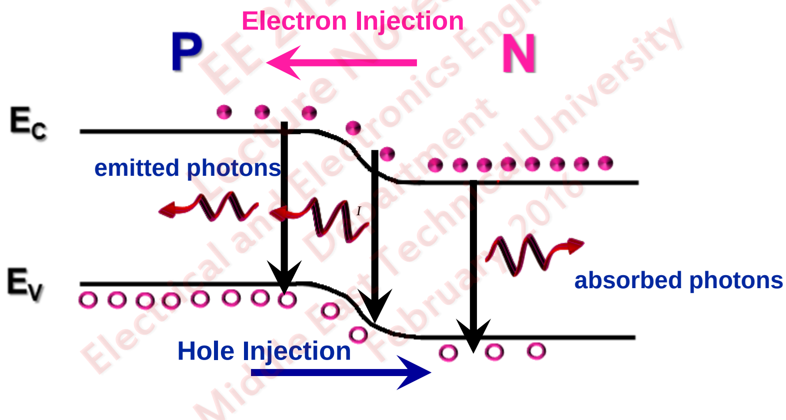
Materials commonly employed for solar cells: Si (monocrystalline, polycrystalline, amorphous), CdTe and GaAs.

Solar Cell Structure



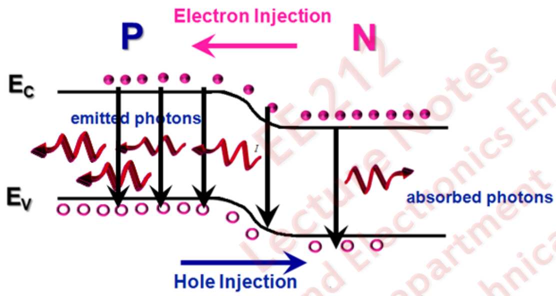
Light Emitting Diode (LED)

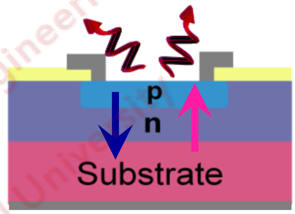
LEDs utilize the emission of photons through radiative recombination of electrons-holes to emit light. The photon emission wavelength is dependent on the energy bandgap of the material. Therefore, different semiconductors are needed for light emission at different colors.



LEDs

Dominant radiative recombination must take place at a location close to the surface in order to minimize reabsorption.



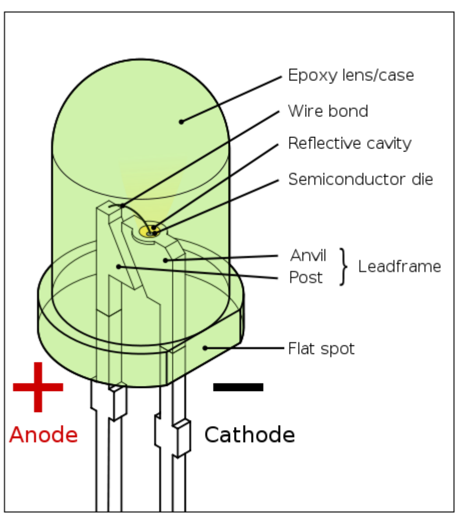


Ref. 2

$$I_p = qA\frac{D_p}{L_p}p_n(e^{\frac{qV}{kT}}-1),\quad I_n = qA\frac{D_n}{L_n}n_p(e^{\frac{qV}{kT}}-1)$$

In case the top layer is p-type as shown above, I_n must be much larger than I_p in order to have most recombination (and emission) occuring in the p-type layer (close to the surface).

LEDs



http://en.wikipedia.org/wiki/File:LED,_5mm,_green_(en).svg
Author: inductiveload

Q.1 Homework 4 (Estimated Time To Complete < 140 min.)

Circle the correct answer for the following 18 questions.

- The nonideality factor (n) in a typical Si p-n junction may approach 2 under
  - a) low forward bias voltages only
  - b) reverse bias only
  - c) moderately large forward bias only
  - d) low and high forward bias voltages
  - e) none of the above
- When the reverse bias voltage magnitude (V_r) across a p-n junction diode is increased, the depletion capacitance
  - a) is increased in proportion to $(V_{bi}+V_r)$
  - b) is increased in proportion to $(V_{bi}+V_r)^{1/2}$
  - c) does not change
  - d) is decreased in proportion to $(V_{bi}+V_r)$
  - e) is decreased in proportion to $(V_{bi}+V_r)^{1/2}$
- When a p-n junction diode is switched from forward to reverse bias at t=0,

i) a considerable current may flow through the junction at $t=0^+$

ii) the junction voltage keeps nearly its forward bias value for a while

iii) the magnitude of the diode current is decreased to (approximately) I_s at steady state under reverse bias

a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

Q.1 Homework 4

- The storage delay time of a p-n junction diode is defined as the amount of time
  - a) required to get rid of the excess carriers injected during forward bias
  - b) required to decrease the diode current to the steady-state reverse bias value after the bias is switched from forward to reverse
  - c) required to increase the diode current to the steady-state forward bias value after a forward bias is applied to the diode under equilibrium
  - d) required to decrease the diode current to 1/e of its value after the bias is switched from forward to reverse
  - e) None of the above
- In a p^+-n junction diode,
  - i) Zener breakdown occurs before the avalanche breakdown
  - ii) the magnitude of the breakdown voltage increases with increasing temperature
  - iii) the breakdown voltage is independent of the doping densities

  a) only i b) i and ii c) only ii d) ii and iii e) i, ii and iii
- In a p-n junction diode, avalanche breakdown occurs due to
  - i) tunneling
  - ii) the large E-field in the depletion region under large reverse bias
  - iii) breaking of covalent bonds by highly energetic carriers in the depletion region

  a) only i b) i and ii c) only ii d) ii and iii e) i, ii and iii

Q.1 Homework 4

- At the onset of Zener breakdown in p-n junction diode,

  i) the conduction band minimum of n side is aligned with the valence band maximum of p-side
  ii) tunneling of electrons starts from the empty states (holes) in the valence band of the p-side to the filled states in the conduction band of the n-side
  iii) the energies of some of the filled valence band states in the p-type material are aligned with some empty conduction band states in the n-type material

  a) only i b) i and ii c) i and iii d) ii and iii e) i, ii and iii

- The transit time of holes (in the n-side) in a short p^+-n junction diode, does not significantly depend on

a) μ_p in n-side b) D_p in n-side c) n-side length d) biasing voltage e) doping density in n-side

- The switching (from forward to reverse) speed of a long p^+-n junction diode can considerably be increased by

a) decreasing the hole recombination lifetime in the n-side
b) increasing the forward bias voltage
c) increasing the diode area
d) decreasing the depletion capacitance
e) none of the above

- In a p^+-n junction diode under forward bias

a) the diode current is dominated by electron diffusion
b) diode capacitance is mostly determined by the junction (depletion) capacitance
c) the voltage drop on the diode decreases with increasing temperature
d) the diode current does not depend on the doping density in the n-side
e) none of the above

Q.1 Homework 4

- The cut off wavelength of a photodetector fabricated wih a semiconductor with energy bandgap of 1.24 eV will be

a) 1.24 μm b) 1 μm c) 0.62 μm d) 2.48 μm e) 3.72 μm

- If a photoconductor is exposed to illumination (low level excitation) with an optical generation rate of g_{op} and the electron recombination lifetime=hole recombination lifetime=τ, the illumination induced change in the conductivity of the material (at steady-state) will be

a) $(\mu_n+\mu_p)g_{op}\tau$ b) $q\eta(\mu_n+\mu_p)g_{op}\tau$ c) $q\eta(\mu_n+\mu_p)g_{op}$ d) $\eta(\mu_n+\mu_p)g_{op}\tau$ e) $q(\mu_n+\mu_p)g_{op}\tau$

- Photovoltaic photodetectors fabricated with low energy bandgap semiconductors need cooling in order to provide good performance. Why?

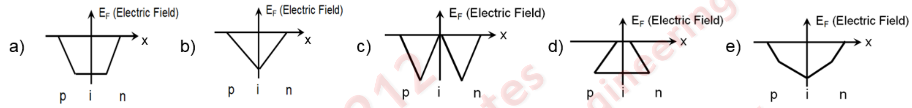
a) to increase the thermally generated minority carrier concentration
b) to decrease n_i
c) to partially ionize the impurity atoms
d) to increase the quantum efficiency
e) none of the above

- The conversion efficiency of a solar cell is defined as

a) (Electrical Power Output/Optical Power Input)x100
b) (Optical Power Output/Electrical Power Input)x100
c) (Electrical Power Output/Electrical Power Input)x100
d) (Optical Power Output/Optical Power Input)x100
e) None of the above

Q.1 Homework 4

- Which of the following represents the E-field distribution in p-i-n junction where "i" layer is constructed with perfectly intrinsic material?



- Which of the following statements is/are **correct** for a p^+-n junction?

i) the reverse bias current increases with increasing temperature
ii) the diffusion capacitance of the junction increases with increasing junction current
iii) the junction voltage increases with increasing temperature under forward bias with a constant current

a) only i b) only i and iii c) only i and ii d) all of them e) only ii and iii

- Which of the following statements is/are **correct** for a p^+-n junction under reverse bias?

i) the magnitude of the diode current is decreased under illumination causing optical generation
ii) the junction (depletion) capacitance decreases with increasing (in magnitude) reverse bias voltage
iii) the depletion region extends farther into the side with lower doping

a) iii b) only ii and iii c) none of them d) all of them e) only ii

- Which of the following statements is/are **correct** for the current flowing through a p-n junction under reverse bias?

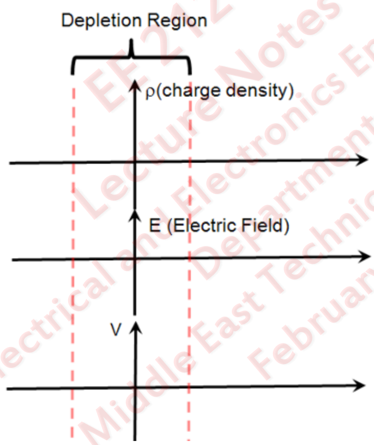
i) reverse current depends on the diffusion lengths of the minority carriers
ii) reverse current is independent of the energy bandgap of the semiconductor
iii) reverse current is mostly drift current

a) only i and ii b) only i c)only i and iii d) all of them e) only ii and iii

Q.2 Homework 4

Consider a p-n junction constructed with a p-type (doped at $N_A >> n_i$) and an n-type (doped at $N_D >> n_i$) semiconductor.

i) Plot the charge density, E-field and electrostatic potential distributions in the junction. Provide the necessary labels.



Q.2 Homework 4

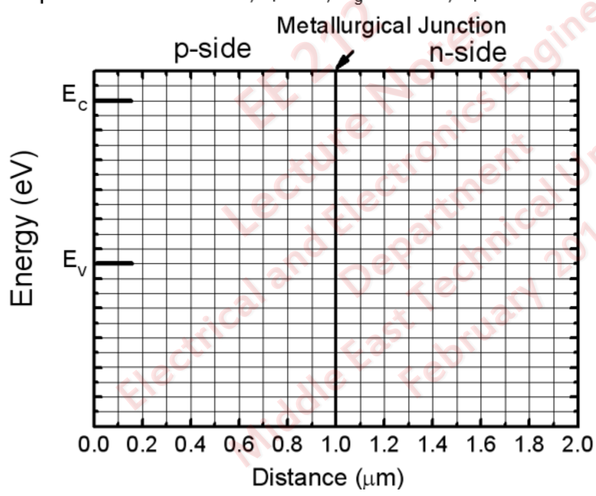
ii) Find the expression for the difference between the Fermi Level position in the n-type semiconductor (E_{Fn}) and the Fermi level position in the p-type semiconductor (E_{Fp}) (before the junction is made) in terms of the doping densities (N_A and N_D) and the other necessary parameters. kT=25.86 meV, $n_i=1\times10^{10}$ cm^{-3}.

iii) Use you answer to part (ii) and write the expression for the built in potential, V_{bi}.

iv) Derive the expression for the depletion width, W, under equilibrium condition in terms of doping densities and the built in potential.

Q.2 Homework 4

v) Plot the energy band diagram of the junction with $N_A=N_D=5.215\times10^{16}$ cm^{-3} and a **reverse** bias voltage (magnitude) of 0.2 V. Show the Fermi levels on the diagram. Depletion layer width must be reflected correctly by your plot. kT=25.86 meV, $\varepsilon_r=9.5$, $E_g=1.1$ eV, $n_i=1\times10^{10}$ cm^{-3}.



EE 212 Lecture Notes Electrical and Electronics Engineering Department Middle East Technical University February 2016

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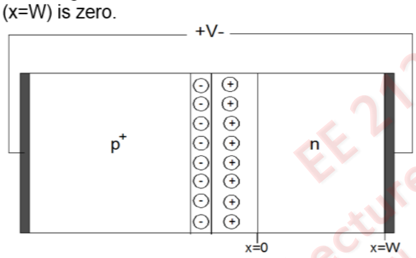
Q.3 Homework 4

Consider the following p^+-n junction diode. The diode is forward biased with V>> kT/q. Assume that the electric field magnitude is zero for 0<x<W and n-side is uniformly doped. The excess carrier density at the contacts (x=W) is zero.



a) Start from the diffusion equation and find the expression for excess hole distribution as a function of position ($\delta p(x)$) for 0<x<W in terms of Δp and other necessary parameters. Do not make any assumptions on W (your expression must be valid for any W).
b) Simplify the above expression for $\delta p(x)$ assuming that $W \gg L_p$ where L_p is the hole diffusion length in the n-side (your expression must reflect the assumption of $W \gg L_p$.).
c) Find the expression for the total charge in the n-side (0<x<W) due to the injected holes for $W \gg L_p$ (your expression must reflect this assumption). Show complete work.
d) Find the expression for the diffusion capacitance of the device using your answer to part c (for W>>Lp) and qualitatively (with words) discuss how and **why** the diffusion capacitance depends on the recombination lifetime of holes in n-side.

Q.4 Homework 4

Material parameters for a silicon p-n junction with an area of 100 μm^2 at 300 K are given in the following table.

Parameter	n-side	p-side
Doping density (N)	10^{15} cm^{-3}	10^{18} cm^{-3}
Minority carrier lifetime (τ)	10^{-6} s	10^{-7} s
Majority carrier mobility (μ)	1350 cm^2/(V-sec)	100 cm^2/(V-sec)
Minority carrier mobility (μ)	500 cm^2/(V-sec)	250 cm^2/(V-sec)

i) Find the zero bias junction capacitance of this diode.

ii) Find the diffusion capacitance of the diode under a forward bias voltage of 0.5V.

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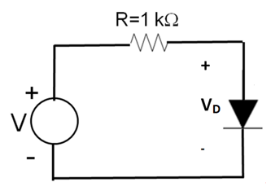
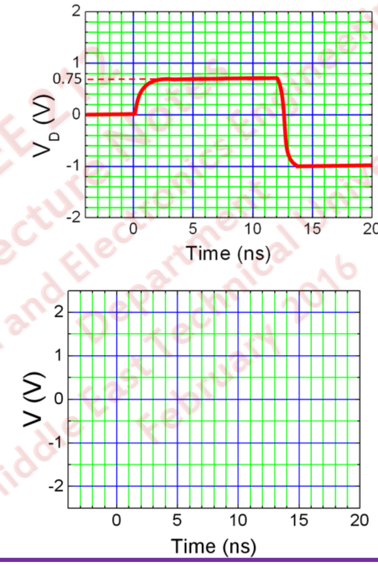
Q.5 Homework 4

The ideality factor, saturation current (I_s) and the storage delay time of the diode in the following circuit are 1.0, 2.225×10^{-16} A and 4 ns, respectively. Plot V(t).

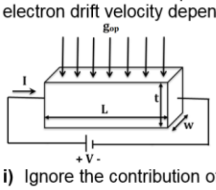
V_T=26 mV.





Q.6 Homework 4

Consider the following photoconductor constructed with a uniform n-type semiconductor. The electron mobility (μ_n) in this semiconductor is much larger than the hole mobility. The photoconductor is under uniform (and continuous) illumination with an optical generation rate of g_{op} EHP/(cm^3-sec) resulting in low level excitation. Assume that electron drift velocity depends linearly on the E-field.



i) Ignore the contribution of holes to conductivity and write the expression for the difference between the currents (I) under illumination and dark (no illumination with g_{op}=0) conditions. No derivation is required. The expression must be in terms of g_{op}, μ_n, V and the other necessary parameters. Write the definitions for the parameters which are not defined in the question.

I_{diff} =

ii) Write the expression for the above described current (I_{diff}) in terms of g_{op}, τ_T and the other necessary parameters where τ_T is the transit time of the electrons through the photoconductor (τ_T=L/v_n where v_n is the electron drift velocity).

iii) Now, define Q_n as the amount of excess electron charge generated in the whole photoconductor in a second due to illumination. Write the expression for the above described current (I_{diff}) in terms of Q_n, τ_T and the other necessary parameters.

iv) Explain (qualitatively) how the expression you obtained in part (iii) describes I_{diff}.

CHAPTER IV

Bipolar Junction Transistors

References

1) B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th Edition, Prentice Hall, 2006.

2) R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.

3) A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, 5th Edition, 2004.

4) R. C. Jaeger and T. N. Blalock, Microelectronic Circuit Design,Mc Graw Hill, 2nd Edition, 2004.

5) J. Singh, *Semiconductor Devices An Introduction*, McGraw-Hill, 1994.

The Role of This Chapter

- After its invention in 1947 by Bardeen, Brattain and Shockley, BJT had functioned for a long time as the only three-terminal device starting a new era in electronics. After the characteristics of the MOSFETs were improved by increasing the quality of the Si-SiO_2 interface, BJT has been challenged by the MOSFETs which have replaced BJTs in a group of applications. However, BJTs, still find a wide application area with certain properties that can not be fullfilled by the field-effect transistors such as high current handling capability and a larger transconductance.

- The objective of this chapter is to provide a sound understanding of the BJT operational principles and physics.

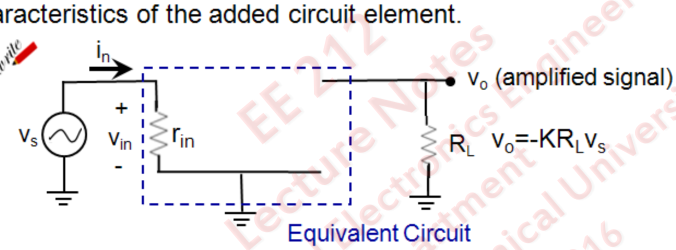
- After studying this chapter, you will have an understanding of the device behavior and characteristics as well as the model parameters used by circuit simulators such as SPICE. This background will allow the utilization of this device in integrated and discrete circuit design more efficiently.

BJTs-The Need for Controlled Current Source

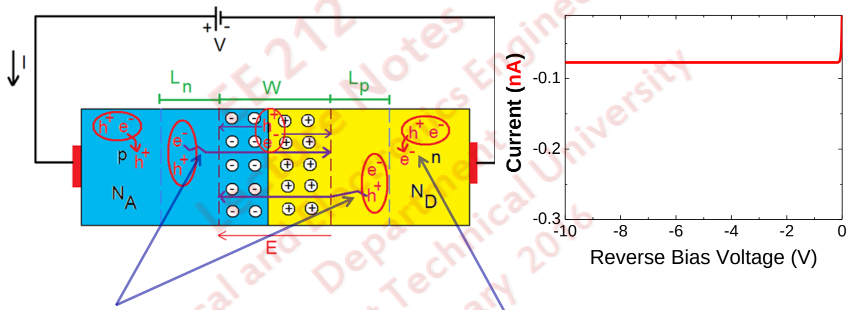
Construction of a Three-Terminal Device for Amplification of AC Signals

Q. Place a circuit element in the circuit below to complete the small signal equivalent circuit of a device that amplifies the ac signal. Plot the I-V characteristics of the added circuit element.

S: write

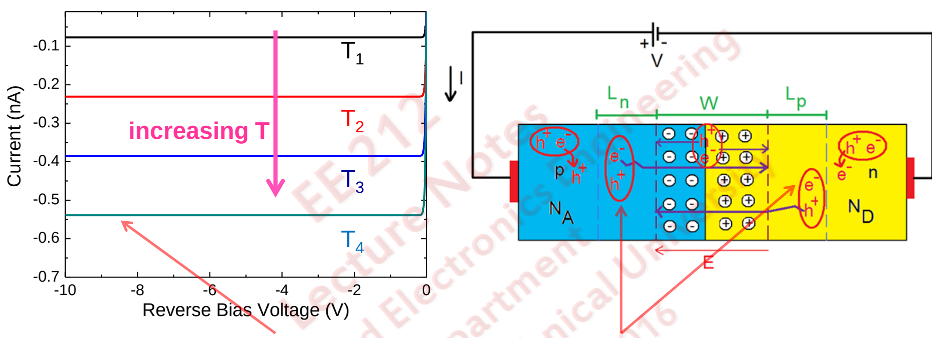


Now let's see how we can construct a controlled current source by using semiconductors. So far we are familiar with p-n junctions which (under ideal conditions) provide a bias independent current in the reverse bias region. This (drift) current is established by the minority carriers created around the depletion region.



Minority carriers that are able to diffuse up to the depletion region (created within a diffusion length from the depletion layer edge) contribute to the drift current.

Other minority carriers are lost by recombination before they reach the depletion region (do not contribute to the drift current).

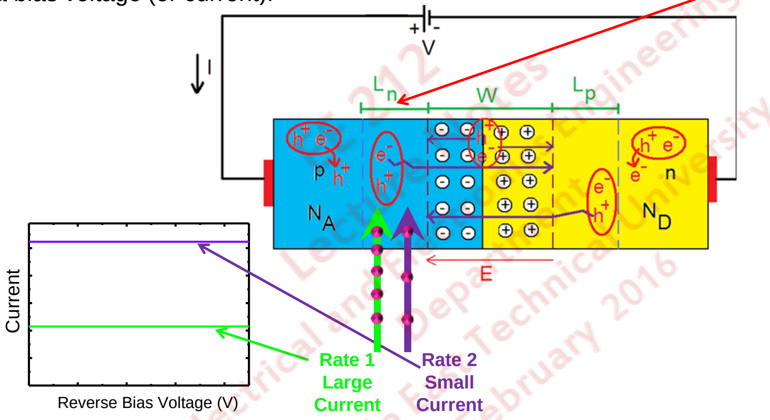


Reverse (drift) current can be controlled by the minority carrier generation rate which depends on temperature and optical excitation rate (if illumination exists).

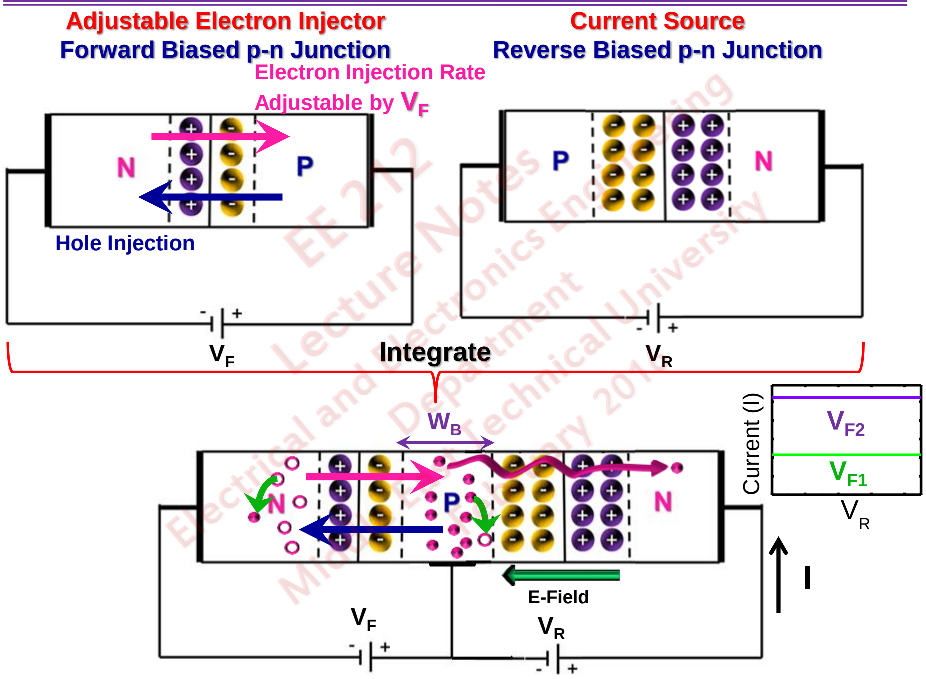
Looks like the characteristics of a controlled current source. However, (of course) it is not a good idea to control the current with temperature and/or optical illumination for amplification.

Furthermore, the drift current due to thermally generated minority carriers is too low (with the bandgap of typical semiconductors such as Si).

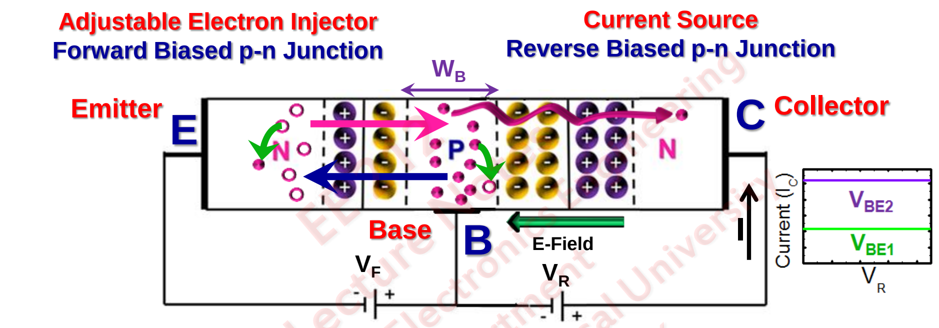
We should find a way to control the reverse current of a p-n junction electrically. This is equivalent to controlling the electron (minority carrier) concentration in this region with a bias voltage (or current).



We need an adjustable electron injector that should be integrated with a reverse biased p-n junction.



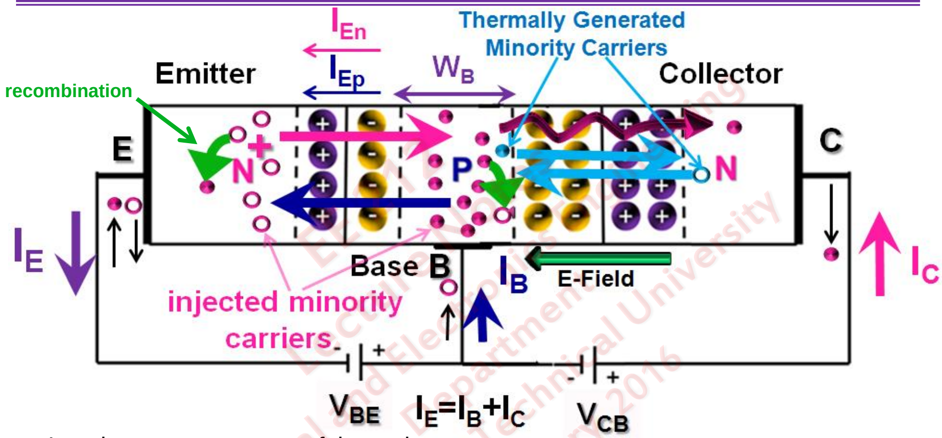
BJTs- Constructing the Transistor



Due to the forward bias across the BE junction electrons are injected (from the emitter) into the base. Some of the injected electrons recombine with the holes in the base. However, most of them reach the BC depletion region (if $W_B << L_n$). Electrons reaching the BC depletion region are swept by the E-field into the collector establishing the collector current which is the drift curent of the reverse biased BC junction. Note that this current is much larger than the drift (reverse) current in a typical p-n junction since the injected electron density is typically much larger than that created by thermal generation in a p-n junction diode.

In a p-n junction diode the reverse current depends on temperature through the thermal generation rate of the minority carriers. In a BJT, the collector current depends on the injected minority carrier density which is adjustable by the forward bias voltage across the BE junction.

BJTs-Operation



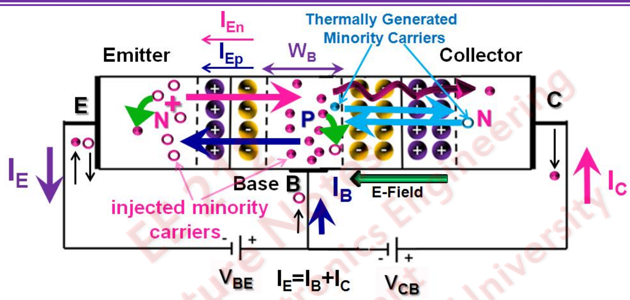
I_{En}: electron component of the emitter current

I_{Ep}: hole component of the emitter current

I_E: total emitter current

I_C: collector current

I_B: base current



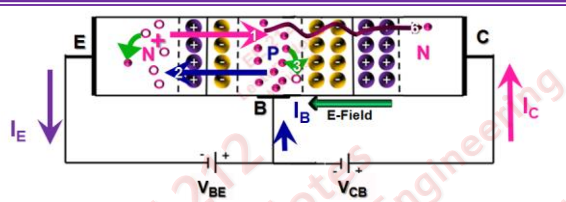
Q: What are the mechanisms establishing the base current?

S:

•Hole injection from the base into the emitter leads to hole depletion in the base. These holes lost due to injection must be resupplied through the base contact.

• Some of the electrons injected from the emitter recombine with the holes in the base. These holes lost due to recombination must be resupplied through the base contact.

• Thermally generated holes (minority carriers) in the collector are swept into the base (by the E-field of BC depletion layer). This mechanism decreases the amount of hole flow into the base through the base terminal (base current).



Q: What happens when the base terminal is open circuited?

S: Hole flow into the base is stopped. No resupply of holes lost due to recombination with the injected electrons and injection from the base to emitter$\rightarrow$negative charge build up in the base$\rightarrow$loss of forward bias across the emitter-base junction$\rightarrow$no more minority carrier injection from the emitter into the base$\rightarrow I_E=I_C\approx 0$.

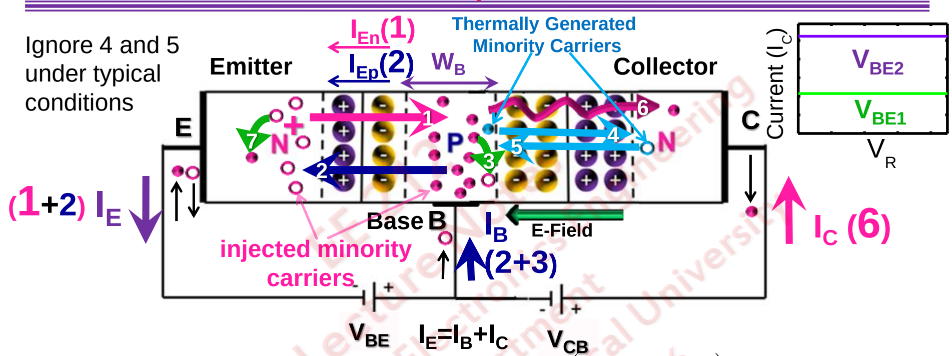
The amount of electron flow through the base (and therefore the collector current) can be adjusted through the control of the base current (large $I_B \rightarrow$large I_C).

• If the base width is kept small, only a small fraction of the injected electrons recombines in the base.
• If the emitter doping is much larger than the base doping, the electron injection from the emitter into the base is much larger than hole injection from base into emitter.

The above conditions result in a collector current much larger than the base current.

Current Gain!

Ignore 4 and 5 under typical conditions



4 and 5 are very small (due low to thermal generation rate (in Si at 300 K)).

Ignore 4 and 5 and define

$$\gamma = \frac{I_{En}}{I_{En}+I_{Ep}} = \frac{(1)}{(1)+(2)} \quad (\textit{Emitter Injection Efficiency})$$

$$B = \frac{I_C}{I_{En}} = \frac{(6)}{(1)} \quad (\textit{Base Transport Factor})$$

$$\beta = \frac{I_C}{I_B} = \frac{(6)}{(2)+(3)} \quad (\textit{Current Gain})$$

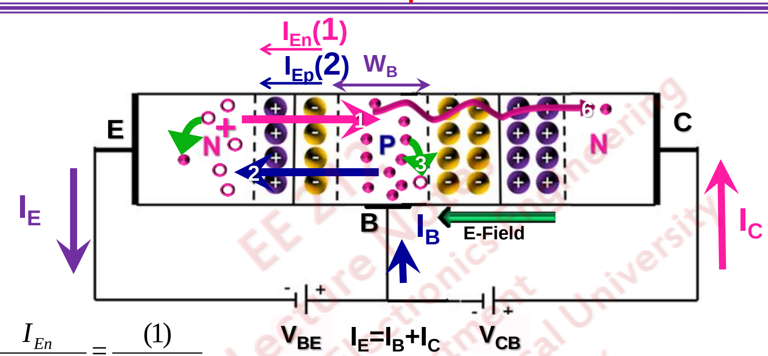
$$\alpha = \frac{I_C}{I_E} = \frac{(6)}{(1)+(2)} \quad (\textit{Current Transfer Ratio})$$

$$\frac{I_C}{I_E} = \alpha = \frac{BI_{En}}{I_{En}+I_{Ep}} = B\gamma$$

$$I_B = I_{Ep} + (1-B)I_{En}$$

$$\frac{I_C}{I_B} = \beta = \frac{BI_{En}}{I_{Ep}+(1-B)I_{En}}$$

$$= \frac{BI_{En}/I_E}{(I_{Ep}+(1-B)I_{En})/I_E} = \frac{B\gamma}{1-B\gamma} = \frac{\alpha}{1-\alpha}$$



$$\gamma = \frac{I_{En}}{I_{En}+I_{Ep}} = \frac{(1)}{(1)+(2)}$$

$$B = \frac{I_C}{I_{En}} = \frac{(6)}{(1)}$$

$$\beta = \frac{I_C}{I_B} = \frac{(6)}{(2)+(3)}$$

$$\alpha = \frac{I_C}{I_E} = \frac{(6)}{(1)+(2)}$$

In a Good npn BJT:

$W_B \ll L_n$ to minimize **(3)**, **$I_{En} \approx I_C$, $B \approx 1$**

(1)>>(2) to make $I_E \approx I_{En}$. ((2) does not contibute to I_C).
This can be achieved by doping Emiter heavily with respect to Base.

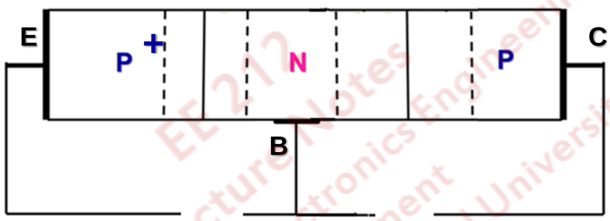
If both conditions are satisfied, **$I_E \approx I_C \rightarrow I_B \approx 0 \rightarrow$ high β and $\alpha \approx 1$.**
Large Current Gain!

BJTs-pnp BJT

CHECK YOURSELF-POINT

Q: Convert the previous slide for a pnp BJT.

S: *write*



$\gamma =$

In a Good pnp BJT:

$B =$

$\beta =$

$\alpha =$

BJTs-Operation

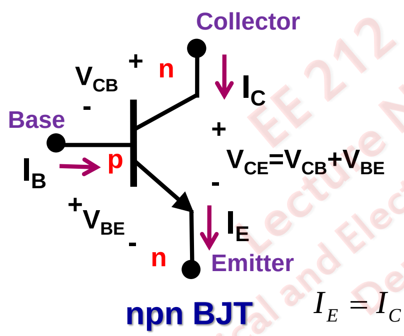
Ref. 1: 7.2

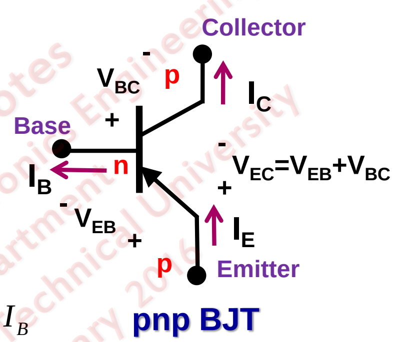
CHECK YOURSELF-POINT

Q: Explain the relation between the β of an npn BJT and the electron recombination lifetime and the electron transit time in the base. Assume unity emitter injection efficiency.

S: *write*

BJTs- Circuit Symbols





$$I_E = I_C + I_B$$

$$I_C = \alpha I_E$$

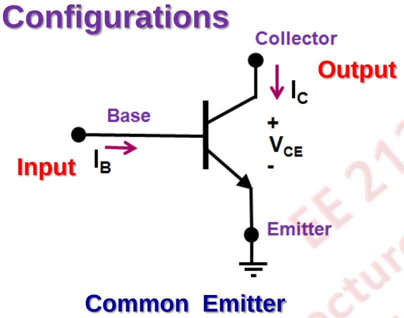
$$I_C = \beta I_B$$

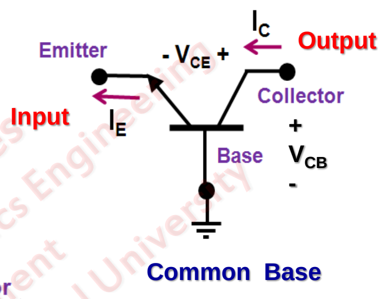
$$I_E = (\beta + 1) I_B$$

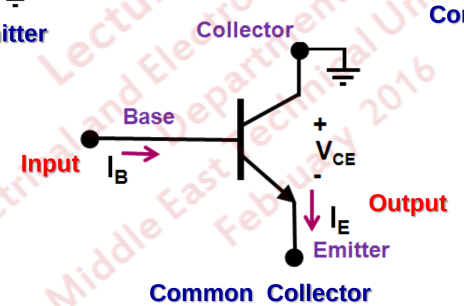
with BE junction forward- and BC junction reverse-biased

BJTs- Operation

Configurations

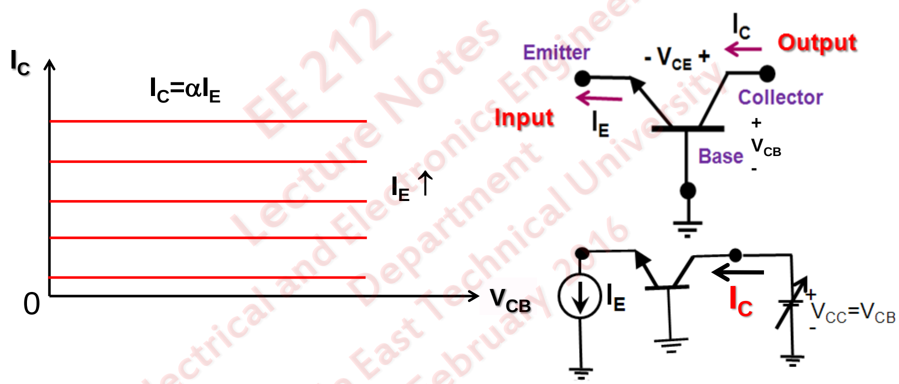






BJTs- Operation

Common Base I_C-V_{CB} characteristics of the npn BJT.

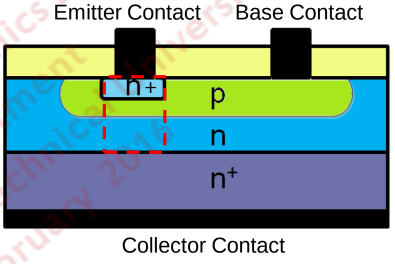


BJTs-Operation

CHECK YOURSELF-POINT

Q: The following figure shows the picture of an npn BJT fabricated on a Si wafer. Discuss the effects of exchanging the emitter and collector terminals on the device performance (Does the device offer the same current gain if the collector is used as emitter (and the emitter as collector) while BC junction is forward- and BE junction is reverse-biased?)

S: *write*



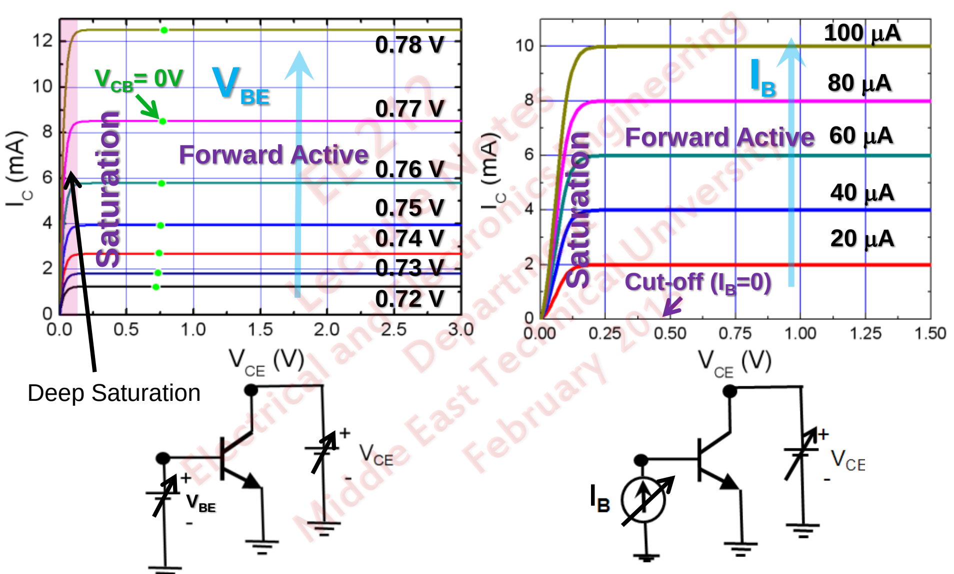
BJTs-Operation Modes

BE Junction	BC Junction	Mode	npn	pnp
Forward	Forward	Saturation	$V_{BE}>0$ $V_{BC}>0$	$V_{EB}>0$ $V_{CB}>0$
Forward	Reverse	Forward Active	$V_{BE}>0$ $V_{BC}<0$	$V_{EB}>0$ $V_{CB}<0$
Reverse	Forward	Reverse Active	$V_{BE}<0$ $V_{BC}>0$	$V_{EB}<0$ $V_{CB}>0$
Reverse	Reverse	Cut off	$V_{BE}<0$ $V_{BC}<0$	$V_{EB}<0$ $V_{CB}<0$

BJTs- Characteristics

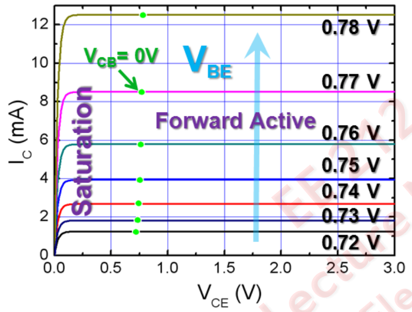
Ref. 4: 5.7

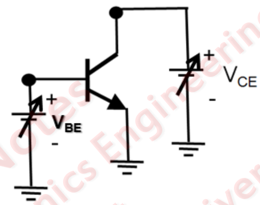
I_C-V_{CE} (Common Emitter) Characteristics of the npn BJT



BJTs- Characteristics

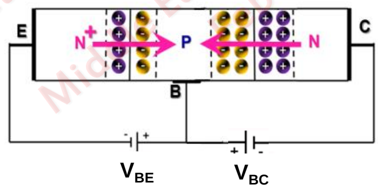
Q: Explain the variation of I_C (with V_{CE}) in the saturation region.





$$V_{CE}=V_{CB}+V_{BE}$$

S: Start from the boundary between FA and SAT regions on a curve (say V_{BE}=0.75 V) and decrease V_{CE}. As V_{CE} goes below =0.75 V, V_{CB} will be negative (BC junction is forward biased). Forward bias across the BC junction results in electron injection from the collector into base opposing the injection from the emitter. As V_{CE} is decreased further with V_{BE} kept constant, the forward bias across the BC junction is increased. Therefore, I_C is decreased with decreasing V_{CE}.

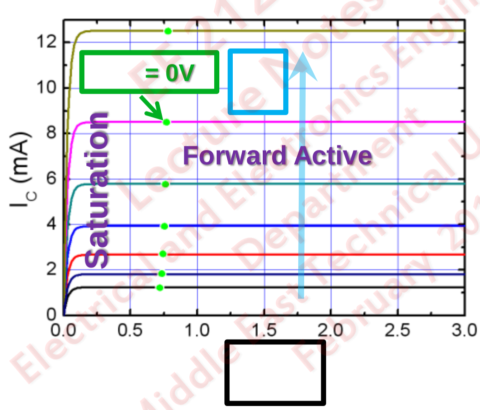


Note that
$I_C \neq \beta I_B$
in SAT.

BJTs- Characteristics

CHECK YOURSELF-POINT

Q: Convert the common emitter characteristics for a pnp BJT.

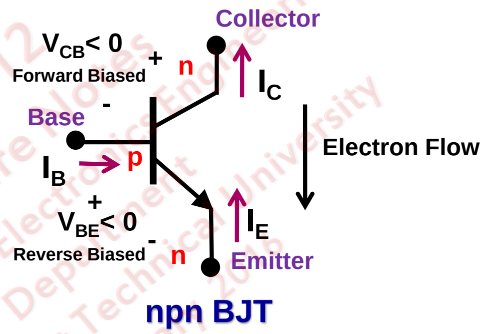


BJTs- Characteristics

Q: Determine the relations between the terminal currents in the reverse active mode of the npn BJT.

S:

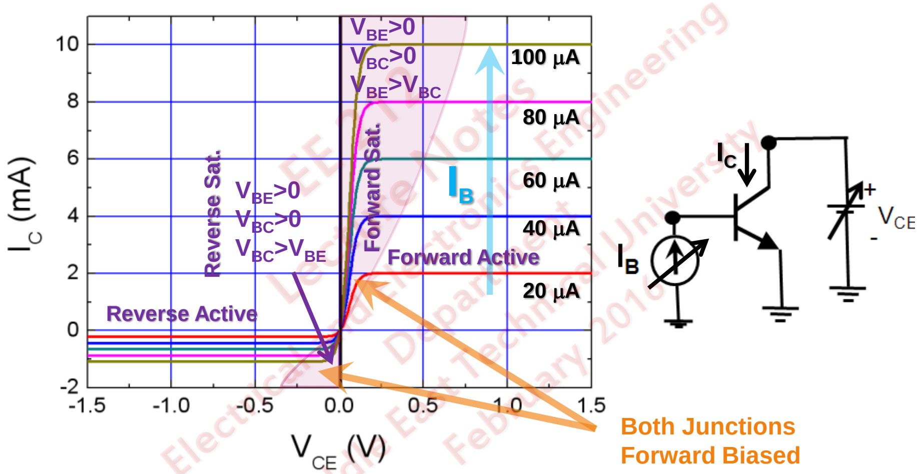
$$I_E = \alpha_R I_C$$
$$I_E = \beta_R I_B$$
$$I_C = (\beta_R + 1) I_B$$
$$\alpha_R = \frac{\beta_R}{\beta_R + 1}$$



BJTs- Characteristics

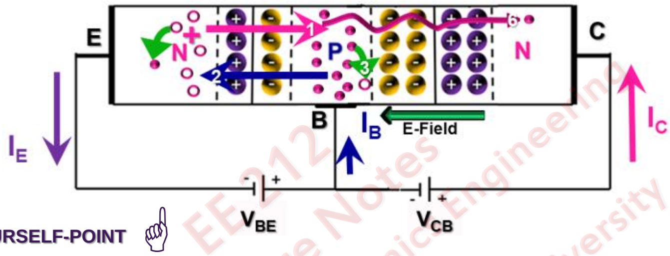
Ref. 4: 5.7

β_F=100, β_R=10



$$V_{CE} = V_{CB} + V_{BE} = V_{BE} - V_{BC}$$

BJTs- Characteristics



CHECK YOURSELF-POINT

Q: Plot the I_B-V_{BE} characteristics of the npn BJT.

plot

Q.1 Homework 5 (Estimated Time To Complete < 60 min.)

Circle the correct answer for the following 30 questions.

- How would you describe an ideal pnp BJT biased in the proper mode for amplification?

a) as a reverse biased n-p junction integrated with a hole injector
b) as a forward biased p-n junction integrated with a hole collector
c) as a reverse biased n-p junction integrated with an electron injector
d) as a voltage controlled resistor
e) none of the above

- A BJT can be used as a good amplifier of AC signals, if

a) it is an npn BJT
b) it operates in the saturation region
c) it operates as a controlled current source
d) it has an emitter injection efficiency >> 1
e) all of the above

- Consider an npn BJT biased in the proper mode for amplification. The function of the emitter in this BJT is

a) to provide the electrons for the drift current through the B-C junction
b) to provide the holes lost from the base in order to maintain charge neutrality
c) to maintain an emitter current independent of the E-B biasing voltage
d) to provide majority carriers (holes) to the base in order to establish the collector current
e) none of the above

- If the electron recombination lifetime in the base and the base transit time are represented by τ_n and τ_T in a typical npn BJT with an emitter injection efficiency smaller than 1,

a) $\beta=\tau_n/\tau_T$ b) $\beta=\tau_T/\tau_n$ c) $\beta>\tau_n/\tau_T$ d) $\beta<\tau_n/\tau_T$ e) $\beta>\tau_T/\tau_n$

Q.1 Homework 5

- The I_C-V_{CE} characteristics of a bipolar junction transistor in the forward active region are similar to that of a

a) voltage controlled resistor
b) current controlled resistor
c) controlled current source
d) capacitor
e) inductor

- Consider a **pnp** BJT in the forward active region. The collector current will be constructed by the

a) holes drifting from base to collector through the base collector depletion region.
b) electrons diffusing in the base between the emitter and collector
c) electrons injected from the base into the collector
d) holes injected from the collector to the base
e) holes injected from the collector into the emitter

- Consider an **npn** BJT in the forward active region. The collector current of this device will be independent of

a) electrons injected from the emitter into the base
b) thermally generated electrons in the base
c) thermally generated holes in the collector
d) recombination lifetime of electrons in the base
e) it depends on all of the above

Q.1 Homework 5

- Consider an **npn** BJT in the forward active region. The base current of this device will not be affected by

a) recombination lifetime of electrons in the base
b) thermally generated holes in the collector
c) hole injection rate from base to emitter
d) electron injection rate from emitter into base
e) it is affected by all of the above

- Which of the following is wrong for a good npn BJT?

a) collector current is larger than the base current
b) emitter doping is higher than base doping
c) hole component of the emitter current is much lower than the electron component of the emitter current
d) base width is much shorter than the diffusion length of majority carriers in the base
e) collector current is nearly equal to the emitter current

- If the emitter and collector terminals of an npn BJT are interchanged, the current gain of the device (β) will be reduced since

a) base-emitter junction area is typically smaller than the base-collector junction area
b) collector doping is much larger than the base doping
c) electron component of the collector current will be much larger than the hole component of the collector current
d) collector current will be much larger than the base current
e) recombination lifetime of the electrons in the base will be reduced

Q.1 Homework 5

- In a pnp BJT in the reverse active region

a) $V_{EB}>0$, $V_{CB}>0$
b) $V_{EB}<0$, $V_{CB}<0$
c) $V_{EB}<0$, $V_{CB}>0$
d) $V_{EB}>0$, $V_{CB}<0$
e) None of the above

- Consider an npn BJT in the forward active region. If the Early effect is ignored, the collector current does not change if

a) V_{BE} is changed by keeping V_{CB} constant
b) V_{BE} is changed by keeping V_{CE} constant
c) V_{CE} is changed by keeping V_{CB} constant
d) V_{CE} is changed by keeping V_{BE} constant
e) None of the above

- Consider a Si npn BJT at the onset of deep saturation. The collector-emitter voltage of this BJT will be approximately

a) $E_g/q=1.1$ V
b) 0.2 V
c) 0.5 V
d) 0.7 V
e) -0.5 V

- Consider a **pnp** BJT. If the collector to emitter voltage (V_{CE}) of this BJT is negative and has a large magnitude (>0.7 V), this BJT operates in the

a) reverse saturation region
b) forward saturation region
c) reverse active region
d) forward active region
e) cut off region

Q.1 Homework 5

- If the base is open circuited in an npn BJT, the emitter and collector currents will be decreased almost to zero, since

a) there will be no injection of holes from base into the collector
b) the density of the ionized acceptors will be larger than that of holes in the base
c) the base transport factor will be reduced to zero
d) there will be no injection of holes from collector into the base
e) all of the above

- Which of the following mechanisms does not have any effect on the base current of a pnp BJT?

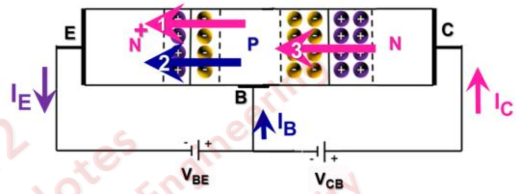
a) electron injection from the base into the emitter
b) hole recombination in the base
c) thermal generation of electrons in the collector
d) electron recombination in the base
e) all of the above have some effect on the base current

- Consider an **npn** BJT in the forward active region. The base current of this device

a) increases linearly with increasing V_{BE}
b) increases exponentially with increasing V_{CB}
c) increases exponentially with increasing V_{BE}
d) increases linearly with increasing V_{CB}
e) does not depend on V_{BE}

Q.1 Homework 5

Refer to the following figure to answer the following nine questions. Current components 1 and 3 are due to electrons, and current component 2 is hole current. $V_{BE}=V_{CB}=0.7$ V, T=300 K.



- Emitter injection efficiency is defined as

a) 1/(1+2)   b) 2/(1+2)   c) (1+2)/2   d) 3/1   e) 3/(1+2)

- Base transport factor is defined as

a) 3/2   b) 2/(1+2)   c) 3/1   d) 2/3   e) 1/(3-2)

- Current transfer ratio (α) is defined as

a) 3/1   b) 3/(1+2)   c) 2/1   d) 1/2   e) I_C/I_B

- Increasing the charge neutral base width (W_B)

a) Decreases 1   b) Decreases 2   c) Increases 2   d) Increases 3   e) none of the above

- If V_{CE} is increased by keeping the V_{BE} fixed,

a) 3 is decreased due to the increase in I_B
b) 3 is increased due to the increase in 2
c) 3 is decreased due to the increase in 1
d) 3 is decreased due to the increase in 2
e) 3 is increased due to the increase in 1

Q.1 Homework 5

- If the polarity of the V_{CB} is reversed,

a) the BJT goes into the reverse active region
b) the BJT goes into the saturation region
c) the direction of I_B is reversed
d) the direction of 2 is reversed.
e) none of the above

- If I_C=1 mA,

a) $\beta\cong 102$ b) $I_S\cong 7\times10^{-16}$ A   c) $I_E\cong 1.1$ mA   d) B=0.9   e) α=0.9

- If the collector doping is considerably increased,

a) base transport factor will considerably decrease
b) 3 will considerably decrease
c) the maximum allowed value of V_{CB} will considerably decrease
d) 1 will considerably decrease
e) none of the above

- Which of the following may not be observed if this BJT is fabricated with a low bandgap semiconductor?

a) Large leakage current
b) Small breakdown voltage
c) Large I_s
d) Large base transit time
e) all of the above will be observed

EE 212 Lecture Notes
Electrical and Electronics Engineering Department
Middle East Technical University
February 2016

Middle East Technical University, EE 212-Semiconductor Devices and Modeling, Lecture Notes

Q.1 Homework 5

- The base transport and emitter injection efficiency factor in an **npn** BJT are both equal to 0.995. The current gain of this BJT is

a) 199 b) 200 c)201 d) 99 e) 49

- If the emitter injection efficiency is 1.0 and and the thermaly generated collector saturation current is neglected, β of a BJT can be defined as

a) ∞ b) τ_t / τ_p c) τ_p / τ_t d) $e^{\tau p / \tau t}$ e) $e^{-\tau p / \tau t}$

- Consider an npn BJT in the forward active region. Decreasing the base width will

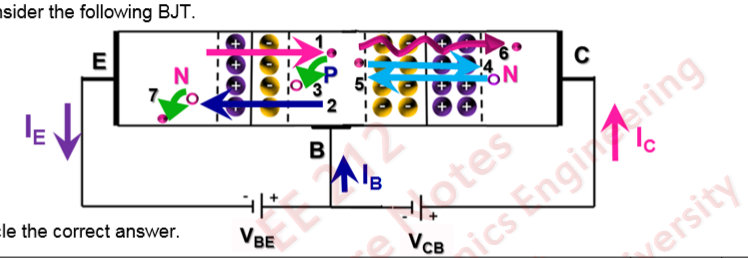
a) not change the hole component of the emitter current
b) increase the current gain
c) increase the current transfer ratio
d) increase the emitter injection efficiency
e) all of the above

- Common base characteristics of an npn BJT show

a) I_C-V_{CE} characteristics
b) I_C-V_{CB} characteristics
c) I_C-V_{BE} characteristics
d) I_B-V_{BE} characteristics
e) I_E-I_B characteristics

Q.2 Homework 5

Consider the following BJT.

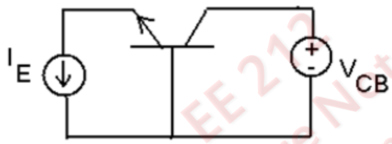


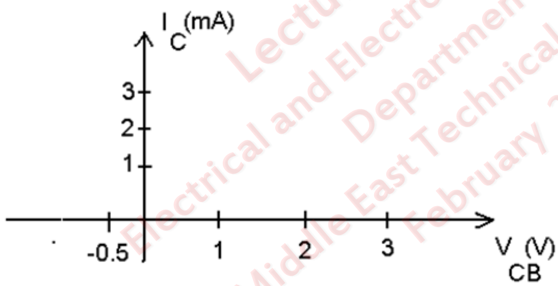
Circle the correct answer.

5 increases I_B	**True**	**False**
3 decreases β	**True**	**False**
3 increases the base transport factor	**True**	**False**
Decreasing base width increases **6**	**True**	**False**
Increasing base doping decreases **3**	**True**	**False**
Increasing emitter length decreases **7**	**True**	**False**
Decreasing emitter length decreases emitter injection efficiency	**True**	**False**
Increasing base doping increases **2**	**True**	**False**
6 does not depend on V_{BE}	**True**	**False**
B-C Junction brekdown voltage decreases with increasing collector doping	**True**	**False**

Q.3 Homework 5

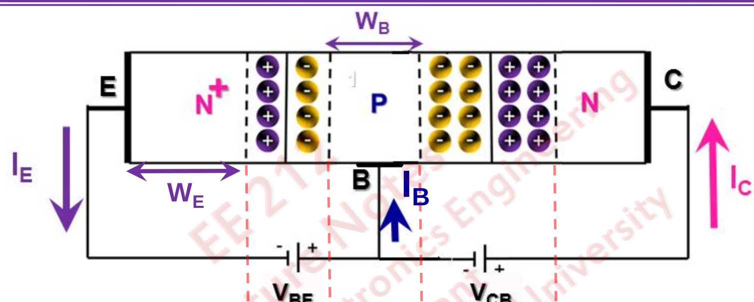
Plot I_C versus V_{CB} in the following circuit for I_E= 1, 2 and 3 mA.
α_F =1 for the BJT. **Ignore Early effect.**





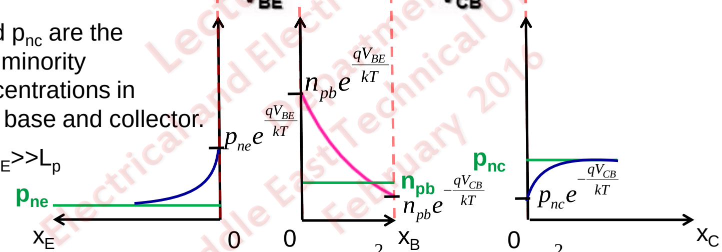
BJTs-Terminal Current Expressions

Ref. 5: 7.3.2



p_{ne}, n_{pb} and p_{nc} are the equilibrium minority carrier concentrations in the emitter, base and collector.

Assume W_E>>L_p



$$\text{Assume doping levels} >> n_i \Rightarrow p_{ne} = \frac{n_i^2}{N_{D_{Emitter}}}, \; n_{pb} = \frac{n_i^2}{N_{A_{Base}}}, \; p_{nc} = \frac{n_i^2}{N_{D_{Collector}}}$$

BJTs-Terminal Current Expressions

Ref. 5: 7.3.2

It can be shown (by solving the diffusion equations with the given boundary conditions) that

$$I_E = qA\left[\frac{D_{nb}n_{pb}}{L_{nb}}Coth(\frac{W_B}{L_{nb}}) + \frac{D_{pe}p_{ne}}{L_{pe}}\right](e^{\frac{qV_{BE}}{kT}}-1) - qA\frac{D_{nb}n_{pb}}{L_{nb}Sinh(\frac{W_B}{L_{nb}})}(e^{\frac{qV_{BC}}{kT}}-1)$$

$$I_C = -qA\left[\frac{D_{nb}n_{pb}}{L_{nb}}Coth(\frac{W_B}{L_{nb}}) + \frac{D_{pc}p_{nc}}{L_{pc}}\right](e^{\frac{qV_{BC}}{kT}}-1) + qA\frac{D_{nb}n_{pb}}{L_{nb}Sinh(\frac{W_B}{L_{nb}})}(e^{\frac{qV_{BE}}{kT}}-1)$$

$I_B = I_E - I_C$

D_{nb}: electron diffusion coefficient in the base, D_{pe}: hole diffusion coefficient in the emitter

L_{nb}: electron diffusion length in the base, L_{pe}: hole diffusion length in the emitter

The above equations assume that $A_{EB}=A_{BC}=A$ and $W_E >> L_{pe}$.

L_{pe} should be replaced with W_E if $W_E << L_{pe}$.

These equations are valid under any mode of operation.

BJTs-Terminal Current Expressions

Ref. 5: 7.3.2

In the forward active region operation with V_{BE}, $V_{CB} >> kT/q$, the terminal currents can be expressed as

$$I_E = qA\left[\frac{D_{nb}n_{pb}}{L_{nb}}Coth(\frac{W_B}{L_{nb}}) + \frac{D_{pe}p_{ne}}{L_{pe}}\right]e^{\frac{qV_{BE}}{kT}}$$

$$I_C = qA\frac{D_{nb}n_{pb}}{L_{nb}Sinh(\frac{W_B}{L_{nb}})}e^{\frac{qV_{BE}}{kT}}$$

$$I_B = I_E - I_C = qA\left[\frac{D_{nb}n_{pb}}{L_{nb}}Coth(\frac{W_B}{L_{nb}}) + \frac{D_{pe}p_{ne}}{L_{pe}}\right]e^{\frac{qV_{BE}}{kT}} - qA\frac{D_{nb}n_{pb}}{L_{nb}Sinh(\frac{W_B}{L_{nb}})}e^{\frac{qV_{BE}}{kT}}$$

D_{nb}: electron diffusion coefficient in the base

L_{nb}: electron diffusion length in the base

D_{pe}: hole diffusion coefficient in the emitter

L_{pe}: hole diffusion length in the emitter

BJTs-Terminal Current Expressions

If $W_B << L_{nb} \rightarrow$ Sinh $(W_B/L_{nb}) \approx W_B/L_{nb}$, Coth $(W_B/L_{nb}) \approx L_{nb}/W_B$

Hole component of a p-n junction current with long n-side

$$\underbrace{I_B = I_E - I_C = \underbrace{qA\frac{D_{nb}n_{pb}}{W_B}e^{\frac{qV_{BE}}{kT}}}_{\text{electron current injected into the base}} + \underbrace{qA\frac{D_{pe}p_{ne}}{L_{pe}}e^{\frac{qV_{BE}}{kT}}}_{\text{hole current injected into the emitter}}}_{I_E} - \underbrace{qA\frac{D_{nb}n_{pb}}{W_B}e^{\frac{qV_{BE}}{kT}}}_{\substack{\text{electron current reaching the collector} \\ \text{=electron current injected into the base} \\ I_C}} = \underbrace{qA\frac{D_{pe}p_{ne}}{L_{pe}}e^{\frac{qV_{BE}}{kT}}}_{\substack{\text{hole current injected into the emitter} \\ I_B}}$$

Q: Explain (qualitatively) the above result.

S: Since $W_B << L_{nb}$, all the electrons injected from the emitter into the base reach the collector since there is no recombination in the base. In this case, the only component of the base current is the hole current injected from the base into the emitter.

BJTs-Ebers-Moll Model

Ref. 5: 7.3.4

Let's now construct an equivalent circuit for the BJT which will be applicable under any biasing condition (F.A, SAT, cut-off or reverse active).

$$I_E = \underbrace{qA\left[\frac{D_{nb}n_{pb}}{L_{nb}}Coth(\frac{W_B}{L_{nb}}) + \frac{D_{pe}p_{ne}}{L_{pe}}\right]}_{I_{ES}}(e^{\frac{qV_{BE}}{kT}}-1) - \underbrace{qA\frac{D_{nb}n_{pb}}{L_{nb}Sinh(\frac{W_B}{L_{nb}})}}_{\alpha_R I_{CS}}(e^{\frac{qV_{BC}}{kT}}-1)$$

$$I_C = -\underbrace{qA\left[\frac{D_{nb}n_{pb}}{L_{nb}}Coth(\frac{W_B}{L_{nb}}) + \frac{D_{pc}p_{nc}}{L_{pc}}\right]}_{I_{CS}}(e^{\frac{qV_{BC}}{kT}}-1) + \underbrace{qA\frac{D_{nb}n_{pb}}{L_{nb}Sinh(\frac{W_B}{L_{nb}})}}_{\alpha_F I_{ES}}(e^{\frac{qV_{BE}}{kT}}-1)$$

Let's express the above equations as

$$\boxed{\begin{aligned} I_E &= I_{ES}(e^{\frac{qV_{BE}}{kT}}-1) - \alpha_R I_{CS}(e^{\frac{qV_{BC}}{kT}}-1) \\ I_C &= \alpha_F I_{ES}(e^{\frac{qV_{BE}}{kT}}-1) - I_{CS}(e^{\frac{qV_{BC}}{kT}}-1) \end{aligned}}$$

Note that $\alpha_F I_{ES} = \alpha_R I_{CS}$

These equations are known as the **Ebers-Moll model** for the npn BJT.

BJTs-Ebers-Moll Model

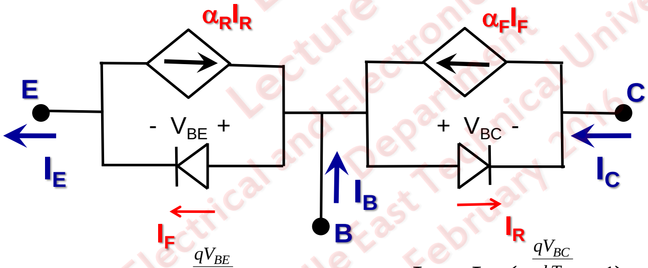
Ref. 5: 7.3.4

$$I_E = I_{ES}(e^{\frac{qV_{BE}}{kT}} - 1) - \alpha_R I_{CS}(e^{\frac{qV_{BC}}{kT}} - 1)$$

$$I_C = \alpha_F I_{ES}(e^{\frac{qV_{BE}}{kT}} - 1) - I_{CS}(e^{\frac{qV_{BC}}{kT}} - 1)$$

$\alpha_F I_{ES} = \alpha_R I_{CS}$

Transistor terminal currents (under any biasing condition) can be calculated if only three parameters (and of course the biasing voltages) are known. Now let's construct an equivalent circuit for the npn BJT based on the above equations.



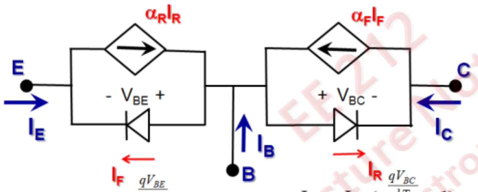
$$I_F = I_{ES}(e^{\frac{qV_{BE}}{kT}} - 1) \qquad I_R = I_{CS}(e^{\frac{qV_{BC}}{kT}} - 1)$$

I_{ES}: saturation current of the EB junction with B shorted to C (V_{BC}=0).
I_{CS}: saturation current of the CB junction with E shorted to B (V_{BE}=0).

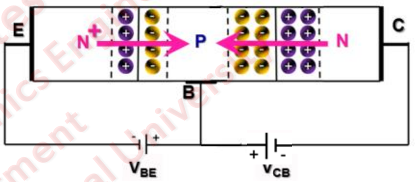
BJTs-Ebers-Moll Model

CHECK YOURSELF-POINT

Q: Explain (qualitatively) how the Ebers-Moll equivalent circuit models the behavior of the BJT under various biasing conditions.



$$I_F = I_{ES}(e^{\frac{qV_{BE}}{kT}} - 1) \qquad I_R = I_{CS}(e^{\frac{qV_{BC}}{kT}} - 1)$$



S: write

BJTs-Ebers-Moll Model

$$I_E = I_{ES}(e^{\frac{qV_{BE}}{kT}} - 1) - \alpha_R I_{CS}(e^{\frac{qV_{BC}}{kT}} - 1)$$

$$I_C = \alpha_F I_{ES}(e^{\frac{qV_{BE}}{kT}} - 1) - I_{CS}(e^{\frac{qV_{BC}}{kT}} - 1)$$

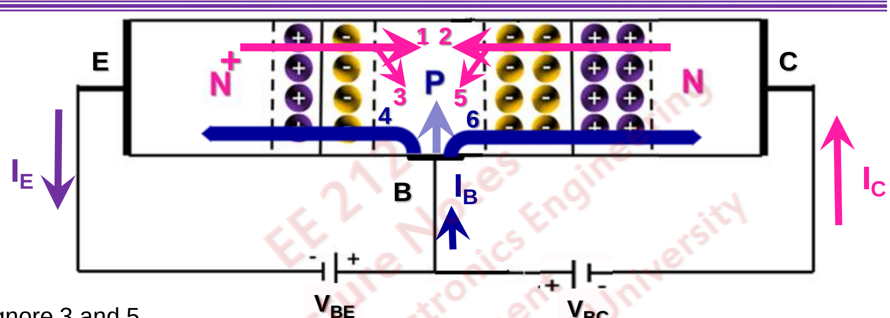
Define $\alpha_F I_{ES} = \alpha_R I_{CS} = I_S$

$$I_E = \frac{I_S}{\alpha_F}(e^{\frac{qV_{BE}}{kT}} - 1) - I_S(e^{\frac{qV_{BC}}{kT}} - 1) = I_S(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}) + \frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1)$$

$$I_C = I_S(e^{\frac{qV_{BE}}{kT}} - 1) - \frac{I_S}{\alpha_R}(e^{\frac{qV_{BC}}{kT}} - 1) = I_S(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}) - \frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1)$$

$$I_B = I_E - I_C = \frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1) + \frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1) \qquad (Note\ that\ \alpha = \frac{\beta}{\beta+1})$$

BJTs-Ebers-Moll Model



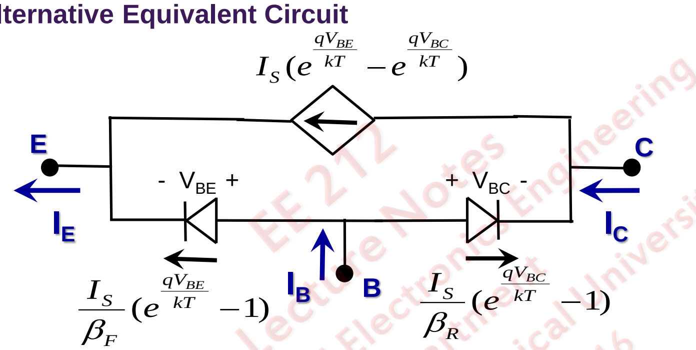
Ignore 3 and 5 for simplicity

$$I_E = \underbrace{I_S(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}})}_{1\text{-}2} + \underbrace{\frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1)}_{4}$$

$$I_C = \underbrace{I_S(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}})}_{1\text{-}2} - \underbrace{\frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1)}_{6}$$

$$I_B = \underbrace{\frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1)}_{6} + \underbrace{\frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1)}_{4}$$

Alternative Equivalent Circuit



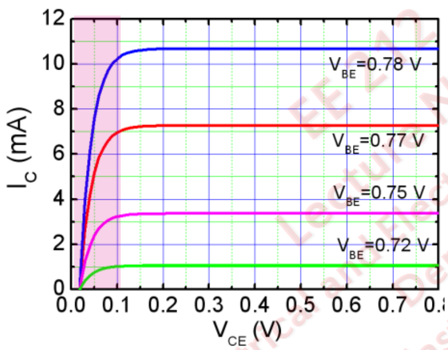
$$I_E = I_S(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}) + \frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1)$$

$$I_C = I_S(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}) - \frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1)$$

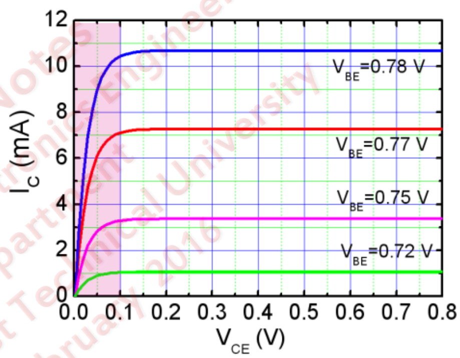
$$I_B = \frac{I_S}{\beta_R}(e^{\frac{qV_{BC}}{kT}} - 1) + \frac{I_S}{\beta_F}(e^{\frac{qV_{BE}}{kT}} - 1)$$

CHECK YOURSELF-POINT

Q: Explain (qualitatively) the following difference between the I_C-V_{CE} characteristics of npn BJTs with different β_R.



I_S=1x10^{-15} A, β_F=100, β_R=1



I_S=1x10^{-15} A, β_F=100, β_R=10

S: write

BJTs-Ebers-Moll Model

CHECK YOURSELF-POINT

Q: Construct the Ebers-Moll model for the pnp BJT (equivalent circuit and the terminal current expressions).

S: *write*

BJTs-Ebers-Moll Model

Ref. 4: 5.9.2

Now, let's simplify the Ebers-Moll model for the npn BJT for F.A. Region operation with $V_{BE} >> kT/q$, $V_{CB} >> kT/q$

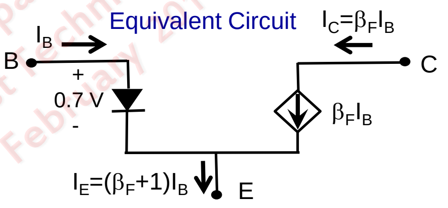
$$I_E = I_S\left(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}\right) + \frac{I_S}{\beta_F}\left(e^{\frac{qV_{BE}}{kT}} - 1\right) \cong I_S e^{\frac{qV_{BE}}{kT}} + \frac{I_S}{\beta_F} e^{\frac{qV_{BE}}{kT}} = \frac{\beta_F + 1}{\beta_F} I_S e^{\frac{qV_{BE}}{kT}} = \frac{I_S e^{\frac{qV_{BE}}{kT}}}{\alpha_F}$$

$$I_C = I_S\left(e^{\frac{qV_{BE}}{kT}} - e^{\frac{qV_{BC}}{kT}}\right) - \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{kT}} - 1\right) \cong I_S e^{\frac{qV_{BE}}{kT}} = \alpha_F I_E$$

$$(Note\ that\ \alpha_F = \frac{\beta_F}{\beta_F + 1})$$

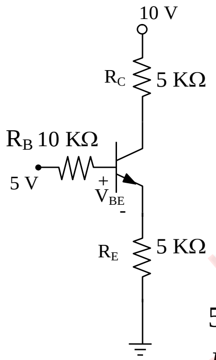
$$I_B = \frac{I_S}{\beta_R}\left(e^{\frac{qV_{BC}}{kT}} - 1\right) + \frac{I_S}{\beta_F}\left(e^{\frac{qV_{BE}}{kT}} - 1\right) \cong \frac{I_S e^{\frac{qV_{BE}}{kT}}}{\beta_F} = \frac{I_C}{\beta_F}$$

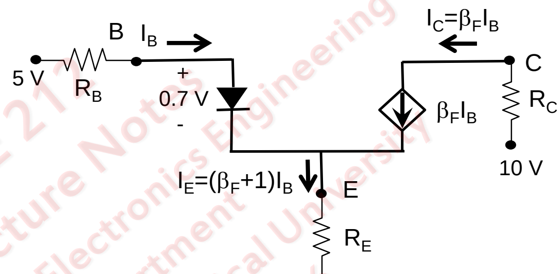
$$I_C = \beta_F I_B, \qquad I_E = (\beta_F + 1) I_B$$



Q: Find the collector current of the BJT in the following circuit. β_F=100.

S:





Assume F.A. Region Operation.

$$5\ V = I_B R_B + 0.7\ V + (\beta_F + 1) I_B R_E$$

$$I_B = 6.4\ \mu A,\ \ I_C = \beta_F I_B = 0.64\ mA$$

Obviously, V_{BE} >0 V.

$$V_C = 10\ V - R_C I_C = 6.8\ V$$

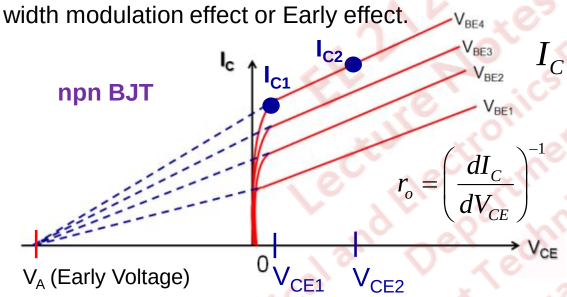
$$V_B = 5\ V - I_B R_B = 4.9\ V$$

$$V_B > V_E,\ V_C > V_B \Rightarrow \ \text{F.A. Region}$$ ✓

 Ref. 4: 5.10.1, 5.10.2

Base Width Modulation

So far we have considered the BJT as an ideal current source in the forward active region assuming that the collector current does not change with V_{CE}. On the other hand, I_C-V_{CE} characteristics of a real BJT are as shown below due to the change in the base width with the reverse bias voltage across the B-C junction. This known as the base width modulation effect or Early effect.



$$r_o = \left(\frac{dI_C}{dV_{CE}}\right)^{-1}$$

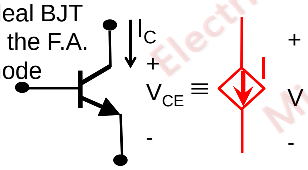
$$I_C \cong I_S e^{\frac{qV_{BE}}{kT}} \ \ \text{in F.A. region}$$

$$\frac{I_{C1}}{\underbrace{V_A + V_{CE1}}_{\approx V_A}} = \frac{I_{C2}}{\underbrace{V_A + V_{CE2}}_{\approx V_A + V_{CB}}}$$

zero V_{CB} I_S

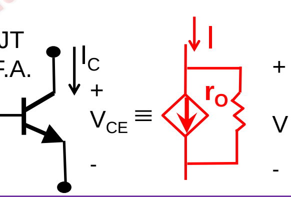
$$\frac{I_{C2}}{I_{C1}} \cong \frac{V_A + V_{CB}}{V_A} \rightarrow I_S = I_{SO}\left(1 + \frac{V_{CB}}{V_A}\right)$$

Ideal BJT in the F.A. mode

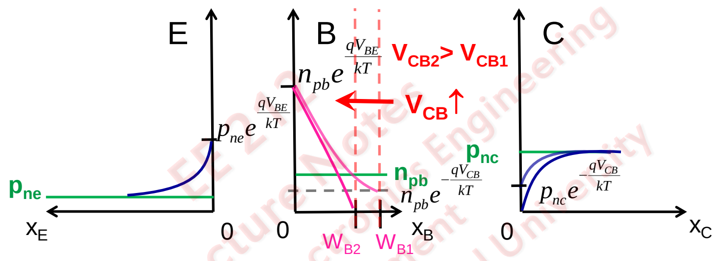


Ideal current source

Real BJT in the F.A. mode



Let's see how the collector current increases with increasing V_{CE} in the F.A. region.



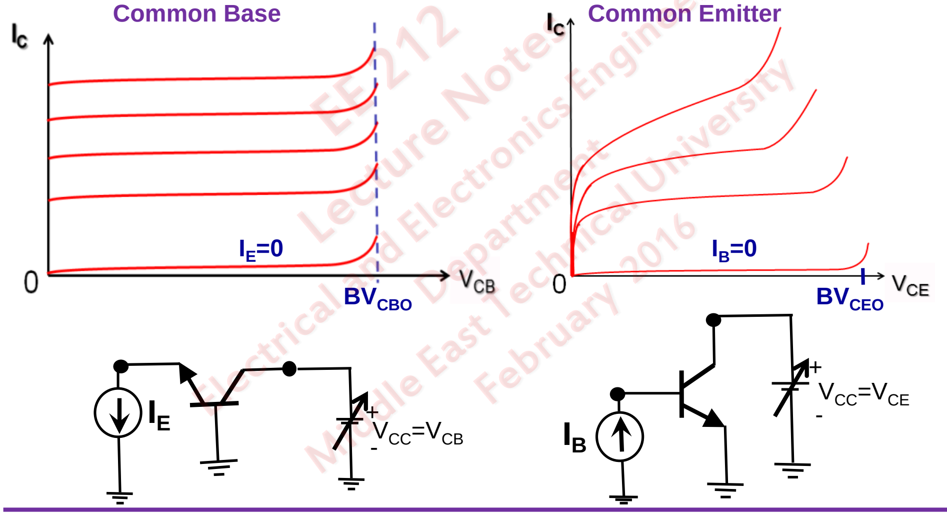
As V_{CE} is increased by keeping the V_{BE} constant, the reverse bias voltage (V_{CB}) across the BC junction is also increased. Due to the larger excess minority carrier concentration gradient in the base, I_{En}, being proportional to $d\delta n(x_B)/dx_B$, attains a larger value.

It should be noted that base width reduction also increases the current gain (β) of the device due to the increase in the base transport factor (less recombination in the base).

Ref. 5: 7.5.3

Avalanche Breakdown

If the reverse bias across a junction (BE or BC) exceeds the breakdown voltage, avalanche breakdown occurs resulting in loss of useful transistor action.



BJTs-Secondary Effects

Q: Which junction (BE or BC) has a larger breakdown voltage?

S: Remember that emitter is heavily doped in order to have a good emitter injection efficiency. Therefore the emitter doping is higher than the collector doping making the avalanche breakdown voltage of the BC junction larger than that of the BE junction.

This does not create a problem for a BJT operating in the forward active region since the BE junction is forward biased in this mode.

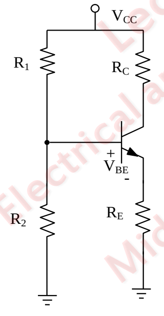
Collector doping must be selected by taking the breakdown voltage (maximum BC junction reverse bias) into account.

BJTs-Biasing

Biasing: In order to use the BJT in a specific mode of operation, proper biasing voltages must be applied to the device terminals. As an example, the device is used in the forward active mode (as a controlled current source) for the amplification of ac signals.

Biasing establishes the operating point of the transistor which determines the device parameters governing the characteristics of the circuit such as the gain, input resistance and the output voltage swing of an amplifier.

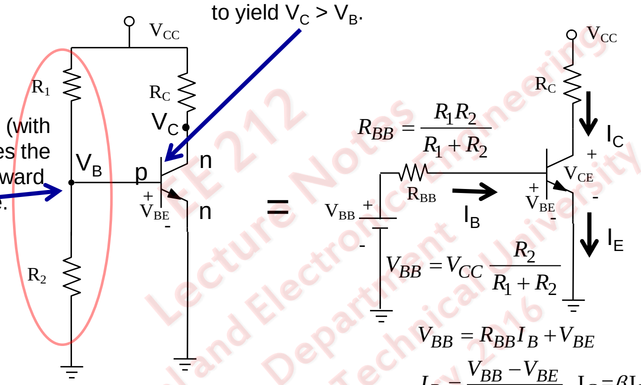
Therefore, the biasing circuit must be carefully designed to achieve the optimum circuit Performance.



An example circuit biasing the BJT in the F. A. region using a DC power supply (V_{CC}) and resistors.

BJT operates in the F.A. region, if R_C is selected properly to yield $V_C > V_B$.

Voltage divider (with V_{CC}) establishes the BE junction forward biasing voltage.



$$R_{BB} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{BB} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$V_{BB} = R_{BB} I_B + V_{BE}$$

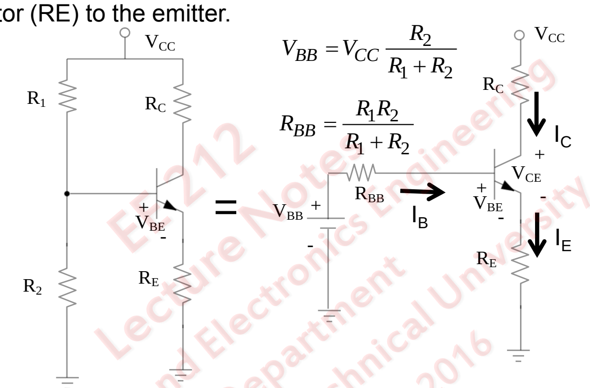
$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB}},\ I_C = \beta I_B,\ I_E = (\beta+1) I_B,$$

$$V_{CE} = V_{CC} - I_C R_C \text{ , Q-point: } (I_C \text{ , } V_{CE})$$

A single DC power supply is sufficient to forward bias the BE junction and reverse bias the BC junction at the same time.

I_B is dependent on V_{BE}, I_C is dependent on $\beta \Rightarrow$ this is not a good design since it does not provide Q-point (bias) stability. As an example, if the BJT is replaced with another one with a different β, a different Q-point is measured or the change in the temperature (changing the BJT characteristics) results in a shift of the Q-point.

Let's add a resistor (RE) to the emitter.



$$V_{BB} = V_{CC}\frac{R_2}{R_1 + R_2}$$

$$R_{BB} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{BB} = R_{BB} I_B + V_{BE} + R_E I_E = R_{BB} I_B + V_{BE} + R_E(\beta+1) I_B$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta+1)R_E},\ I_C = \beta I_B,\ I_E = (\beta+1) I_B,\ V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Q-point: $(I_C \text{ , } V_{CE})$

Assume large β

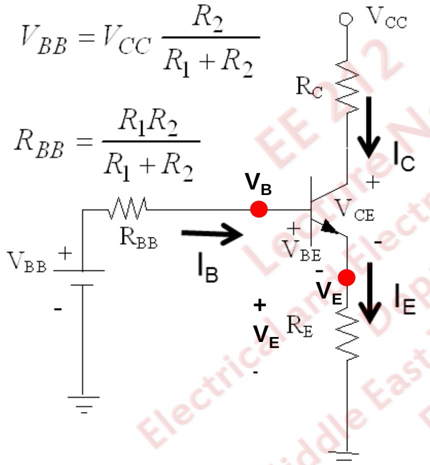
I_E and I_C are stabilized!

$$\text{if } (\beta+1)R_E \gg R_{BB} \text{ and } V_{BB} \gg V_{BE},\ I_B \cong \frac{V_{BB}}{(\beta+1)R_E},\ I_C \cong I_E \cong \beta I_B \cong \frac{V_{BB}}{R_E}$$

Q: How does the addition of R_E provide Q-point stability?;

$$V_{BB} = V_{CC}\frac{R_2}{R_1+R_2}$$

$$R_{BB} = \frac{R_1R_2}{R_1+R_2}$$



Let's assume that I_C and I_E are **increased** for some reason. This will increase V_E resulting in a smaller V_{BE} if V_B is almost fixed. Decrease in V_{BE} calls for a **decrease** in I_C and I_E. The feedback action of R_E keeps I_C (and V_{CE}) constant.

Q: How do I assure a constant V_B?

S:

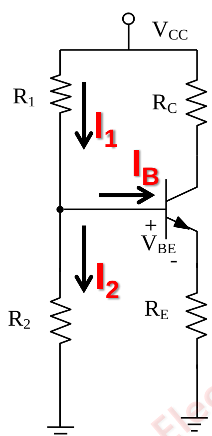
$$V_B = V_{BB} - I_BR_{BB} = \underset{\uparrow \text{ fixed}}{V_{BB}} - \frac{I_E}{\beta+1}\underset{\uparrow}{R_{BB}}$$

R_{BB} should be small enough to have negligibly small voltage drop on R_{BB}

$$V_B \cong V_{BB} = V_{CC}\frac{R_2}{R_1+R_2} \cong V_E = I_ER_E >> \frac{I_E}{\beta+1}R_{BB} \Rightarrow (\beta+1)R_E >> R_{BB}$$

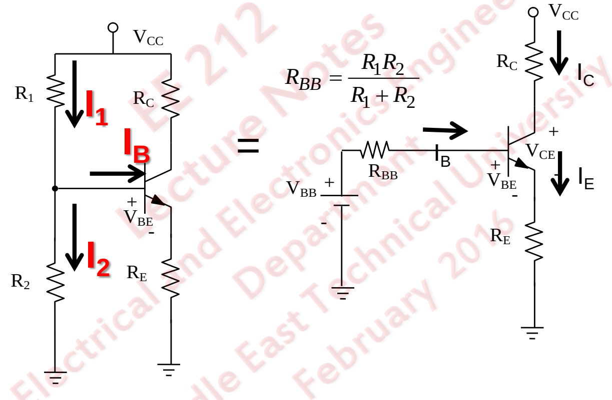
CHECK YOURSELF-POINT

Q: Show that the above condition is equivalent to having $I_1 >> I_B$ and $I_1 \approx I_2$.



S: write

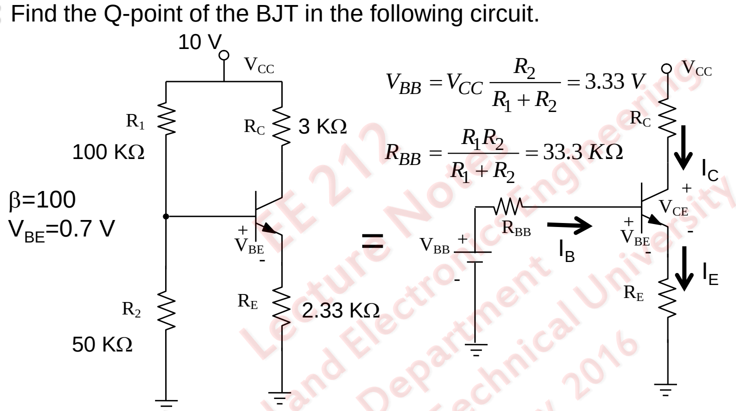
Do not choose R_1 and R_2 too low in order to achieve a small R_{BB}. Small R_1 and R_2 leads to a large current sink from the power supply as well as a low small signal input resistance (as we will see later).



$$R_{BB} = \frac{R_1 R_2}{R_1 + R_2}$$

Choosing R_1 and R_2 to yield $I_1 \approx I_2 \approx I_C/10$ will be acceptable under typical conditions.

Q: Find the Q-point of the BJT in the following circuit.



$$V_{BB} = V_{CC}\frac{R_2}{R_1 + R_2} = 3.33\ V$$

$$R_{BB} = \frac{R_1 R_2}{R_1 + R_2} = 33.3\ K\Omega$$

$$V_{BB} = R_{BB} I_B + V_{BE} + R_E I_E = R_{BB} I_B + V_{BE} + R_E(\beta + 1) I_B$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta + 1) R_E} = \frac{3.33 - 0.7}{33.3 + 101x2.33} \cong 10\ \mu A$$

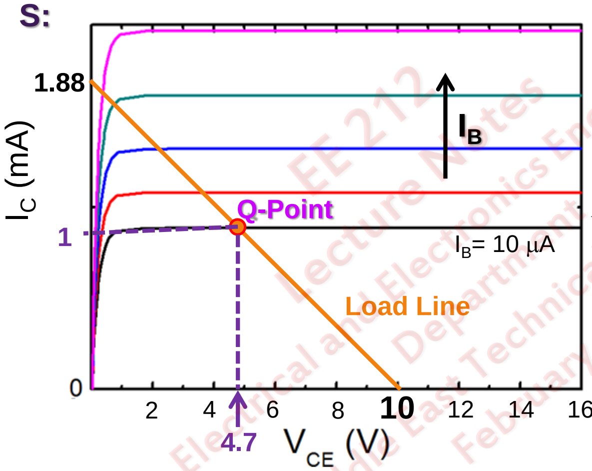
$I_C = \beta I_B = 1$ mA $\cong I_E$, $V_{CE} = V_{CC} - I_C R_C - I_E R_E \cong 4.7$ V

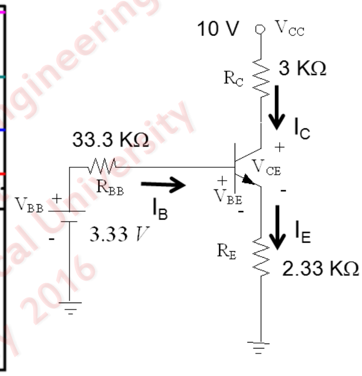
Q-point: (1 mA, 4.7 V)

BJTs-Biasing

Q: How do I find the Q-point, if the BJT I-V characteristics are provided?

S:



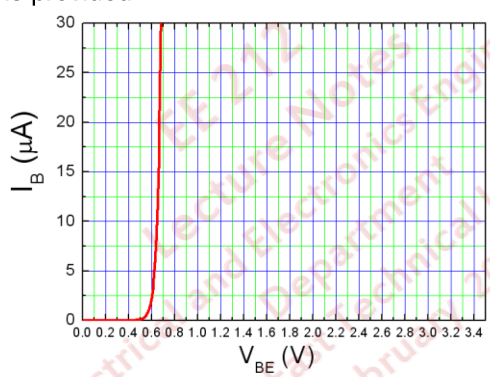


$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \cong V_{CC} - I_C (R_C + R_E) = 10\text{ V} - I_C \times 5.33\,K\Omega$$

BJTs-Biasing

CHECK YOURSELF-POINT

Q: How do you perform a more accurate analysis if the I_B-V_{BE} characteristic of the BJT is provided.



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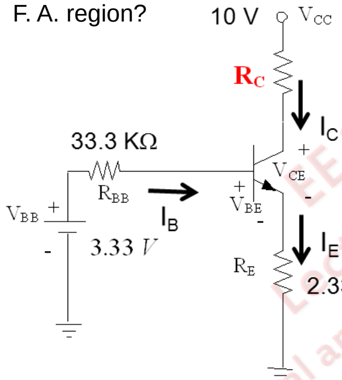
BJTs-Biasing

Q: How does the Q-point change when R_C is increased by keeping the BJT in the F. A. region?



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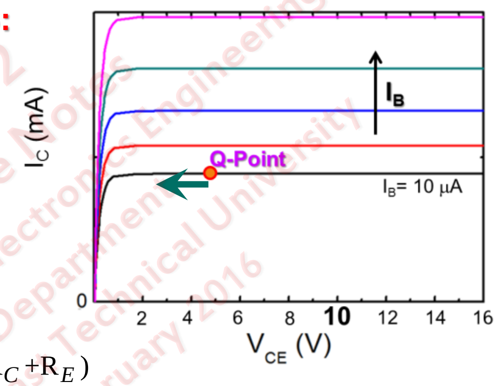
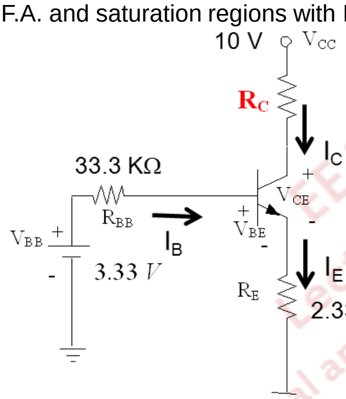


$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \cong V_{CC} - I_C (R_C + R_E)$$

Note that I_C is independent of V_{CB} (and V_{CE} with fixed with V_{BE}) as long as the BJT remains in the forward active region. I_C is dependent on V_{BB}, R_{BB} and R_E through V_{BE} and I_B. It does not depend on R_C since variation in R_C is reflected as a change in V_{CE} which (ideally) has no effect on I_C in the F. A. region.

BJTs-Biasing

Q: Find the required value of R_C to operate the BJT on the boundary between the F.A. and saturation regions with I_B=10 µA.



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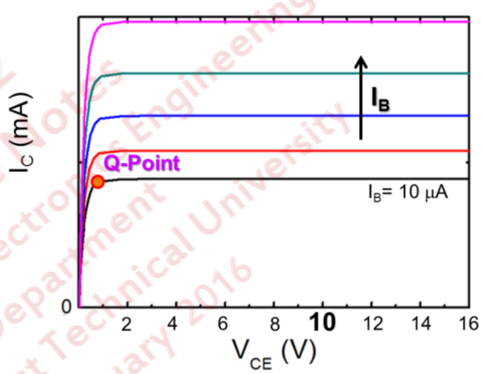


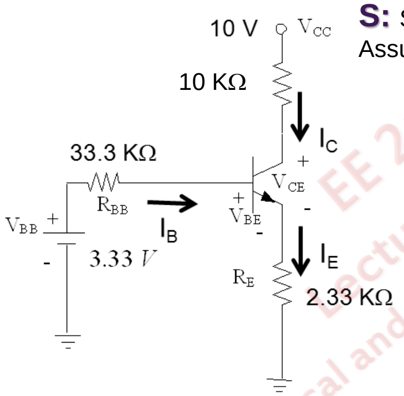
Let's define the boundary between the F.A. and saturation regions with V_{CE}=0.2 V.

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \cong V_{CC} - I_C (R_C + R_E) = 10 - 1\text{ mA}(R_C + 2.33\text{ K}\Omega) = 0.2\text{V}$$

$$R_C \cong 7.5 K\Omega$$

Note that I_C is constant at 1 mA up to the boundary.

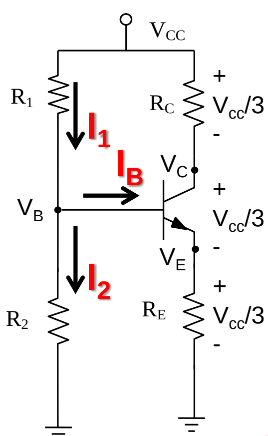
Q: Find the collector current in the following circuit.



S: Since R_C >7.5 KΩ, BJT is in the saturation region. Assume $V_{CEsat} \approx 0.2$ V.

$$3.33V = 33.3KI_B + 0.7V + 2.33KI_E$$
$$10V = 10KI_C + V_{CEsat} + 2.33KI_E$$
$$I_E = I_C + I_B$$
$$\textit{Solve to get}$$
$$I_E = 0.81 \text{ mA}$$
$$I_C = 0.79 \text{ mA}$$
$$I_B = 0.02 \text{ mA}$$
$$I_C \neq \beta I_B$$

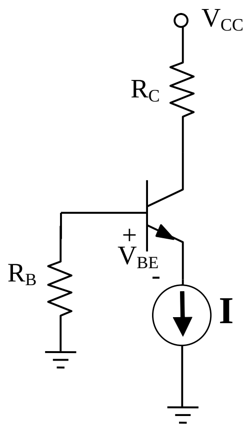
If R_C is increased to 20 KΩ, I_E=0.488 mA, I_C=0.443 mA, I_B=0.045 mA.



In order to achieve a specific I_C with a given β_{min} and V_{CC}

- $R_E = V_{CC}/(3I_E) \approx V_{CC}/(3I_C)$
- Make $I_1 >> I_{Bmax} = I_C/\beta_{min}$, choose $I_1 = I_C/10$ if β is sufficiently large (make sure $I_1 \geq 10\, I_B$) $\rightarrow V_B \approx V_{cc}R_2/(R_1+R_2) \approx V_E = V_{cc}/3$
- $R_1 + R_2 \cong \dfrac{V_{CC}}{I_1}$, $\quad V_B \cong V_{CC}\dfrac{R_2}{R_1+R_2} = \dfrac{V_{CC}}{3}$,

  Find R_1 and R_2.
- $R_c = \dfrac{V_{CC} - V_c}{I_C}$



Current I forced through the emitter develops a forward biasing voltage across the BE junction.

The BJT operates in the F.A. Region (Is there any other possible mode of operation in this configuration?)

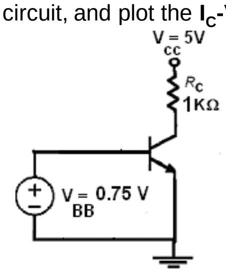
Main Advantage:

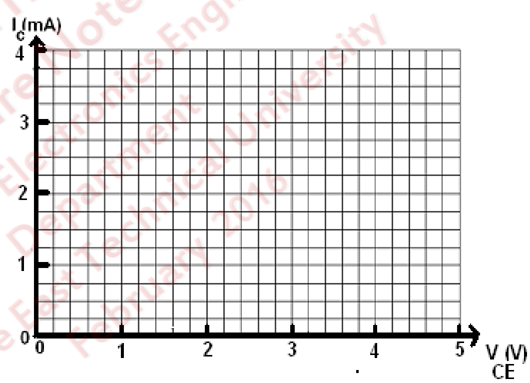
Stable emitter and collector currents with the freedom of selecting R_B large (high input resistance).

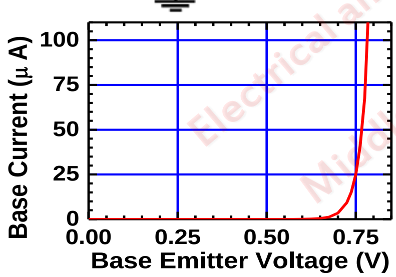
BJTs-EXERCISE QUESTIONS

Q.1 (to be solved on white board) **I_B-V_{BE}** characteristic of the npn BJT used in the following circuit is given below. Emitter injection efficiency and base transport factor of the BJT are both equal to **0.995**. Contribution of the thermally generated minority carriers around the B-C depletion region to base current is negligible.

a) Find the **collector current** and **collector-emitter voltage** of the BJT in the following circuit, and plot the **I_C-V_{CE} characteristic** of the BJT on the provided graph.

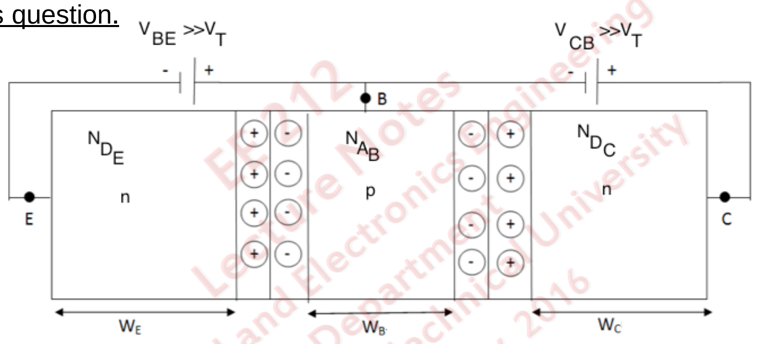






S: write

Q.2: (to be solved on white board) Consider the following Si n-p-n bipolar junction transistor. Do not use the Ebers-Moll equations to answer any part of this question.



a) Ignore recombination in the base and the contribution of the thermally generated minority carriers to the collector current. Derive the expression for the collector current in terms of n_i, V_{BE}, W_B, D_n (electron diffusion coefficient in the base), junction cross sectional area (A) and the other necessary parameters. Show complete work and simplify your expression (V_{BE} and $V_{CB}>>V_T$). You do not need to derive the expressions for the excess carrier distributions.

BJTs-EXERCISE QUESTIONS

S:

BJTs-EXERCISE QUESTIONS

b) Express the saturation current (I_s) of this transistor under the conditions of part (a).

S:

c) CIRCLE the correct answer. Ignore the Early Effect.

I_c is independent of V_{CB} .	**YES**	**NO**
N_{AB} does not affect the base transport factor.	**YES**	**NO**
BE junction diffusion capacitance is independent of W_B.	**YES**	**NO**
I_c is the drift current of the BC junction.	**YES**	**NO**
Injected electrons travel through charge neutral base mostly by diffusion.	**YES**	**NO**
Thermally generated minority carriers around BC junction decreases I_B.	**YES**	**NO**
The above BJT is slower than a pnp BJT.	**YES**	**NO**
I_c is kept constant if V_{BE} decreases and V_{CB} increases by same amount.	**YES**	**NO**

d) What is the emitter injection efficiency of this transistor if W_E=W_B, N_{DE}=N_{AB} and there is no recombination in the emitter and base .

S:

e) Find the β of the transistor under the conditions of part (d) and explain your result qualitatively based on the operational principles of BJT. Also explain how you can improve the performance of this transistor.

S:

Explanation:

f) How does N_{DC} affect the I_C-V_{CE} characteristics of this device under large collector to emitter voltages? Explain what happens if N_{DC} is increased.

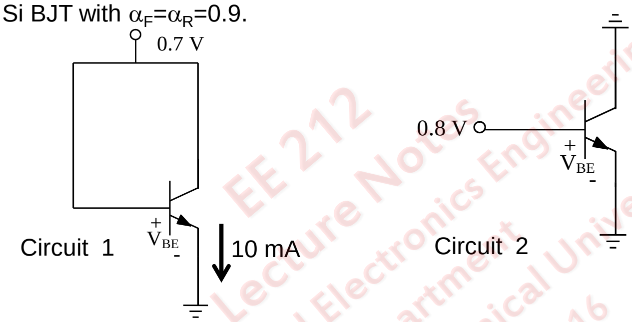
S:

g) Now let's assume that W_E=W_B=W_C, N_{DE}=N_{AB}=N_{DC}, EB junction area=BC junction area and no recombination takes place in the device. Express V_{CB} (in terms of V_{BE}) required to have zero <u>electron diffusion current</u> in the base.

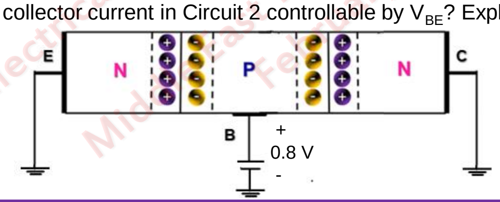
S:

BJTs-EXERCISE QUESTIONS

Q.3 (to be solved on white board) The following circuits are constructed by using the same Si BJT with $\alpha_F=\alpha_R=0.9$.



a) Use the Ebers Moll Model to determine I_E, I_B and I_C in Circuit 2.
b) What is the operation region of the BJT in Circuit 2.
c) Show and label the electron and hole flow directions due to minority carrier injection for the BJT of Circuit 2. Is the collector current in Circuit 2 controllable by V_{BE}? Explain your reasoning.



BJTs-EXERCISE QUESTIONS

S: write

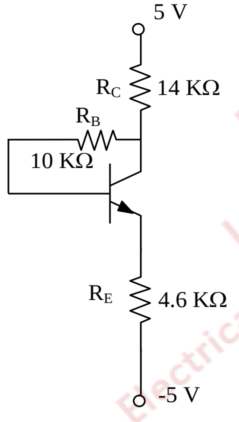
BJTs-EXERCISE QUESTIONS

Q.4 (to be solved on white board) Find the expressions for the base transit time and the diffusion capacitance of an npn BJT operating in the F. A. Region.

S: write

BJTs-EXERCISE QUESTIONS

Q.5 (to be solved on white board) Find the emitter current and V_{CE} in the following circuit constructed with a BJT having a very large β. Comment on the value of V_{CE} (note that a small current is flowing through R_B) .



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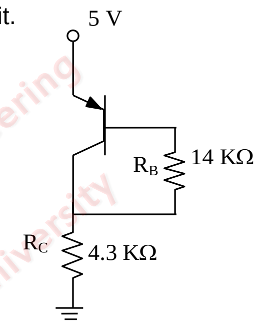
Electrical and Electronics Engineering Department
Middle East Technical University
February 2016

BJTs-EXERCISE QUESTIONS

Q.6 (to be solved on white board) Consider the following circuit.



a) What are the possible modes of operation for the BJT?

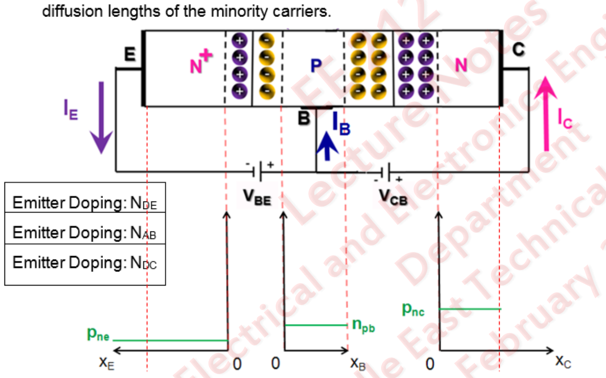
S:

b) Find operating (Q) point of the transistor (β=30).

S:

Q.1 Homework 6 (Estimated Time To Complete < 100 min.)

Consider the following BJT biased in the F.A. region. Plot the minority carrier distributions in the emitter, base and collector on the figure provided below. Provide the expressions for the minority carrier concentrations at the edges of the depletion regions **in terms of the doping densities** and other necessary parameters. Minority carrier distribution in the base must reflect recombination. Emitter and collector lengths are much larger than the diffusion lengths of the minority carriers.



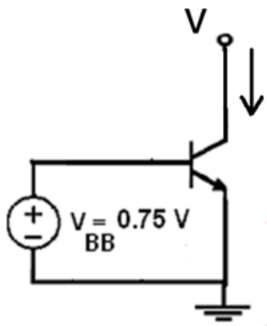
P_{ne}: equilibrium hole concentration in the emitter

n_{pb}: equilibrium electron concentration in the base

p_{nc}: equilibrium hole concentration in the collector

Q.2 Homework 6

Write the conditions required for the following npn BJT to behave as an ideal 2 mA current source.



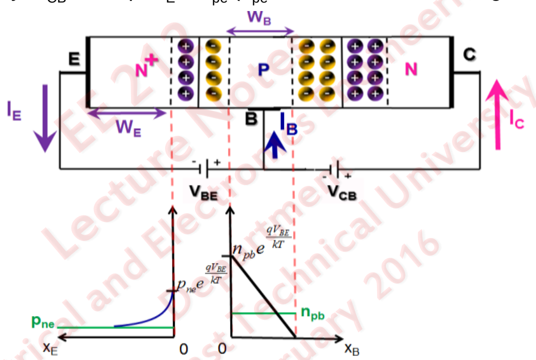
V_A:

V:

I_S:

Q.3 Homework 6

Consider the following BJT with the given minority carrier distributions in the emitter and base. p_{ne} and n_{pb} are the equilibrium minority carrier concentrations in the emitter and base, respectively. V_{CB}>>kT/q, W_E>>L_{pe} (L_{pe} is the hole diffusion length in emitter).

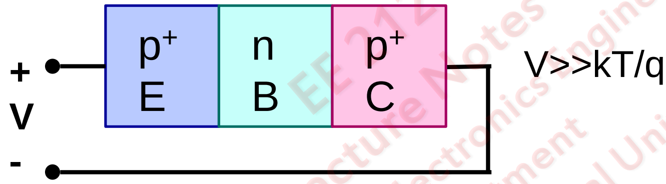


i) Derive the expression for the emitter injection efficieny of the device in terms of the electron diffusion coefficient in the base (D_{nb}), the hole diffusion coefficient in the emitter (D_{pe}), hole recombination lifetime in the emitter (τ_{pe}), p_{ne}, n_{pb} and the other necessary parameters.

ii) Use your answer to part (i) to find the expression for the β of the device in terms of the electron diffusion coefficient in the base (D_{nb}), the hole diffusion coefficient in the emitter (D_{pe}), hole recombination lifetime in the emitter (τ_{pe}), p_{ne}, n_{pb} and the other necessary parameters.

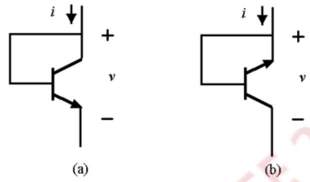
Q.4 Homework 6

Consider a symmetrical p^+-n-p^+ BJT biased as shown below. Calculate the emitter-base voltage at 300 K bu using the generalized terminal current expressions.
Hint: Think about the biasing of the E-B and B-C junctions.



Q.5 Homework 6

Consider the following BJTs.

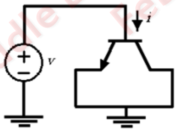


i) Derive expressions for the *i-v* characteristics of the transistors shown in figures (a) and (b) in terms of I_s, α_F, and α_R.

ii) When the two transistors in figures (a) and (b) are identical, and the currents are made equal to a value I, it is found that the voltage *V* is 0.7 V for the diode in (a) and 0.6 V for the diode in (b). Find α_F / α_R.

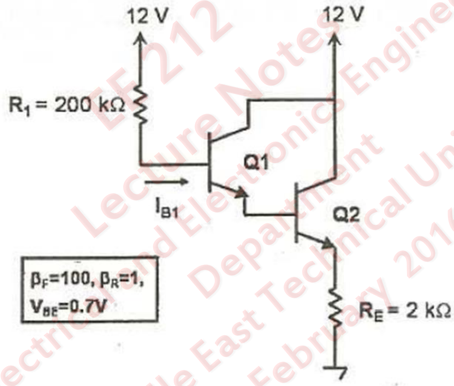
iii) Assume that the ratio α_F/α_R is obtained for an n^+pn^+ transistor (emitter doping density =collector doping density). What does this ratio imply about the transistor geometry?

iv) For the transistor circuit shown below, find expressions for i_E and i in terms of V, I_s, β_R and β_F. Find the ratio of the two currents (i / i_E). Assume V>>0 and β_F >>β_R.



Q.6 Homework 6

Find I_{B1} in the circuit given below.



CHAPTER V

MOS Capacitor

and

MOSFET

References

1) B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th Edition, Prentice Hall, 2006.

2) J. Singh, *Semiconductor Devices An Introduction*, McGraw-Hill, 1994.

3) R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996.

4) A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, 5th Edition 2004.

5) R. C. Jaeger and T. N. Blalock, Microelectronic Circuit Design,Mc Graw Hill, 2nd Edition 2004.

6) R. T. Howe and C. G. Sodini, *Microelectronics, An Integrated Approach, Prentice Hall Electronics and VLSI Series*, 1997.

The Role of This Chapter

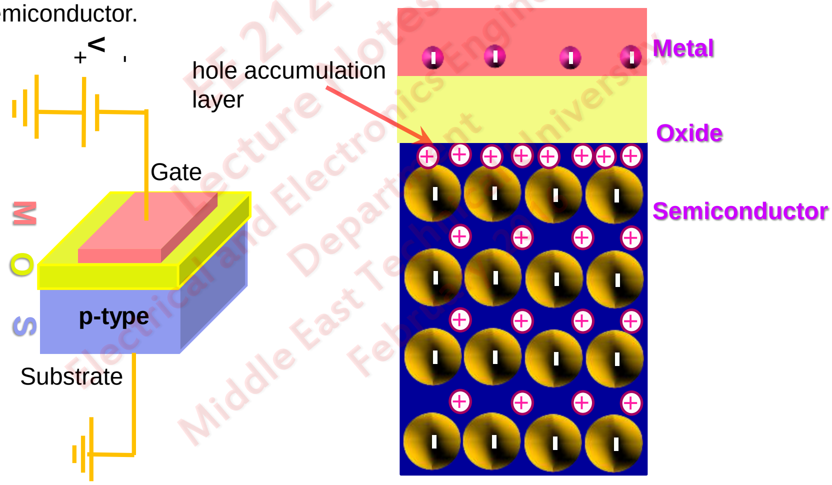
Metal oxide semiconductor field effect transistor (MOSFET) is the most widely used electron device that has greatly accelerated the development of electronics. The construction of the fast computers and many other electronic equipment we use today has been made possible mainly through the improvements in the MOSFET technology. This chapter presents an introductory level discussion on MOSFETs including preliminary device physics, operational principles and biasing.

We will start by introducing the MOS capacitor which forms the voltage controllable channel of the MOSFET. Understanding the characteristics of the MOS capacitor will allow us comprehend the operational principles of MOSFETs.

MOS Capacitor-Accumulation

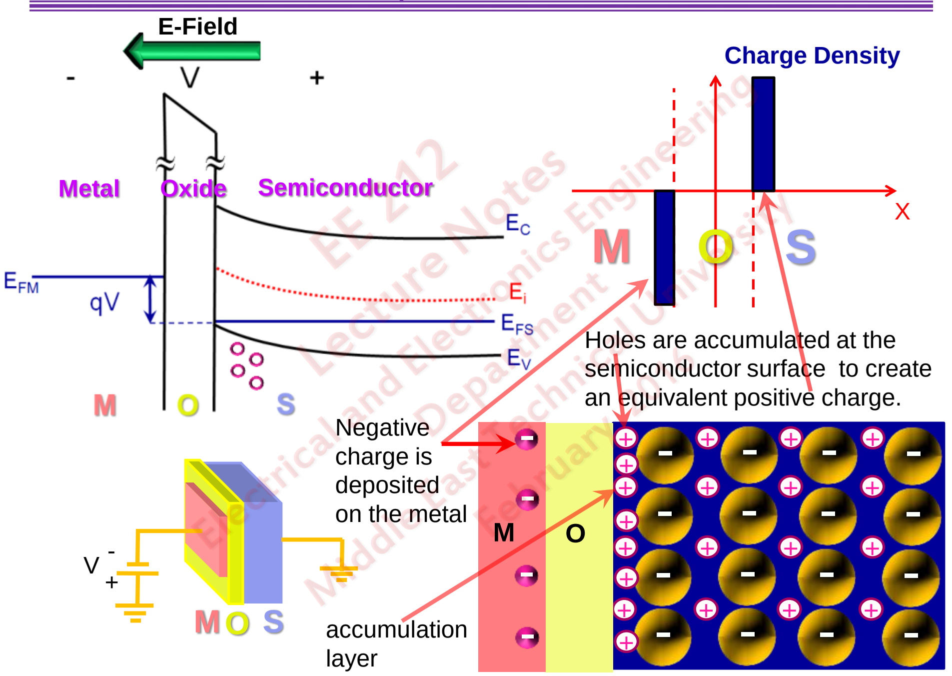
Ref. 3: 16.1, 16.2

Consider a Metal/Oxide (Insulator)/p-type Semiconductor (MOS) structure. If a bias voltage is applied to have negative potential on the metal (gate) with respect to the semiconductor (substrate), negative charge appears on the gate. This negative charge must be balanced with positive charge on the semiconductor side. This balance is achieved by attracting the positive charge (holes) to the interface between the oxide and the semiconductor.



MOS Capacitor-Accumulation

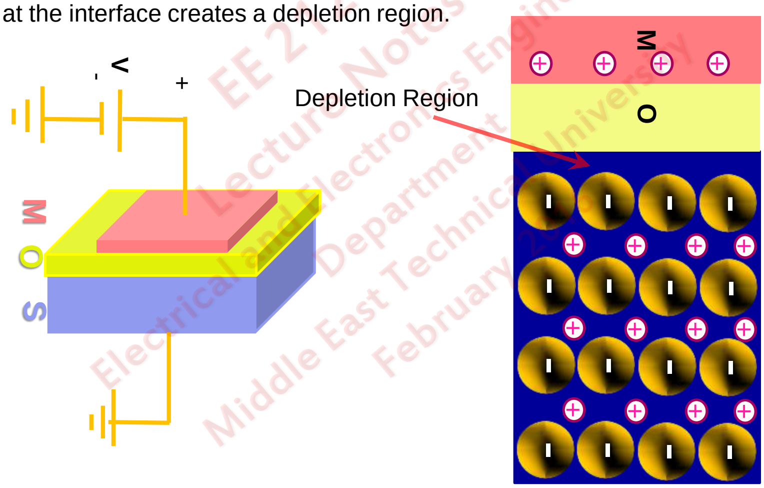
Ref. 3: 16.1, 16.2



MOS Capacitor-Depletion

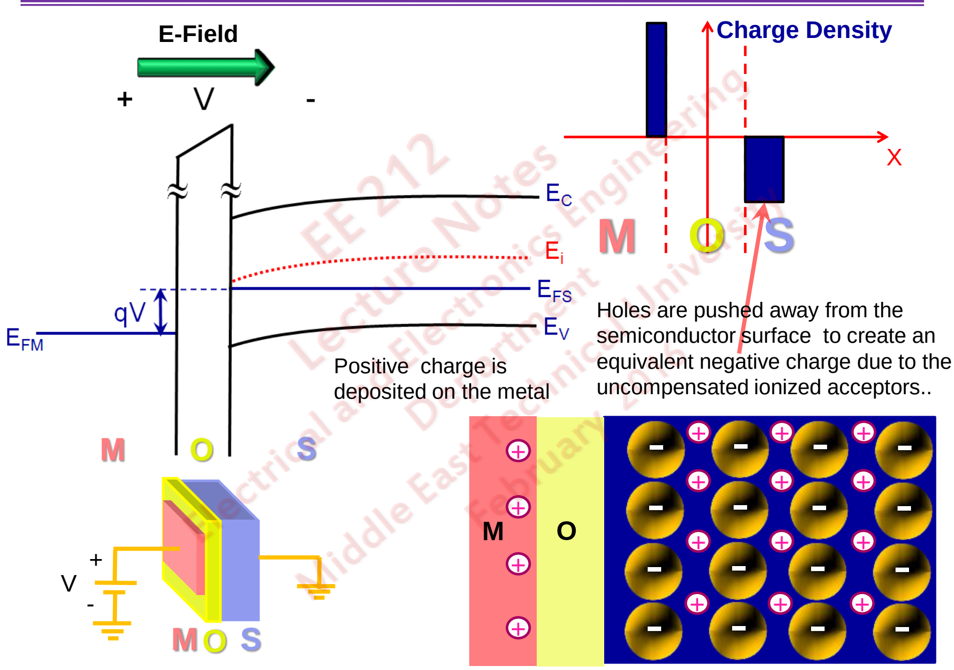
Ref. 3: 16.1, 16.2

If a bias voltage is applied to have positive potential on the metal (gate) with respect to the semiconductor (substrate), positive charge appears on the gate. This positive charge must be balanced with negative charge on the semiconductor side. This balance is achieved by pushing the holes away from the interface between the oxide and the semiconductor. Absence of the holes (compensating the ionized acceptor charge) at the interface creates a depletion region.

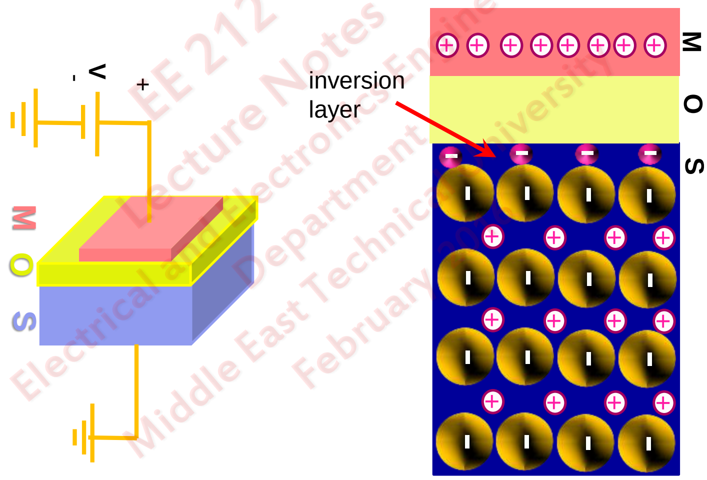


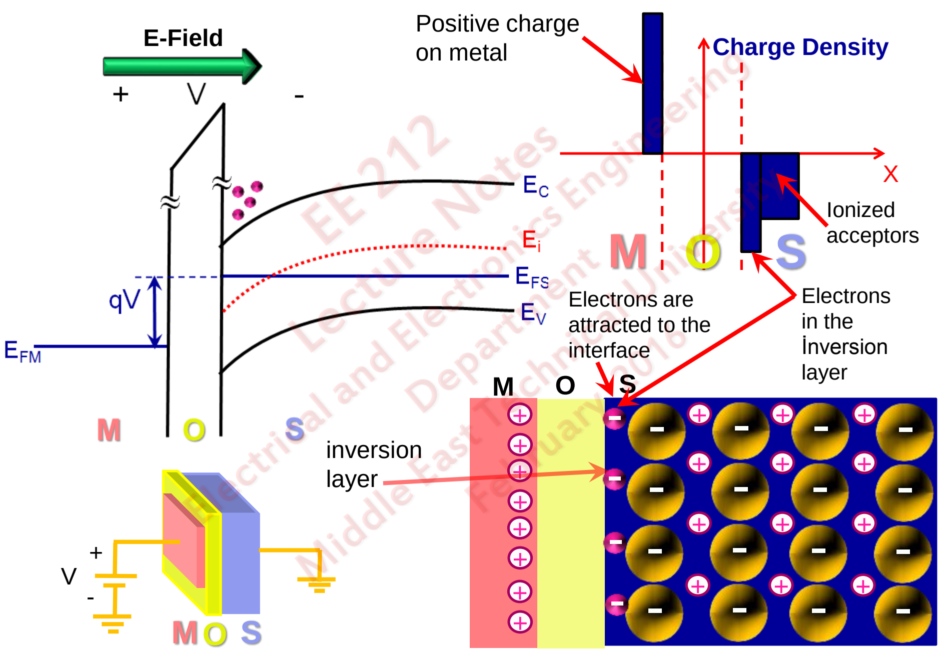
MOS Capacitor-Depletion

Ref. 3: 16.1, 16.2



If the bias voltage is increased, electrons in the p-type substrate are attracted to the interface to balance increasing positive charge on the gate. The presence of the electrons at the interface inverts this region from p to n-type.





MOS Capacitor-Inversion

CHECK YOURSELF-POINT

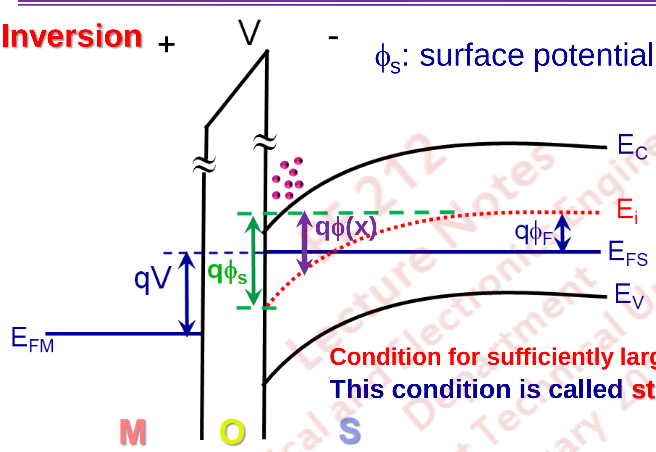
Q: Draw the energy band diagrams and charge distributions for a MOS structure on n type substrate under accumulation, depletion and inversion.

S: write

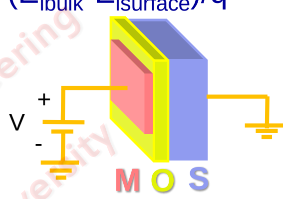
MOS Capacitor

Ref. 3: 16.1, 16.2

Inversion



ϕ_s: surface potential=$(E_{ibulk}-E_{isurface})/q$



Condition for sufficiently large inversion: $q\phi_s=2q\phi_F$

This condition is called strong inversion.

$$n = n_i e^{\frac{E_F-E_i}{kT}},\ p = n_i e^{\frac{E_i-E_F}{kT}},\ p_{bulk} = n_i e^{\frac{q\phi_F}{kT}},\ n_{surface} = n_i e^{\frac{q(\phi_s-\phi_F)}{kT}} = n_o e^{\frac{q\phi_s}{kT}}$$

The surface electron concentration is equal to the hole (majority) carrier concentration in the bulk (substrate).

MOS Capacitor

Q: Find the surface potential required for inversion of a MOS structure constructed on p-type Si substrate doped to N_A=1x10^{16} cm^{-3}. T=300 K.

S:

$$p_{bulk} \cong N_A = n_i e^{\frac{E_i - E_F}{kT}} = n_i e^{\frac{q\phi_F}{kT}} \Rightarrow \phi_F = \frac{kT}{q}\ln(\frac{N_A}{n_i})$$

$$= 26mV\ln(\frac{1x10^{16}}{1x10^{10}}) = 0.36\ V,\ \ \phi_s = 2\phi_F = 0.72\ V$$

Typical layer thicknesses in a MOS Structure:

Inversion layer < 10 nm

Depletion layer: several hundred nm

Charge on the metal is confined to a several A thick region

MOS Capacitor

Ref. 1: 6.4.2

Q: Find the expression for electron density at the semiconductor side of a MOS structure in terms of the potential, ϕ(x).

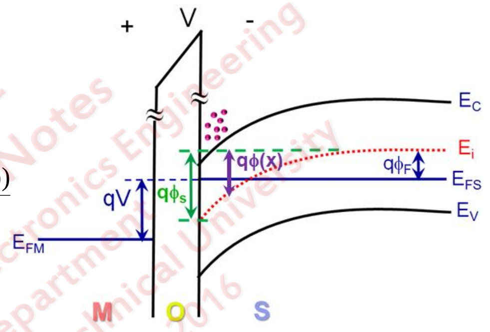
S:

$$p_o = n_i e^{\frac{E_{ibulk} - E_F}{kT}} = n_i e^{\frac{q\phi_F}{kT}},$$

$$p(x) = p_o e^{-\frac{q\phi(x)}{kT}} = n_i e^{\frac{q(\phi_F - \phi(x))}{kT}}$$

$$p_o n_o = n_i^2 \Rightarrow n_o = n_i e^{-\frac{q\phi_F}{kT}},$$

$$n(x) = n_i e^{\frac{-q(\phi_F - \phi(x))}{kT}} = n_o e^{\frac{q\phi(x)}{kT}}$$



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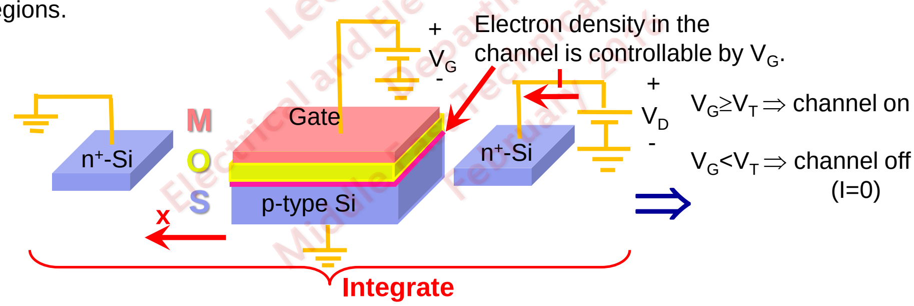
MOSFETs – Introduction

We have used two p-n junctions to construct a controlled current source called BJT. Now let's see if we can build a similar circuit element (that can be used for amplification and switching) by using a MOS structure. So far we know that the electron concentration in the inversion layer of a MOS capacitor (on p substrate) can be controlled with the voltage applied to the metal electrode. Let's call this electrode 'gate' and the conductive layer forming beneath it 'channel'. How do I turn this device into a controlled current source?

Obviously, I should add two more electrodes through which a current proportional to the channel electron density will flow as a result of an E-field created in the x direction due to the biasing voltage applied between these two terminals. Since the channel is n-type (on a p-type substrate), I should connect the additional electrodes through n-type Si regions.



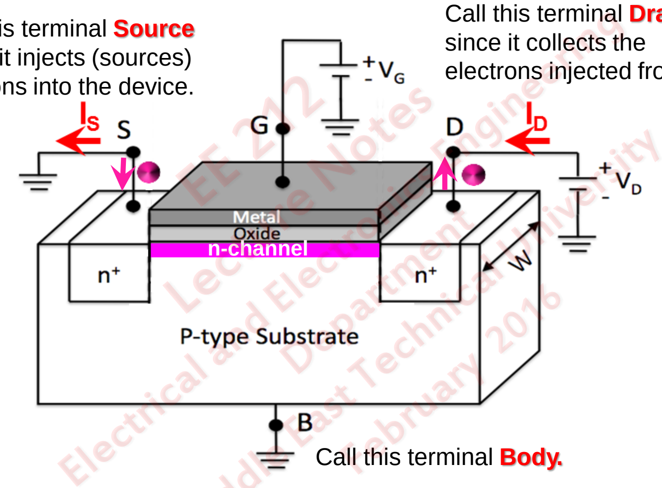
MOSFETs – Introduction

Ref. 4:4.1.1-4.1.5

Resultant Structure

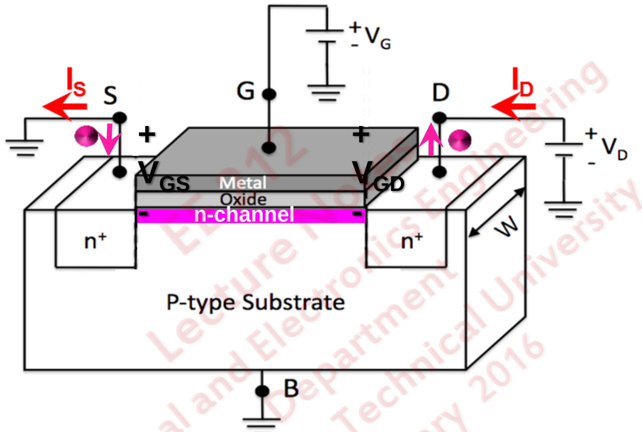
Call this terminal **Source** since it injects (sources) electrons into the device.

Call this terminal **Drain** since it collects the electrons injected from the Source.



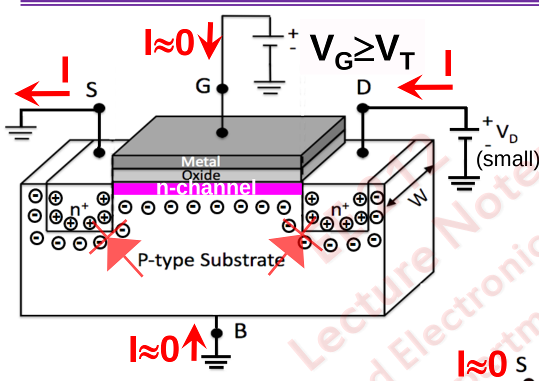
Call this terminal **Body.**

Note that the inversion layer (channel depth) with a real thickness of several nm is exaggerated in this drawing.



The gate voltage required to induce the inversion layer (n-channel) is called the **threshold voltage** (V_T). The voltage across the oxide (v_{ox}) must be larger than V_T in order to have the inversion layer at a location in the channel. For example,

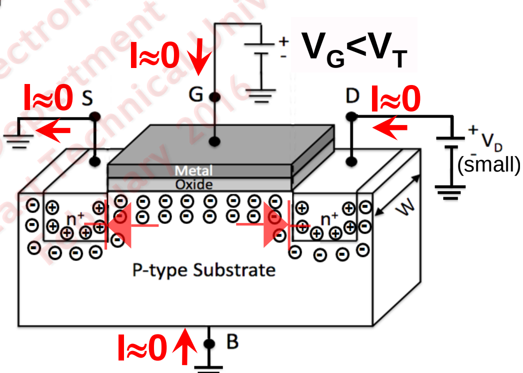
if $V_{GS}=V_G$ (since $V_S=0$)$>V_T$ inversion layer (n-channel) exists at the source end
if $V_G-V_D=V_{GD}>V_T$ inversion layer (n-channel) exists at the drain end



Under both conditions, the p-n diodes between the p type substrate and n-type drain/source contacts are reverse biased and no current flows through the substrate (body) terminal.

Channel ON

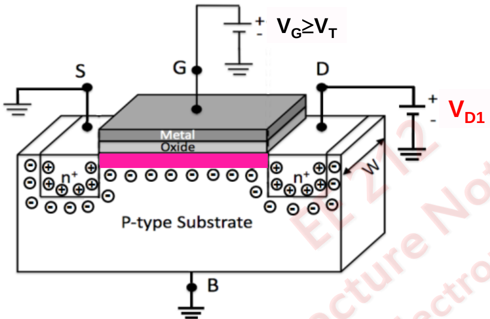
MOS capacitor working in the inversion mode

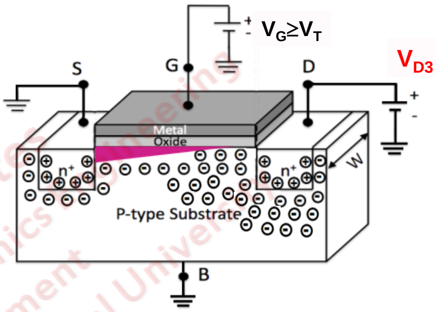


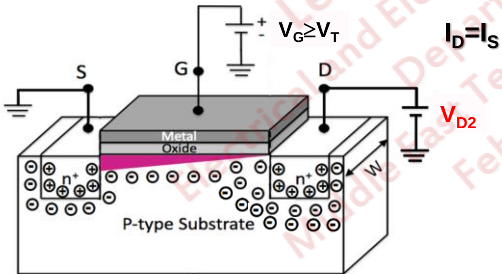
Channel OFF

MOS capacitor working in the depletion mode

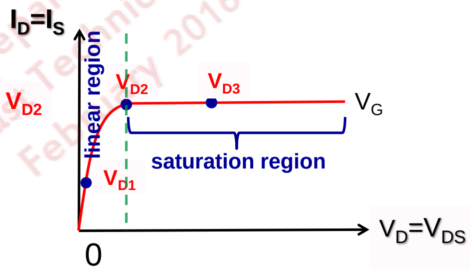
Ref. 4:4.1.1-4.1.5







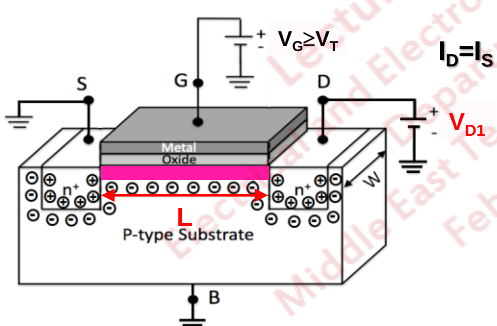
Channel is pinched off at the drain end.

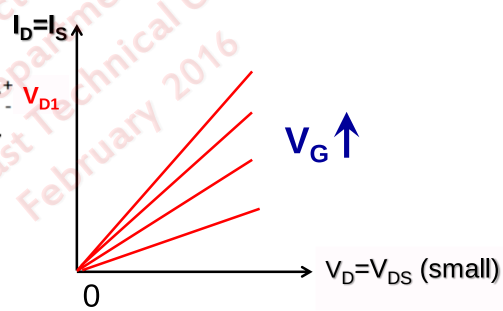


Case 1: small V_{DS} (V_D=V_{D1}) with V_G>V_T.

The inversion layer extends throughout the entire region between the drain and source. This region of operation is called the linear region. The device operates like a resistor in this region. However, note that this is a voltage controlled resistor since the resistivity of the channel is controlled by the gate voltage (V_G=V_{GS}). Conductivity (σ) of the channel depends on the electron density in the inversion layer (channel) which is controlled by V_G.

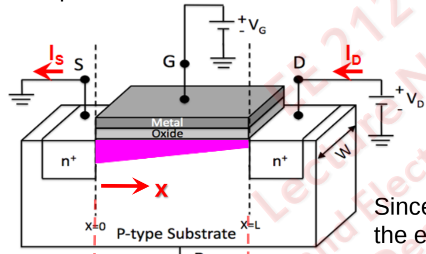
$$R = \rho \frac{L}{wt} = \frac{1}{\sigma}\frac{L}{wt}$$

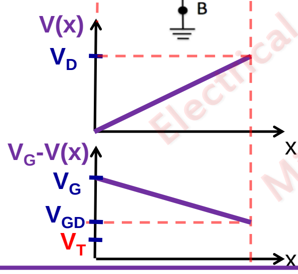




Q: Is the electron concentration in the inversion layer uniform through the channel?

S: No, it is not. Note that the electron concentration in the inversion layer at any location in the channel depends on the difference between V_G and the potential of that particular location in the channel V(x). Potential on the metal is of course uniform.





Potential on the metal side is V_G. (constant through the channel)

Channel potential V(x) is V_D at the drain end.

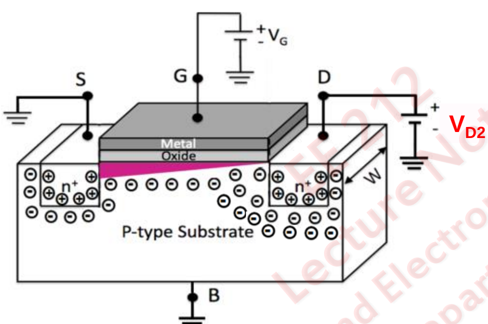
Channel potential V(x) is 0 at the source end.

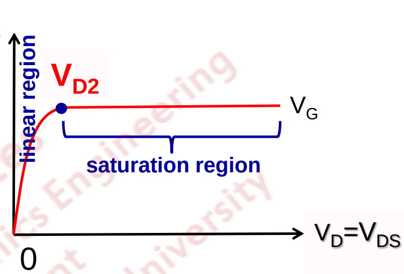
Since V_G-V(x) is not uniform through the channel, the electron density (or the channel depth) has a tapered shape. Since V_G-V(x) is larger at the source end, this point has the largest electron density.

Q: What are the required conditions to operate the n-channel MOSFET in the linear region.

S: V_G-V(x)>V_T through the entire channel. Since V_D>V_S , it is sufficient to check if the inversion layer exists at the drain end (V_{GD}>V_T). If it does, the device is operating in the linear region

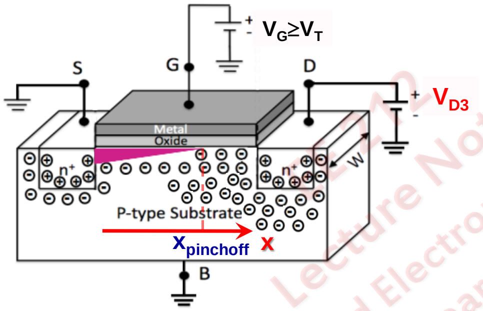
Case 2: V_D=V_{D2} with V_G>V_T.

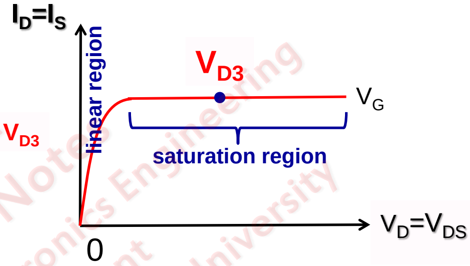




The channel is pinched off (disappears) at the drain end. In order to have this condition, V_G-V_D=V_G-V_{D2}=V_T⇒V_{GD}=V_T. The dependence of I_D on V_D exhibits a different characteristic beyond this point when V_D is further increased. Under ideal conditions, the drain current does not increase any more with increasing V_D (now, we have a **current source!**). Therefore, this point is a boundary between two different operation regions of the MOSFET.

Case 3: $V_D=V_{D3}$ with $V_G>V_T$.



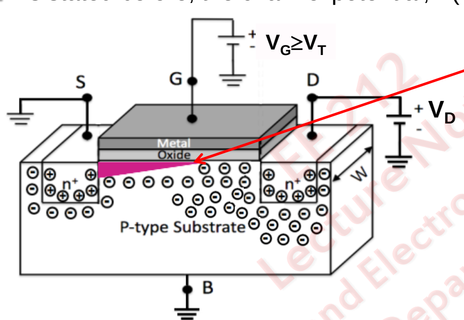


The pinch off point moves toward the source end since V_G-V_D=V_{GD}<V_T or V_G-V(x)=V_T at a location closer to the source end (V(x) decreases in this direction). Note that

$$V_G - V(x_{pinchoff}) = V_T \quad \text{or} \quad V(x_{pinchoff}) = V_G - V_T = V_{GS} - V_T$$

Q: Why does the drain current saturate when the channel is pinched off at the drain end?

S: As stated before, the channel potential, V(x)=V_G-V_T at the pinch off point.



This means that the voltage drop across the undepleted channel is independent of the drain voltage. The rest of V_D drops across the depleted part of the channel (which exhibits much higher resistance). Since the voltage drop across the invesion layer is fixed by V_G and V_T, the drain current does not change with V_D once the channel is pinched off at the drain end.

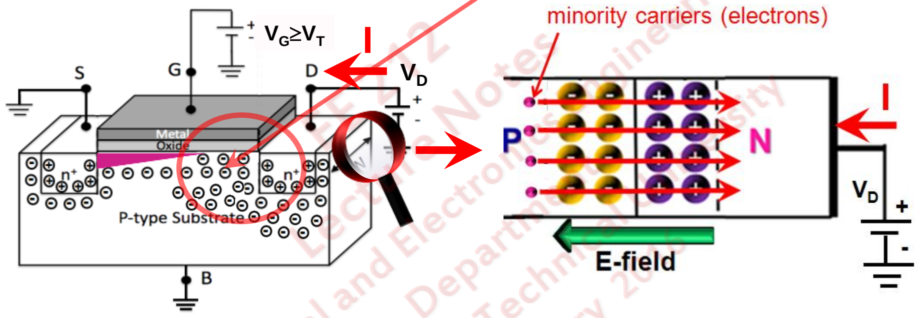
Q: What about the pinch off point moving toward the source end with increasing V_D? I still expect V_D dependent I_D, since the channel resistance should be decreased with decreasing channel length resulting in a larger I_D.

S: Yes it does. Indeed the drain current in a real MOSFET increases with increasing V_D because of this reason. This is called channel length modulation effect which will be discussed later. Let's ignore this effect at this stage.

MOSFETs – Introduction

Q: How does the drain current flow through the depleted part of the channel?

S: The current flow through the depleted part of the channel is similar to the current flow through a reverse biased p-n junction.

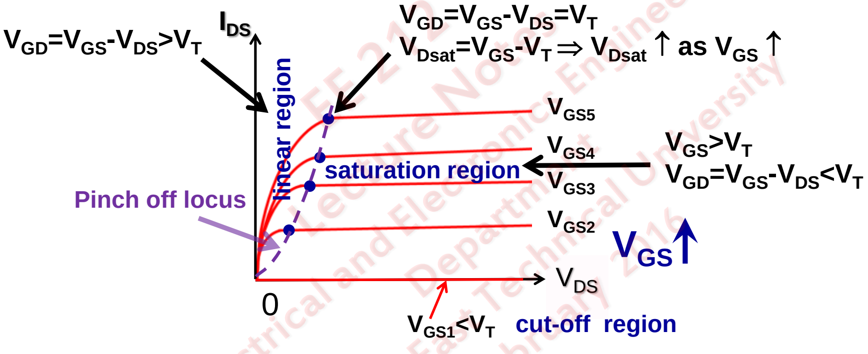


The carriers contributing to the drift (drain) current are provided by the electron inversion layer. The large E-field at the drain junction sweeps the electrons to the drain. The drain current (in saturation) is independent of the drain voltage exceeding V_{dsat} (additional increase appears as reverse bias across the drain junction depletion region).

MOSFETs – I-V Characteristics

Q: How do the I_D-V_{DS} characteristics of the n-channel MOSFET look like under varying V_{GS} and V_{DS}?

S:



The MOSFET can be used as a **voltage controlled current source** in the **saturation region**.

MOSFETs – Derivation of Drain Current Expression Ref. 5:4.2.2

We will derive the expression for the drain current of an n-channel MOSFET in the linear region.

I_D should depend on biasing voltages as well as the device parameters.

Remember that the channel behaves as a voltage controlled resistor in the linear region. Therefore, the drain current is governed by the resistance of the channel as well as the drain voltage.

Since, the resistance of the channel depends on the electron density in the inversion, layer which is set by the gate voltage, we should expect to get an expression in terms of both V_D and V_G.

It is a good idea to start by establishing the relation between the channel electron density and the gate voltage.

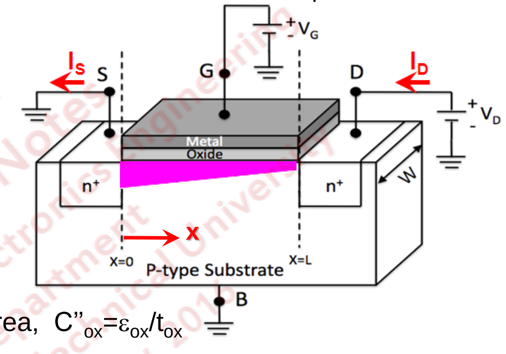
MOSFETs – Derivation of Drain Current Expression Ref. 5:4.2.2

In order to induce inversion layer charge on the semiconductor side at point x (under strong inversion):

$$V_G - V(x) = V_T$$

$$C_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}} : \text{oxide capacitance}$$

t_{ox} : oxide thickness



Define C''_{ox}: oxide capacitance per area, $C''_{ox}=\varepsilon_{ox}/t_{ox}$

Inversion layer charge per unit area (Q_{inv}'') at location x is

$$|Q_{inv}''(x)| = C_{ox}''(V_G - V(x) - V_T)$$

$$I(x) = Q_{inv}'(x)v_{dn}(x)$$

charge per unit length

electron drift velocity=$-\mu_n E(x)$

MOSFETs – Derivation of Drain Current Expression Ref. 5:4.2.2

$$I(x) = -W\left|Q_{inv}''(x)\right|\mu_n \frac{dV(x)}{dx} = -\mu_n \frac{dV(x)}{dx} WC_{ox}''\left[V_G - V(x) - V_T\right]$$

$$\int_0^L I(x)dx = -C_{ox}''\mu_n W \int_0^{V_D}\left[V_G - V(x) - V_T\right]dV$$

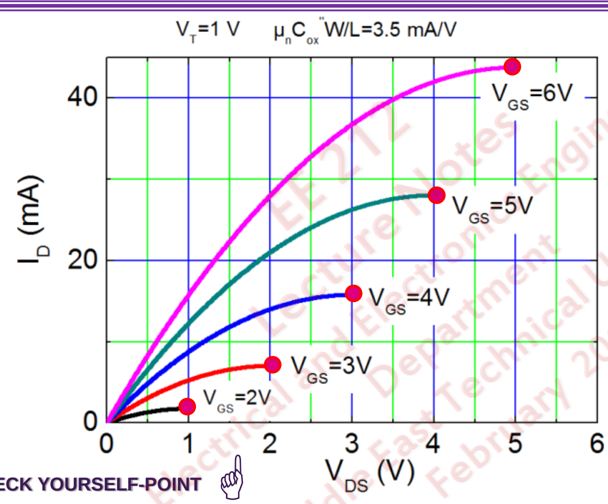
$$-I(x) = I_D \text{ (independent of position)}$$

$$I_D = C_{ox}''\mu_n \frac{W}{L}(V_G - V_T - \frac{V_D}{2})V_D$$

$$or\ I_D = C_{ox}''\mu_n \frac{W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \text{ if the source is not grounded } (V_S \neq 0 \text{ V})$$

Let's take a closer look at this expression. The following figure shows the I_D-V_{DS} characteristics of a MOSFET calculated using the above expression.

MOSFETs – Derivation of Drain Current Expression



CHECK YOURSELF-POINT

Q: The above expression predicts I_D correctly up to the marked V_{DS} voltages. Why?

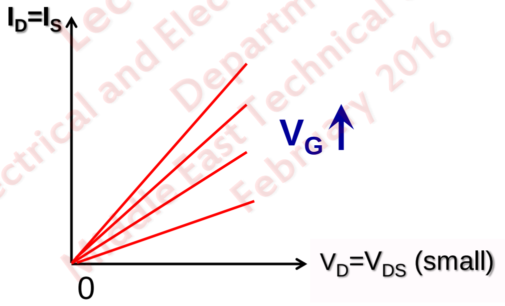
S: write

For small V_{DS},

$$I_D = \frac{C_{ox}''\mu_n W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right] \cong \frac{C_{ox}''\mu_n W}{L}(V_G-V_T)V_{DS}$$

Then the conductance of the device in the linear region is

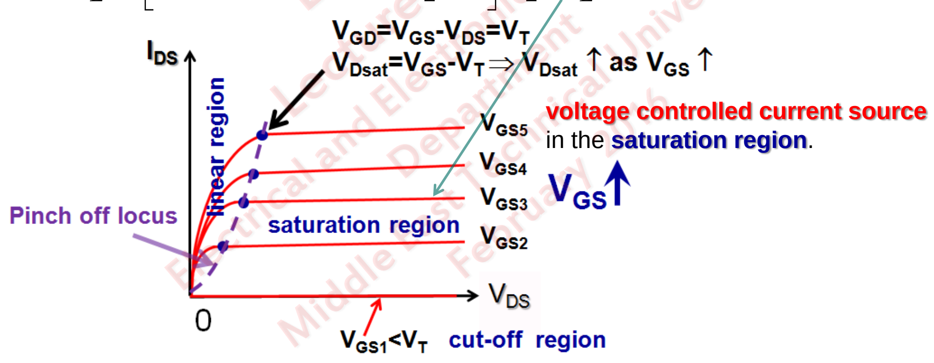
$$g_D = \frac{\partial I_D}{\partial V_D} = \frac{C_{ox}''\mu_n W}{L}(V_{GS}-V_T)$$ **voltage controlled resistance**



Saturation Current: The current expression for the linear region is applicable up to the boundary between the linear and saturation regions. Since the drain current is ideally constant beyond this point:

$$I_{D_{sat}} = I_{Dlinear}\Big|_{V_{Dsat}=V_G-V_T} = \frac{C_{ox}''\mu_n W}{L}\left[(V_{GS}-V_T)V_{DSsat}-\frac{V_{DSsat}^2}{2}\right]$$

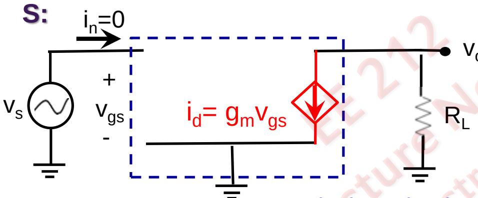
$$= \frac{C_{ox}''\mu_n W}{L}\left[(V_{GS}-V_T)(V_{GS}-V_T)-\frac{(V_{GS}-V_T)^2}{2}\right] = \frac{1}{2}\frac{C_{ox}''\mu_n W}{L}(V_{GS}-V_T)^2$$



MOSFETs – Transconductance

Q: A MOSFET (operating in the saturation region) is utilized as a voltage controlled current source to amplify ac signals as shown below. Find the expression for g_m in terms of device parameters.

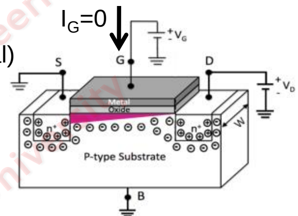
S:



equivalent circuit

$v_o = -g_m R_L v_s$

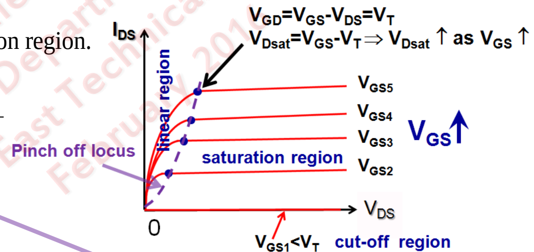
$$\frac{v_0}{v_s} = -g_m R_L$$



$$I_D = \frac{1}{2}\frac{C_{ox}{}^{"}\mu_n W}{L}(V_{GS}-V_T)^2 \text{ in the saturation region.}$$

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = C_{ox}{}^{"}\mu_n \frac{W}{L}(V_G - V_T) = \frac{2I_D}{V_{GS}-V_T}$$

Transconductance



Q: List the requirements to achieve a large voltage gain (high transconductance) with this MOSFET.

S: High electron mobility in the inversion layer and small channel length.

MOSFETs – Current Expressions

n-channel MOSFET

$$I_D = C_{ox}^{"}\mu_n \frac{W}{L}(V_{GS}-V_T-\frac{V_{DS}}{2})V_{DS} \text{ in linear region, } V_{GS}>V_T,\ V_{GD}>V_T\ (V_{GS}-V_{DS}>V_T)$$

$$I_D = \frac{1}{2}\frac{C_{ox}{}^{"}\mu_n W}{L}(V_{GS}-V_T)^2 \text{ in saturation region, } V_{GS}>V_T,\ V_{GD}<V_T\ (V_{GS}-V_{DS}<V_T)$$

$$I_D = 0 \text{ in cut off, } V_{GS}<V_T$$

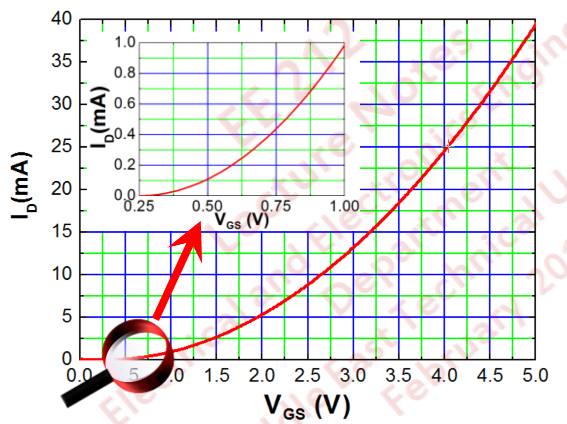
$$Define\ \ K_n = \mu_n C_{ox}^{"}\frac{W}{L} \quad \text{(transconductance parameter)}$$

$$I_D = K_n(V_{GS}-V_T-\frac{V_{DS}}{2})V_{DS} \text{ in linear region, } V_{GS}>V_T,\ V_{GD}>V_T\ (V_{GS}-V_{DS}>V_T)$$

$$I_D = \frac{1}{2}K_n(V_{GS}-V_T)^2 \text{ in saturation region, } V_{GS}>V_T,\ V_{GD}<V_T\ (V_{GS}-V_{DS}<V_T)$$

$$I_D = 0 \text{ in cut off, } V_{GS}<V_T$$

Transfer Characteristic-Saturation Region



MOSFET Parameters:

C''_{ox}=3.5x10^{-7} F/cm^2

V_T =0.25 V

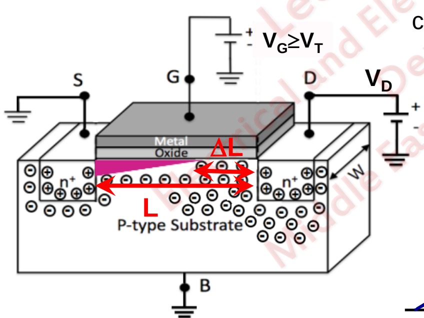
$\mu_n C_{ox}$W/L=3.5 mA/V

The drain current of a real MOSFET is not constant (increases with V_{DS}) in the saturation region. This is due to the movement of the pinch off point toward the source end shortening the channel. As discussed before, the channel potential is constant at $V(x)=V_G-V_T$ (if V_G is kept constant) at the pinch off point. A reduction of ΔL in the channel length results in a proportional decrease in the channel resistance ($\Delta R/R \; \alpha \; \Delta L/L$).

$$R=\rho\frac{L}{wt}=\frac{1}{\sigma}\frac{L}{wt},\quad I_D=I_{Dsat}\left(\frac{R}{R-\Delta R}\right)=I_{Dsat}\left(\frac{L}{L-\Delta L}\right)=I_{Dsat}\left(\frac{1}{1-\Delta L/L}\right)\cong I_{Dsat}\left(1+\frac{\Delta L}{L}\right)$$

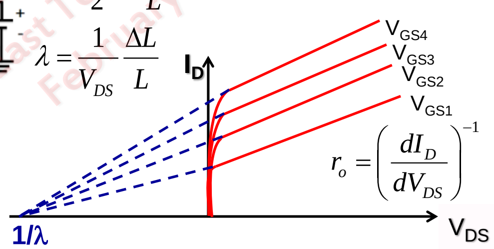
$$for\ \Delta L << L$$

This effect is modeled using a parameter called channel length modulation parameter, λ.



$$I_D=\frac{1}{2}\frac{C_{ox}\mu_n W}{L}(V_G-V_T)^2(1+\lambda V_{DS}),$$

$$\lambda=\frac{1}{V_{DS}}\frac{\Delta L}{L}$$

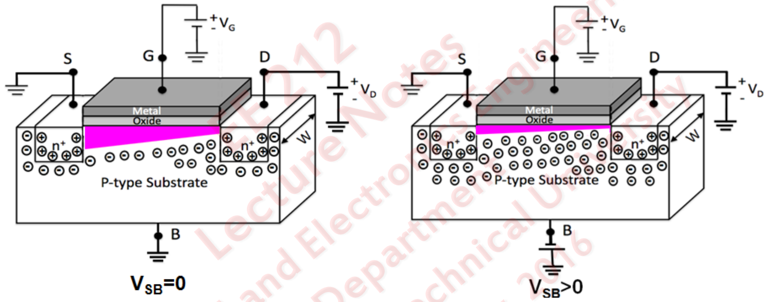


$$r_o=\left(\frac{dI_D}{dV_{DS}}\right)^{-1}$$

MOSFETs – Body Effect

Ref. 4:4.2.5

We have so far assumed that the Source and Body terminals of the MOSFET are short circuited. In some circuit configurations it is not possible to have V_{SB}=0. Under this condition, threshold voltage of the device is modified which is known as the Body Effect.



Nonzero (negative) Body voltage increases the depletion region width in the substrate.

Due the increase in the amount of depletion charge in the case of nonzero V_{SB}, larger gate voltage is necessary to have the same inversion layer charge (electron density) with V_{SB}=0.

$$V_T == V_{TO} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$

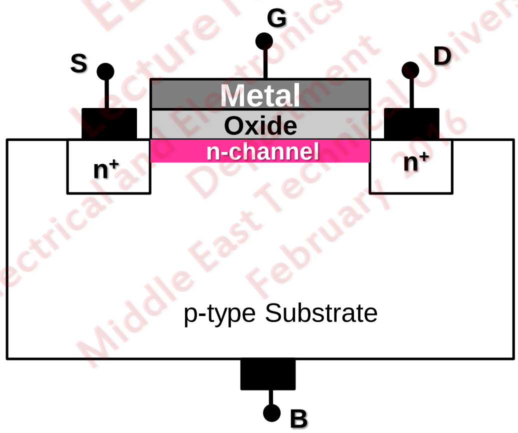
$$\gamma : Body\ Effect\ Parameter,\ \ V_{TO} : V_T\ \ when\ V_{SB} = 0.$$

MOSFETs – Depletion Mode

Ref. 5:4.2.9

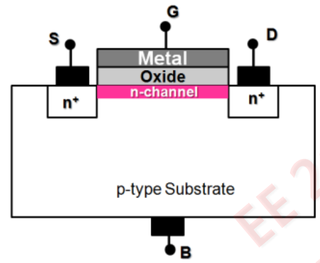
A physically implanted n-channel exists in the depletion type MOSFET. Since an n-channel is already present, the device conducts current even when V_{GS}=0 V. In order to turn the drain current off, a sufficiently large negative bias voltage must be applied to the gate. This bias voltage is defined as the threshold voltage of the depletion type MOSFET.

n-channel depletion mode MOSFET

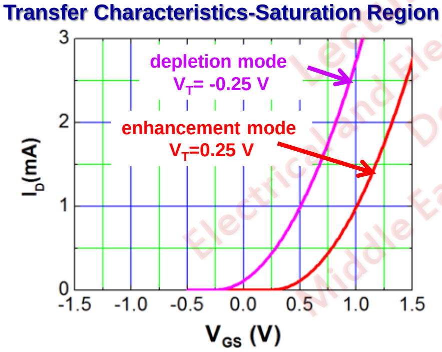


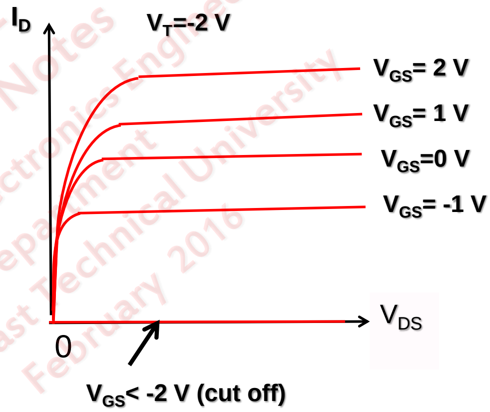
MOSFETs – Depletion Mode

Ref. 5:4.2.9



Transfer Characteristics-Saturation Region



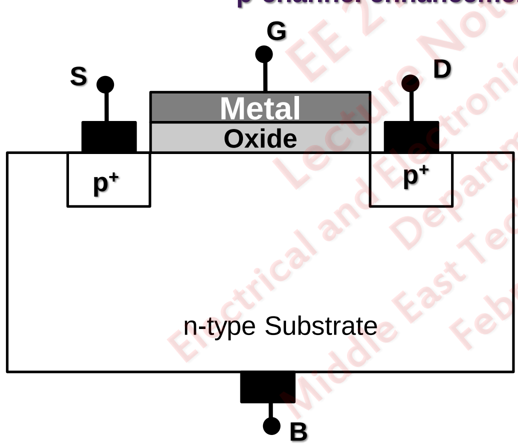


MOSFETs – p-channel

Ref. 5:4.3

p-channel MOSFET (PMOS) is constructed on an n-type substrate. A p-channel (hole inversion layer is formed between the p+ drain and source regions by the application of a negative gate voltage with a sufficiently large magnitude.

p-channel enhancement mode MOSFET



$V_{DS}<0$ ($V_S>V_D$)

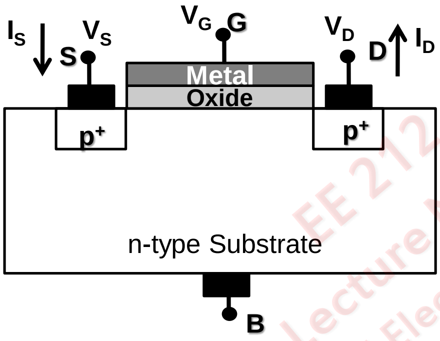
V_T negative

$V_{GS}<V_T$ to have the inversion layer at the source end

$V_B>V_S$, V_D

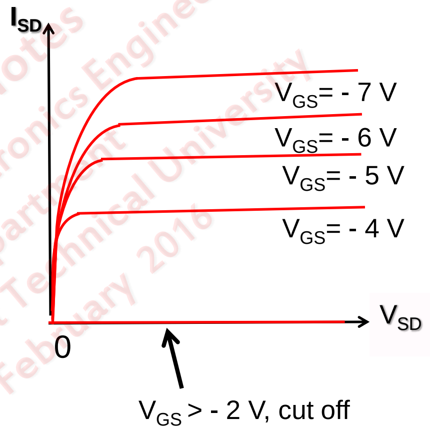
MOSFETs – p-channel

Ref. 5:4.3



$V_{DS}<0$ ($V_S>V_D$)

V_T =-2 V negative



MOSFETs – Current Expressions

Ref. 5:4.3

p-channel enhancement type MOSFET

$V_{DS}<0$ ($V_S>V_D$) V_T negative

Define $K_p = \mu_p C_{ox}'' \dfrac{W}{L}$ (transconductance parameter)

$$I_{SD} = K_p (V_{SG} + V_T - \frac{V_{SD}}{2}) V_{SD}$$

in linear region, V_{GS} negative and $|V_{GS}|>V_T$, V_{GD} negative and $|V_{GD}|>V_T$

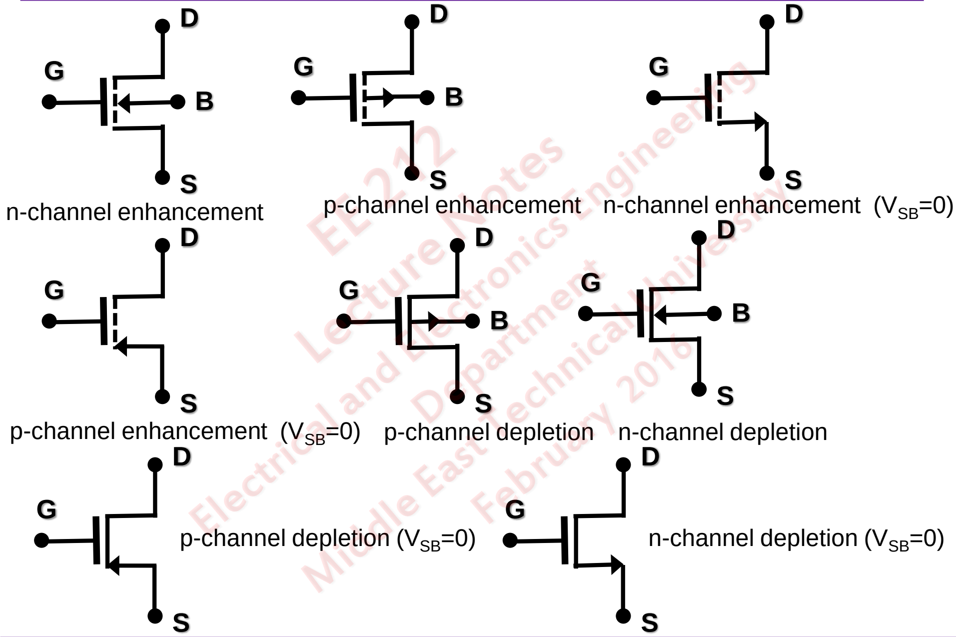
$$I_{SD} = \frac{1}{2} K_p (V_{SG} + V_T)^2 (1+\lambda V_{SD})$$

in saturation region, V_{GS} negative and $|V_{GS}|>V_T$, $V_{GD} > V_T$

$I_{SD} = 0$ in cut off, $V_{GS} > V_T$

MOSFETs – Circuit Symbols

Ref. 5:4.4



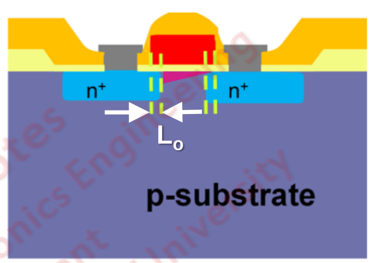
MOSFETs – Capacitances

Ref. 4: 4.8.1

Saturation Region

$$C_{GS} = \frac{\partial Q'_{inv}}{\partial V_G} = \frac{2}{3} WLC_{ox}$$

gate-source capacitance



In addition to the above capacitance, the overlaps of the gate and drain regions result in an additional capacitance that should be taken into accout. Therefore, the total gate-source capacitance is

$$C_{GS} = \frac{2}{3} WLC_{ox} + WC_{OG}$$ where C_{OG} is the gate to source overlap capacitance in units of F/μm.

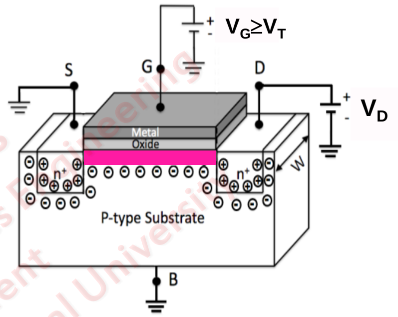
Assuming that the drain voltage has no effect on the channel charge, gate to drain capacitance is

$$C_{GD} = WC_{OD}$$ where C_{OD} is the gate to drain overlap capacitance in units of F/μm.

Gate Capacitances in the Linear Region

Divide the gate capacitance equally between gate-source and gate-drain

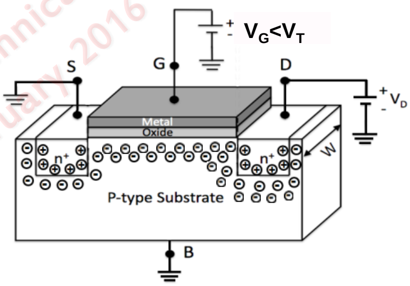
$$C_{GS} = C_{GD} = \frac{1}{2} WLC_{ox} + WC_o$$



Gate Capacitances in the Cut-off Region

No inversion layer,

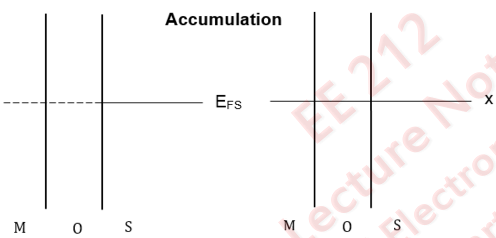
$$C_{GS} = C_{GD} = WC_o$$

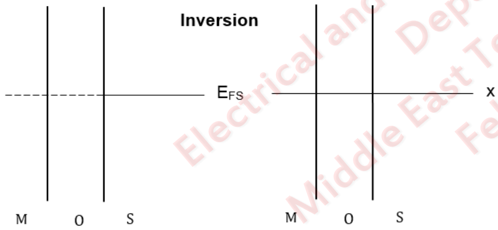


Q.1 Homework 7 (Estimated Time To Complete < 140 min.)

Draw the energy band diagrams and charge distributions for a MOS structure on **n type substrate** under accumulation and inversion.

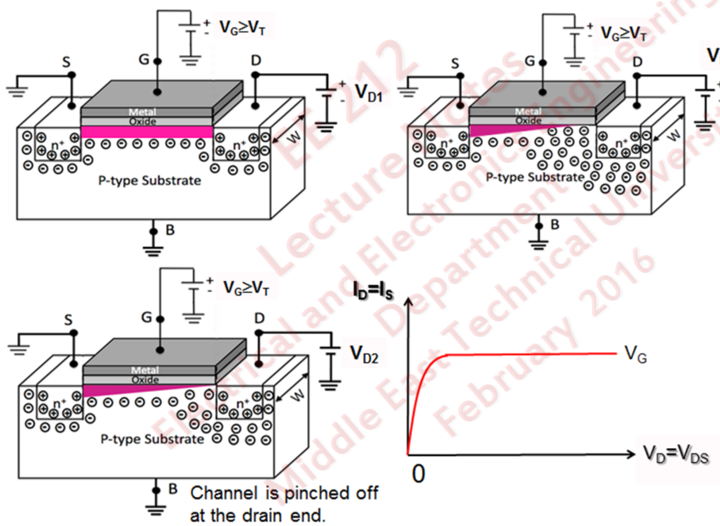
Energy Band Diagram **Charge Distribution**





Q.2 Homework 7

Show (write) V_{D1}, V_{D2} and V_{D3} at the proper locations on the given I_D-V_D characteristic plot.



Q.3 Homework 7

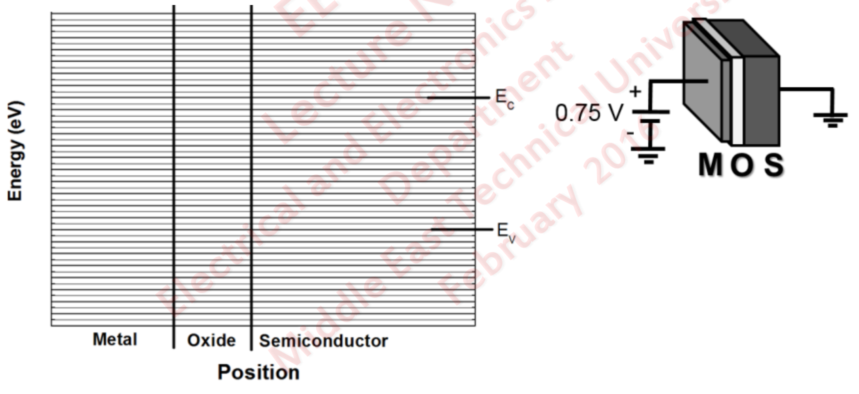
CIRCLE the correct answers to fill in the blanks.

If the drain voltage of an n-channel enhancement type MOSFET (with $V_{GD}<V_T$) is increased while keeping the gate voltage constant, the drain current will be ...(1)... since a larger V_D leads to a smaller ...(2)... layer length. Noting that the voltage drop across the … (3) … layer is constant (independent of V_D), the ….(4)… in the channel conductance is responsible for this characteristic. This affect results in a nonideal controlled …(5)… source characteristic in the …(6)… operation region. A …(7)… is added to the equivalent circuit of MOSFET to model this effect by connecting it between …(8)… and source.

(1)	increased	decreased
(2)	inversion	depletion
(3)	inversion	depletion
(4)	increase	decrease
(5)	voltage	current
(6)	linear	saturation
(7)	resistance	current source
(8)	gate	drain

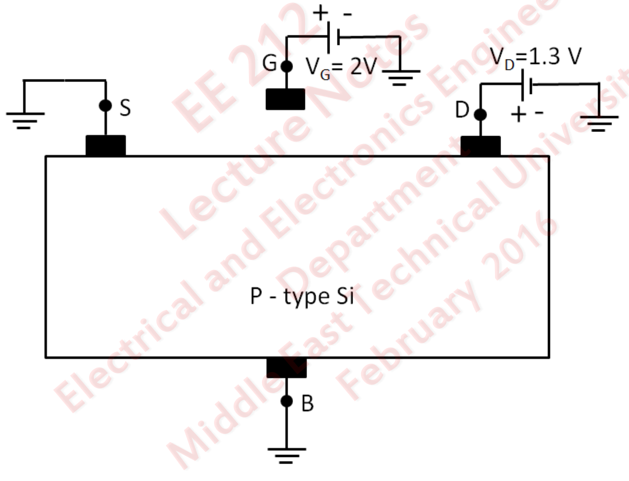
Q.4 Homework 7

i) Consider the following ideal MOS structure constructed with p-type Si doped at N_A=1.2x10^{16} cm^{-3}. Ignore the voltage drop on the oxide and draw the energy band diagram of the structure with the biasing arrangement shown in the figure. Show and label the metal Fermi level (E_{FM}), semiconductor Fermi Level (E_{FS}), intrinsic level (E_i), E_C and E_V. State the operation region and express the electron concentration in the semiconductor side as a function of position (n(x)) in terms of the potential ϕ(x), n_i and N_A. ϕ is zero in the bulk (away from the interface).



Q.4 Homework 7

ii) Now assume that an enhancement type MOSFET with threshold voltage of 0.7 V is constructed on the semiconductor described above. Complete the following figure to show all the details of the MOSFET structure including the depletion and the inversion regions with V_D=1.3V. Provide the necessary labels and minimize the overlap capacitances.



Q.4 Homework 7

iii) If the B terminal is connected to a negative supply voltage, the charge in the inversion layer is ……………… since the charge due to ionized acceptors is ……………………. and a ……………… gate voltage must be applied to have the same inversion layer electron density with the case when V_{SB}=0V. This is called ………………………….. effect.

iv) Now, assume that the drain voltage is decreased to 0.1 V. Express the channel current I(x) in terms of the channel potential (V(x)), electron mobility in the inversion layer (μ_n), oxide capacitance per unit area (C_{ox}''), gate voltage (V_G), the threshold voltage (V_T) and the channel width (W).

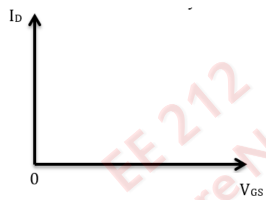
I(x)=

v) Use your answer to part (iv) to derive the expression for the drain current in terms of the drain potential (V_D), electron mobility in the inversion layer (μ_n), oxide capacitance per unit area (C_{ox}''), gate voltage (V_G), threshold voltage (V_T), channel width (W) and channel length (L).

vi) If the gate voltage is 2 V, the expression derived in part (v) will be applicable up to a drain voltage of ………. V.

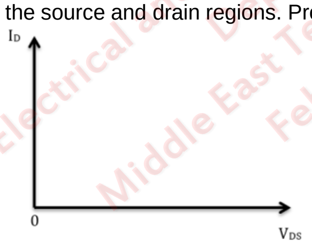
Q.4 Homework 7

vii) Roughly plot the I_D versus V_{GS} characteristic of this MOSFET with V_D=2V. Provide the necessary label.



viii) If V_D = 4 V, V_G = 2 V and V_T = 0.7 V, the voltage drop across the depleted (pinched off) part of the channel is ……….. V.

ix) Draw the I_D versus V_{DS} characteristics of this MOSFET (with different gate-source voltages including positive, negative and zero V_{GS}) which will be obtained, if an n channel is physically implanted between the source and drain regions. Provide the necessary labels.

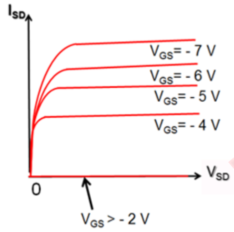


EE 212 Lecture Notes Electrical and Electronics Engineering Department Middle East Technical University February 2016

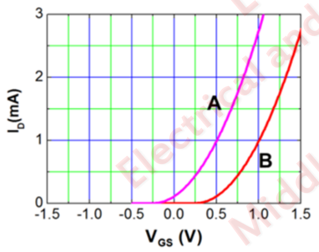
Middle East Technical University, EE 212-Semiconductor Devices and Modeling, Lecture Notes

Q.5 Homework 7

i) What is the type of the MOSFET with the following characteristics?
What is the threshold voltage of the device?

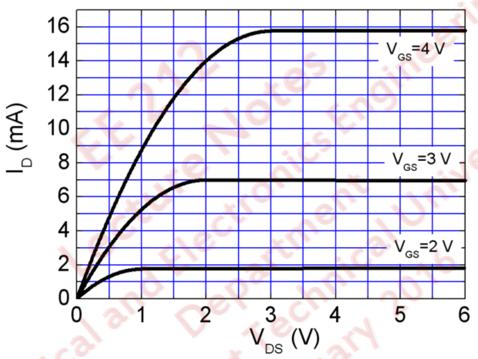


ii) What are the types of the MOSFETs having the following characteristics A and B?



Q.6 Homework 7

The following figure shows the characteristics of an enhancement type MOSFET. Provide the required information.



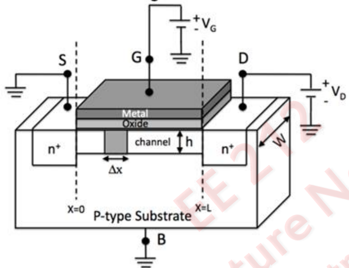
MOSFET Type (n or p-channel):

Threshold Voltage:

Transconductance Parameter:

Q.7 Homework 7

Consider the following MOSFET. Assume that V_D is small enough to operate the device in the linear region.



$V(x)=V_D=V_{DS}$ at $x=L$
$V(x)=V_S=0$ at $x=0$
Threshold voltage=V_T
Channel thickness (depth) at $x=h(x)$

i) Write the expression for the resistance (ΔR) of the elemental volume (with length Δx) in terms of Δx, μ_n, inversion layer charge per unit area ($Q''(x)$) and the other necessary parameters.

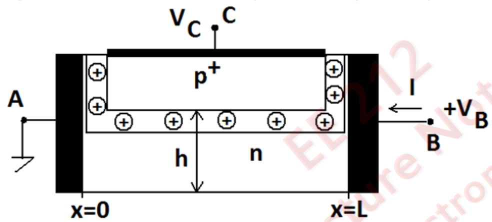
ii) Express $Q''(x)$ in terms of ε_{ox}, t_{ox}, $V(x)$, V_{GS} and the other necessary parameters.

iii) Express the potential drop (ΔV) on the elemental volume (with length Δx) in terms of I_D, t_{ox}, ε_{ox}, $V(x)$, V_{GS}, μ_n, Δx and the other necessary parameters.

iv) Derive the expression for I_D in terms t_{ox}, ε_{ox}, V_D, V_{GS}, μ_n, Δx and the other necessary parameters. You must use your result in part (iii).

Q.8 Homework 7

Consider the following semiconductor device. In this device the current between terminals A and B are controlled by the voltage applied at terminal C. The width of the device is W. Note that the depletion layer on the n-side is shown (that on the p+ side (much thinner) is not shown). $N_D >> n_i$.



The thickness of the depletion layer around the p-n junction can be approximated as

$T_D = \sqrt{\dfrac{2\varepsilon(-V_{CX})}{qN_D}}$ where V_{CX} is the potential difference between terminal C and location x in the n-type channel. N_D is the doping density of the channel. Assume that the depletion layer never completely depletes the n-type channel while answering the following questions.

i) Explain how the current I is controlled by V_C.

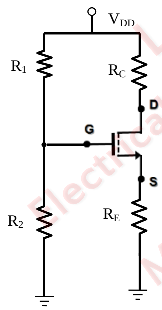
ii) Derive an approximate expression for the channel current I in terms of h, W, V_C, N_D, V_B and other necessary parameters under very small V_B. State your assumptions and show complete work. Note that $V_C < 0$ and $|V_C| >> V_B$.

MOSFETs-Biasing

Biasing: In order to use the MOSFET in a specific mode of operation, proper biasing voltages must be applied to the device terminals. As an example, the device is used in the saturation mode (as a controlled current source) for the amplification of ac signals.

Biasing establishes the operating point of the transistor which determines the device parameters governing the characteristics of the circuit such as the gain and the output voltage swing of an amplifier.

Therefore, the biasing circuit must be carefully designed to achieve the optimum circuit performance.



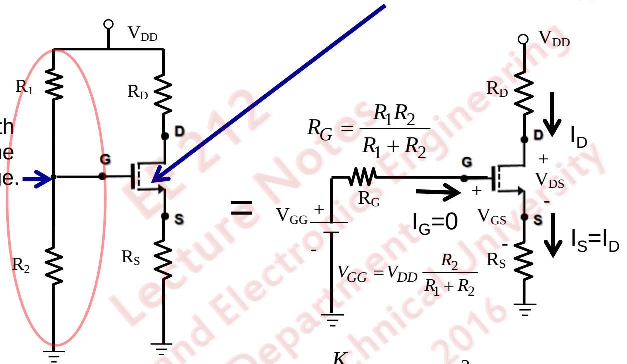
An example circuit biasing the MOSFET in the saturation region using a DC power supply (V_{DD}) and resistors.

MOSFETs-Biasing

Ref. 4:4.3, Ref. 5: 4.8, 4.9

MOSFET operates in the saturation region if $V_{GS}>V_T$ and $V_{GD}<V_T$.

Voltage divider (with V_{DD}) establishes the gate biasing voltage.



$V_{GG} = V_{GS} + I_D R_S$. *Assume sat. region operation*, $I_D = \frac{K_n}{2}(V_{GS}-V_T)^2$

$V_{GG} = V_{GS} + R_S\frac{K_n}{2}(V_{GS}-V_T)^2$ (ignore channel length modulation)

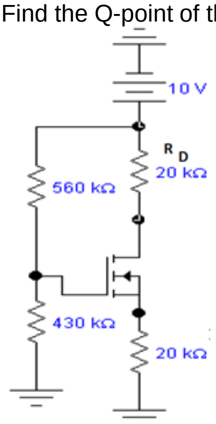
Solve the above equation to find V_{GS} (choose the solution that makes sense),

Find I_D from $I_D = \frac{K_n}{2}(V_{GS}-V_T)^2$ and check to see if $V_{GD} = V_{GS} - V_{DS} < V_T$ (verify sat. region assumption

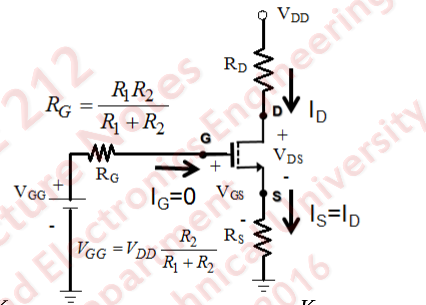
$V_{DS} = V_{DD} - I_D(R_D + R_S)$, Q-point: ($I_D$, V_{DS})

MOSFETs-Biasing

Q . The threshold voltage and transconductance coefficient of the n-channel enhancement mode MOSFET in the following circuit are V_T=1 V and K_n= 6 mA/V^2 (λ=0). Find the Q-point of the MOSFET.



S:



$$V_{GG} = 10\frac{430K}{990K} = 4.34V = V_{GS} + I_D 20K, \quad I_D = \frac{K_n}{2}(V_{GS}-1)^2 = 3x10^{-3}(V_{GS}-1)^2$$

$$4.34 = V_{GS} + 2x10^4 x3x10^{-3}(V_{GS}-1)^2$$

$$V_{GS} = 1.228V, 0.755V. \qquad 0.755V < V_T \Rightarrow V_{GS} = 1.228V$$

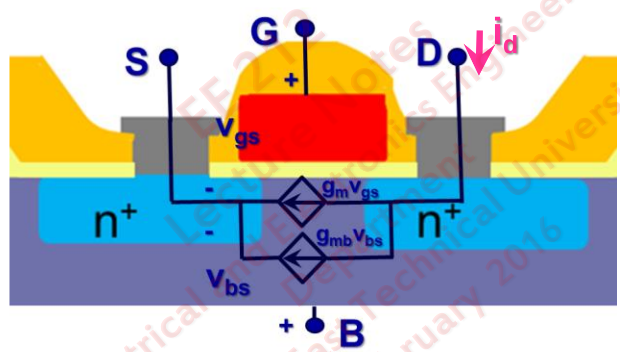
$$I_D = 1.56x10^{-4}A, \quad V_{DS} = 10 - I_D(20K\Omega + 20K\Omega) = 3.76V$$

$$V_{GD} = V_{GS} - V_{DS} = -2.53V < V_T \Rightarrow \text{saturation assumption is correct}$$

Q-point: (1.56x10^{-4}A, 3.76V)

MOSFETs –Exercise Questions

Q.1 Consider the following equivalent circuit for the n-channel MOSFET. g_{mb} is the backgate transconductance due to the Body effect. Discuss how the Body effect is modeled in this equivalent circuit.



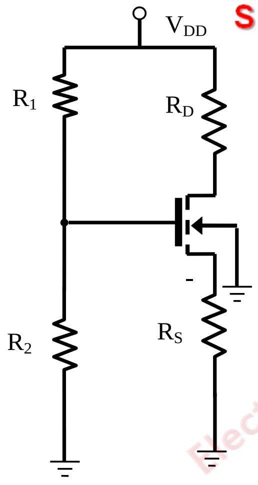
S: write

MOSFETs-EXERCISE QUESTIONS

Ref. 5: 4.8

Q.2 (to be solved on white board) Discuss how you find the Q-point of the MOSFET in the following circuit if the values of V_{DD}, R_1, R_2, R_D, R_S, K_n, V_{TO} and γ are given.

S: write



MOSFETs-EXERCISE QUESTIONS

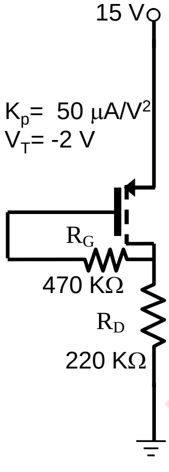
Q.3 (to be solved on white board) Consider the following circuit.

i) What are the possible regions of operation for the MOSFET?

S: write

i) Find the Q-point of the MOSFET.

S: write

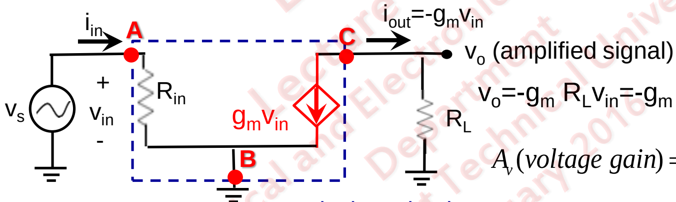


MOSFETs-EXERCISE QUESTIONS

Q.4 (to be solved on white board) Consider the following amplifer equivalent circuit under the following conditions.

Case 1: an n-channel enhancement type MOSFET (in saturation region) is performing the amplification with gate, source and drain connected to A, B and C, respectively.

Case 2: an npn BJT (in F.A. region) is performing the amplification with base, emitter and collector connected to A, B and C, respectively.



$v_o = -g_m R_L v_{in} = -g_m R_L v_s$

$$A_v(voltage\ gain) = \frac{v_o}{v_s} = -g_m R_L$$

equivalent circuit

i) What is R_{in} in the case of MOSFET?

S: write

MOSFETs-EXERCISE QUESTIONS

ii) We have obtained g_m as $g_m = \frac{2I_D}{V_{GS} - V_T}$ in the case of MOSFET? What is the g_m expression for the BJT?

Hint: Remember that $I_C \cong I_S e^{\frac{V_{BE}}{V_T}}$ in the forward active region.

S: write

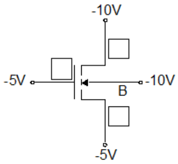
iii) Which transistor is likely to provide a larger voltage gain? (Assume that both devices are operating at a DC current of 10 mA and V_{GS}-V_T=1 V for the MOSFET).

S: write

Q.1 Homework 8 (Estimated Time To Complete < 45 min.)

For the transistors and bias voltages given in parts a) and b), determine the sign (positive or negative) of the threshold voltage and the region of operation of the transistor. In part a) also label the gate (G), drain (D), and source (S) of the transistor.

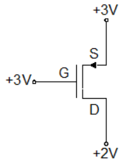
a)



Enhancement-mode NMOSFET. $|V_{TN}| = 2V$

V_{TN} =
Calculation/Reasoning:
Region of operation:

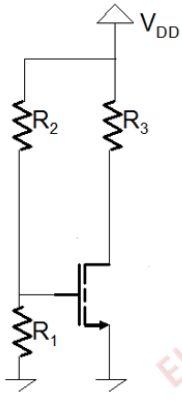
b)



V_{TP} =
Calculation/Reasoning:

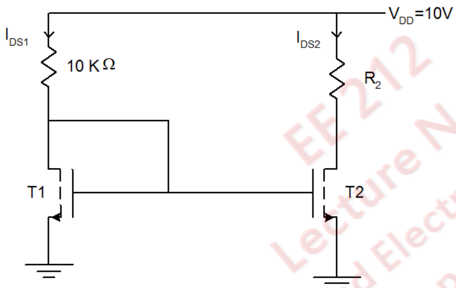
Q.2 Homework 8

For the enhancement type n-MOSFET in the following circuit: K_n = 0.2 mA / V^2 and V_{tn} = 2V.
R_2 = 8MΩ and V_{DD}=10 V.
Find the value of R_1 if the transistor is operating at the boundary of the linear and saturation operation regions.



Q.3 Homework 8

For the following circuit the parameters of MOSFETs T1 and T2 are K_n=1.6mA/V^2 and V_{TN}=1.5V



i) Find the operation region of transistor T1.

ii) Find I_{DS1}.

iii) Consider the range of R_2 values making I_{DS1}=I_{DS2} when the channel length modulation effect is included and ignored.

CHAPTER VI

Small Signal Modeling

&

Introduction to Transistor Amplifiers

References

1) A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, 2004.

2) R. C. Jaeger and T. N. Blalock, Microelectronic Circuit Design,Mc Graw Hill, 2003.

The Role of This Chapter

We will see in this chapter how the transistors can be utilized for linear amplification of ac signals. The purpose of this discussion is to provide the preliminary background on transistor amplifiers which will be considerably extended in the junior level course EE311-Analog Electronics. We will limit the discussion at this stage to the Common Emitter BJT and Common Source MOSFET amplifiers. As you will see in EE 311 in the following semester, it is possible to use the transistors in different configurations (in terms of connection of the terminals to the input signal and load) which provide different amplifier properties (such as voltage and current gains, input and output resistances).

We will start with an introduction to small signal modeling which is essential for linear amplification. This discussion will be followed by the construction of small signal models and their utilization in the analysis of transistor amplifer circuits.

It is essential to comprehend the material in this section in order to understand the possibilies offered by BJTs and MOSFETs for signal amplification.

Notation:

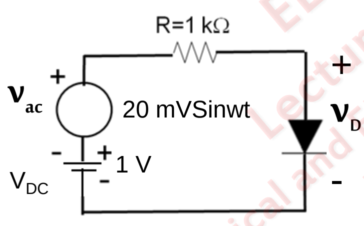
lowercase ↘ ν_{ac} ↖ lowercase $\rightarrow$ **purely ac signal**

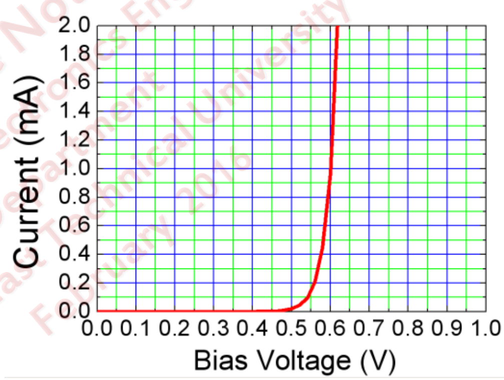
CAPITAL ↘ V_{DC} ↖ CAPITAL $\rightarrow$ **purely DC signal**

lowercase ↘ ν_{AC+DC} ↖ CAPITAL $\rightarrow$ **ac+DC signal**

As an introduction to small signal modeling, let's start with a question.

Q: How do you find the diode voltage in the following circuit containing both ac and DC voltage sources if the diode characteristics are provided? ν_{ac} is a small amplitude ac signal.

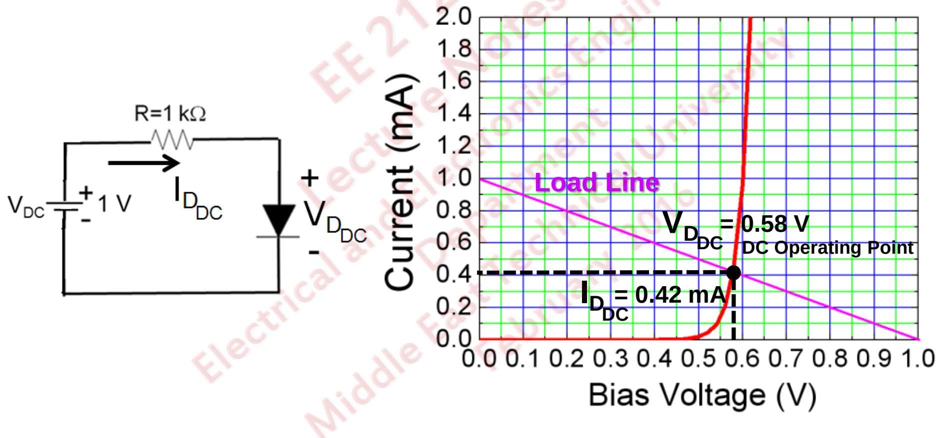




Small Signal Modeling-Diode

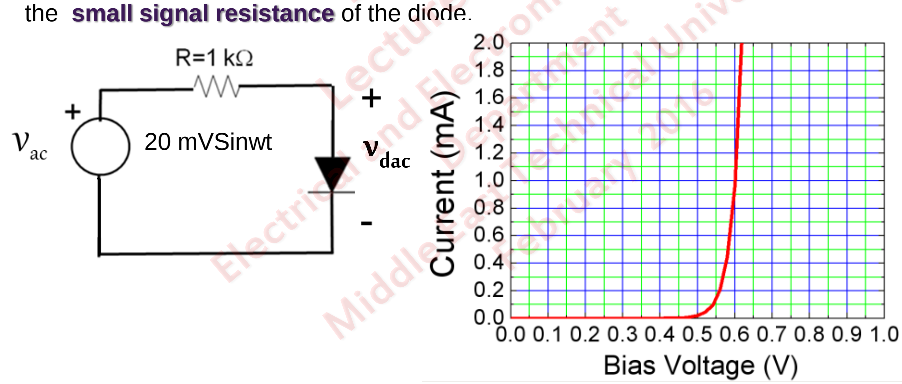
It is not difficult to find the DC voltage on the diode.

Draw the DC equivalent circuit and plot the load line on the diode I-V characteristic. You should be familiar with this approach.



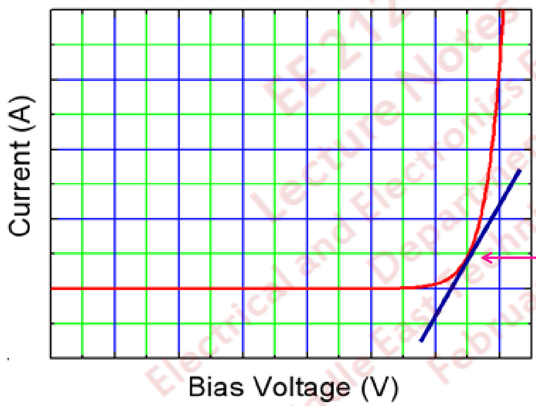
Small Signal Modeling-Diode

What about the diode ac voltage?
You can construct the ac equivalent circuit as follows. Note that the diode is still under forward bias with the 1 V DC voltage supply even though it is (naturally) not shown in the ac equivalent circuit. Diode ac voltage is obviously not equal to $\mathbf{v}_{ac}$ due to the voltage drop on R. In other words $\mathbf{v}_{ac}$ is divided between R and the diode. In order to apply the voltage division rule, we need to find out the resistance displayed by this diode to small amplitude ac signals. This is called the **small signal resistance** of the diode.



Small Signal Modeling-Diode

The small signal (dynamic) resistance can be found from the slope of the diode I-V characteristic at the DC operating point. Note that the slope depends on the operating point (DC biasing condition) therefore we must first carry out the DC analysis to identify the DC operating point.

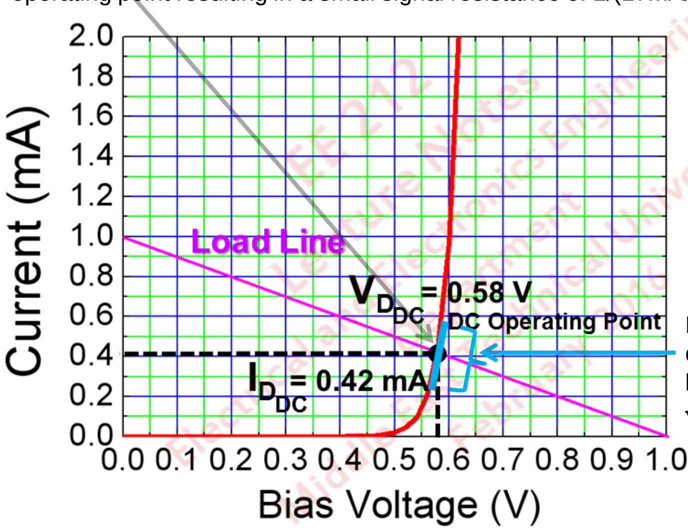


$$r_d = \left(\frac{dI}{dV}\right)^{-1}$$

at the operating point

Small Signal Modeling-Diode

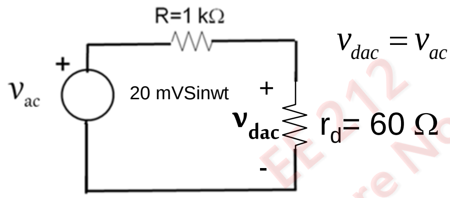
The slope of the I-V characteristic of our diode is approximately 17 mA/V at the DC operating point resulting in a small signal resistance of 1/(17mA/V)≈60 Ω.



Diode I-V characteristic can be considered to be linear in this small $\boldsymbol{\nu}_D$ interval.

Small Signal Modeling-Diode

The diode can be represented by a 60 Ω resistor in the small signal equivalent circuit. Then we can apply the voltage division rule as



$$v_{dac} = v_{ac}\frac{r_d}{r_d + R} \cong 0.057 v_{ac} \cong 1.1 mVSinwt$$

Then the total (ac+DC) voltage on the diode is $\underbrace{0.58\ \text{V}}_{\text{DC}}+\underbrace{1.1\ \text{mVSinwt}}_{\text{ac}}$

CHECK YOURSELF-POINT

Q: While the diode current depends nonlinearly on the diode voltage, we have modeled the diode as a resistor in the ac equivalent circuit. What is the (specified) condition justifying this approach?

S: write

Small Signal Modeling-Diode

CHECK YOURSELF-POINT

Q: How does r_d depend on V_{DC}. Explain qualitatively.

S: write

In case, you do not have access to the graphical diode data, you can use the diode equation to carry out an equivalent analysis. The saturation current (I_S) of the diode in the circuit is 77 fA and n=1 (ideal diode). If we write the diode equation

$$i_D = I_S(e^{v_D/V_T} - 1) \rightarrow I_D + i_d = I_S(e^{\frac{V_D+v_d}{V_T}} - 1)$$

$$Since\ V_D >> V_T, I_D + i_d \cong I_S e^{\frac{V_D+v_d}{V_T}} = I_S e^{\frac{V_D}{V_T}} e^{\frac{v_d}{V_T}} = I_S e^{\frac{V_D}{V_T}}\left[1 + \frac{v_d}{V_T} + \frac{1}{2}(\frac{v_d}{V_T})^2 + ...\right]$$

$$\cong I_S e^{\frac{V_D}{V_T}}(1 + \frac{v_d}{V_T}) \text{ if } \frac{v_d}{V_T} >> \frac{1}{2}(\frac{v_d}{V_T})^2 \text{ or } v_d << 2V_T$$

Small Signal Modeling-Diode

$$I_D + i_d \cong I_S e^{\frac{V_D}{V_T}}\left(1+\frac{v_d}{V_T}\right) = \underbrace{I_S e^{\frac{V_D}{V_T}}}_{\text{DC}} + \underbrace{\frac{I_S e^{\frac{V_D}{V_T}}}{V_T} v_d}_{\text{ac}} \quad \text{if } v_d << 2V_T \cong 50mV \text{ at } 300\text{ K}$$

$$i_d = \frac{I_S e^{\frac{V_D}{V_T}}}{V_T} v_d = \frac{I_D}{V_T} v_d, \text{ then } r_d = \frac{V_T}{I_D}$$

diode small signal resistance

DC diode current

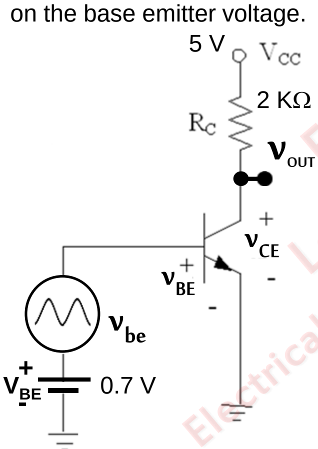
The small signal resistance of the diode is determined by the DC operating point as expected. Furthermore, we see that in order to have the ac diode current linearly depend on the ac diode voltage (represent the diode with a resistor in the ac equivalent circuit), the ac voltage on the diode should be much smaller than approximately 50 mV at room temperature. This is the **small signal condition** discussed previously.

The DC current of the diode in our circuit was 0.42 mA. Then r_d=25 mV/0.42 mA≈60 Ω which is equal to the small resistance found by graphical analysis. Note that the conditions satisfy the small signal requirement, since the amplitude of the ac voltage on the diode (≈1 mV) is much smaller than $2V_T$.

Introduction to BJT Amplifiers

Ref. 4: 5.6

If an ac signal is applied to the base of an npn BJT biased in the forward active region, this signal introduces an ac component to the base-emitter junction voltage of the BJT. As result, the collector current in the circuit includes an ac component since it depends on the base emitter voltage.



Remember that $I_C \cong I_S e^{\frac{V_{BE}}{V_T}}$ in the forward active region.

$$i_C = I_S e^{\frac{V_{BE}+v_{be}}{V_T}} = I_S e^{\frac{V_{BE}}{V_T}} e^{\frac{v_{be}}{V_T}} \cong I_S e^{\frac{V_{BE}}{V_T}}\left(1+\frac{v_{be}}{V_T}\right)$$

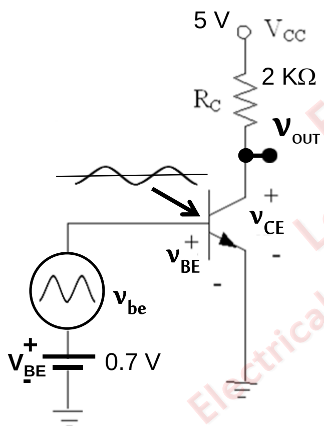
if $v_{be} << V_T$

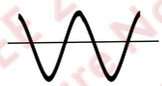
$$= \underbrace{I_S e^{\frac{V_{BE}}{V_T}}}_{I_C \text{ DC}} + \underbrace{I_S e^{\frac{V_{BE}}{V_T}} \frac{v_{be}}{V_T}}_{i_c \text{ ac}}$$

($e^x \approx$ 1+x for small x)

$$v_{CE} = v_{OUT} = V_{CC} - i_C R_C = V_{CC} - (I_C + i_c)R_C = \underbrace{V_{CC} - I_C R_C}_{\text{DC}} + \underbrace{- i_c R_C}_{\text{ac}}$$

For small amplitude $\mathbf{v}_{be}$:





$$v_{OUT} = \underbrace{V_{CC} - I_C R_C}_{\text{DC}} + \underbrace{- i_c R_C}_{\text{ac}}$$

$\mathbf{v}_{be} \rightarrow$ ac input signal

$\mathbf{v}_{ce} = -\mathbf{i}_c R_C \rightarrow$ ac output signal

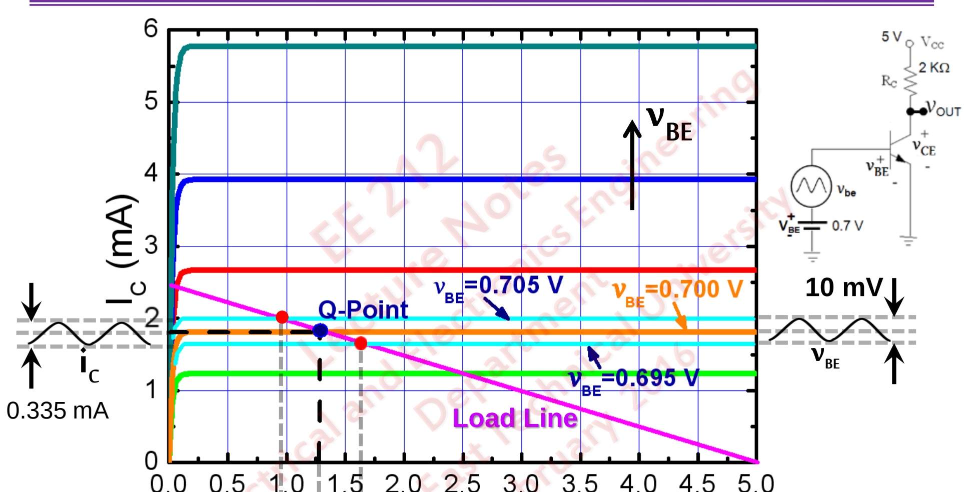
$$v_{ce} = -i_c R_C = -I_S e^{\frac{V_{BE}}{V_T}} \frac{v_{be}}{V_T} R_C = -\frac{I_C}{V_T} R_C v_{be}$$

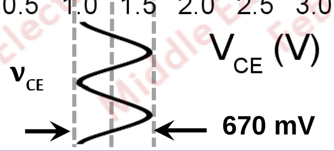
180° phase difference

$$A_V\,(voltage\ gain) = \frac{v_{out}}{v_{be}} = -\frac{I_C}{V_T} R_C = -g_m R_C$$

$$g_m = \frac{I_C}{V_T} \quad \text{Transconductance of the BJT}$$

Note that $i_c = g_m v_{be}$





$$A_V\,(voltage\ gain) = \frac{v_{out}}{v_{be}} = -67$$

Q: Does the amplifier in the above circuit amplify linearly under the given condition.

S: Yes, it does since,

$$v_{out} = v_{ce} = -\underbrace{\frac{I_C}{V_T} R_C}_{\text{constant (set by DC biasing conditions)}} v_{be}$$

output (ν_{out}) depends linearly on input (ν_{be})

Q: What is the required condition for linear amplification?

S: Remember that we have assumed small amplitude ν_{be} so that

$$i_C = I_S e^{\frac{V_{BE}+v_{be}}{V_T}} = I_S e^{\frac{V_{BE}}{V_T}} e^{\frac{v_{be}}{V_T}} \cong I_S e^{\frac{V_{BE}}{V_T}} (1+\frac{v_{be}}{V_T}) = \underbrace{I_S e^{\frac{V_{BE}}{V_T}}}_{I_C} + \underbrace{I_S e^{\frac{V_{BE}}{V_T}} \frac{v_{be}}{V_T}}_{i_c}$$

i_c linearly depends on ν_{be}.

Q: How small ν_{be} should be for linear amplification?

S: Small enough to have

$$e^{\frac{v_{be}}{V_T}} = \left[1+\frac{v_{be}}{V_T}+\frac{1}{2}(\frac{v_{be}}{V_T})^2+....\right] \cong 1+\frac{v_{be}}{V_T} \Rightarrow$$

$$\frac{v_{be}}{V_T} >> \frac{1}{2}(\frac{v_{be}}{V_T})^2 \Rightarrow v_{be} << 2V_T$$

This is the small signal condition for amplification with BJTs.

Q: What happens if this condition is not satisfied?

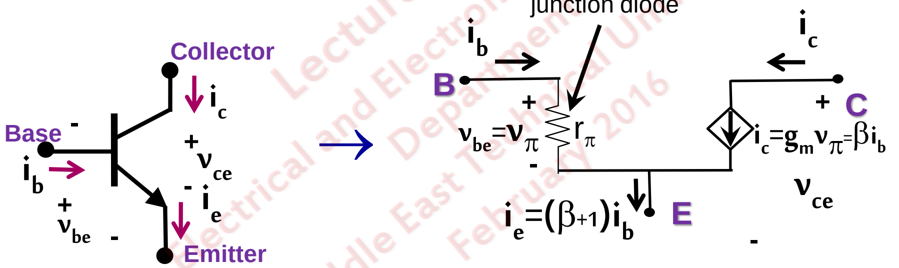
S: Nonlinear amplification $\rightarrow$ **Distortion !**

Q: How do I find the small signal ac characteristics (such as ac voltage gain) of a BJT amplifier without going through (tedious) graphical analysis?

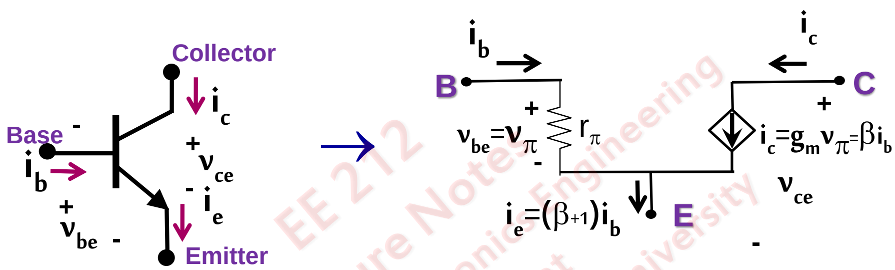
S: Similar to what we have done for the diode, you need to replace the BJT with a small signal ac equivalent circuit. Now let's construct this equivalent circuit. So far we found that

$$i_c = g_m v_{be} = \frac{I_C}{V_T} v_{be}$$

small signal resistance of the forward biased base-emitter junction diode



The above equivalent circuit is called the **Hyrid-π Small Signal Equivalent Circuit**

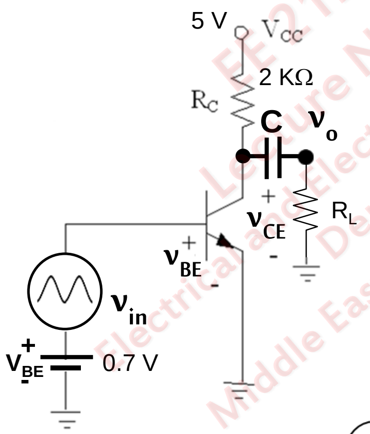


$$r_\pi = \frac{v_{be}}{i_b} = \frac{v_\pi}{i_c/\beta} = \frac{\beta v_\pi}{g_m v_\pi} = \frac{\beta}{g_m} = \frac{\beta}{I_C/V_T} = \frac{V_T}{I_B}$$

$$g_m = \frac{I_C}{V_T}$$

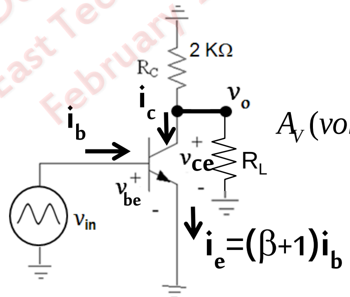
Small signal model parameters depend on the DC biasing conditions!

Q: Find the small signal voltage gain of the following circuit.



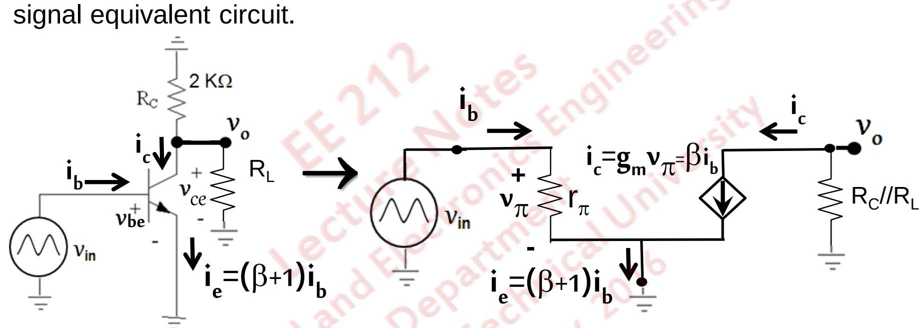
S: Since we are interested in the ac voltage gain, we start by drawing the ac equivalent circuit.

		Replace	
Ideal **DC Power Supply**	→	**Short Circuit**	
Ideal **DC Current Supply**	→	**Open Circuit**	
Large Enough **Capacitor**	→	**Short Circuit**	
Large Enough **Inductor**	→	**Open Circuit**	



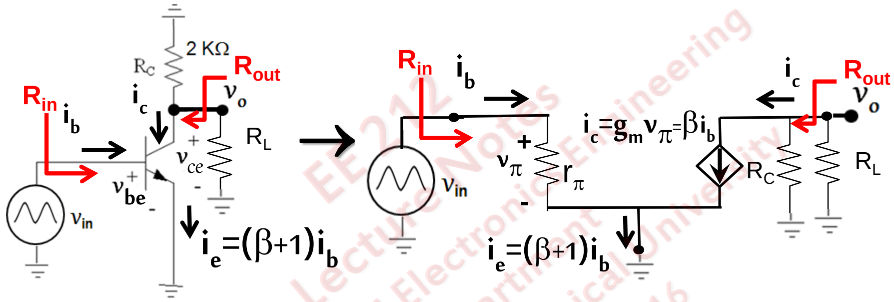
$$A_V(voltage\ gain)=\frac{v_o}{v_{in}}$$

After drawing the ac equivalent circuit, the BJT is replaced with the small signal equivalent circuit.



$$A_V=\frac{v_o}{v_{in}}=\frac{-g_m v_\pi (R_C//R_L)}{v_\pi}=-g_m(R_C//R_L)$$

Now let's find the small signal input and output resistances of the circuit.



$$R_{in} = \frac{v_{in}}{i_b} = \frac{v_\pi}{i_b} = r_\pi, \qquad R_{out} = R_C$$

CHECK YOURSELF-POINT

Q: How is the input resistance affected by the Q-point of the BJT?

S: write

CHECK YOURSELF-POINT

Q: How large a capacitor should be in order to be replaced with a short circuit in the ac equivalent circuit? Discuss qualitatively.

S: write

CHECK YOURSELF-POINT

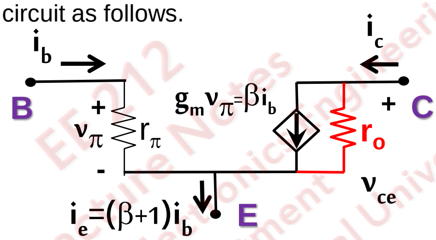
Q: How do you represent nonideal DC voltage and current sources in the ac equivalent circuit?

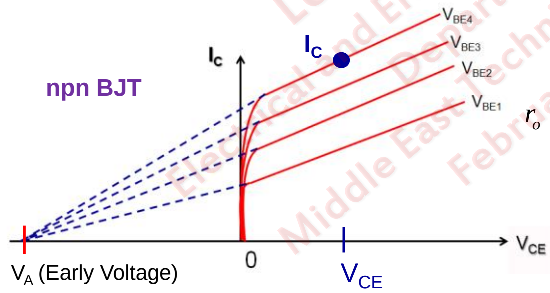
S: write

Introduction to BJT Amplifiers

Ref. 4: 5.6

So far we have modeled the BJT (in the F.A. region) as an ideal controlled current source. However, we know from an earlier discussion that the collector current depends on the collector emitter voltage through the Early Effect which can be included in the small signal equivalent circuit as follows.





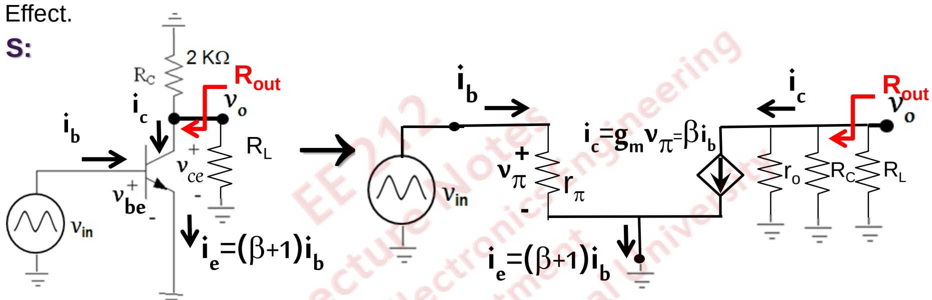
$$r_o = \left(\frac{dI_C}{dV_{CE}}\right)^{-1} = \frac{V_A + V_{CE}}{I_C} \cong \frac{V_A}{I_C}$$

Introduction to BJT Amplifiers

Ref. 4: 5.6

Q: Find the voltage gain and the output resistance of the amplifier including the Early Effect.

S:



$$A_V = \frac{v_o}{v_{in}} = \frac{-g_m v_\pi (R_C // R_L // r_o)}{v_\pi} = -g_m (R_C // R_L // r_o) \qquad R_{out} = R_C // r_o$$

Q: What is the voltage gain of the above amplifier in terms of the DC voltage drop on R_C if $R_L // r_o >> R_C$.

S:

$$A_V = \frac{v_o}{v_{in}} = \frac{-g_m v_\pi (R_C // R_L // r_o)}{v_\pi} \cong -g_m R_C = -\frac{I_C R_C}{V_T} \quad \text{(Remember that } g_m = \frac{I_C}{V_T}\text{)}$$

Q: What is the voltage gain of the amplifier if $I_C R_C = V_{CC}/3$ (Remember the biasing design guidelines).

S: $$A_V = -\frac{I_C R_C}{V_T} = \frac{V_{CC}}{3V_T} \cong 13V_{CC}$$

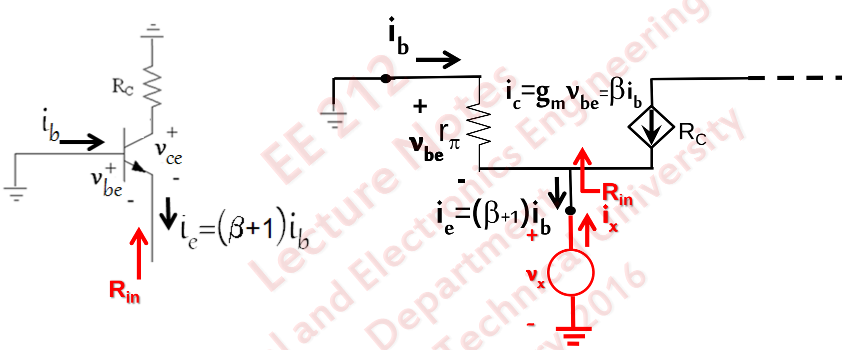
CHECK YOURSELF-POINT

Q: Is it possible (practically) to have a very large small signal voltage gain with a single BJT amplifier?

S: *write*

Q: Find the resistance seen from the emitter of a BJT with the base grounded.

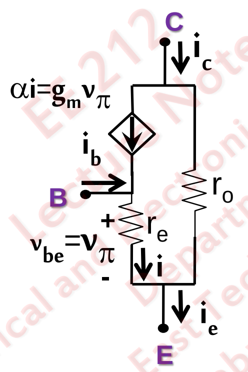
S:



$$R_{in} = \frac{v_x}{i_x} = \frac{v_{be}}{i_e} = \frac{i_b r_\pi}{(\beta+1)i_b} = \frac{r_\pi}{(\beta+1)} = r_e, \quad \text{Note that } v_x = -v_{be} \text{ and } i_x = -i_e$$

The resistance seen from the base with emitter grounded (r_π) is larger than this resistance (r_e) by a factor of β+1. **Resistance Reflection Rule:** multiply the resistance connected to the emitter by β+1 to reflect it to the base.

Based on the above discussion, it should be clear that the following equivalent circuit can be used as an alternative to the hybrid-π model to represent the small signal equivalent of the npn BJT.



T-Equivalent Circuit

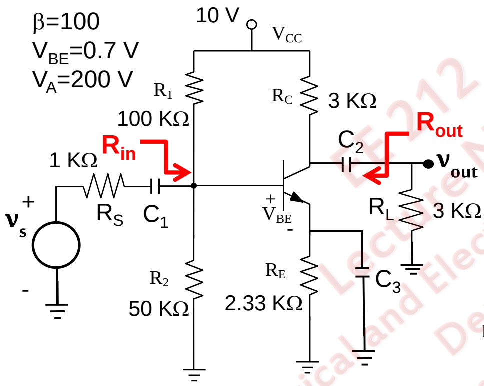
CHECK YOURSELF-POINT

Q: Draw the small signal models for pnp BJT.

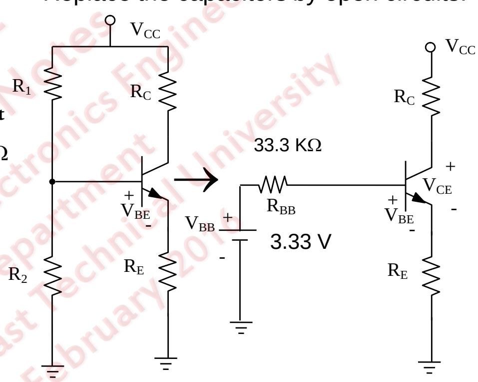
S: write

Introduction to BJT Amplifiers-Common Emitter Amplifier

Q: Find the voltage gain and the input and output resistances of the following amplifier.



S: Start with DC analysis.
Replace the capacitors by open circuits.



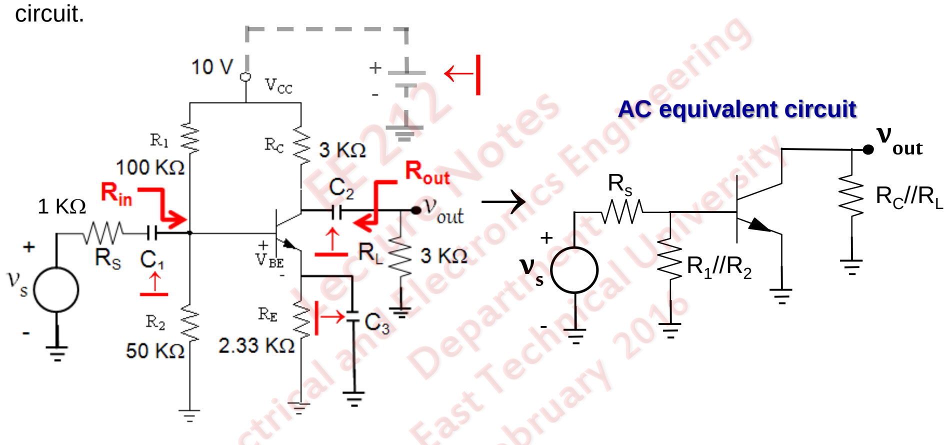
C_1, C_2: coupling capacitors (input source and load can be coupled without disturbing the Q-point.)
C_3: bypass capacitor (increases the gain of the amplifier by removing R_E from the ac equivalent circuit).

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta+1)R_E} = \frac{3.33 - 0.7}{33.3 + 101x2.33} \cong 10\ \mu A$$

$$I_C = \beta I_B = 1\text{ mA},\ \ V_{CE} = V_{CC} - I_C R_C - I_E R_E \cong 4.7\text{ V}$$

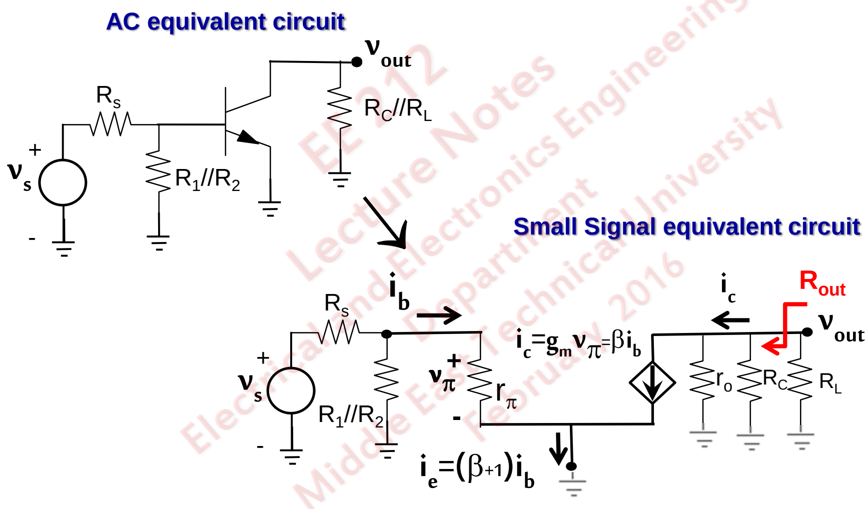
Introduction to BJT Amplifiers-Common Emitter Amplifier

Draw the AC equivalent circuit. Replace the capacitors and dc voltage sources by short circuit.

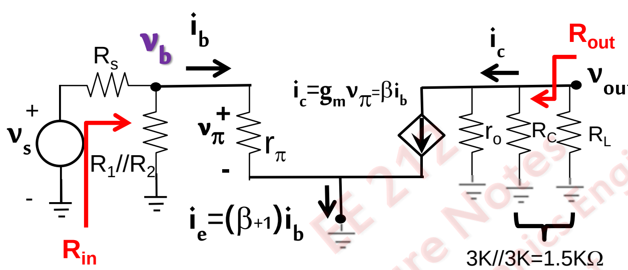


Introduction to BJT Amplifiers-Common Emitter Amplifier

Replace the BJT with the small signal equivalent circuit.



Introduction to BJT Amplifiers-Common Emitter Amplifier



$$g_m=\frac{I_C}{V_T}=\frac{1mA}{26mV}=38.5\ mA/V$$

$$r_\pi=\frac{V_T}{I_B}=\frac{\beta}{g_m}=\frac{100}{38.5x10^{-3}}=2.6K\Omega$$

$$r_o=\frac{V_A}{I_C}=\frac{200V}{1mA}=200K\Omega$$

$$r_o>>R_C//R_L$$

$$A_V=\frac{v_{out}}{v_s}=\frac{v_{out}}{v_b}\frac{v_b}{v_s}=\frac{-g_m v_\pi(R_C//R_L//r_o)}{v_\pi}\frac{R_{in}}{R_S+R_{in}}$$

$$=-g_m(R_C//R_L//r_o)\frac{R_1//R_2//r_\pi}{R_S+R_1//R_2//r_\pi}\cong-40$$

$$R_{in}=R_1//R_2//r_\pi\cong 2.4K\Omega,\quad R_{out}=R_C//r_o\cong R_C=3K\Omega$$

Introduction to BJT Amplifiers-Common Emitter Amplifier

CHECK YOURSELF-POINT

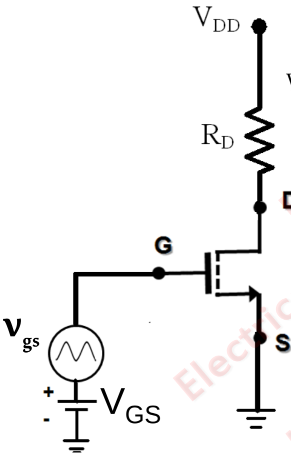
Q: Discuss qualitatively how you can improve the voltage gain of the above amplifier.

S: write

Introduction to MOSFET Amplifiers

Ref. 4: 4.6

If an ac signal is applied to the gate of an n-channel enhancement mode MOSFET biased in the saturation region, this signal introduces an ac component to the gate-source voltage of the MOSFET. As result, the drain current in the circuit includes an ac component since it depends on the gate-source voltage.



Remember that $i_D = \frac{K_n}{2}(v_{GS} - V_T)^2$ in the saturation region

where $K_n = \frac{C_{ox}''\mu_n W}{L}$.

$$i_D = I_D + i_d = \frac{K_n}{2}(v_{GS} - V_T)^2 = \frac{K_n}{2}(V_{GS} + v_{gs} - V_T)^2$$

$$= \frac{K_n}{2}\left[(V_{GS} - V_T)^2 + 2(V_{GS} - V_T)v_{gs} + v_{gs}^2\right]$$

$$if\ \ v_{gs}^2 << 2(V_{GS} - V_T)v_{gs} \ \text{ or } v_{gs} << 2(V_{GS} - V_T)$$

$$i_D = I_D + i_d = \underbrace{\frac{K_n}{2}(V_{GS} - V_T)^2}_{\text{DC}} + \underbrace{K_n(V_{GS} - V_T)v_{gs}}_{\text{ac}}$$

DC + ac

$$i_d = K_n(V_{GS} - V_T)v_{gs} \qquad if \quad v_{gs} << 2(V_{GS} - V_T)$$

ac drain current depends linearly on ac gate-source voltage → linear amplification.

This is the **small signal condition** for MOSFET.

As found in the preceeding chapter (and as obvious from the above result):

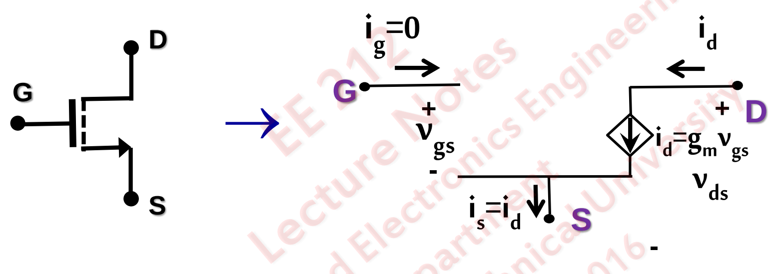
$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{\text{Q-point}} = C_{ox}{}'' \mu_n \frac{W}{L}(V_{GS} - V_T) = K_n(V_{GS} - V_T) = \frac{2I_D}{V_{GS} - V_T}$$

CHECK YOURSELF-POINT

Q: Compare the small signal requirements for BJT and MOSFET. Which device can handle larger amplitude ac input signals while providing linear amplification?

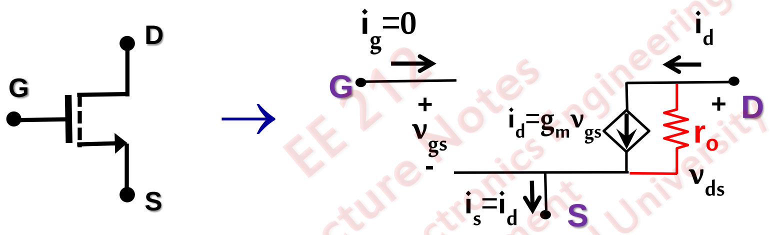
S: write

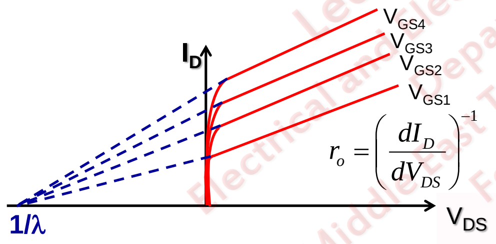
Now, let's construct the small signal equivalent circuit for the MOSFET operating in the saturation region.



$$g_m = K_n(V_{GS} - V_T) = \frac{2I_D}{V_{GS} - V_T}$$

In order to account for the channel length modulation effect the finite output resistance should be added to the equivalent circuit.



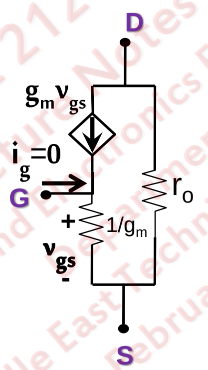


$$r_o = \frac{1/\lambda + V_{DS}}{I_D} \cong \frac{1}{\lambda I_D}$$

CHECK YOURSELF-POINT 

Q: Show that the following T-small signal model for the MOSFET is equivalent to the above model.

S: write



T-Equivalent Circuit

CHECK YOURSELF-POINT

Q: Draw the small signal equivalent circuit for the p-channel MOSFET.

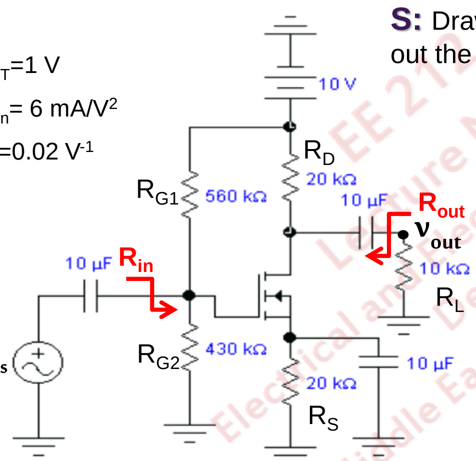
S: write

Q: Find the small signal voltage gain and the input and output resistances of the following MOSFET amplifier.

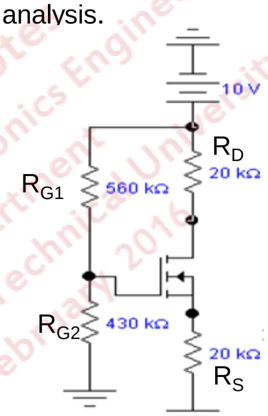
V_T=1 V

K_n= 6 mA/V^2

λ=0.02 V^{-1}



S: Draw the DC equivalent circuit and carry out the DC analysis.



Q-point: (1.56×10^{-4}A, 3.76V)

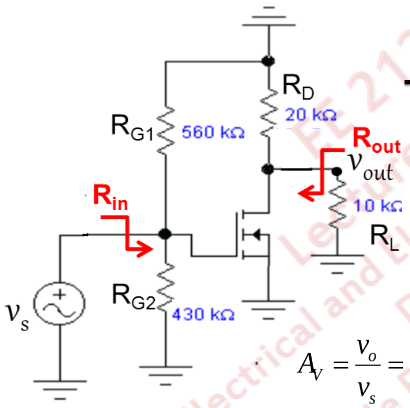
V_{GS}=1.23V

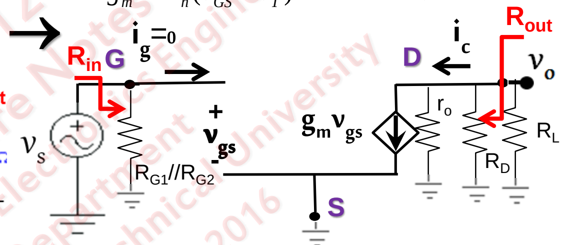
Introduction to MOSFET Amplifiers-Common Source Amplifier

Draw the ac equivalent circuit and replace the MOSFET with the small signal equivalent circuit.

$$r_o \cong \frac{1}{\lambda I_D} = 320K\Omega$$

$$g_m = K_n(V_{GS} - V_T) = 1.38\ mA/V$$





$$A_V = \frac{v_o}{v_s} = \frac{-g_m v_{gs}(R_D // R_L // r_o)}{v_{gs}} = -g_m(R_D // R_L // r_o) \cong -9$$

$$R_{in} = R_{G1} // R_{G2} = 243K\Omega$$

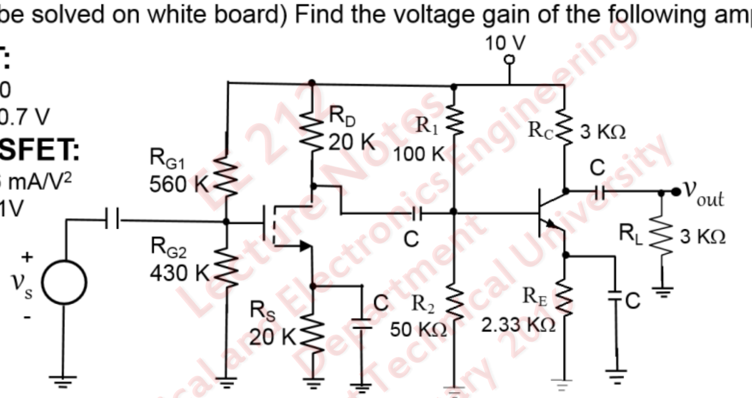
$$R_{out} = R_D // r_o \cong R_D \cong 19K\Omega$$

TWO-STAGE AMPLIFIER EXAMPLE

Q: (to be solved on white board) Find the voltage gain of the following amplifier.

BJT:
β=100
V_{BE}=0.7 V

MOSFET:
Kn=6 mA/V²
V_T = 1V



S: write

TWO-STAGE AMPLIFIER EXAMPLE

Q.1 Homework 9 (Estimated Time To Complete < 100 min.)

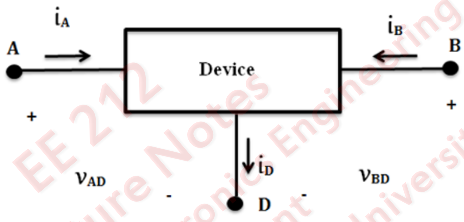
An engineer, just out of school, approaches you and says “as suggested by the equation

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

the collector current of a BJT is increased exponentially with increasing base-emitter voltage. However, in a small signal amplifier ac equivalent circuit, you model the BJT as a controlled current source ($g_m v_{be}$) which means a linear relation between the ac collector current and the ac base-emitter voltage. Moreover, you say that g_m depends on the dc collector current. I am totally confused.” Help him by providing an explanation as complete as possible.

Q.2 Homework 9

Consider the following three-terminal semiconductor device with the given terminal current-voltage relations.



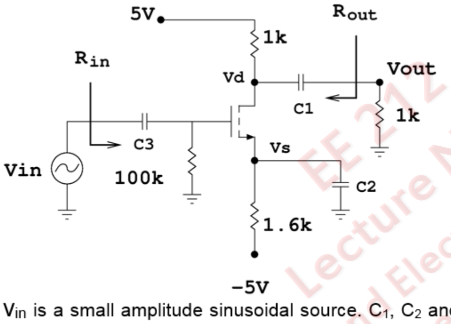
$$i_B = Cv_{AD}^2 \qquad i_D = i_B \qquad i_A = 0$$

i) Find the small-signal requirement on the input voltage (V_{ad}) such that the ac **output current (i_b)** depends linearly on the ac input voltage v_{ad}.

ii) Draw the small signal equivalent circuit and find the expression(s) for the small signal model parameter(s).

Q.3 Homework 9

Consider the amplifier below. All the resistances are given in Ohms.



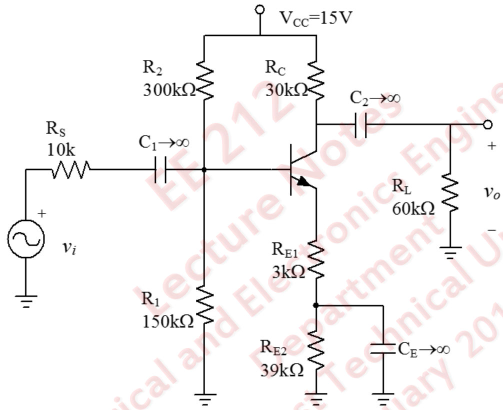
V_{in} is a small amplitude sinusoidal source. C_1, C_2 and C_3 are large capacitors. The transistor is an n-channel enhancement type MOSFET and has a threshold voltage of 1 V and transconductance parameter (K_n) of 0.01 A/V^2 (λ=0).

i) Calculate the DC bias (Q) point (the quiescent bias point).
ii) Calculate the small signal transconductance of the MOSFET.
iii) Draw the small signal equivalent circuit of the amplifier.
iv) Calculate the small signal voltage gain from vin to vout.
v) Calculate the input and output resistances.

Q.4 Homework 9

Consider the BJT amplifier circuit shown below. C_1, C_2 and C_E are large enough.

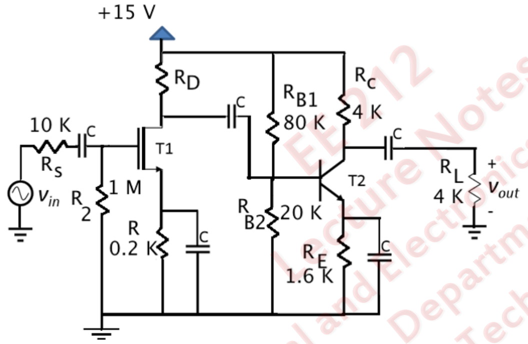
β=100
V_{BE}= 0.7 V



i) Determine the emitter quiescent (DC) current, I_{EQ}.
ii) Draw the small signal AC equivalent of the circuit, and calculate the values of the small signal model parameters.
iii) Determine the small-signal voltage gain $A_v = \dfrac{v_0}{v_i}$.

Q.5 Homework 9

Consider the following circuit constructed with a n-channel depletion mode MOSFET and an npn BJT. The capacitors are large and V_{in} is a small signal.



MOSFET Parameters:
K_n=10 mA/V^2
V_{TN}= -2 V
λ=0

BJT Parameters:
β= 150
$V_{BE\ (DC)}$= 0.7 V
V_A= ∞

i) Find the value of R_D that results in a DC drain-source voltage (V_{DS}) of 11 V in T_1.
ii) Find the Q-point of T_2.
iii) Draw the small signal equivalent circuit of the amplier.
iv) Find the expression for the small signal voltage gain of the amplifier and calculate it.