A Simple Behavioral Electro-Thermal Model of GaN FETs for SPICE Circuit Simulation

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***Abstract*— This paper develops a behavioral electro-thermal model of GaN FETs for power-electronic circuit simulation in SPICE software environment. The model couples an available GaN FET electrical model with a thermal *RC* network for junction temperature estimation, while using modification circuits between an eGaN FET device and its gate driver to embed thermal impacts on the device performance. Both the static and switching characteristics of the developed model are compared with those from the original electrical model. Performance and functionality of the developed electro-thermal model in a boost converter, based on time-domain simulation studies in the SPICE environment, are evaluated and experimentally verified.**

***Index Terms*— Device characterization, electro-thermal modeling, GaN FET, SPICE circuit simulation.**

I. Introduction

THE Wide Band-Gap (WBG) switching devices, particularly the GaN devices, have become attractive switching devices for power electronic systems due to their unique electrical and thermal capabilities/characteristics compared with their Si counterparts, enabling considerable reduction of the size of passive components and thermal management effort and improvement of the efficiency and power density [1]–[5]. However, as the devices and the power electronic systems become smaller, the heat dissipation becomes more difficult and new challenges are imposed on thermal management [6]. Therefore, at the design stage of GaN-based power electronic systems, it is necessary to determine the junction temperature profile of the switching devices to ensure that they operate within their safe operation area. The junction temperature also has significant impacts on the electrical performance of GaN FET devices, and therefore, for accurate temperature estimation, the device model needs to take the thermal impacts into account [7], [8]. Consequently, the electro-thermal modeling of GaN devices is one of the important steps for system design/integration.

Despite the importance of electro-thermal modeling of GaN devices, as mentioned in [9], an electro-thermal model for the GaN FET that considers the device self-heating is not yet readily available. Efforts have been made to develop the electro-thermal models for GaN HEMTs, which considered nonlinear thermal effects, self-heating effects, and bias dependence [7], [10], [11], for radio frequency applications. Reference [8] presents the electro-thermal models for both GaN vertical MOSFETs and GaN lateral HEMTs based on device physics. However, physical models generally involve many device parameters with mutual couplings, which make their implementation difficult for circuit simulation [12]. On the other hand, the results obtained from physics-based models may not be as accurate as those from behavioral models [13]. Thus, simple and accurate behavioral models are considered more favorable for circuit simulations. In addition, the existing electro-thermal models focus on the effect of junction temperature on the I_{ds}–V_{ds} relationship during the device conduction period. The thermal effects on the device switching characteristics, however, are only explored in terms of switching losses instead of parameters, such as dv/dt and di/dt, which are important for loss evaluation, system reliability, and Electromagnetic interference issues [7]–[11]. The PLECS toolbox is capable of providing lookup-table-based electro-thermal model for a power device at different temperatures and estimating the device temperature based on its power losses. However, the PLECS toolbox does not take junction temperature of the device as an input to include the temperature impact on the device characteristics [14]. Furthermore, the model in the PLECS toolbox focuses mainly on the power loss perspective and does not provide detailed transient waveforms as those obtained from circuit simulations. After all, to the best of the authors' knowledge, no behavioral electro-thermal model for circuit simulation that considers both the device static and switching characteristics has been developed for GaN FETs.

In this paper, a simple behavioral electro-thermal model for EPC2010C GaN FET is developed in the LTSPICE software environment. The model couples an available electrical model of the device with a thermal *RC* network to count the self-heating effects. The developed model embeds the impacts of junction temperature on the device static and switching characteristics by using a gate voltage modification circuit. The accuracy of the developed model is validated against the original fixed-temperature electrical model. To demonstrate the capability/accuracy of the developed model in estimating the junction temperature profile of the device in the SPICE circuit simulation, a boost converter is used as the benchmark system. The simulation waveforms based on the developed model are compared with their experimental counterparts obtained from a Double Pulse Tester (DPT) circuit built based on EPC2010C GaN FETs, and the thermal measurement of an EPC2010C GaN FET operating in a boost converter.

This paper is organized as follows. In Section II, the proposed electro-thermal model of GaN FET, including the operating principles of the gate voltage modification circuit during conduction periods and switching transients, is

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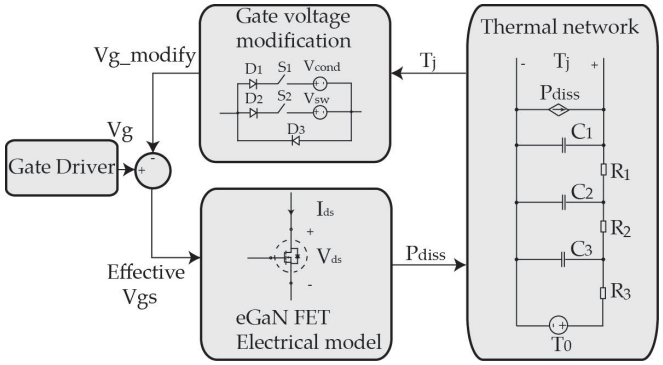


Fig. 1. Block diagram of the proposed electro-thermal model.

introduced. In Section III, the performance of the developed electro-thermal model is validated against the original electrical model for the static and switching characteristics and the gate voltage/current waveforms. The performance of the developed model in circuit simulation is also demonstrated in Section III. Experimental results from a DPT circuit built based on EPC2010C GaN FETs are presented and used to validate the developed model in Section IV. Section IV also compares the estimated device temperature based on the developed model with that from PLECS toolbox and thermal measurement of the device operating in a boost converter. Finally, Section V concludes the paper.

II. Proposed Electro-Thermal Model of the GaN FET

In general, an electro-thermal model consists of an electrical model of the device coupled with a thermal *RC* network [7], [15]. The thermal network, as shown in Fig. 1, takes the dissipated power in the device as the input and provides the voltage across the network, which represents the junction temperature, as the output. The junction temperature is fed back into the electrical model, impacting the device parameters and characteristics. Although the available electrical models have built-in functions to calculate the device parameters at various junction temperatures, they are not capable of dynamically updating the parameters with a variable temperature profile during simulation. In this paper, a gate voltage modification circuit is developed, which, as shown in Fig. 2(a), modifies the gate voltage of the device based on its junction temperature profile, thereby attaining an accurate electro-thermal model.

As shown in Fig. 2, three diodes are considered in each branch of the gate modification circuit, which ensure the gate current flows in the expected direction. Furthermore, two switches S_1 and S_2 are turned ON/OFF with optimal timing to complete the gate voltage modification during device conduction period and switching transients, respectively. To minimize the impacts on the device performance during the SPICE simulation, ideal diodes with no forward voltage drop have been used. S_1 and S_2 are the ideal switches with voltage across the GaN switch as the control signal. If the voltage across the GaN switch falls below 0.3 V, the switch is identified to be operating in the conduction mode and S_1 conducts while S_2 is blocked. If the voltage is beyond 0.3 V, the GaN switch is identified in the switching transition mode and S_2 conducts while S_1 is blocked. The dissipated power P_{diss} is modeled as

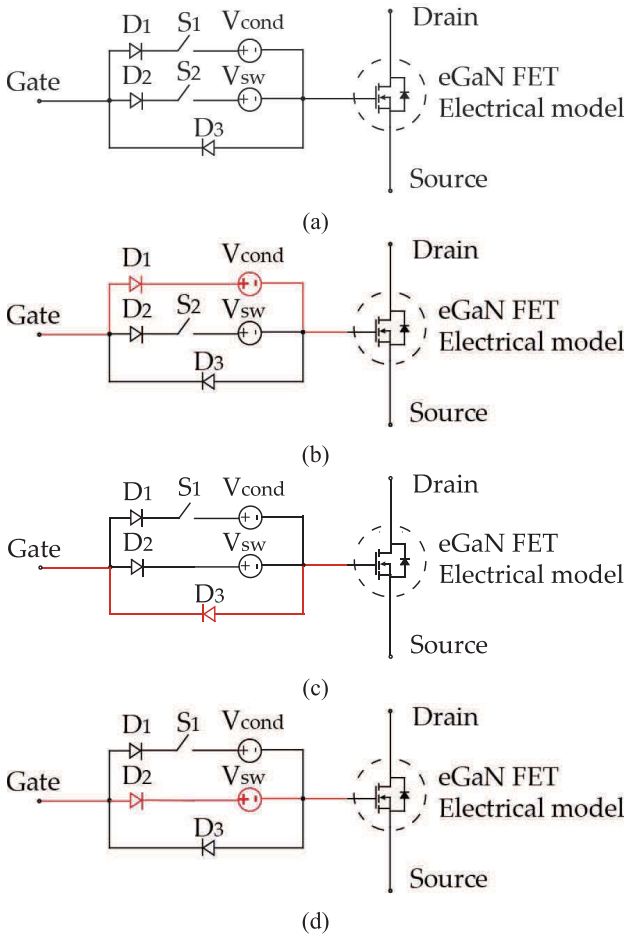


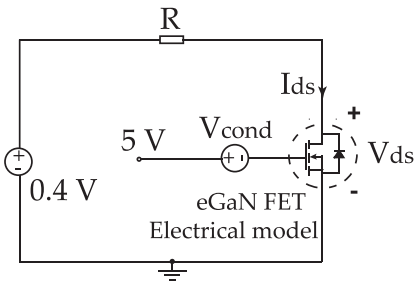
Fig. 2. (a) Proposed gate voltage modification circuit and (b), (c), and (d) its operation principles during device conduction period and turn-OFF and turn-ON transients, respectively.

a controlled current source whose value is calculated as the product of the device voltage and current.

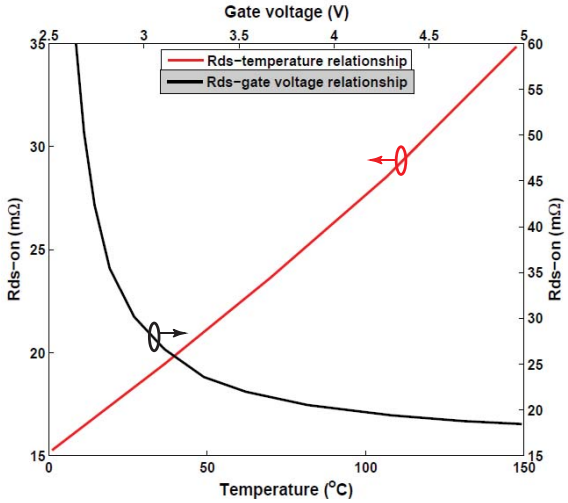
The operating principles and implementation of the modification circuit applied to the gate terminal are explained in detail in section II-A and II-B.

A. Modeling of Static Characteristic

The key parameter for the static characteristic of the device, which refers to I_{ds}–V_{ds} relationship during conduction period, is the ON-state resistance, $R_{ds,ON}$. The ON-state resistance of GaN FET is a near-linear function of its junction temperature, as shown in Fig. 3(b) [16]. On the other hand, at fix-temperature simulations of the circuit in Fig. 3(a), $R_{ds,ON}$ is also found to be a function of the gate voltage V_{gs}, as shown in Fig. 3(b). Thus, by using an additional voltage source V_{cond} controlled by the junction temperature during conduction period as shown in Fig. 2(b), $R_{ds,ON}$ can be changed based on the junction temperature profile. The value of V_{cond} is determined by a lookup table reflecting $R_{ds,ON}$–V_{gs} relationship obtained from Fig. 3(a) by applying several different gate voltages. During an electro-thermal simulation using the proposed model, first, $R_{ds,ON}$ corresponding to the current temperature is calculated based on $R_{ds,ON}$-temperature relationship, and an arbitrary behavioral voltage source in LTSPICE is used as V_{cond} with values determined based on the $R_{ds,ON}$–V_{gs} lookup table.



(a)



(b)

Fig. 3. (a) Circuit to test $R_{ds,ON}$–V_{gs} relationship. (b) Relationship between the ON-state resistance, junction temperature, and gate voltage.

B. Modeling of Switching Characteristics

To model the temperature-dependent switching characteristics of the device, the impacts of junction temperature on the device turn-OFF and turn-ON transients need to be identified. By using a conventional DPT circuit as shown in Fig. 4 in the LTSPICE environment, it is observed that the turn-OFF transient is almost independent of junction temperature, while dV_{ds}/dt during the turn-ON transition has a near-linear relationship with the junction temperature. Thus, during turn-OFF transition, the device is connected directly to the gate driver through the diode D_3, as shown in Fig. 2(c). During turn-ON transition, dV_{ds}/dt is determined by [17]

$$\frac{dV_{ds}}{dt} = -\frac{V_{gs,ON} - V_{plateau}}{R_g C_{gd}} \tag{1}$$

where V_{ds} is the drain–source voltage, $V_{gs,ON}$ is the turn-ON voltage provided by the gate driver, $V_{plateau}$ is the Miller plateau voltage, R_g is the gate resistance, and C_{gd} is the gate–drain capacitance of the device. Therefore, by using an additional voltage source V_{sw} in the gate loop during the turn-ON transient as shown in Fig. 2(d), the effective $V_{gs,ON}$ of the device can be modified. This, accordingly, changes dV_{ds}/dt. To determine the value of V_{sw} for a given temperature, V_{sw} is varied in the circuit simulation in Fig. 4 under 25 °C until dV_{ds}/dt becomes the same with that under the given temperature. A lookup table reflecting V_{sw}-temperature relationship is built by repeating this process.

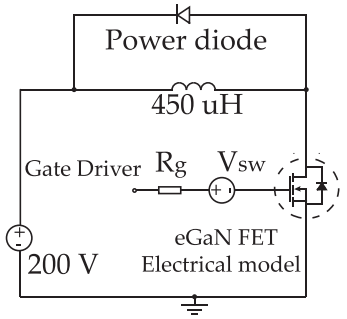
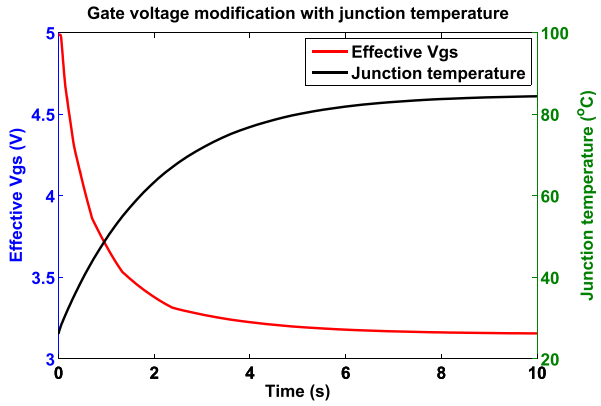
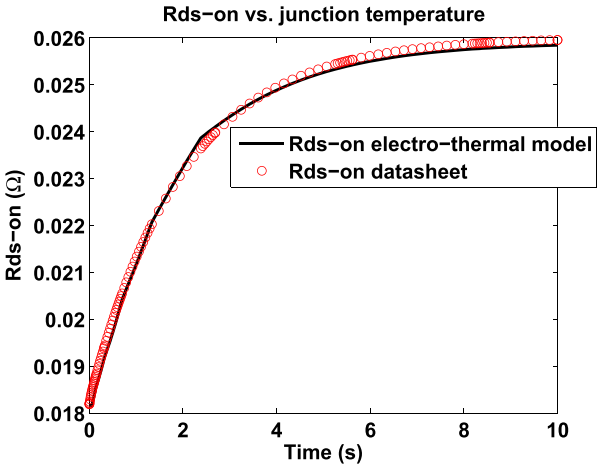


Fig. 4. DPT circuit used in simulation.



(a)



(b)

Fig. 5. (a) Gate voltage modification of the electro-thermal model during conduction mode with the junction temperature profile. (b) Modeled temperature-dependent ON-state resistance and the resistance calculated based on datasheet.

An arbitrary behavioral voltage source in LTSPICE is used as V_{sw} with values determined based on the V_{sw}-temperature lookup table.

III. Model Validation

A. Static Characteristic

To validate the temperature-dependent static characteristic, the developed model is coupled with a time-varying temperature profile generated from a constant power source and a thermal RC network derived from the device datasheet [16], being under DC bias to extract the ON-state resistance. As shown in Fig. 5(a), the effective gate–source voltage observed by the electrical device model is changed according to the varying

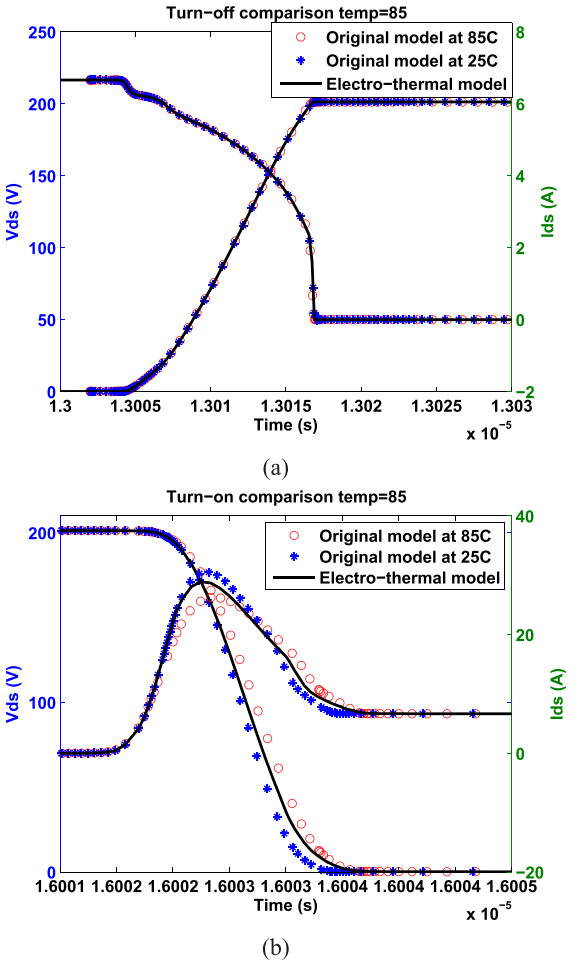


Fig. 6. (a) Turn-OFF and (b) turn-ON switching transients.

junction temperature, and the modeled ON-state resistance is consistent with the resistance estimated based on datasheet throughout the time period, as shown in Fig. 5(b).

B. Switching Characteristics

For switching transients, the developed model is implemented in a DPT circuit at various fixed temperatures, assuming that the time constant of the thermal system is sufficiently large so the temperature remains constant during a switching event [12]. The drain–source voltage V_{ds} and current I_{ds} waveforms during switching transients are shown in Fig. 6 at a junction temperature of 85 °C. By comparing the switching characteristics of the device based on the original electrical model at 25 °C and 85 °C, the impacts of junction temperature on the switching characteristics are shown in Fig. 6. As shown in Fig. 6(a), the estimated turn-OFF transient of the device based on the developed model at 85 °C is similar to the one from the original electrical model. The estimated turn-ON transient of the device is also closely matched with the one from the original electrical model. Nevertheless, the overshoot current waveform of I_{ds} during the turn-ON transition is not modeled quite accurately, because under fixed-temperature simulation, the simulation temperature also impacts other devices such as diodes in the circuit, while the proposed electro-thermal model only accounts for the GaN FET. However, the accuracy of the developed model is illustrated by dI_{ds}/dt prior to the overshoot and the end of turn-ON transient.

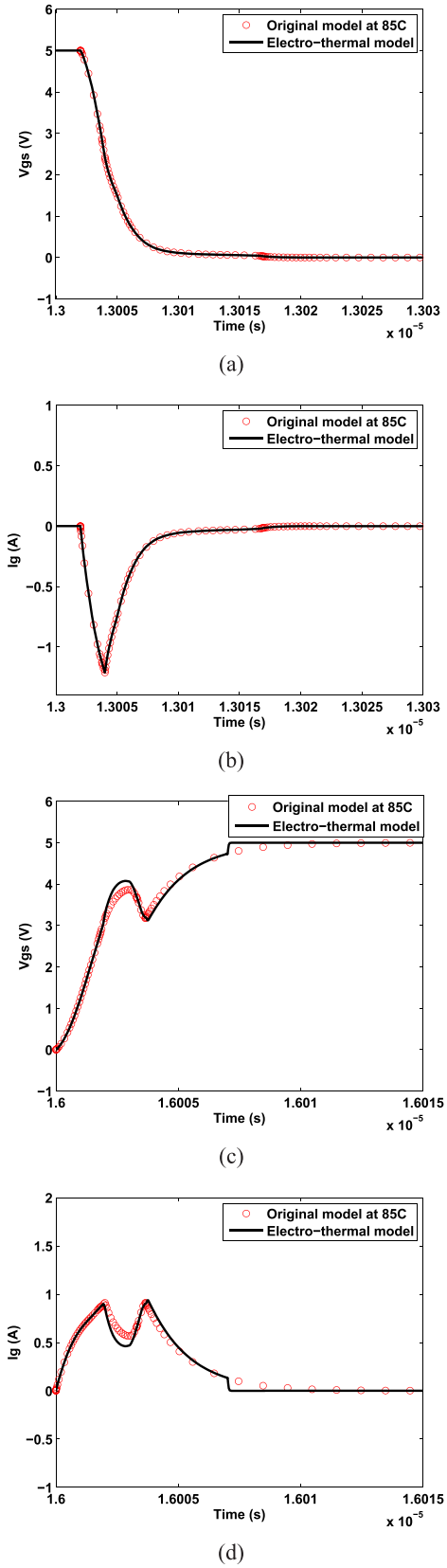


Fig. 7. (a) and (b) Turn-OFF gate voltage and current and (c) and (d) turn-ON gate voltage and current at 85 °C.

C. Gate Voltage and Current

One consideration in the development of the proposed model is to have minimal impacts on the outer circuit while

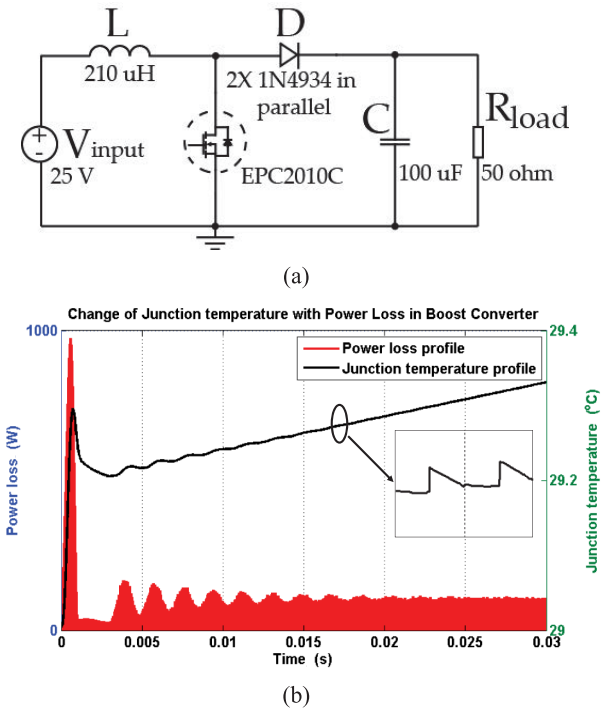


Fig. 8. (a) Boost converter benchmark system and (b) junction temperature and power loss profile of the main switch based on the proposed electro-thermal model.

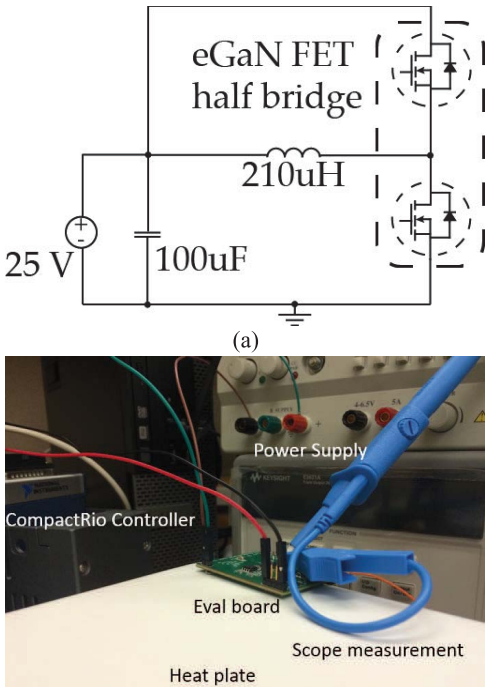


Fig. 9. (a) Block diagram and (b) experimental setup of the DPT circuit.

being capable of electro-thermal modeling. The gate voltage and current supplied by the gate driver are important factors that should not be interfered by the developed device model. Thus, it is desired that the gate voltage and current viewed from the gate driver side remain the same for the developed model as well as the original one. To explore the impact of gate voltage modification circuit on the gate voltage and current, the gate voltage and current at the gate driver terminal are recorded

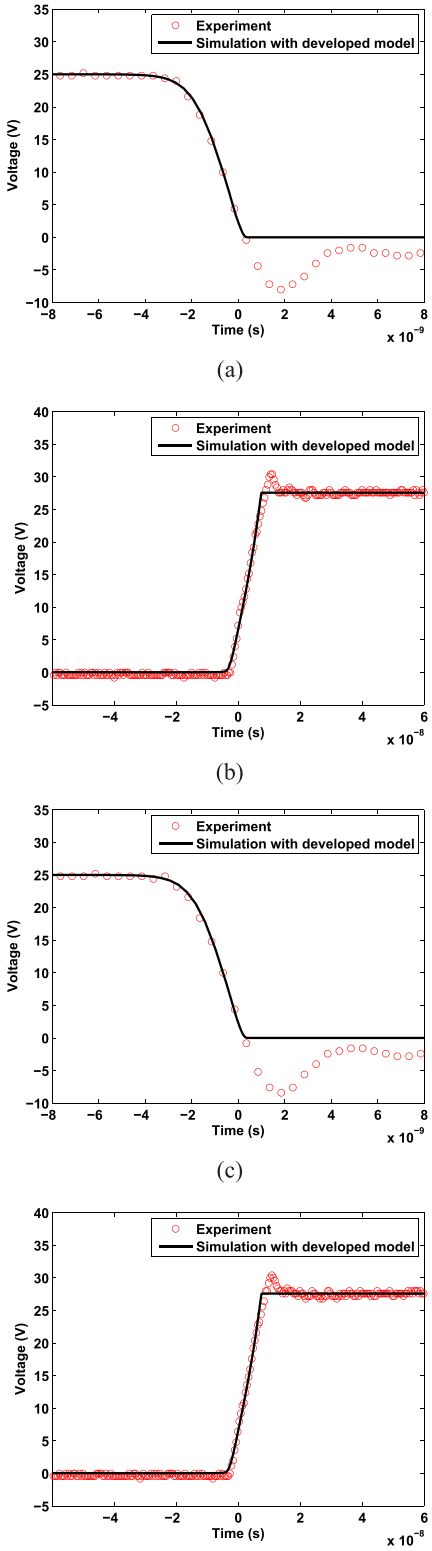


Fig. 10. Comparison of the experimental and simulation results of V_{ds} of the lower switch at 50 °C during (a) and (b) lower switch turn-ON and turn-OFF transients and at 70 °C during (c) and (d) lower switch turn-ON and turn-OFF transients.

from the DPT circuit simulation in Fig. 4 and compared with those obtained with the original model at 85 °C, as shown in Fig. 7. The turn-OFF gate voltage and current are the same with original model, as shown in Fig. 7(a) and (b). As shown in

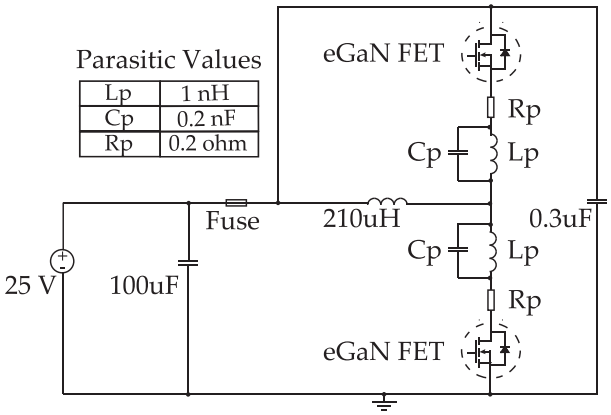


Fig. 11. DPT circuit simulation including parasitics.

Fig. 7(c) and (d), there are differences in the gate voltage and current caused by the gate voltage modification circuit during the turn-ON transient. However, the differences are very limited in terms of both amplitude and pattern of the waveforms, and thus does not induce much influence into the analysis.

D. Circuit Simulation

To demonstrate the performance of the developed model for circuit simulation studies, a 25–50 V boost converter operating at 100 kHz is constructed in the LTSPICE software environment, using the developed electro-thermal model for the main switch, as shown in Fig. 8(a). The coupled thermal RC network is developed based on the thermal SPICE model provided by EPC [18]. The power loss profile of the main switch and the corresponding junction temperature variations during the first 30 ms of simulation time are shown in Fig. 8(b). As shown in Fig. 8(b), the developed model is capable of dynamically estimating the junction temperature transients during switching cycles.

In order to measure the simulation speed, the time to run the same boost converter simulation for 3000 cycles at 100 kHz with and without the developed model is recorded. With the developed model implemented, the simulation time is about 1 min, while the simulation time with only the original model is 26.71 s, both with a PC using Intel 3.40 GHz processor with 16-GB RAM.

IV. Experimental Validation

A. Switching Performance Validation

To validate the developed electro-thermal model with experimental results, a DPT circuit is built based on an EPC2010C half-bridge evaluation board from EPC shown in Fig. 9. The board is placed on a heatplate to conduct experiments under various controlled temperatures.

A comparison of the experimental and simulation results obtained with the developed electro-thermal model of V_{ds} of the lower switch at 50 °C during both the turn-ON and turn-OFF transients is shown in Fig. 10(a) and (b), and at 70 °C in Fig. 10(c) and (d), respectively. Based on Fig. 10(a) and (c), the simulated dV_{ds}/dt during the transient is closely matched with the experimental result at different temperatures. On the other hand, the turn-OFF transient with the developed model also shows dV_{ds}/dt that is close to the experimental result as shown in Fig. 10(b) and (d). However, the negative

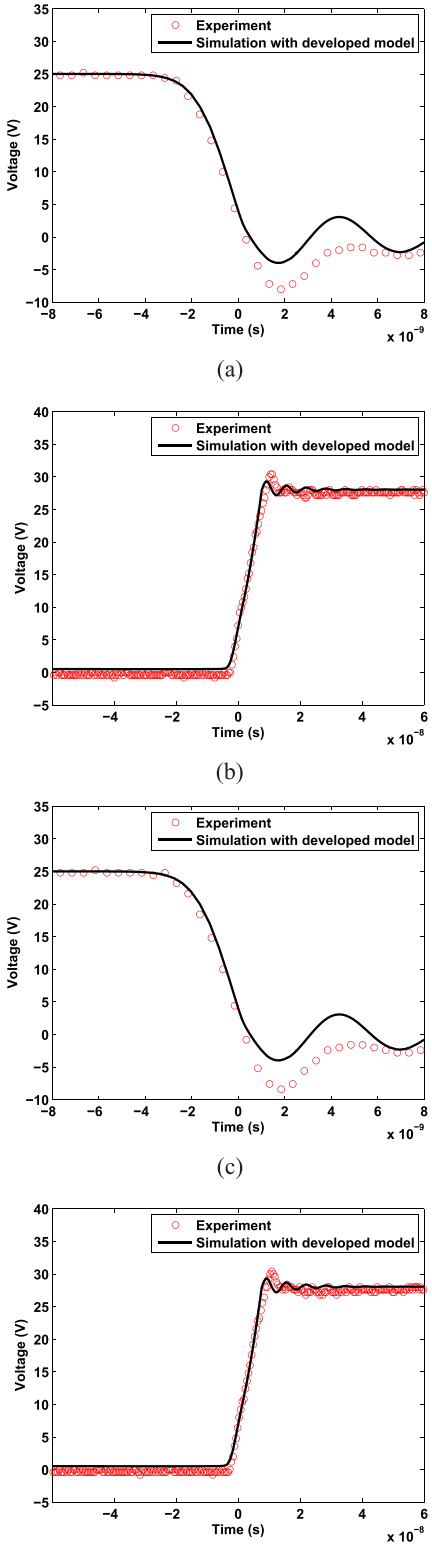


Fig. 12. Comparison of the experimental and simulation results of V_{ds} of the lower switch with parasitics in circuit considered at (a) and (b) 50 °C and (c) and (d) 70 °C during lower switch turn-ON and turn-OFF transients.

overshoot in V_{ds} present in the experimental result as shown in Fig. 10(a) and (c), as well as the positive voltage overshoot in Fig. 10(b) and (d), are not present in the simulation results. This is due to the circuit parasitics in the circuit [19], which are not included in this simulation.

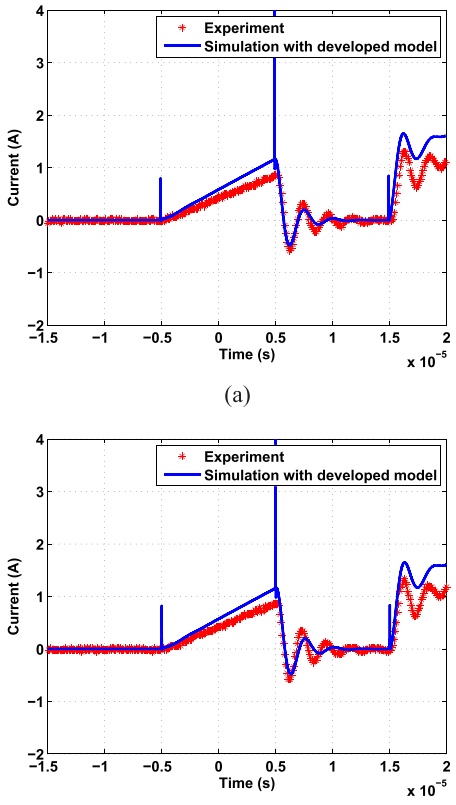


Fig. 13. Comparison of the experimental and simulation results of current through the lower switch with parasitics in circuit considered at (a) 50 °C and (b) 70 °C.

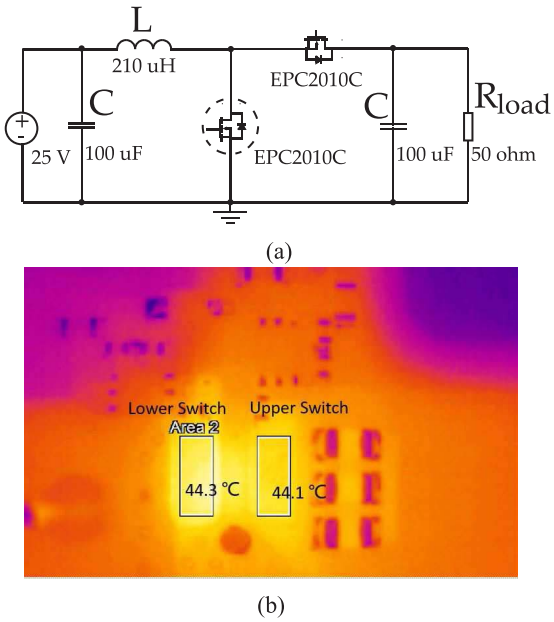


Fig. 14. (a) Boost converter setup. (b) Thermal image of the boost converter focusing on GaN FETs operating in steady state.

In order to include the parasitics in the circuit simulation, the circuit parasitics estimated based on [19] have been added into the simulation as shown in Fig. 11. With the parasitics considered, the switching transients can be simulated more accurately, as shown in Fig. 12. The current through the device, which is experimentally measured under 50 °C and 70 °C and

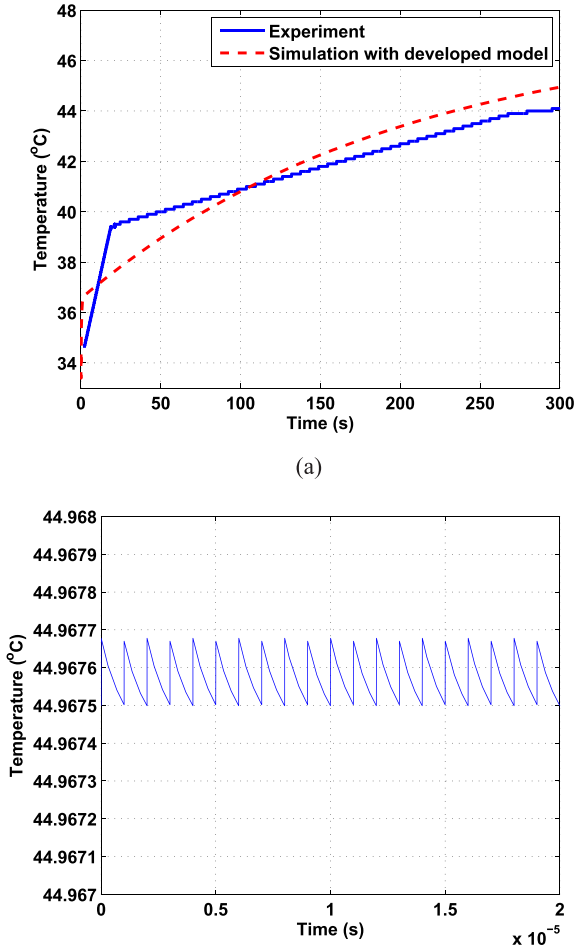


Fig. 15. Case temperature of the GaN FET based on (a) developed model in the LTSPICE and experimental measurement during 5 min of operation in the boost converter system and (b) PLECS steady-state analysis.

compared with its corresponding simulation result, is shown in Fig. 13(a) and (b). Based on comparison, dI/dt has been modeled very accurately and the simulated transients are very close to the experimental measurements. Current spikes can be observed in the simulation during the switching transients but are not present in the experimental measurement. This is mainly due to the limited resolution of current measurement devices that cannot follow the very fast transients of GaN devices.

B. Temperature Estimation Validation

To demonstrate the capability of the developed model in estimating the device temperature during circuit simulation and to compare the estimated result with experimental measurement, a boost converter system as shown in Fig. 14(a) is prototyped. The system runs for 5 min until the temperature settles down with the GaN FET operating at 500 kHz. The case temperature of the device is measured and recorded by an IR thermal imager as shown in Fig. 14. The measured data are then compared with the simulation result based on the developed electro-thermal model, as shown in Fig. 15(a). In addition, an electro-thermal model for EPC2010C is developed in the PLECS toolbox based on the device power losses at various temperatures obtained from LTSPICE simulation

using the method in [20]. The same system is simulated in the PLECS environment with its steady-state analysis tool, as shown in Fig. 15(b). Since the IR thermal imager measures the case temperature of the device, for a meaningful comparison, the case temperature estimations are obtained by subtracting the junction-case temperature drop calculated by the junction-case thermal network provided in [18] from the junction temperature estimation obtained directly from the simulations. The case temperature of the GaN FET (lower switch) increases from 34.3 °C to 44.3 °C during 5 min of operation, while the estimated final temperature, based on the developed and PLECS models, is 44.94 °C and 44.96 °C, respectively. As shown in Fig. 15, the final case temperature of device as well as the trend of temperature increases obtained from the developed model is very close to that from thermal measurement.

V. Conclusion

In this paper, a new behavioral electro-thermal model for the GaN FETs that considers the self-heating and thermal effects on the device characteristics is developed. The model, which is developed in the LTSPICE software environment, is validated under both the conduction and switching conditions and is compared against an available electrical model. To demonstrate the capability/accuracy of the developed model in estimating the junction temperature transients, simulation studies are conducted on a boost converter benchmark system. Experiments are also carried out to validate the developed model. The switching performance results from the proposed model is closely matched with the experimental results obtained from a DPT circuit at different temperatures. The case temperature estimation based on the developed model is also closely aligned with the thermal measurement of the GaN FET during its operation in a boost converter system and with the simulation results from PLECS. The developed electro-thermal model for GaN FET is capable of accurately modeling the temperature impacts on device characteristics as well as estimating the device temperature in the SPICE circuit simulations.

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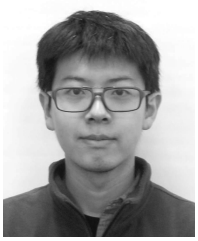

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A Simple Behavioral Electro-Thermal Model of GaN FETs for SPICE Circuit Simulation

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Sıcaklığa bağlı modelleme yapılmış, parasiticler konusunda eksik.

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Vgs için sıcaklık geri beslemesi kullanılmış

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Turn-off sırasında Vds ve Ids farklı sıcaklıklarda aynı değişimi gösterirken, Turn-on sırasında Vds vs Ids farklı sıcaklıklarda farklı değişimler gösteriyor.

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Fig.10'da parasiticler hesaba katılmamış, Fig.12'de parasiticler de hesaba katılmış.

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