Comprehensive Compact Electro-Thermal GaN HEMT Model

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***Abstract*—In this work we demonstrate a semi-empirical GaN HEMT model implemented in Verilog-A format. The model captures accurately the DC operation of test devices fabricated and measured at IMS CHIPS including the thermal effects. In addition, the off-state leakage current is physically modeled as a space-charge limited current prior to the onset of the physical breakdown. The dynamic current recovery of the transistor after stress bias is physically included by implementing the model in the form of a finite state machine, capturing the memory effect of the device. The drain current is modified to be a summation of multiple exponential terms, each corresponding to a given trapping center. This model can be used to predict the overall performance of the GaN HEMTs based on the epitaxial material composition or to infer the material composition and quality based on the measured device characteristics.**

Keywords—Compact modeling; GaN HEMT; Pulsed current; Off-state leakage current; Current recovery; Charge trapping

I. INTRODUCTION

Gallium Nitride (GaN) based electron devices have attracted a lot of attention for more than three decades as viable candidates for power electronics and high frequency applications [1]. Having a wide bandgap, high electron saturation velocity and high stability at elevated temperatures, GaN-based semiconductor devices, especially High Electron Mobility Transistors (HEMTs), proved to be alternatives to the traditional Silicon (Si)-based switches. Their superior intrinsic material properties allowed the GaN HEMT to possess higher breakdown voltage (> 1 kV), higher current density and much higher operational temperature as compared to the currently available commercial Si-based devices [2].

In order to utilize GaN based devices in any application, one has to be able to predict the performance of GaN HEMTs using device compact models, thus, enabling circuit and system level simulations and design. Unlike the well-established and standardized compact modeling process of Si-based devices, the development of compact models of GaN HEMTs is challenging due to the lack of a readily available material model. The unintentional incorporation of a wide span of species (dopants) during GaN epitaxy introduces several DC and dynamic effects which vary from supplier to supplier. In addition, commercially available GaN wafers are always grown on foreign substrates and, thus, feature a relatively high defect density (> 10^9 cm^{-2} for GaN/Si) which varies from supplier to supplier. Such defects are electrically active and influence both the DC and dynamic properties of the device, namely the leakage current and the dynamic on-resistance (current dispersion) [3].

Several attempts have been made in order to develop accurate GaN HEMT compact models as summarized in [4]. Among these is Angelov's model which has been modified to be used to model GaN HEMTs. This model is classified as an empirical equivalent circuit model. Given an accurate parameter extraction methodology, the Angelov model can accurately represents the GaN HEMT's electrical characteristics. However, accurate conclusions about the epitaxial material quality can be barely inferred. The Curtice3 model is also available for GaN HEMTs; it is also an empirical model. This model is neither an electro-thermal model nor geometry scalable. However, many models have been developed since then to account for its shortcomings like the CMC (Curtice/Modelithics/Cree), CFET and EEHEMT. Other models have been developed to account for self-heating effects in GaN HEMTs and the dynamics of the drain current. In [5] an empirical model is proposed, which is able to capture self-heating effects as well as charge trapping/de-trapping kinetics in GaN HEMTs. Hou, Bilbro and Trew [6] proposed a multi-region physical model where the conducting channel in the HEMT is divided into several regions. These multi-region models, however, did not account for the physical leakage current or the dynamics of charge trapping/de-trapping in the HEMT.

In this work, a semi-empirical compact model with emphasis on the physics of the off-state leakage current and the kinetics of charge trapping and de-trapping is developed. This model can serve as a platform for GaN HEMT developers (suppliers, foundries and designers) to directly infer the effect of the epitaxial layers quality and composition on the performance of the GaN HEMTs. The model is implemented in Verilog-A format and, thus, suitable for circuit simulations.

II. PROPOSED GAN HEMT COMPACT MODEL

A. Proposed model background

A HEMT structure is characterized by a Two-Dimensional Electron Gas (2DEG) channel at the hetero-interface between a barrier layer and a channel, which is a result of the charge balance between the polarization discontinuity at the interface and the counter charge at the surface (Fig. 1). The presence of unintentional n-type dopants such as Oxygen and Si hinders the high voltage operation of the devices. As such, a compensation-doped layer is typically grown in order to

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achieve the high resistivity needed for high voltage and low leakage current applications. This compensation is achieved by doping the layer with deep acceptors such as Iron (Fe) or Carbon (C). These deep acceptors together with the dislocations in the material act as trapping centers. During the device operation, particularly during the off-state stress bias, charge injection into surface or buffer traps causes a reduction in the channel density and, hence, a higher on-resistance. This coupling between the channel and the different trapping centers can be visualized as an RC circuit with a specific time constant as depicted in Fig. 1. These equivalent circuits can be unfolded into multiple circuits, each representing a certain species in the material. Specific for each of the species are the capture and emission time constants. These time constants are a function of the trap density of states, trap energy level and the capture cross-section. In this work, the model puts emphasis on capturing the dynamics imposed by this wide span of trapping centers in the material. The charge transport dynamics to and from the trapping centers are assumed to be negligible in comparison to the dynamics of trapping and de-trapping.

B. Proposed model structure

The proposed model consists of four main modules: (1) the DC core module, (2) the off-state high-voltage module, (3) the charge trapping and de-trapping kinetics module and (4) the thermal network module. The non-linear AC parameters module is not considered in this work.

Starting with the DC module, the threshold voltage can be physically expressed as:

$$V_{\mathrm{th}}(x) = \frac{1}{q}[\phi_{\mathrm{B}}(x) - \Delta E_{\mathrm{c}}(x)] - \frac{\sigma(x)}{C_{\mathrm{AlGaN}}(x)} \qquad (1)$$

where ϕ_{B} is the energy barrier height between the gate metal and the semiconductor, ΔE_{c} is the conduction band discontinuity between the AlGaN barrier and the GaN buffer, σ is the polarization discontinuity between the AlGaN and GaN, C_{AlGaN} is the effective barrier capacitance and finally x is the Aluminum (Al) composition in the barrier layer [7]. In case of a HEMT with an additional gate dielectric layer and considering the presence of dielectric charges, the threshold voltage is adjusted as:

$$V_{\mathrm{th,MIS}} = V_{\mathrm{th}} \cdot \left(1 + \frac{C_{\mathrm{AlGaN}}}{C_{\mathrm{dielectric}}}\right) - \frac{Q_{\mathrm{it}} + Q_{\mathrm{dielectric}}}{C_{\mathrm{dielectric}}} \qquad (2)$$

where $C_{\mathrm{dielectric}}$ is the capacitance of the gate dielectric and Q_{it} & $Q_{\mathrm{dielectric}}$ are the interface and dielectric charges respectively. The charge function, and hence the current equation, are adopted from the MIT Virtual Source Model (VSM) [8]. The drain current can be represented as:

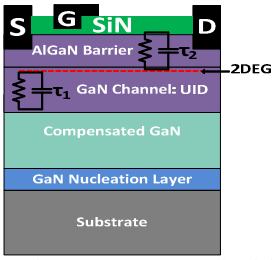

Fig. 1: Cross-section of a GaN HEMT epitaxial stack. The channel coupling to surface and buffer traps characterized by time constants τi.

$$I_{\mathrm{D}} = W \cdot Q \cdot v \qquad (3)$$

where W is the total device's width, Q is the channel density function defined by (4) and v is the electron velocity function defined by (5).

$$Q = C_{\mathrm{inv}} \cdot n \cdot \varphi_{\mathrm{t}} \cdot \ln\left(1 + exp\,\frac{V_{\mathrm{gs}} - V_{\mathrm{th}}}{n \cdot \varphi_{\mathrm{t}}}\right) \qquad (4)$$

$$v = F_s \cdot v_{\mathrm{SAT}} = \frac{{}^{V_{\mathrm{ds}}}/_{V_{\mathrm{ds,SAT}}}}{\left(1 + ({}^{V_{\mathrm{ds}}}/_{V_{\mathrm{ds,SAT}}})^{\beta}\right)^{1/\beta}} \cdot v_{\mathrm{SAT}} \qquad (5)$$

where n is the sub-threshold slope factor, φ_{t} is the thermal voltage, $V_{\mathrm{ds,SAT}} = \frac{L_{\mathrm{g}} \cdot v_{\mathrm{SAT}}}{\mu_{\mathrm{n}}}$ (L_{g} is the channel length and μ_{n} is the 2DEG electron mobility) is the drain voltage determining the onset of current saturation, v_{SAT} is the saturation velocity and β is a fitting parameter to determine the transition profile from linear to saturation regimes.

The second aspect, namely the off-state leakage current modeling, can be categorized into two partitions: 1) the forward and reverse physical breakdown of the gate-drain as well as the gate-source section modelled as Schottky diode and 2) the leakage current profile prior to the onset of physical breakdown.

In the forward direction (positive gate bias), the forward breakdown can be described by the Schottky diode equation as:

$$I_{\mathrm{gs,Forward}} = I_0 \cdot \exp\left(\frac{-\varphi_{\mathrm{B}}}{\eta \cdot \varphi_{\mathrm{t}}}\right) \cdot \left[\exp\left(\frac{V'_{\mathrm{gs}}}{\eta \cdot \varphi_{\mathrm{t}}}\right) - 1\right] \qquad (6)$$

where: $V'_{\mathrm{gs}} = V_{\mathrm{gs}} - V_{\mathrm{dielectric}} - V_{\mathrm{TO}}$ where $V_{\mathrm{dielectric}}$ is the forward voltage drop on the gate dielectric, V_{TO} is the turn-on voltage of the respective diode, I_0 is the pre-exponent diode current derived from the thermionic emission, φ_{B} is the energy barrier height collected experimentally and η is the diode ideality factor. The reverse break down can be calculated as:

$$I_{\mathrm{gs,Reverse}} = I_0 \cdot (1 + K_{\mathrm{bd,s}} \cdot exp\,\frac{V'_{\mathrm{sg}} - V_{\mathrm{bd,s}}}{\varphi_{\mathrm{bd}}}) \qquad (7)$$

where $V_{\mathrm{bd,s}}$ is the reverse breakdown voltage of the gate-source diode extracted from the device geometry design and $K_{\mathrm{bd,s}}$ & φ_{bd} are technology related fitting parameters accounting for the surface electric field distribution effects [9]. It is worth mentioning that the gate-drain diode equations have the same form as in (6) and (7) used for the gate-source diode.

Before the onset of the physical breakdown of the HEMT, the vertical leakage current is said to follow a Space-Charge Limited Current (SCLC) profile in the presence of trapping centers and background doping concentration. As will be shown in Section III, in the case of a SCLC the current starts with an ohmic profile at low applied voltages until a certain voltage where most of the background compensation acceptor dopants and/or trapping centers are filled with electrons from the background doping and/or from the injected electrons from the electrodes. At this voltage the ohmic trend develops to a quadratic dependence of the current on the applied voltage which is a characteristic of the SCLC [10]. This transition voltage can be calculated as:

$$V_{\mathrm{transition}} \approx \frac{q \cdot (N_{\mathrm{t}} - N_{\mathrm{D}})}{2 \cdot \varepsilon} \qquad (8)$$

where N_t is the effective density of free acceptor traps, N_D is the effective density of n-type donor dopants responsible for the background n-type carriers and ε is the dielectric constant of the material. However, in this work this transition voltage is calculated dynamically during the run time of the model as a function of the state of the device as will be shown in Section III. The SCLC equation is then approximated by [10]:

$$J_{\mathrm{SCLC}} \approx \frac{9}{8} \cdot \mu \cdot \varepsilon \cdot \theta \cdot \frac{V^2}{L^3} \cdot \exp\left[\frac{\left(\frac{q^3 \cdot V}{\pi \cdot \varepsilon \cdot L}\right)^{0.5}}{K \cdot T}\right] \quad (9)$$

where θ is the ratio between free electrons and trapped electrons, L is the length that has to be travelled with the charge carriers (in this case the thickness of the epitaxial layer) and T is the absolute temperature. The exponential term accounts for Poole-Frenkel (PF) emission and its importance is highlighted in Section III.

The last module is the dynamic charge trapping and de-trapping in the buffer layer which is also related to the SCLC discussed above. For each of the species that act as trapping centers, the trap signature has to be identified. This trap signature consists of the capture cross-section, the trap energy level and its degeneracy and the density of states of that trapping level. If known, one can calculate the capture and emission time constants, and accordingly, the dynamics of the HEMT. The stress-time dependent density of trapped charges, the specific capture time constant and the emission time constant are given as ([11]):

$$n_t(t) = \sigma_n \cdot v_{th} \cdot n \cdot \tau_{capture} \cdot N_t \cdot \ln\left[1 + \frac{t}{\tau_{capture}}\right] \quad (10)$$

$$\tau_{capture} = \frac{K \cdot T \cdot n_{T0}}{q \cdot \varphi_0 \cdot N_t \cdot \sigma_n \cdot v_{th} \cdot n} \quad (11)$$

$$\tau_{emission}^{-1} = A \cdot \sigma_n \cdot v_{th} \cdot N_c \cdot \exp\left[\frac{-q \cdot (E_t - \beta \cdot \sqrt{\xi})}{K \cdot T}\right] \quad (12)$$

where σ_n is the capture cross-section for electrons, v_{th} is the thermal velocity of electrons in the semiconductor, n is the background free carrier concentration, N_t is the total trap density with an energy level E_t, ξ is the applied electric field, $\beta = \sqrt{\frac{q^3}{\pi \cdot \varepsilon}}$, φ_0 is the initial energy barrier at the trapping site and A is a fitting parameter which is between 0.9 and 1 in this work. The equilibrium density of trapped charges is calculated as:

$$n_{T0} = \frac{N_t}{1 + \frac{1}{g} \exp\left[\frac{E_t + \beta \cdot \sqrt{\xi} - E_{FQ}}{K \cdot T}\right]} \quad (13)$$

with E_{FQ} as the quasi Fermi level for electrons in the presence of an applied external field and g as the degeneracy of the trapping level.

The time-dependent on-state drain current of the transistor is then modified as:

$$I_{ds}(t) = I_{ds,0} \cdot \left(1 - \sum_{i=1}^{J} \alpha_i \cdot e^{\frac{-t}{\tau_{emission,i}}}\right) \quad (15)$$

where $I_{ds,0}$ is the original drain current without charge trapping, J is the total number of trapping species in the material and α is the ratio between the density of trapped electrons to the total density of the conducting channel.

Finally, a one-pole thermal node is added to the model where the threshold voltage, electron mobility and saturation velocity are a function of the calculated device's temperature [12]. In addition, parasitic source and drain linear resistances are added to account for the metal-semiconductor contact resistances and the drain and source access regions.

C. Model implementation

The proposed model is implemented in Verilog-A format in the form of a Finite State Machine (FSM). The FSM concept is employed so that the memory of the device operation can be tracked. Fig. 2 depicts a simplified flow chart of the algorithm (not all states are included for simplicity).

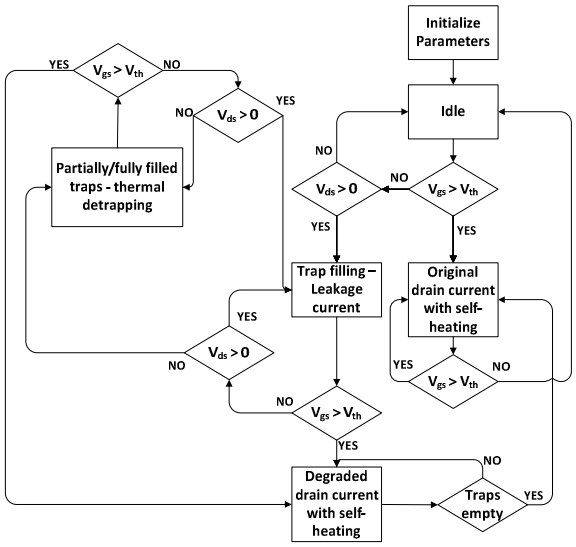

Fig. 2: Selected scenario of the FSM implementation of the model

If the device is biased in the on-state directly after initialization, the maximum device's current is generated (no charge trapping). If the device is initialized in the off-state at a finite drain bias, the charge trapping module is activated. Depending on the level of the off-state stress bias and the amount of time spent in this condition, the degraded on-state current dynamics are determined and used when the device state changes to on-state.

III. Measurement Results and Model Verification

In order to verify the model, three test cases are considered for the fabricated devices in this study: 1) The DC output characteristics including the device's self-heating, 2) the off-state leakage current as a function of the applied bias and 3) the dynamic current recovery after off-state stress bias. This dynamic measurement is carried out with a resolution of millisecond using two Keithley 24xx series synchronized together by using hardware trigger links. The composition of the material used is given by the material supplier to be: Oxygen = 1.5E16 cm^{-3}, Silicon = 3E16 cm^{-3} and Carbon 1E17 cm^{-3}. The corresponding trap signatures are acquired from [11].

Starting with the DC characteristics, Fig. 3a depicts the simulated and measured output characteristics of an AlGaN/GaN HEMT with 4 µm gate length and 100 µm gate width. The model captures the measured data with high accuracy in strong inversion. However, in the moderate and

weak inversion, the model deviates from the measured current. This could be corrected using a more accurate charge function.

The dynamic current recovery after stress biasing the HEMT in off-state is depicted in Fig. 3b where the voltage is pulsed with a period of 100 ms (with 50 % duty cycle) in which 100 measurements are conducted in order to capture the current recovery. The stress bias is applied at a drain voltage of 100 V at gate voltage of -5 V. In the on-state the drain voltage is set to 1 V and the gate is set to 0 V. The model is able to capture accurately the global trend of the drain current (blue line in Fig. 3b). However, there is a discrepancy between the measured and modeled data regarding the starting point of the current directly after the stress bias. This is due to the fact that the trapping centers included in the model are only those typically reported by the wafer supplier, disregarding those originating from process variations or threading dislocations. This fitting can be improved once all the species are known. Alternatively, the model can be used to infer the composition and quality of the material based on the measured data.

The final aspect to be verified, namely the off-state three terminal leakage current, is then measured and the results are compared to the model in Fig. 4a. Depending on the state of occupancy of the traps, which is dynamically calculated in the model, the leakage current is selected to either follow a SCLC or a conventional linear behavior of a lightly doped semiconductor. In Fig. 4b, the device is stressed in off-state for 1 hr and then the leakage current is measured again. In this case, the trapping sites are filled from the beginning of the stress (charge de-trapping time constant > measurement time) and thus, a SCLC behavior is seen across the entire voltage range. In addition, the SCLC model including the PF emission is compared with that without the PF emission. From this comparison it is obvious that the model without the PF effect

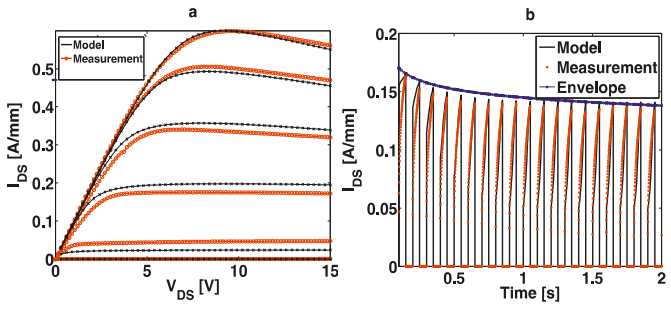

Fig. 3: (a) Measured vs. simulated DC output characteristics of the HEMT (V_{gs} = 0 V : -5 V), (b) measured vs. simulated pulsed I_{ds} after stress-bias

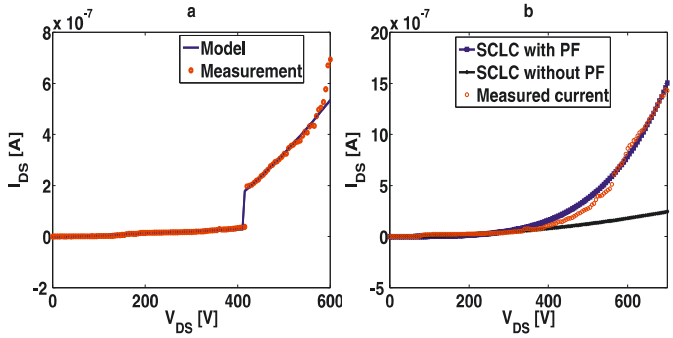

Fig. 4: Off-state 3-terminal leakage current of (a) fresh device and (b) 1 hr. stressed device with and without PF emission

underestimates the current at higher drain biases since electron emission from trapping sites is not included.

IV. Conclusions

In this work a comprehensive GaN HEMT semi-empirical Verilog-A model with a focus on the off-state leakage current and the kinetics of charge trapping and de-trapping is presented and experimentally verified. The model is able to capture the DC characteristics, the off-state leakage characteristics as well as the dynamic current recovery of the fabricated GaN HEMTs. As such, the model directly relates to the structure and properties of the GaN epitaxial layers and the carrier substrate. The model can, therefore, be used to fit the measured data in order to deduce information about the species incorporated during the growth based on the dynamics extracted by the model.

V. References

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01 Furkan Karakaya Page 1

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02 Furkan Karakaya Page 2

3/11/2017 6:35

03 Furkan Karakaya Page 2

3/11/2017 6:35