"Investigation of Dynamic Performance and Switching Loss Accuracy of Enhancement-Mode GaN Power Transistor Computer Models"

ABSTRACT
In this paper, voltage and current transients and resulting switching loss accuracy of three different computer models for 650V enhancement- mode GaN power FETs are investigated. Importance of parasitics on the dynamic performance of GaN transistors are discussed and their effects on turn-on & turn-off switching losses and transients are presented.

INTRODUCTION

In each day, technology is developed more and new products begin to take older product's place rapidly. This development is also seen in semiconductor market where the new wide band-gap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) semiconductors are spreading. Even though, the GaN devices in the market are limited in the meaning of current (<60A) and voltage (<650V) ratings, they are very attractive with their fast switching capability, low on-state resistance ($R_{ds\text{-}on}$), high breakdown barrier and high electron mobility. Since GaN devices can be produced with smaller sizes, their parasitic components are much smaller than Si based semiconductors that enables faster switching speeds [1].

Although the faster switching speed makes switching losses lower, it also requires special attention to model the dynamic behavior of the devices. Firstly, due to the fast switching capability, the GaN device has the risk of false turn-on; therefore, a negative gate-source voltage needs to be applied [2]. Behind this, computer models has to be created considering fast switching characteristic and there are several models proposed in the literature, which are focusing on the static and dynamic behaviors simultaneously [3], [4]. Moreover, the manufacturers also provide different models, which includes different parasitic and temperature-dependent components [5]. Furthermore, the detailed turn-on loss analysis is required to model turn-on loss, which is significantly greater than turn-off loss [6]. However, the single effect of the each parasitic component on the dynamic behavior, which affects switching losses and the turn-off characteristics that is specific to GaN devices is not described in detail. Consequently, in this paper, different models are proposed to investigate the effect of each parasitic components on the dynamic behavior. In addition, the resulting switching loss accuracy of each model is discussed and the turn-off characteristics of GaN is explained.

GaN MODELLING AND TEST CIRCUIT

A model for a transistor includes two behavioral aspects that are static and dynamic actions. In this study, the static behavior of the GaN power FET is modeled with a voltage-dependent current source, which is the channel of the device, and temperature dependent resistances. The equations for voltage-dependent channel current are provided in (1) and (2). Those equations imply that there is an exponential relation between channel current and gate-source voltage. On the other hand, those equations show that an ohmic region occurs for low drain-source voltages where channel current changes with a constant ratio, $R_{ds\text{-}on}$, as given in Fig. 2(a). The constant channel resistance, $R_{ds\text{-}on}$, is important for conduction loss. Conversely, when the drain-source voltage is high, the GaN power FET operates in saturation region, so the channel current is constant. In order to improve the static model so that the dynamic behavior is included, it is required to add parasitic capacitances and inductances also. The resulting model of GaN power FET is shown in Fig. 1(a). Note that, the parasitic capacitances are voltage-dependent and importance of the modelling the voltage-dependent capacitances on the switching transients is discussed in Section III. Furthermore, the static characteristic of GaN power FET model at 25 ^{o}C is given in Fig. 2. Comparing to manufacturer provided results, it is seen that the static behavior of the model is accurate.

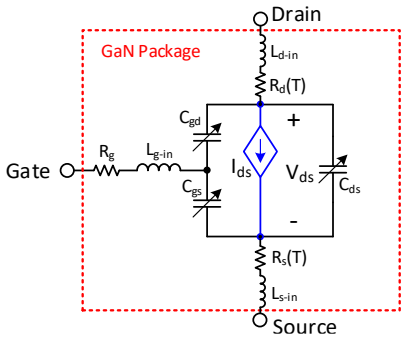


Fig.1 (a) Proposed hybrid model of e-mode GaN power FET

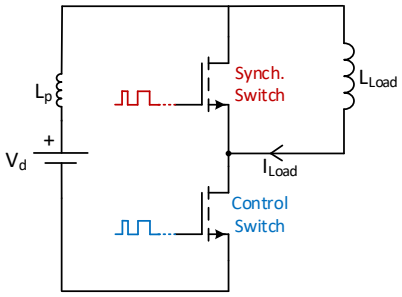
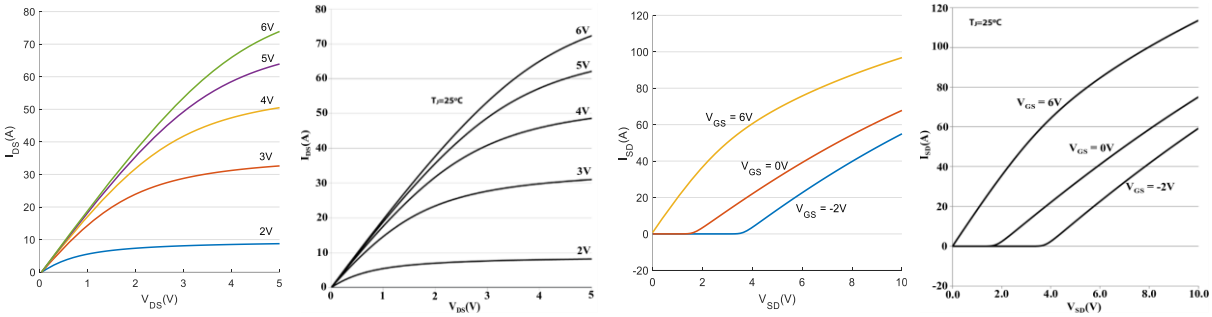


Fig. 1(b) The DPT circuit used for the analysis

$$I_{ds} = K_1 * \ ln\left[1 + e^{\left(\frac{V_{gs}-V_{th}}{K_2}\right)}\right] * \frac{V_{ds}}{1 \ + \max\left(K_4 + K_5 * \left(V_{gs} + K_6\right), K_7\right) * V_{ds}}, K_i \ are \ constant \quad (1)$$

$$I_{ds} = -K_1 * ln\left[1 + e^{\left(\frac{V_{gd}-V_{th}}{K_8}\right)}\right] * \frac{V_{sd}}{1 \ + \max\left(K_4 + K_5 * \left(V_{gd} + K_9\right), K_7\right) * V_{sd}}, K_i \ are \ constant \quad (2)$$

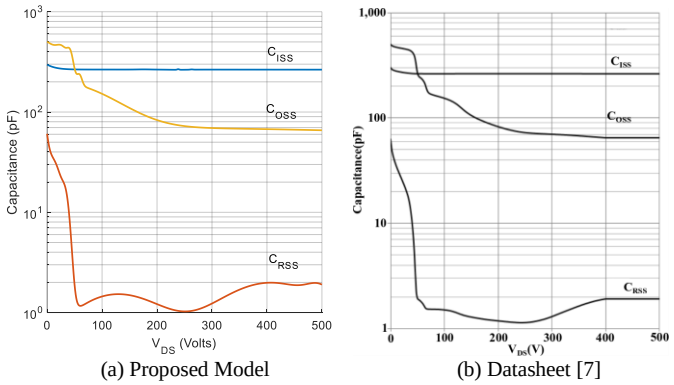


(a) Forward conduction (model) (b) Forward conduction [7] (c) Reverse conduction (model) (d) Reverse conduction [7]

Fig.2. Steady-state characteristics of GS66508B obtained by the proposed model and the actual characteristics

Secondly, the voltage-dependent parasitic capacitances are modeled using curve fitting obtained from datasheet, [7], and [2]. The resultant curves are given in Fig. 3 and Fig. 4. The manufacturer provides the curve for parasitic capacitances with respect to the drain-source voltage and it is seen that C_{ISS} is constant. However, the C_{ISS} changes significantly with varying gate-source voltage and the model should be constructed by identifying the gate charge. Therefore, in this paper, in order to model the dynamic behavior accurately, C_{ISS}-V_{GS} curve is obtained from the reference graph given in [2].

Moreover, the resultant MATLAB/Simulink GaN power FET model is used on Double-Pulse-Test (DPT) circuit, Fig. 1(b), to analyze transient performance of the device. DPT circuit is selected to have the same test circuit with the manufacturer. The nominal values of this test circuit, which are obtained from manufacturer model and test setup, are listed in Table 1.



(a) Proposed Model (b) Datasheet [7]

Fig.3. Variation of the parasitic capacitances with respect to V_{DS}

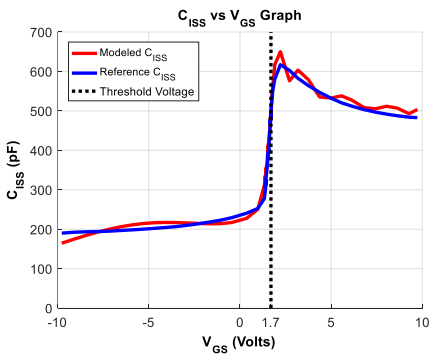


Fig. 4. Variation of C_{ISS} with respect to V_{GS} [2]

Table 1. The parameters used for the test circuit in MATLAB/Simulink [7], [8]

Input voltage (V_d)	400 V	Gate loop inductance ($L_{g\text{-}ex}$)	3.0 nH	Dead-time (t_{dead})	10 ns
Load Inductance (L_{LOAD})	480 µH	Internal gate resistance (R_g)	1.5 Ω	Gate parasitic inductance ($L_{g\text{-}in}$)	0.65 nH
Applied gate voltage (V_{gs})	-3V/+6V	Turn-on gate resistance ($R_{G\text{-}ON}$)	10 Ω	Drain parasitic inductance($L_{d\text{-}in}$)	0.062 nH
Power loop inductance(L_p)	3.0 nH	Turn-off gate resistance ($R_{G\text{-}OFF}$)	2 Ω	Source parasitic inductance($L_{s\text{-}in}$)	0.45 nH

DYNAMIC PERFORMANCE AND LOSS ACCURACY OF THE MODELS

The loss analysis is conducted on three different model types, Fig. 5, to see the magnitude of the effect of the parasitics on the results. In the first model, the parasitic capacitances are kept constant at datasheet nominal values and the internal parasitic inductances of the GaN power FETs are excluded from model. In the second model, the parasitic capacitances are variable but the inductances are excluded again. In the third model, the parasitic capacitances are variable and the internal parasitic inductances are included. Note that, the static characteristics of both models are the same and gives accurate results as expected.

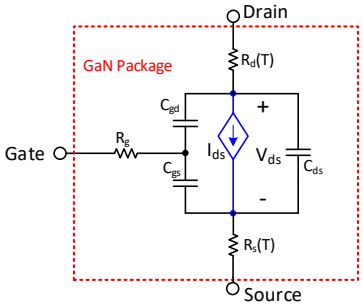


Fig.5 (a) Model I

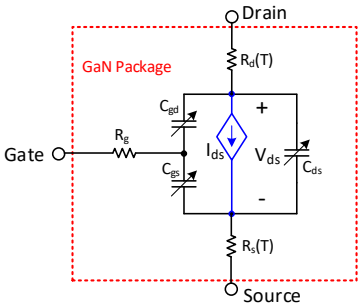


Fig.5 (b) Model II

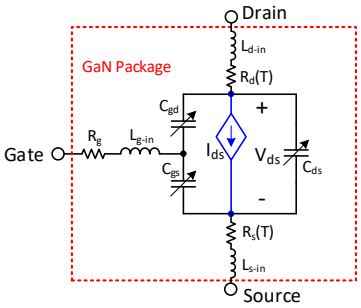


Fig.5 (c) Model III

For each model, turn-on and turn-off losses of the control switch are obtained from simulation results for different load current ratings and they are given in Fig.6 (a) & Fig.6 (b). To calculate switching loss in simulations, the instantaneous power is calculated by multiplying the voltage and current instantaneous values and it is integrated over the switching period. Then, the total switching losses of the models are compared with the experimental results, which are provided by manufacturer [8], as shown in Fig.6(c). The comparison tells that treating the capacitances as constant results in inaccurate dynamic behavior. On the other hand, switching energy losses of the Model 2 and the Model 3 are closer to each other and experimental results. As a result, having the parasitic inductances in model has a minor effect in comparison with the variable parasitic capacitances because inductances affect the transient times slightly whereas the variable capacitances change the durations significantly. Therefore, for a model to have an accurate dynamic characteristic the capacitances should be modeled correctly.

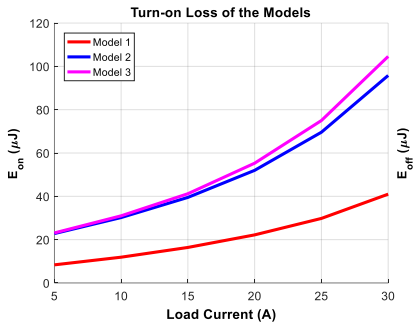


Fig.6 (a) Turn-On Losses

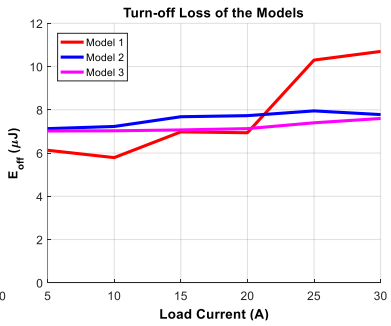


Fig.6 (b) Turn-Off Losses

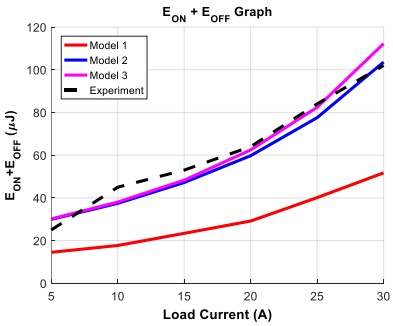


Fig.6 (c) Total Switching Loss

Moreover, it can be deduced from the Fig. 6(c), Model 3 gives the most accurate results. Now, to visualize the switching waveforms of the control switch, the turn-on and turn-off waveforms of the Model 3 are given in Fig.7 (a) & Fig.7 (b) where the load current is 30 Amperes. At the starting moment of the turn-on switching period, a dip is seen on the drain-source voltage waveform. That dip is caused because of the immediate change in power loop current; in other words, since the $\partial I/\partial t$ ratio is high, there occurs a voltage drop on the loop inductance. In addition, it is seen that, the drain-source current makes an overshoot when the switch turns-on. This happens because the C_{OSS} of the synch. switch is

being discharged and since its gate-source voltage is set to -3V, its channel cannot conduct the current. Thus, an overshoot occurs on the channel current of the control switch to discharge C_{OSS} of the synch. switch. The amount of overshoot depends on the input voltage and switching speed.

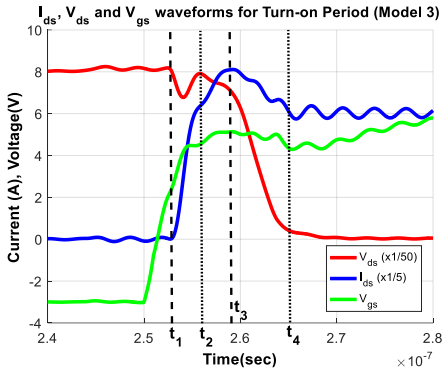


Fig.7 (a) Turn-On Waveforms

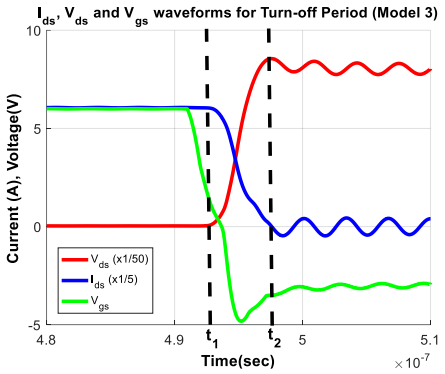


Fig.7 (b) Turn-Off Waveforms

Further, an interesting switching waveform is observed during the turn-off period of the Control switch; that is, the drain-source current and the drain-source voltage change simultaneously as seen in the Fig. 7(b), so it is inaccurate to use commonly preferred switching waveform which says the voltage rises first and then current falls to zero. This phenomenon occurs only in GaN power FETs because compared to silicon-based transistors, they have no body diode and they conduct current reversely through their channel. When the current of the Control switch starts to fall (under constant load current), the remaining amount of current has to flow through the synch. switch reversely. However, a problem arises over the reverse conduction of the synch. switch. The problem is that a GaN power FET cannot conduct current reversely through its channel, when the drain-source voltage is positive. As seen on Fig. 7(b), even though the current decreased in the duration t_1-t_2, the drain-source voltage of the control switch could not rise up to the input voltage that means the drain-source voltage of the synch. switch is still positive but it has to conduct reversely. Therefore, the parasitic capacitances play a significant role in this condition; that is, when the drain-source current of the control switch starts decreasing, the reverse current does not flow through the channel of synch. switch but it flows through the parasitic capacitances of synch. switch so that the parasitic capacitances can be discharged. The discharging continues until the drain-source voltage of synch. switch becomes negative. When the drain-source voltage has a negative value, the channel of the synch. switch starts conducting reversely. Because of this phenomenon, the drain-source current and voltages of the control switch change simultaneously during turn-off period, so the current fall time is definitely equal to the voltage rise time during this period. Because of this fact, the turn-on loss is significantly higher than the turn-off loss.

The voltage and current transient times are given in Fig. 8 for each model. For the turn-on period, the t_1-t_3 period is called as current rise time (t_{cr}) and the t_2-t_4 period is called as voltage fall time (t_{vf}). Similarly, for the turn-off period, the t_1-t_2 period is called as current fall time (t_{cf}) and voltage rise time (t_{vr}). As explained above, current fall time is strictly equal to voltage rise time.

Similar to turn-on and turn-off loss results, for the current and voltage transient durations, the Model 1 behaves quite differently as shown in Fig.8 and the results obtained from simulation of the Model 1 are not correct. However, it is observed that there is a similarity between the Model 2 and the Model 3 that verifies the deduction made before, which is the impact of the variable parasitic capacitances is higher than the impact of the parasitic inductances on the dynamic characteristic of GaN power FET.

As observed in turn-off switching waveforms, again, the trend of the current fall time (or voltage rise time) graph is different. Even though the voltage fall time and current rise time increase with increasing load current, the voltage rise time decreases. Actually, it is a result of the same phenomenon. As explained above, for the synch. switch to conduct reversely, the parasitic capacitances should be

discharged and these capacitances are discharged with load current, which flows through them in reverse direction. Thus, higher load current means faster discharging, so the voltage rise time decreases with the increasing load current. In addition, as observed in Fig. 6(a) & 6(b), even though the turn-on loss increases significantly with increasing load current, the turn-off loss does not change much, which is because of the decreasing voltage rise time (or current fall time) with increasing load current. As seen in Fig. 6(b), the load current affects the amount of turn-off loss 1µJ as maximum. This change is very low considering the total switching loss, so it can be said that the load current does not change turn-off loss significantly for the same input voltage.

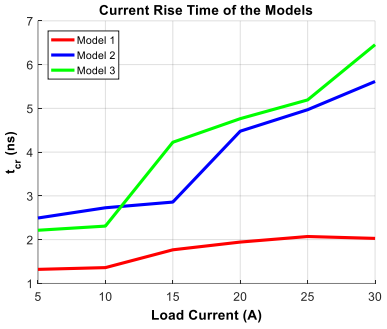


Fig.8 (a) Current Rise Time

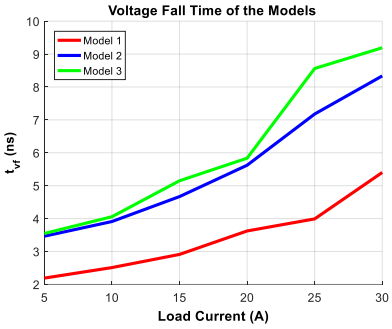


Fig.8 (b) Voltage Fall Time

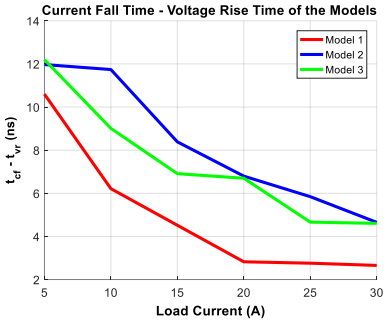


Fig.8 (c) Current Fall /Voltage Rise Time

CONCLUSIONS and FUTURE WORK

In this paper, the dynamic behaviors and loss accuracy of three different e-mode GaN power FET models are presented and discussed. Impacts of the parasitics on the dynamic behavior are compared and the significance of voltage-dependent parasitic capacitance modelling is emphasized. It is showed that using the nominal capacitance values provided in datasheet gives incorrect results. Moreover, it is shown that GaN power FET has a turn-off mechanism, which is definitely different from silicon-based transistors. The turn-off loss is independent of varying load current under same input voltage because the transient period get shorter with increasing load current.

In the final paper, the simulation results will be supported by the instantaneous power dissipation results and they will be compared with the experimental results. In experimental results, GS66508B-EVBDB daughter board will be used. It is aimed to express better the effect of the different parameters on dynamic behavior in the finalized paper.

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