Characterization of an Enhancement-Mode 650-V GaN HFET

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***Abstract*— GaN heterojunction field-effect transistors (HFETs) in the 600-V class are relatively new in commercial power electronics. The GaN Systems GS66508 is the first commercially available 650-V enhancement-mode device. Static and dynamic testing has been performed across the full current, voltage, and temperature range to enable GaN-based converter design using this new device. A curve tracer was used to measure $R_{ds\text{-}on}$ across the full operating temperature range, as well as the self-commutated reverse conduction (i.e. diode-like) behavior. Other static parameters such as transconductance and gate current were also measured. A double pulse test setup was constructed and used to measure switching loss and time at the fastest achievable switching speed, and the subsequent over-voltages due to the fast switching were characterized. Based on these results and analysis, an accurate loss model has been developed for the GS66508 to allow for GaN-based converter design and comparison with other commercially available devices in the 600-V class.**

Keywords—GaN; Gallium Nitride; wide bandgap; double pulse test; device characterization

I. Introduction

Wide bandgap (WBG) semiconductors such as Gallium Nitride (GaN) are a game-changing technology for power electronics, enabling high-voltage and high-frequency converters with improved efficiency, smaller size, and lower cost. GaN wafer fabrication technology is still a major challenge for vertical GaN devices, but lateral GaN-on-Si devices are a promising alternative. Lateral heterojunction field-effect transistors (HFETs), also known as high electron mobility transistors (HEMTs), take advantage of the dense layer of electrons formed at the heterojunction between GaN and AlGaN. This "two-dimensional electron gas" (2DEG) acts as a normally-on low-resistance current path between the drain and source, meaning that the HFET is inherently a depletion-mode device [1,2].

Cascode GaN devices are a convenient way to produce a normally-off device, but they have reliability and switching performance limitations. Alternatively, an enhancement-mode GaN device can be directly fabricated with several different gate structures. The e-mode gate can be insulated with a dielectric, or it can be non-insulated to produce a diode-like gate characteristic with a DC gate current [1].

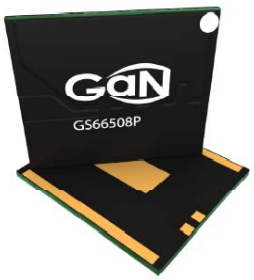

Fig. 1. GaN Systems GS66508.

At 650 V and 30 A, the GaN Systems GS66508 (shown in Fig. 1) is the highest-rated GaN HFET commercially available. However, the full datasheet has not yet been made available with static performance curves or switching loss data [3]. Performance characterization has been published about other commercial and near-commercial GaN devices, such as Transphorm, EPC, Panasonic, IR, and HRL [4]-[8]. The goal of this paper is to provide a full range of performance data, for loss estimation in an enhancement-mode GaN-based converter with GS66508P-E04 devices.

II. Static Testing

A. Test Setup

Static performance was tested using the Tektronix 371b curve tracer. The surface-mount device was soldered on a PCB and connected to the curve tracer with a four-wire Kelvin connection, and the results were compensated for the 3.7 mΩ wires soldered directly to the pads of the device. The device was heated by a digitally controlled custom Wenesco hot plate, connected through the board with thermal vias, an aluminum block, and thermal grease. Junction temperature was verified with a temperature transducer soldered beside the device on the same copper plane. The curve tracer provides a controllable gate driving voltage and a variable load for I_d and V_{ds}, producing I-V curves at a chosen gate voltage.

A 1 kΩ resistor was connected in series with the gate and its voltage drop was measured with a precision multimeter to determine DC gate current. The driving voltage was increased to compensate for the voltage drop across resistor, so the given gate-source voltage in the following figures is the actual voltage on the device terminals, and not simply the driving voltage from the curve tracer.

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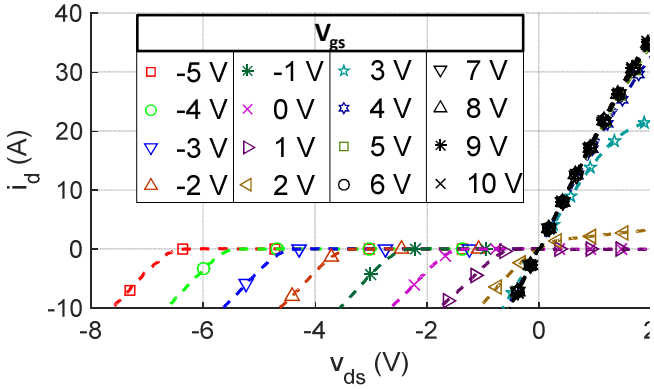

Fig. 2. Output characteristic at T_j = 25 ºC.

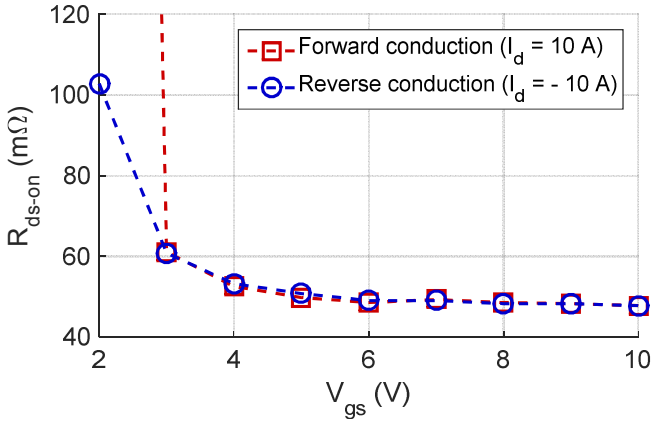

Fig. 3. On-resistance at T_j = 25 ºC, over increasing gate voltage.

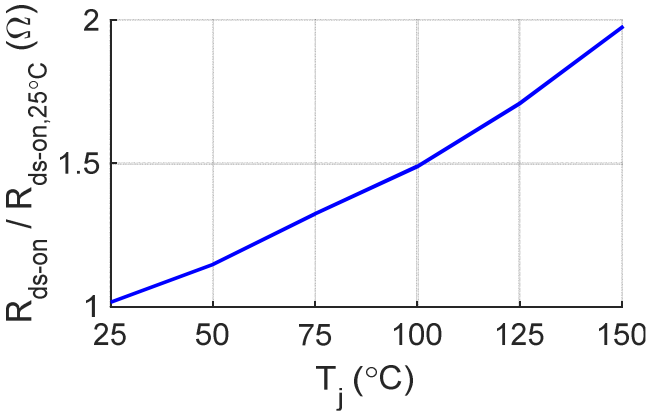

Fig. 4. On-resistance over increasing junction temperature.

B. Output Characteristic

Fig. 2 shows the first and third quadrant output characteristic of the device at room temperature, including the on-state operation with the gate voltage above the threshold and the so-called "self-commutated reverse conduction" (SCRC) operation that behaves similar to a body diode. It is noteworthy that in enhancement-mode GaN HFETs, the slope of the SCRC I-V curve is still approximately R_{ds-on} at any given gate voltage and temperature, but the V_{ds} offset scales linearly as V_{gs} drops below the reverse threshold voltage (~1.4 V). This

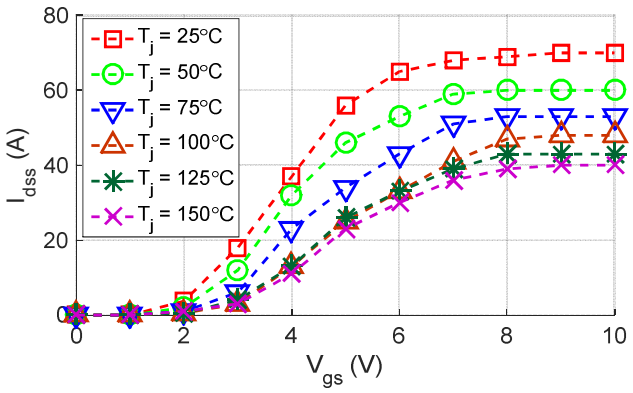

Fig. 5. Transfer characteristic over increasing junction temperature.

is because SCRC is not truly diode behavior. Rather, as the name suggests, the device turns on its own channel when the output voltage V_{ds} biases the gate-drain voltage V_{gd} sufficiently high to turn on the device in the reverse direction. As such, there is also no reverse recovery involved in SCRC.

Output characteristics were also recorded with junction temperatures up to 150 ºC. The on-resistance was then calculated with a load current of 10 A in both forward and reverse conduction. As expected, the forward-conduction and reverse-conduction values of R_{ds-on} were equivalent, and this resistance drops slightly as the gate voltage increases. However, the reduction in on-resistance is not very significant above 5 V. The results are shown in Fig. 3.

As the junction temperature increases, on-resistance increases linearly with temperature, and nearly doubles at the maximum operating temperature of 150 ºC as shown in Fig. 4

The published R_{ds-on} from the manufacturer is actually higher than the results shown here. This may be intended to account for some dynamic R_{ds-on} due to the current collapse phenomenon. However, dynamic R_{ds-on} is very difficult to measure accurately, and a special test fixture must be designed for this purpose. The characterization of dynamic R_{ds-on} will be performed as part of a separate work.

C. Transfer Characteristic

The transfer characteristic was also recorded with V_{ds} = 5 V to capture the saturation current I_{dss}, transconductance g_{fs}, and threshold voltage $V_{gs,th}$. The results are shown in Fig. 5. One notable feature of this GaN HFET is that its transconductance drops significantly as the junction temperature increases. In contrast, Si and SiC devices do not typically experience much change in transconductance with elevated temperature. This characteristic is typical for e-mode GaN devices, and have consequences for switching loss that will be explained in the next section.

D. Gate Current

Although the manufacturer has not published any literature as to whether to the gate is insulate or non-insulated, a DC gate current was observed at the mA scale within the rated gate voltage range, shown in Fig. 6. This is similar to the diode-like

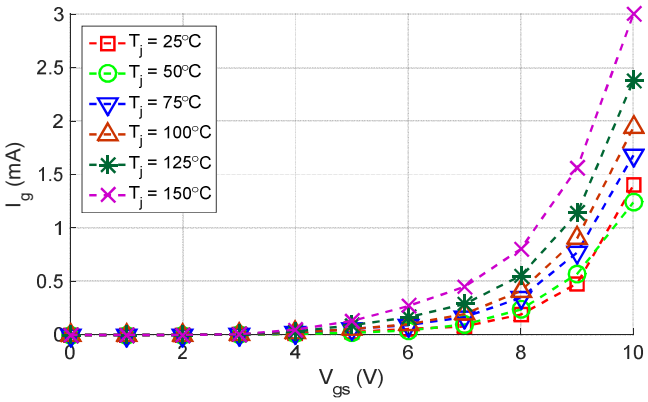

Fig. 6. DC gate current over increasing gate voltage and junction temperature.

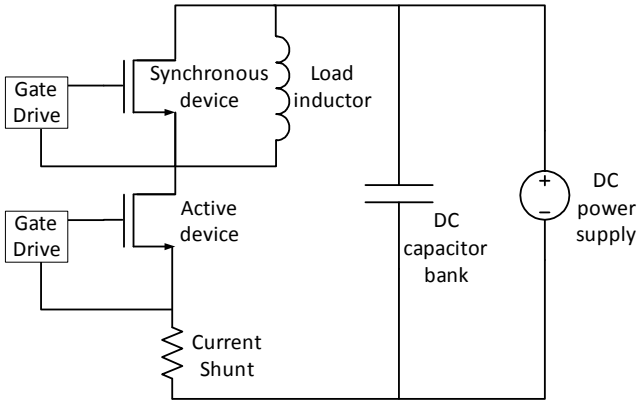

Fig. 7. Double pulse test circuit schematic.

gate behavior of the Panasonic and EPC devices with non-insulated gate structures. The data sheet specifies 40 µA gate leakage current at room temperature and the recommended driving voltage of 7 V, but at higher junction temperature, this gate leakage current increases by an order of magnitude, and also increases significantly with increased driving voltage above 7 V. This does not indicate a problem with the device, but should be considered in gate driver IC selection and converter design. No significant rise in device temperature was observed as an effect of this gate current, so this should not be a critical design parameter in thermal design.

III. Dynamic Testing

A. Double Pulse Test Setup

The dynamic switching performance was characterized with a double pulse test (DPT) board, using the circuit shown in Fig. 7 and test setup shown in Fig. 8. Typical DPT methodology was followed as described by [9]. The PWM input to the gate driver was provided by an Agilent 33522A function generator, and the current and voltage waveforms were recorded with a Tektronix MSO4104B-L oscilloscope using a sample size of 0.4 ns. Gate voltage was measured with a TPP1000 low-voltage passive probe, with a bandwidth of 1 GHz. Drain-source voltage was measured with a TPP0850 high-voltage single-ended probe, with a bandwidth of 800 MHz. The drain current was measured with a 100 mΩ coaxial shunt from T&M Research, with a bandwidth of 2 GHz. The coaxial shunts were modified to reduce parasitic inductance by trimming the plastic around the base, so that the connecting nuts could clamp around the PCB with no need for metal standoffs or additional nuts. Both devices were heated in the same method as in the static test setup, with a temperature transducer used to verify junction temperature. A 2.1-mH inductor was used as the load.

The drain-source voltage and drain current were aligned in the oscilloscope to within 0.1 ns, by adjusting the current channel deskew until the initial drop in v_{ds} was graphically aligned to the calculated voltage drop across the parasitic load inductance L_{ds} on the oscilloscope during the turn-on transient. This method is most effective at high load current when the displacement *dv/dt* transient is delayed, so the alignment was initially performed with 37 A, then verified at other operating

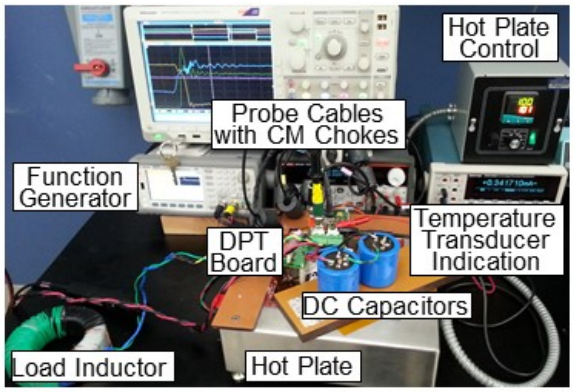

Fig. 8. Double pulse test setup.

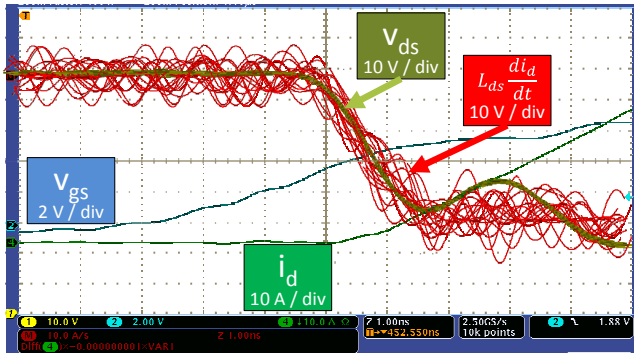

Fig. 9. I-V alignment waveforms, used to verify current channel deskew.

conditions to check for consistency. Fig. 9 shows twenty of these alignment waveforms overlaid to verify proper alignment.

For each test condition (DC bus voltage, load current, and junction temperature), five points were recorded for turn-on and turn-off. Data was then processed in MATLAB to construct time-base waveforms, and to calculate turn-on and turn-off energy and times as well as other relevant parameters. A low-amplitude, low-frequency oscillation was observed in the current

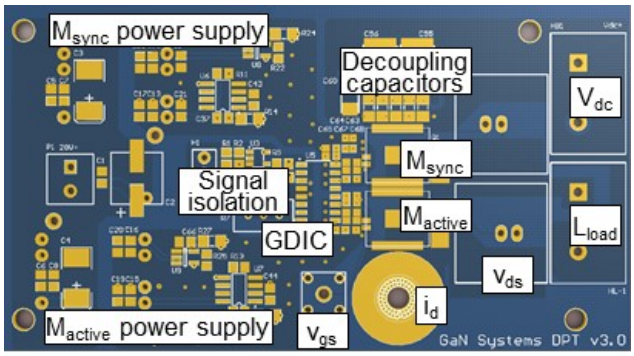

Fig. 10. DPT board layout.

B. DPT Board Design

The double pulse test board was designed very densely to minimize gate loop and power loop inductance, as recommended by [10] and conventional DPT methodology for WBG devices. Decoupling capacitors for both the gate loop and power loop were placed very close to the device so that the fastest switching speed could be achieved, and a four-layer board was used with large copper planes used to minimize power loop inductance. Fig. 10 shows the DPT board layout used in this work.

Both the active (lower) and synchronous (upper) devices were driven by the Si8233 high-side/low-side gate driver IC, each with a single gate resistor to control the switching speed. The resistance was reduced to 0 Ω with 8 V / 0 V driving voltages for optimal switching speed and loss. Initially, different gate voltages and resistances were explored. However, the best switching performance was achieved with this configuration, without violating the device ratings. Shoot-through was observed in all cases during turn-on of the active/lower device, caused by cross-talk. Since cross-talk is only a concern for some topologies, this phenomenon was ignored for now and will be studied further as a separate work. In a practical converter design, a gate driver is required for both switches, but for this work the gate and source pads of the upper/synchronous device were shorted together with solder to minimize gate loop inductance and subsequent cross-talk. Ref. [11]-[12] describe the cross-talk mechanism in wide bandgap devices and methods for cross-talk mitigation.

The Si8233 includes RF-based digital isolation specified at 45 V/ns common-mode transient immunity (CMTI), and isolated power supplies were used for the upper and lower devices. Additionally, small capacitors were added at the digital input of the gate driver IC to prevent false firing caused by EMI and inductive coupling on the board during turn-on transients.

C. Switching Transient Waveforms

Figs. 11 and 12 show the processed turn-on and turn-off waveforms respectively, recorded at 25 ºC with 400 V DC bus voltage and 10 A load current. The variables shown in the figures are defined as follows:

- t_1: v_{gs} has risen to 10% of the driving voltage

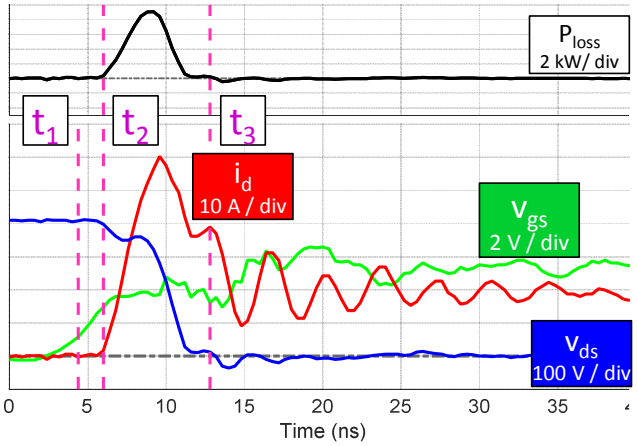

Fig. 11. Turn-on waveform at 400 V, 10 A, 25 ºC.

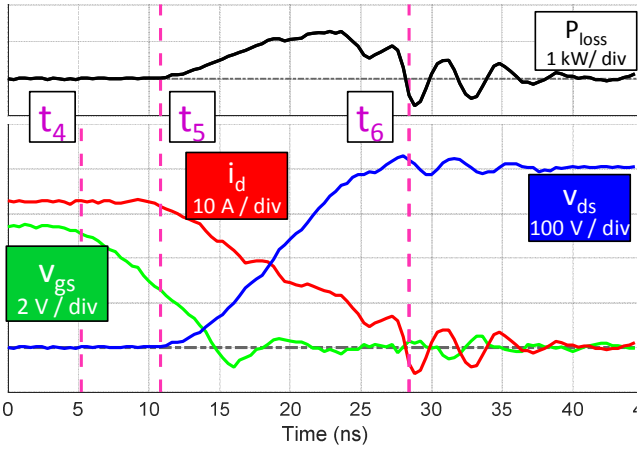

Fig. 12. Turn-off waveform at 400 V, 10 A, 25 ºC.

- t_2: i_d has risen to 1% of the load current
- t_3: v_{ds} has dropped to 99% of the DC bus voltage
- t_4: v_{gs} has dropped to 90% of the driving voltage
- t_5: v_{ds} has risen to 1% of the DC bus voltage
- t_6: i_d has dropped to 1% of the load current

The DC bias of v_{ds} was adjusted to $I_L R_{ds\text{-}on}$ based on the average during the on-state just after t_3 and before t_4, using the temperature-dependent values for $R_{ds\text{-}on}$ measured during static testing. Likewise, the DC bias of i_d was adjusted to 0 A based on the average during the off-state just after t_6 and before t_1.

The current overshoot between t_2 and t_3 is due to the displacement current that charges the upper/synchronous device output capacitor as it turns off. During this same time, the active device discharges its output capacitor through its own channel and causes further loss, but this current is internal and cannot be observed during a DPT. However, this energy loss is captured between t_5 and t_6 as the active device output capacitor is charged during the preceding turn-off transient. It is also important to note that the current overshoot between t_2 and t_3 does not include any reverse recovery in this case, as it

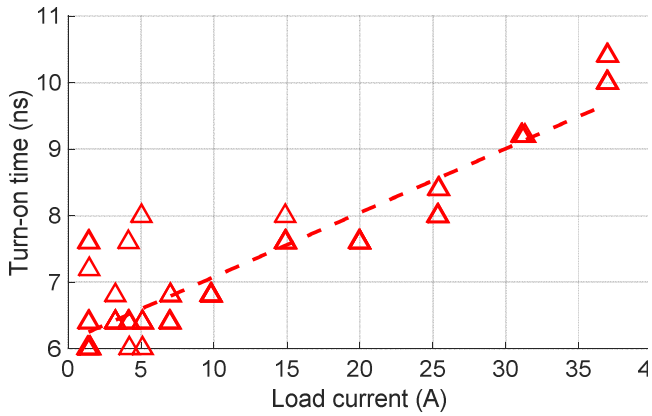

Fig. 13. Turn-on times at 400 V, 25 ºC.

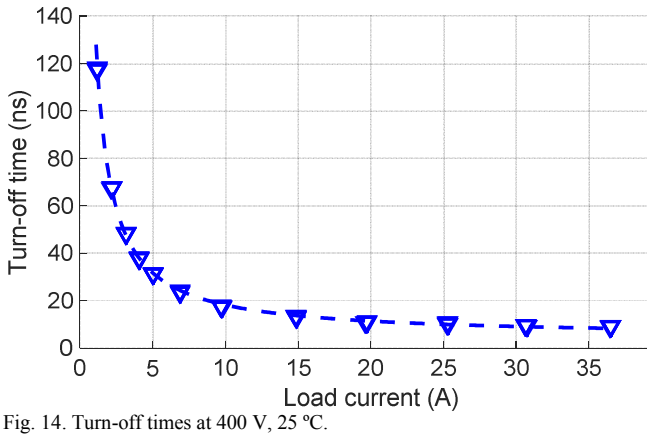

Fig. 14. Turn-off times at 400 V, 25 ºC.

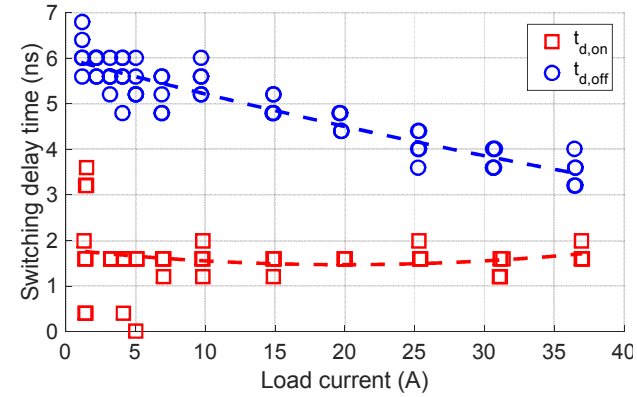

Fig. 15. Delay times at 400 V, 25 ºC.

would with a Si or SiC MOSFET body diode. The GaN device does not have a true body diode, so there is no stored minority carrier charge to remove when the synchronous device turns off.

D. Switching Time

Switching times were then calculated based on the time variables described in the previous section. The turn-on delay time is the difference between t_1 and t_2, and the turn-off delay time is the difference between t_4 and t_5. The turn-on time is then the difference between t_2 and t_3, and the turn-off time is the difference between t_5 and t_6. Figs. 13 and 14 show the turn-on and turn-off times, respectively. Turn-on time increases linearly with load current, whereas turn-off time is proportional to the inverse of load current. Both relationships can be approximated accurately with a first-order relationship as shown with the dashed lines. The turn-on and turn-off delay times are shown in Fig. 15. The turn-on delay is approximately 2 ns with no correlation to load current, and the turn-off delay is approximately 5 ns with a slight decrease at higher load current.

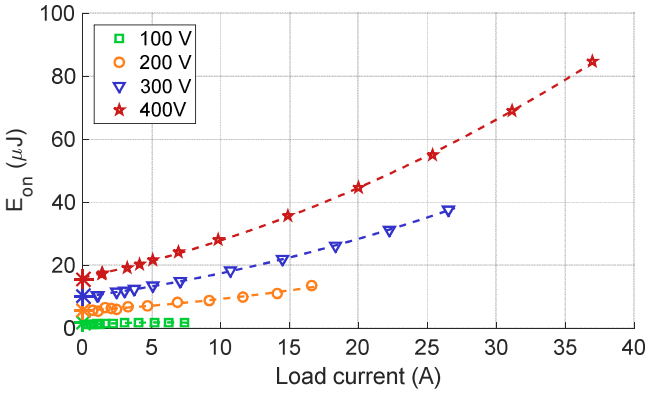

Fig. 16. Turn-on energy E_{on} at 25 ºC.

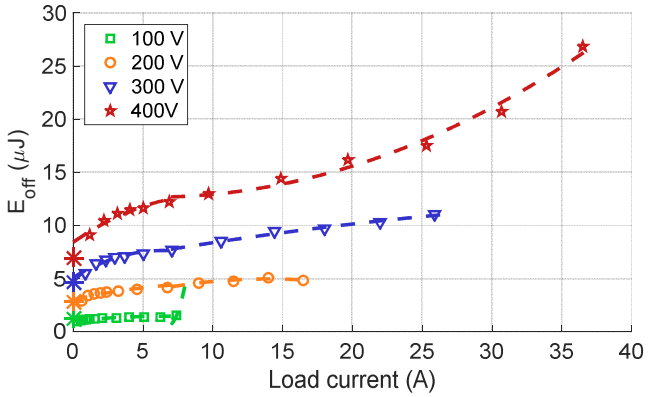

Fig. 17. Turn-off energy E_{off} at 25 ºC.

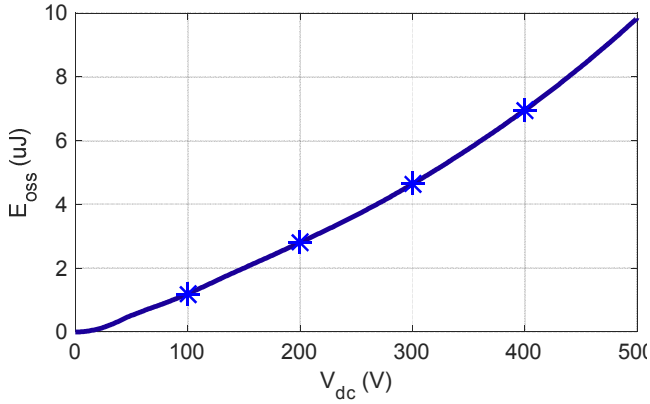

Fig. 18. Output capacitance stored energy E_{oss}, calculated from data sheet.

E. Switching Energy

The turn-on energy E_{on} and turn-off energy E_{off} were calculated as the integral of power between t_2 and t_3, and between t_5 and t_6 respectively. The ringing in the power that occurs after t_6, as shown in Fig. 12, was ignored since it does not contain any significant energy loss. Initial turn-off loss calculations did included this ringing, but this caused additional error due to the low-frequency common mode noise in the oscilloscope ground loop. Therefore, the loss calculation was more accurate with this ringing ignored.

Figs. 16 and 17 show the turn-on and turn-off loss, respectively. Both plots also show the theoretical no-load turn-on and turn-off loss, $E_{on,0A}$ and E_{oss}, marked with asterisks on the y axis. These values were calculated as functions of V_{dc}, using (1) and (2), along with the published C_{oss} curve from the manufacturer [13].

$$E_{oss}(V_{dc}) = \int_0^{V_{dc}} [C_{oss}(v) \times v] dv \quad (1)$$

$$E_{on,0A}(V_{dc}) = V_{dc} \int_0^{V_{dc}} [C_{oss}(v)] dv - E_{oss}(V_{dc}) \quad (2)$$

The load-based trends at each tested DC bus voltage can be approximated well with second-order equations as shown with dashed lines in Figs. 16 and 17. However, the turn-off loss must be split into two separate trends near the 7 A point to achieve an effective approximation, due to the nonlinear junction capacitance of the device. E_{on} and E_{off} for a hard-switching converter can be calculated across the voltage and current range using (3) and (4) and the coefficients listed in Tables I and II.

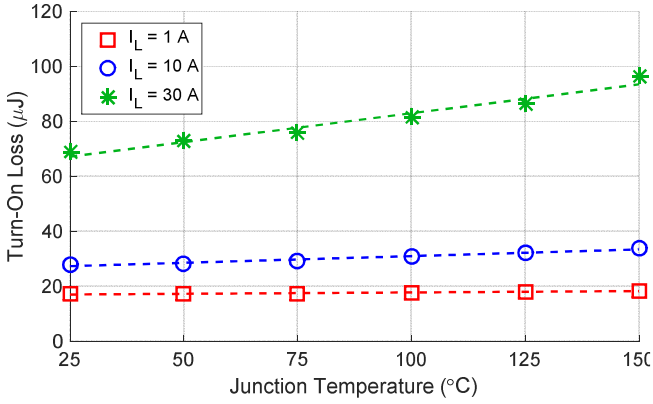

Fig. 19. Turn-on energy E_{on} at 400 V with elevated junction temperature.

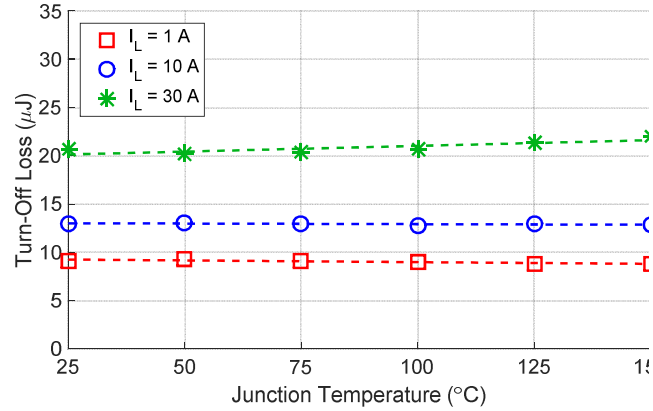

Fig. 20. Turn-off energy E_{off} at 400 V with elevated junction temperature.

TABLE I. E_{ON} SECOND ORDER APPROXIMATION COEFFICIENTS

Operating Conditions	k_1	k_2	k_3
400 V, 0-37 A	0.0247	0.9302	16.1406
300 V, 0-27 A	0.0176	0.5667	10.0385
200 V, 0-17 A	0.0119	0.2464	5.6710
100 V, 0-7 A	-0.0228	0.2655	1.1071

TABLE II. E_{OFF} SECOND ORDER APPROXIMATION COEFFICIENTS

Operating Conditions	k_4	k_5	k_6
400 V, 0-7 A	-0.0455	-0.8996	8.4322
400 V, 7-37 A	0.0143	-0.1622	13.1320
300 V, 0-7 A	-0.0626	0.7972	5.1050
300 V, 7-27 A	-0.0024	0.2482	6.1443
200 V, 0-17 A	-0.0157	0.3099	2.9879
200 V,7-17 A	-0.0155	0.4343	1.9345
100 V, 0-7 A	-0.0095	0.1297	1.0273

$$E_{on} = k_1 {I_L}^2 + k_2 I_L + k_3 \quad (3)$$

$$E_{off} = k_4 {I_L}^2 + k_5 I_L + k_6 \quad (4)$$

As mentioned previously, the energy E_{oss} is stored in the active device's junction capacitor between t_5 and t_6, then later lost inside the device during the following turn-on transient. However, in a soft-switching converter, the ZVS turn-on recovers that stored energy. Therefore, the total switching losses in a soft-switching converter can be estimated by subtracting E_{oss} from the hard-switching E_{off}, as given in (5). Fig. 18 shows the calculated values of E_{oss} for use with (5).

$$E_{off,soft-switching} = E_{off} - E_{oss} \quad (5)$$

Because of the reduced transconductance and saturation current at elevated temperature, the turn-on loss has a positive temperature coefficient that is proportional to load current as shown in Fig. 19. The turn-on loss increases 5% from 25 ºC to 125 ºC at 1 A, 15% at 10 A, and 25% at 30 A. The positive temperature coefficient of turn-on loss has been previously demonstrated for other enhancement-mode GaN HFETs [4]. During the turn-on transisiton, the lower transconductance at elevated temperature makes the active device channel more resistive and therefore limits the displacement current through both output capacitances, increasing the turn-on time and loss. As shown in Fig. 20, turn-off loss does not show a strong correlation with temperature.

F. Drain and Gate Voltage Overshoot

It is well-known that the parasitic power loop inductance L_{ds} causes a drain-source voltage overshoot at turn-off. Fig. 21 shows this voltage overshoot at 400 V over increasing load current, which can be approximated well as a first-order relationship as shown with the dashed line. As mentioned previously, turn-off speed is not strongly proportional to

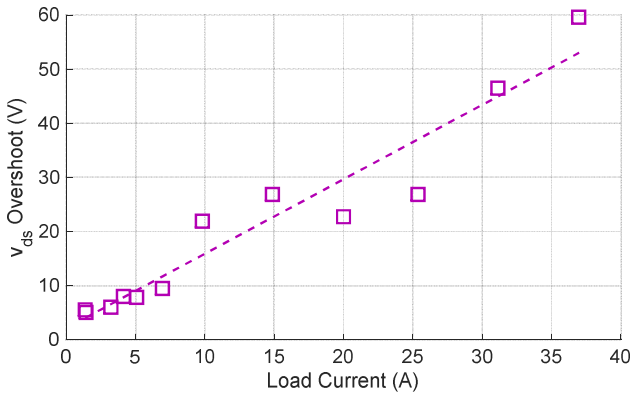

Fig. 21. Drain-source voltage overshoot at 400 V.

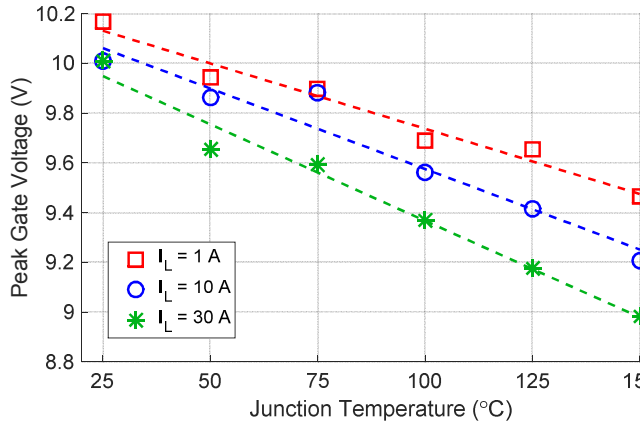

Fig. 22. Gate-source voltage overshoot at 400 V.

temperature. Since this voltage overshoot is mainly due to the speed of the *di/dt* transient during turn-off, it is also not very temperature-dependent. The maximum voltage reached at 400 V operation and the rated load current of 30 A was 445 V, which is well within the voltage blocking capability of the device.

Additionally, the gate loop inductance and resistance cause a v_{gs} overshoot at turn-on. In contrast with v_{ds}, the gate voltage overshoot is strongly proportional to junction temperature, due to the reduced turn-on speed. Fig. 22 shows this relationship. The overshoot exceeds the rated gate voltage in the light-load case, which could lead to long-term reliability issues, but only at an operating temperature below 50 ºC.

Reducing the driving voltage from 8 V to 7.5 V would also bring the gate voltage overshoot down below the rated maximum, but this may not be necessary for converters with operating temperatures above 50 ºC. Choosing the higher driving voltage of 8 V provides benefits in both turn-on and turn-off loss. For turn-on, increasing the driving voltage provides higher gate current during the entire turn-on transient, increasing turn-on speed and reducing E_{on}. The higher driving voltage also increases the peak gate current at the beginning of the turn-off transient, and the energy stored in the parasitic gate loop inductance L_{gs} provides a higher gate current during the Miller plateau. Therefore, the higher driving voltage reduces

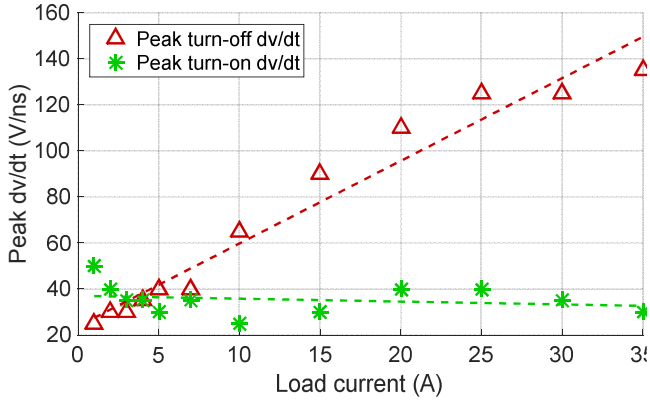

Fig. 23. Peak dv/dt during turn-on and turn-off at 400 V.

E_{off} as well, especially in the heavy load condition when the Miller plateau is longest.

In fact, choosing 8 V are the driving voltage over the recommended 7 V offsets the loss increase experienced from operation at 125 ºC instead of 25 ºC. The total switching losses with V_{gs} = 8 V and T_j = 125 ºC are approximately the same as the total switching losses with V_{gs} = 7 V and T_j = 25 ºC, across the full load range. Since 8 V driving is only practical at higher temperatures due to the gate voltage overshoot, this tradeoff can be leveraged for optimal converter design at operating temperatures above 50 ºC.

G. Peak dv/dt

The peak *dv/dt* was calculated for the turn-on and turn-off transients, by calculating the slope of the voltage across every 0.8 ns of data, averaging over two points to reduce the effect of measurement noise. Fig. 23 shows this calculated value at 400 V and 25 ºC.

The peak *dv/dt* is not as effective for measuring the switching speed as the turn-on and turn-off time presented previously. However, this calculation is an important parameter for selection of gate driving signal isolation. Most available digital isolators are only rated up to 50 V/ns, but some are rated as high as 100 V/ns. The isolator used in this work was only rated at 45 V/ns, but no CMTI problems were observed during testing. However, this may not be suitable for long-term operation above 5 A, where the turn-off *dv/dt* is shown to exceed 45 V/ns.

IV. Observed Device Failures

Because the devices were tested beyond their rated limits for this characterization, several failure modes were observed. The most common failure was due to shoot-through overcurrent, caused by issues in the DPT board or test setup. With sufficient stored energy in the decoupling capacitors and insufficient overcurrent protection, this completely destroyed the device. With less stored energy or sufficient overcurrent protection, this only led to an electrical breakdown of the device and a partially burned package. In this case, all or most of the pins of the device were shorted together, including the drain, source, gate, and substrate. The measured resistance between any of these pins was less than 100 Ω.

The second most common failure mode was gate dielectric breakdown from ESD, caused by improper handling before or during soldering the device to the board. In this failure mode, the gate functioned as a diode with its voltage pulled down to ~0.3 V, and the device was permanently turned off. However, the device could still conduct reverse current in SCRC operation.

Lastly, gate breakdown also occurred due to extended operation with v_{gs} at the maximum rated gate voltage of 10 V for several minutes. This did not seem to be a thermal breakdown, because the case temperature was measured with the board-mounted transducer and it did not show a temperature increase as this breakdown occurred. In this failure mode, the gate voltage was initially pulled low and the gate current increased dramatically, but the device could still effectively turn on and off. However, after some time with the increased gate current, all the pins were shorted together as in the overcurrent failure mode described previously. It is noteworthy that the peak gate voltage during dynamic testing routinely reached 10 V, and no devices failed due to transient gate overvoltage during repeated pulse testing.

V. Conclusion

The preceding characterization shows a commercially available enhancement-mode GaN device with low on-resistance and switching losses, allowing for higher efficiency and smaller overall converter size. The test results presented here will aid in effective gate driver design, board layout, and thermal design. The temperature-based characterization will be especially useful for choosing an appropriate thermal design and preventing thermal runaway, considering that the total losses at the maximum operating temperature will be roughly 50% higher than at room temperature. These results also support the manufacturer's device current rating, which drops from 30 A to 23 A at higher temperature based on the lower saturation current. The best switching performance was achieved by driving the gate at 8 V with 0 Ω external gate resistance, although the DC gate current was shown to be higher at that voltage. Therefore, the gate current capability should be considered carefully in gate drive design when optimizing switching performance.

Future work will include a complete characterization of the cross-talk phenomenon and resulting shoot-through losses in both the active and synchronous devices, with a variety of gate driver designs and separate turn-on and turn-off gate resistances. The relationship between junction temperature and turn-on loss will be studied further based on these experimental results, and a model will be developed to explain this relationship. Additionally, the dynamic $R_{ds\text{-}on}$ of this device will be characterized with a test fixture designed to capture accurate low-voltage oscilloscope waveforms within a short time scale (< 100 ns) after turn-on.

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