

Characterization and Modeling of a Gallium Nitride Power HEMT



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Abstract—In this paper, a simple and accurate circuit-simulator compact model for gallium nitride (GaN) high electron mobility transistor is proposed and validated under both static and switching conditions. A novel feature of this model is that it is valid also in the third quadrant, which is important when the device operates as a freewheeling diode. The only measurements required for the parameter extraction are simple I - V static characteristics and C - V characteristics. A detailed parameter extraction procedure is presented. Furthermore, a double-pulse test-bench is built to characterize the resistive and inductive switching behavior of the GaN device. A simulation model is built in Pspice software tool, considering the parasitic elements associated with the printed circuit board interconnections and other test-bench components (load resistor, load inductor, and current shunt monitor). The Pspice simulation results are compared with experimental results. The comparison shows good agreement between simulation and experimental results under both resistive and inductive switching conditions. Operation in the third quadrant under inductive switching is also validated.

Index Terms—Modeling, power conversion, power electronics, power semiconductor devices, power semiconductor diode switches, power semiconductor switches, semiconductor device modeling.

I. INTRODUCTION

GALLIUM NITRIDE (GaN) is considered one of the most promising semiconductor material candidates for high-frequency, high-efficiency, and high-power density power conversion applications with significant advantages over silicon because of its excellent electrical properties, such as wider bandgap, higher thermal conductivity, and higher critical breakdown electric field [1]–[3]. The GaN high-electron-mobility transistor (HEMT) is the most promising active device in GaN and is currently available from various manufacturers, such as efficient power conversion (EPC), International Rectifier (now acquired by Infineon), Transphorm, GaN Systems, and others. GaN HEMT has a better Baliga figure of merit compared to state-of-the-art Si MOSFETs, because GaN HEMT exhibits low

Manuscript received November 19, 2015; revised May 22, 2016; accepted June 20, 2016. Date of publication July 7, 2016; date of current version November 18, 2016. Paper 2015-PEDCC-0781.R1, presented at 2014 Energy Conversion Congress and Exposition, Pittsburgh, PA, USA, Sep. 14–18, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Power Electronic Devices and Components Committee of the IEEE Industry Applications Society. This work was supported by the Office of Naval Research under Grant N00014-08-1-0080.

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Digital Object Identifier 10.1109/TIA.2016.2587766

on-state resistance, small parasitic device capacitance, and high critical electric field [4]. As a result, GaN HEMT can switch at faster speeds and exhibit lower conduction and switching losses [5]–[8]. Since power semiconductor device performance plays a key role in power electronics applications, power electronics designers need validated circuit-oriented device models to evaluate the performance of GaN HEMTs in different applications. The objective of this work is to develop a simple and accurate circuit-simulator compact device model, and validate it for commercially available GaN HEMT devices under static and switching conditions.

So far several device models have been proposed for GaN HEMT, most of them based on device physics. These physics-based device models provide more accuracy but have some disadvantages: They typically require several device parameters (which are usually unavailable to circuit designers) to apply the model to a specific device; they are complicated; and they require long simulation time [9]. Additionally, most of these models have originally been developed for high frequency or microwave applications, which are quite different from power electronics applications. Very few papers have been published on the development of a device model for GaN HEMT in the power conversion area. In [10], a simple GaN power transistor model for dc–dc converters has been proposed, and it is shown to have good static characteristics in most respects. However, this paper does not provide switching characteristics and does not consider the reverse channel current conduction behavior of GaN HEMT. The reverse channel current conduction is of vital importance, because the GaN transistor has no body diode. When GaN HEMT is required to operate in the third quadrant, the reverse channel current conduction from source to drain functions as an equivalent body diode. In [11], a GaN HEMT model has been developed in SaberRD and static I - V and C - V characteristics have been validated, but the validation of switching characteristics is not provided.

This paper describes the development and validation of a simple GaN HEMT device model including forward and reverse channel current conduction. The device under investigation is the commercially available EPC2001 (100 V/7 mΩ) from EPC. The simulation software used in this modeling work is Pspice. In Section II, the model equations are given. In Section III, static characterization is performed using a curve tracer and C - V analyzer. Parameter extraction procedure is proposed to extract device model parameter values. The model validation is presented in Section IV. For dynamic switching characterization, a double-pulse tester (DPT) printed circuit board (PCB) with both a resistive load and an inductive load is built. The 3-D inductance extraction software program

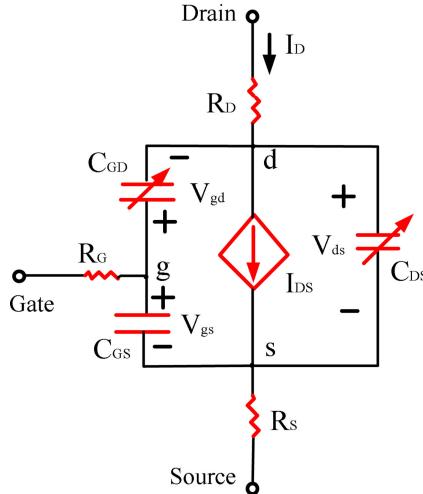


Fig. 1. Structure of the GaN HEMT model.

FastHenry is used to estimate the parasitic inductances from DPT circuit PCB layout. The extracted gate drive loop and drain-to-source main switching loop parasitic inductances from the PCB layout are used in Pspice simulation circuit together with the developed GaN HEMT model to accurately simulate the resistive and inductive switching transient behavior of the power devices.

II. DEVELOPMENT OF A DEVICE SIMULATION MODEL

The simple circuit-simulator compact GaN HEMT model developed in this work is shown in Fig. 1. The model comprises a voltage-dependent current source I_{ds} , two voltage-dependent capacitances C_{gd} and C_{ds} , a voltage-independent gate-source capacitance C_{gs} , and three parasitic resistances R_g , R_s and R_d . The voltage-dependent current source I_{ds} is used to model static current-voltage (I - V) characteristics for both forward and reverse conduction. The three parasitic capacitances play a vital role in determining device switching performance. Note that for simplicity dynamic on-resistance effects—the so-called current collapse phenomenon—are not considered in this model.

A. Voltage-Dependent Current Source I_{ds}

The voltage-dependent current source I_{ds} is a bidirectional current source function of internal device node voltages V_{ds} and V_{gs} . Since the device has a nearly symmetrical lateral structure, a positive gate-to-drain voltage will enhance channel conduction in the third quadrant in the same way as a positive gate-to-source voltage does in the first quadrant. Therefore, the forward and reverse channel conduction modes are both taken into account. In order to accurately predict power converter performance at different operating temperatures, accurate temperature-dependent device transconductance parameter K_p is used in the circuit model.

The voltage-dependent current source I_{ds} determines the model I - V characteristics in the four operating modes: forward linear, forward saturation, reverse linear, and reverse saturation modes. These operating regions and the corresponding

TABLE I
OPERATING REGIONS OF VOLTAGE-DEPENDENT CURRENT SOURCE

Operating region	Condition	Equation
Cut off	$V_{gs} < V_{th1}$, $V_{ds} \geq 0$ or $V_{gd} < V_{th2}$, $V_{sd} \geq 0$	$I_{ds} = 0$
Forward conduction linear region	$V_{ds} < V_{gs} - V_{th1}$ and $V_{ds} > 0$	$I_{ds} = K_{p1}[(V_{gs} - V_{th1}) - V_{ds}^2/2]$
Forward conduction saturation region	$V_{ds} > V_{gs} - V_{th1} > 0$ and $V_{ds} > 0$	$I_{ds} = K_{p1}(V_{gs} - V_{th1})^2/(1 + \lambda_1 V_{ds})/2$
Reverse conduction linear region	$V_{sd} < V_{gd} - V_{th2}$ and $V_{sd} > 0$	$I_{ds} = -K_{p2}[(V_{gd} - V_{th2})V_{sd} - V_{sd}^2/2]$
Reverse conduction saturation region	$V_{sd} > V_{gd} - V_{th2} > 0$ and $V_{sd} > 0$	$I_{ds} = -K_{p2}(V_{gd} - V_{th2})^2/2$

current equations are listed in Table I where V_{th1} is the threshold voltage for forward channel conduction, and V_{th2} is the threshold voltage for reverse channel conduction. Note that this model neglects the temperature effect on threshold voltages, which can be taken into account in future work. K_{p1} is the temperature-dependent device transconductance parameter in forward conduction mode. K_{p2} is the temperature-dependent device transconductance parameter in reverse conduction mode. λ_1 is the channel length modulation parameter for forward channel conduction.

B. Parasitic Capacitances C_{gs} , C_{gd} , and C_{ds}

Since gate-source capacitance is relatively independent of the voltage potentials applied to the electrodes, a constant gate-source capacitance C_{gs} is used in this device model. This assumption is justified by device capacitance measurement shown in Fig. 8. Capacitances C_{gd} and C_{ds} are nonlinear voltage-dependent parasitic capacitances, given by

$$C_{gd} = \frac{C_{gd0}}{\left(1 + \frac{|V_{gd}|}{PB1}\right)^{m_1}} \quad (1)$$

$$C_{ds} = \frac{C_{ds0}}{\left(1 + \frac{|V_{ds}|}{PB2}\right)^{m_2}} \quad (2)$$

where C_{gd0} is the zero-bias gate-to-drain capacitance, and C_{ds0} is the zero-bias drain-to-source capacitance. $PB1$ and $PB2$ are the junction built-in potentials for gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} , respectively. The parameters m_1 and m_2 are the junction grading coefficients for gate-drain capacitance C_{gd} and drain-source capacitance C_{ds} , respectively.

C. Parasitic Resistances R_g , R_s , and R_d

Internal gate resistance R_g is assumed to be zero, combined with the external gate resistance typically introduced to open transient oscillations during switching transients. Resistances R_s and R_d are assumed to be constant and represent the distributed nature of terminal contact mesh.

TABLE II
GAN HEMT MODEL PARAMETERS

K_{p1}	Forward conduction device transconductance parameter at room temperature
K_{p2}	Reverse conduction device transconductance parameter at room temperature
V_{th1}	Forward conduction gate threshold voltage
V_{th2}	Reverse conduction gate threshold voltage
λ_1	Forward conduction channel length modulation coefficient
C_{gs}	Gate-source capacitance
C_{gd0}	Zero-bias gate-drain capacitance
PB_1	Built-in potential for gate-drain capacitance
m_1	Junction grading coefficient for gate-drain capacitance
C_{ds0}	Zero-bias drain-source capacitance
PB_2	Built-in potential for drain-source capacitance
m_2	Junction grading coefficient for drain-source capacitance
R_d	Drain parasitic resistance
R_s	Source parasitic resistance
T_{c1-1} T_{c2-1}	Temperature coefficients for forward conduction device constant
T_{c1-2} T_{c2-2}	Temperature coefficients for reverse conduction device constant

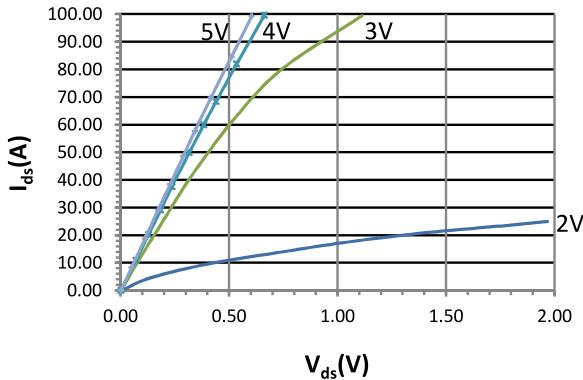


Fig. 2. Measured forward output I - V characteristics at room temperature 25°C for EPC 2001.

D. Temperature Dependence of the Device Transconductance Parameter K_p

In order to accurately estimate the device conduction I_c versus temperature, the device model should include the temperature dependence of the device transconductance parameter K_p , which determines the voltage drop across the device as a function of current. A quadratic fit for the temperature dependence of the device transconductance parameter K_p is proposed

$$K_p = K_{p0} / (1 + T_{c1}(T - T_0) + T_{c2}(T - T_0)^2) \quad (3)$$

where K_{p0} is the nominal device transconductance parameter at room temperature, T_0 is nominal room temperature, and T_{c1} and T_{c2} are temperature coefficients.

The complete list of the needed parameters for the considered device model is shown in Table II.

III. STATIC CHARACTERIZATION AND PARAMETER EXTRACTION

The parameter extraction approach used in this paper is based on static characterization of the semiconductor device. Static I - V characteristics are measured with a Tektronix 371A curve

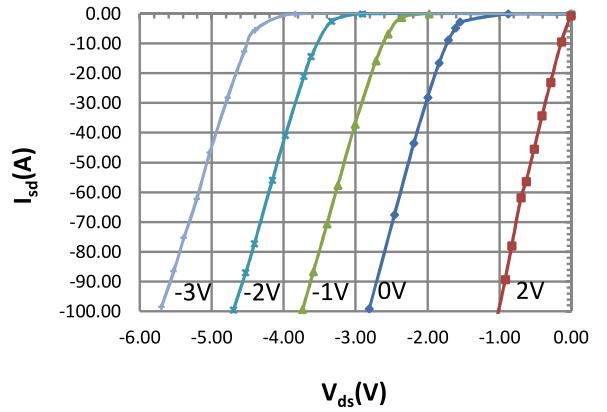


Fig. 3. Measured reverse output I - V characteristics at room temperature 25°C for EPC 2001.

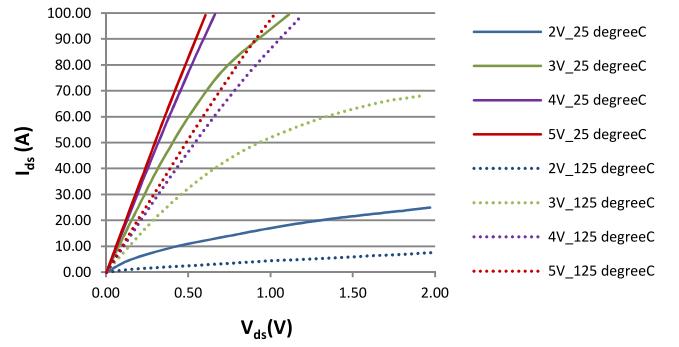


Fig. 4. Measurement of forward temperature-dependent output characteristics at 25°C (solid) and 125°C (dashed).

tracer, and capacitance C - V characteristics with a Keithley 590 CV analyzer.

A. Static Characteristics of GaN HEMT

The forward output characteristic family of curves is measured under different gate-source voltage bias conditions (from 2 V up to 5 V) in Fig. 2. The reverse output characteristic curves under different gate-source voltage bias conditions (from -3 V up to 2 V) are shown in Fig. 3. It is interesting to notice that the reverse characteristic curves do not exhibit saturation characteristics similar to the forward characteristics curves. This is due to the fact that these characteristics are measured with a curve tracer under constant gate-source voltage $V_{gs} = \text{const.}$, but for reverse conduction the controlling voltage is the gate-drain voltage V_{gd} . As source-drain voltage V_{sd} increases, gate-drain voltage also increases according to

$$V_{gd} = V_{gs} + V_{sd} = \text{const} + V_{sd}. \quad (4)$$

The measured forward output characteristic curves ($V_{gs} = 2/3/4/5$ V) under operating temperatures 25 and 125°C are shown in Fig. 4. As seen, the slope of the I - V curve decreases with increasing temperature, indicating the decreasing channel conductivity. This is due to the lower

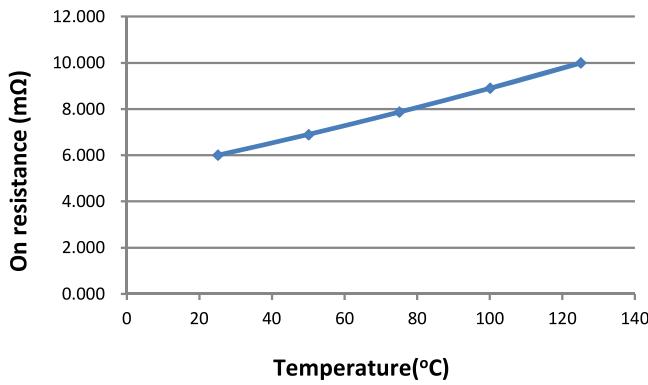


Fig. 5. Measured on resistance of GaN HEMT at 5 V gate–source voltage as a function of junction temperature.

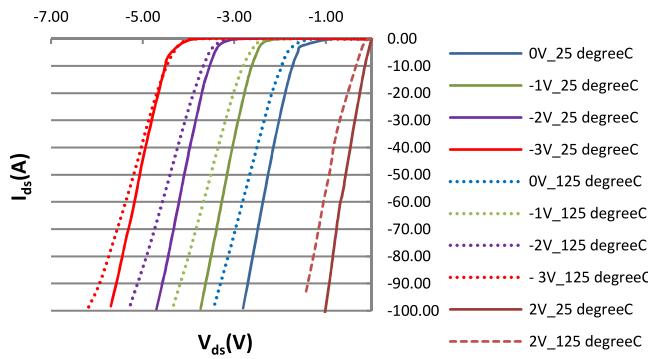


Fig. 6. Measurement of reverse temperature-dependent output characteristics at 25°C (solid) and 125°C (dashed).

channel carrier mobility under higher operating temperatures. This device characteristic is potentially beneficial to device paralleling. Fig. 5 shows the measured on-resistance at maximum gate–source voltage ($V_{gs} = 5$ V) as a function of junction temperature. The measured on-resistance of GaN HEMT increases from 6.01 to 10.01 mΩ, as device junction temperature rises from 25 to 125°C.

The measured reverse output characteristics curves ($V_{gs} = -3/-2/-1/0/2$ V) under operating temperatures 25 and 125°C show a similar behavior in Fig. 6.

The measured transfer characteristic of GaN HEMT at room temperature is shown in Fig. 7, which describes drain current I_{ds} as a function of gate–source voltage V_{gs} at a constant drain–source voltage V_{ds} .

A plot of measured device parasitic capacitances is shown in Fig. 8. These measurements justify the choice of having a constant gate–source capacitance C_{gs} , since from Fig. 8 one can see that $C_{gs} = C_{iss} - C_{rss}$ approximately constant.

B. Parameter Extraction

The parameter extraction process for GaN HEMT is developed using only measured static I – V and C – V characteristics. The parameter extraction process using static characterizations is described as follows.

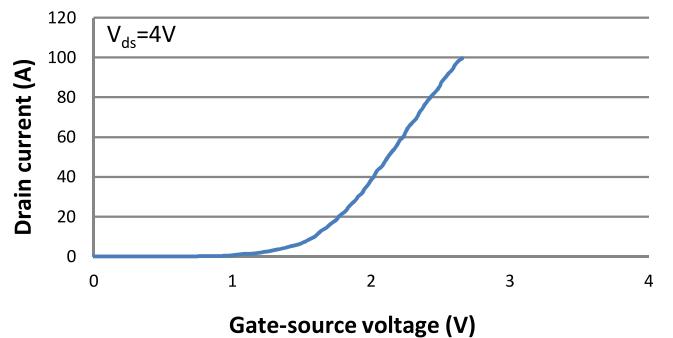


Fig. 7. Measurement of transfer characteristic at room temperature.

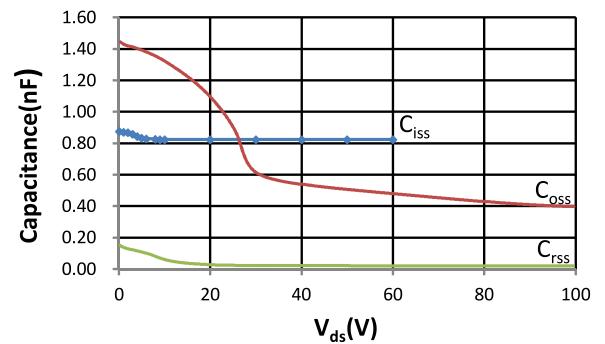


Fig. 8. Measured capacitances versus drain-to-source voltage for EPC 2001.

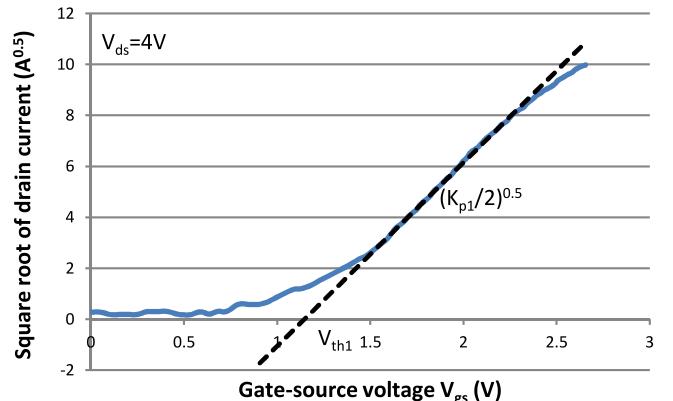
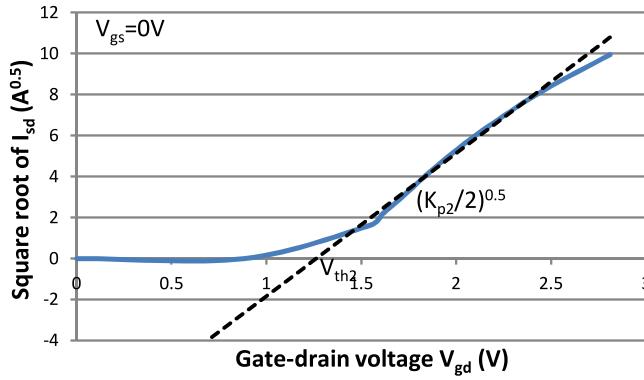
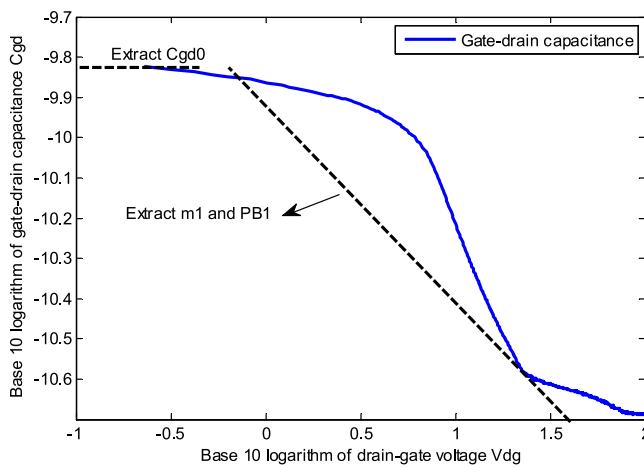


Fig. 9. Plot of the square root of I_{ds} versus gate–source voltage.

1) *Forward Conduction Device Transconductance Parameter K_{p1} and Threshold Voltage V_{th1} :* A curve of the square root of I_{ds} versus gate–source voltage V_{gs} shown in Fig. 9 is plotted to extract the forward conduction device transconductance parameter K_{p1} and threshold voltage V_{th1} . The parameter $(K_{p1}/2)^{0.5}$ is extracted from the slope of an operating point on the curve, when the GaN HEMT operates in the saturation region of forward conduction. The threshold voltage V_{th1} is extracted from the point of intersection of the tangent line to the curve with the x -axis.

2) *Forward Conduction Channel Length Modulation Coefficient λ_1 :* The channel-length modulation coefficient λ_1 is

Fig. 10. Plot of the square root of I_{sd} versus gate-drain voltage.Fig. 11. Log-log plot of C_{gd} versus drain-gate voltage.

extracted from the slope of forward output I - V characteristics in the saturation region.

3) *Inverse Conduction Device Transconductance Parameter K_{p2} and Threshold Voltage V_{th2} :* A curve of the square root of I_{sd} versus gate-drain voltage V_{gd} shown in Fig. 10 is plotted to extract the reverse conduction device transconductance parameter K_{p2} and threshold voltage V_{th2} . The parameter $(K_{p2}/2)^{0.5}$ is extracted from the slope of an operating point on the curve, when the GaN HEMT operates in the saturation region of reverse conduction. The threshold voltage V_{th2} is extracted from the point of intersection of the tangent line to the curve with the x -axis.

4) *Gate-Source Capacitance C_{gs} :* Gate-source capacitance C_{gs} is approximately constant. The parameter C_{gs} is extracted from C_{iss} and C_{rss} measurements.

5) *Zero-Bias Gate-Drain Capacitance C_{gd0} , Built-in Potential PB₁, and Junction Grading Coefficient m₁:* The zero-bias gate-drain capacitance C_{gd0} is extracted from C_{rss} measurement at low gate-drain bias. As shown in Fig. 11, the junction grading coefficient m_1 is extracted from the slope of gate-drain capacitance curve at high drain bias. The built-in potential PB₁ is extracted from a linear interpolation of the curve. The accuracy could be improved by using a higher order interpolation at the cost of increased model complexity.

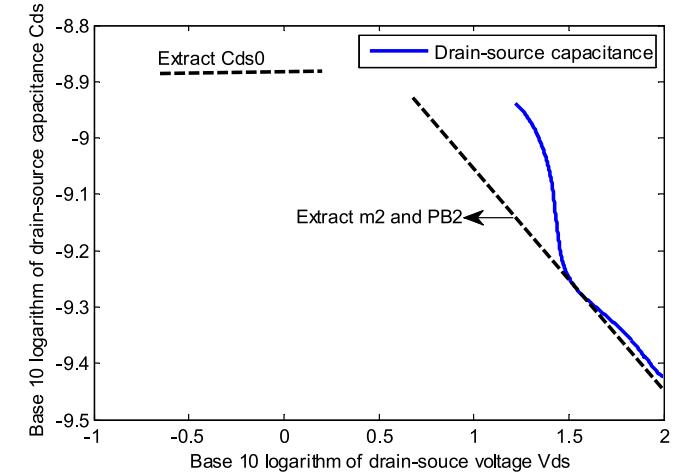
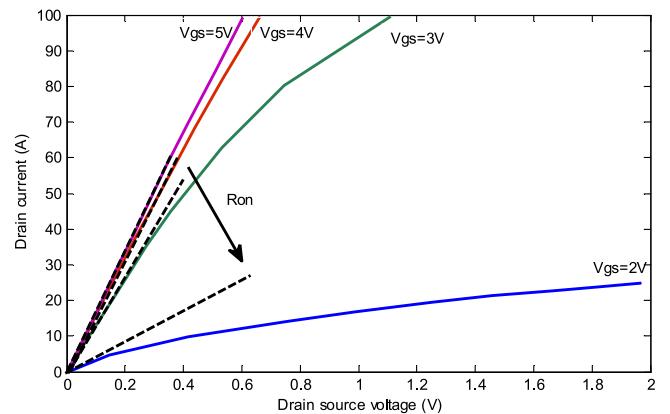
Fig. 12. Log-log plot of C_{ds} versus drain-source voltage.

Fig. 13. Forward conduction output characteristics and on-resistance extraction.

accuracy could be improved by using a higher order interpolation at the cost of increased model complexity.

6) *Zero-Bias Drain-Source Capacitance C_{ds0} , Built-in Potential PB₂, and Junction Grading Coefficient m₂:* The zero-bias gate-drain capacitance C_{ds0} is extracted from C_{oss} and C_{rss} measurements at low drain-source bias. As shown in Fig. 12, the junction grading coefficient m_2 is extracted from the slope of drain-source capacitance curve at high drain bias. The built-in potential PB₂ is extracted from a linear interpolation to the curve.

7) *Main Parasitic Resistance R_d and Source Parasitic Resistance R_s :* The total forward conduction on-resistances at varied gate-source voltages are extracted from output characteristics shown in Fig. 13. In the linear I - V region, the parasitic resistances R_d and R_s are connected in series with the internal channel resistance.

With on-resistances extracted from Fig. 13, a curve of total on-resistance as a function of $1/(V_{gs} - V_{th1})$ is given in Fig. 14 to estimate the sum of parasitic resistances R_d and R_s . The sum of R_d and R_s is extracted from the point of intersection of tangent line to the curve with the y -axis [12].

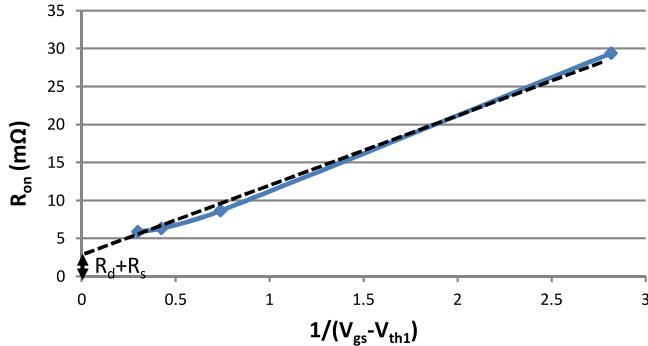


Fig. 14. Plot of on-resistance R_{on} versus $1/(V_{gs} - V_{th1})$.

TABLE III
EXTRACTED MODEL PARAMETER VALUES FOR EPC 2001

Parameter	Value	Source
K_{p1}	103.664 A/V^2	DC transfer characteristics
K_{p2}	102.259 A/V^2	DC transfer characteristics
V_{th1}	1.155 V	DC transfer characteristics
V_{th2}	1.285 V	DC transfer characteristics
λ_1	0.241 A/V	DC output characteristics
C_{gs}	0.804 nF	C-V characteristics
C_{gd0}	0.151 nF	C-V characteristics
PB_1	1.216 V	C-V characteristics
m_1	0.451	C-V characteristics
C_{ds0}	1.299 nF	C-V characteristics
PB_2	1.805 V	C-V characteristics
m_2	0.302	C-V characteristics
R_d	2.400 mΩ	DC output characteristics
T_{c1-1}	0.013	Temperature
T_{c2-1}	1.906×10^{-5}	Temperature
T_{c1-2}	0.002	Temperature
T_{c2-2}	6.241×10^{-5}	Temperature

Considering the lateral device structure of GaN HEMT, drain parasitic resistance R_d is much larger than source parasitic resistance R_s . Therefore, source parasitic resistance R_s is assumed to be zero in this model.

8) *Temperature Coefficients $T_{c1-1}, T_{c1-2}, T_{c2-1}$ and T_{c2-2} :* Only parameters K_{p1} and K_{p2} have temperature dependence. The nominal device transconductance parameters at room temperature K_{p0-1} and K_{p0-2} are extracted at room temperature (25°C). To extract the temperature coefficients, the same extraction procedure for parameters K_{p1} and K_{p2} is performed at several higher temperatures (50, 75, 100, and 125°C). Only the temperature-dependent parameters are extracted at each temperature, while the temperature-independent parameters are fixed at their room temperature values. Values for parameters K_{p1} and K_{p2} are obtained at several temperature points. Using temperature dependence (3), the temperature coefficients are extracted using the parameter values as a function of temperature.

IV. MODEL VALIDATION

The parameter extraction method of a GaN HEMT model is described in Section III. Table III lists the extracted model parameter values for EPC 2001 (100 V/7 mΩ) GaN HEMT. In

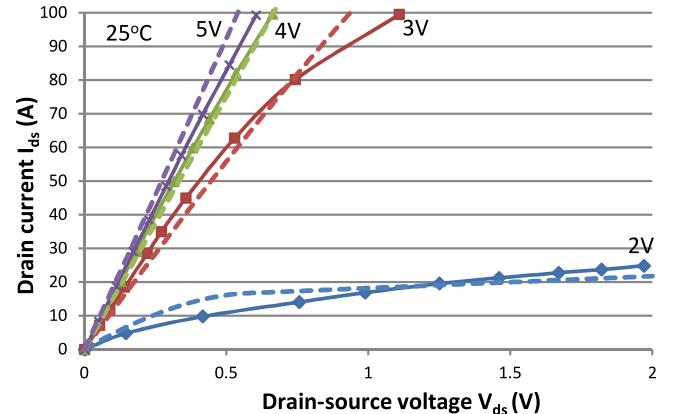


Fig. 15. Forward I - V characteristic comparison between simulation (dashed) and measurement (solid) at room temperature 25°C.

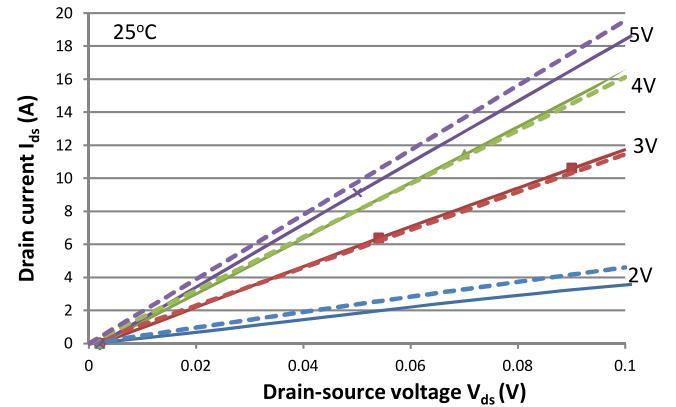


Fig. 16. Forward I - V characteristics comparison between simulation (dashed) and measurement (solid) in linear region (zoom-in of prior figure) at room temperature 25°C.

this section, the developed GaN HEMT model is validated under static and switching conditions.

A. Validation of Static Characteristics

Fig. 15 shows the comparison of simulated (dash lines) I - V characteristics of GaN HEMT in forward conduction mode based on the extracted parameters with experimental (solid lines) static characteristics. The simulation I - V curves are in good agreement with experimental data under different gate bias conditions; however, discrepancies can be observed in the saturation region. In order to capture the device on-state behavior, accurate modeling of the output characteristics in the linear region is crucial. Fig. 16 shows the comparison of simulated (dash lines) I - V characteristics of GaN HEMT in the forward linear region based on the extracted parameters with experimental (solid lines) static characteristics. Good agreement between measured and simulated results is shown. Fig. 17 shows the comparison between simulation (dash lines) I - V curves and experimental I - V characteristics (solid lines) in reverse conduction mode. The simulation results have very good matching with experimental results.

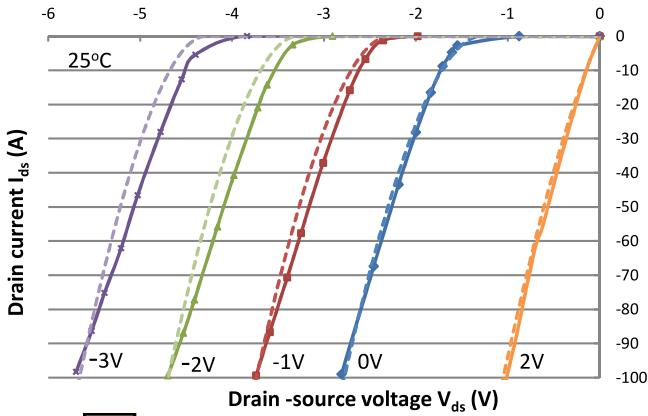


Fig. 17. Reverse $I-V$ characteristic comparison between simulation (dashed) and measurement (solid) at room temperature 25°C.

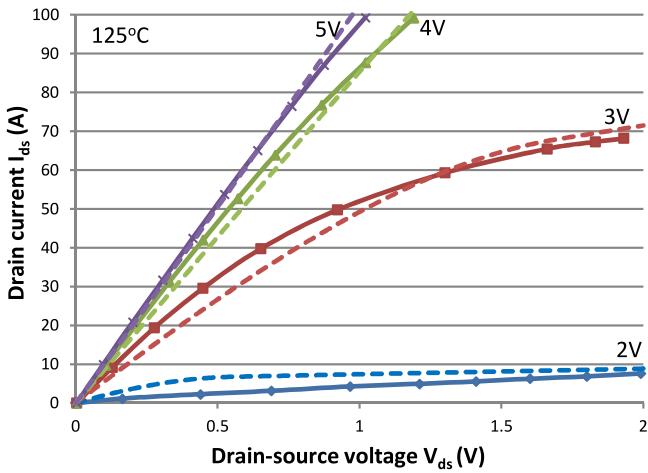


Fig. 18. Forward $I-V$ characteristic comparison between simulation (dashed) and measurement (solid) at 125°C.

The measured and simulated $I-V$ characteristics in forward conduction mode at 125°C are shown in Fig. 18. Fig. 19 shows the measured and simulated $I-V$ characteristics in reverse conduction mode. Excellent agreement is observed between simulation and measurement in $I-V$ characteristics at 125°C.

The comparison of on-resistance at maximum gate voltage ($V_{gs} = 5$ V) between simulations and experiments is shown in Fig. 20. The simulated on-resistance is in agreement with the measured result over the temperature ranging from 25 to 125°C.

Fig. 21 shows the plot of measured and simulated capacitances of GaN HEMT, showing a discrepancy in the C_{oss} voltage dependence at low drain voltage. This is probably due to the specific geometry of the drain-source region.

B. Validation of Switching Characteristics

A PCB DPT circuit has been built to verify the accuracy of the proposed GaN HEMT device model under switching conditions. Figs. 22 and 23 show the double-pulse test circuit schematic and PCB prototype. The double-pulse test circuit has a phase leg structure with a GaN HEMT EPC 2001 pair. The

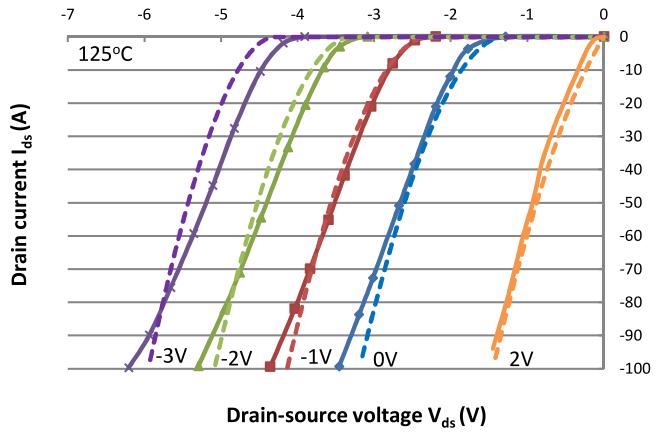


Fig. 19. Reverse $I-V$ characteristic comparison between simulation (dashed) and measurement (solid) at 125°C.

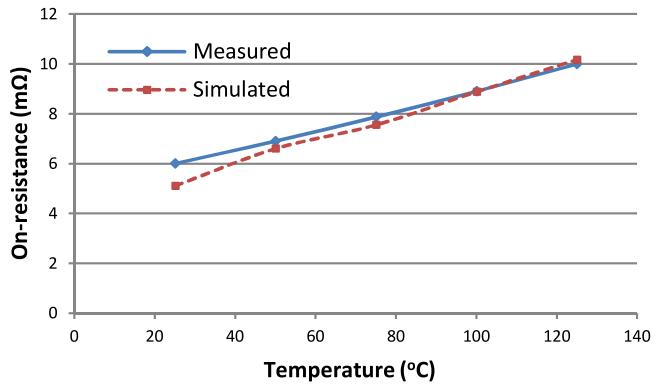


Fig. 20. On-resistance comparison between simulation (dashed) and measurement (solid) at 5 V gate-source voltage.

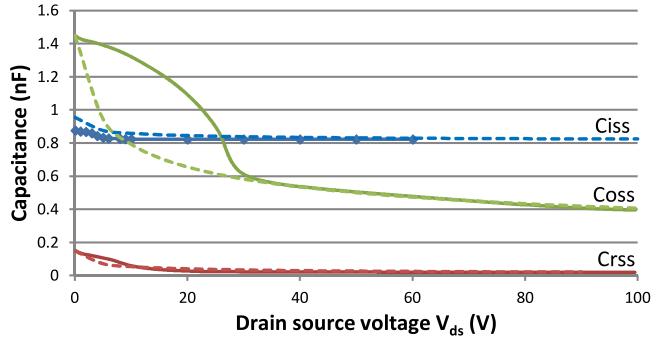


Fig. 21. Comparison of $C-V$ characteristic between simulation (dashed) and measurement (solid).

PCB layout is carefully designed to minimize parasitic elements. The current waveforms are measured by a coaxial shunt resistor (0.1 Ω) with high bandwidth and low parasitics from T&M Research Products, Inc. The gate driver is driver IC LM5113 from Texas Instruments, which is designed to drive both high side and low side enhancement mode GaN HEMTs in a half-bridge configuration. The gate driver LM5113 has separate turn-ON and turn-OFF driving pins, so that different gate resistances

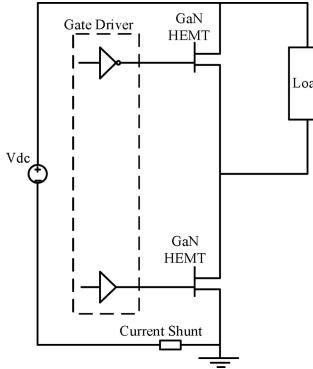


Fig. 22. Double-pulse test circuit schematic.



Fig. 23. Picture of DPT PCB board.

can be used for turn-ON and for turn-OFF. Switching characterization is done under resistive load conditions and inductive load conditions at room temperature.

The 3-D inductance extraction software program FastHenry is used to estimate parasitic inductances in the DPT circuit PCB layout [13]. The circuit components in the DPT—including load inductor, load resistor, and current shunt—are modeled on the basis of frequency domain measurements performed using the Agilent 4395A network analyzer. These parasitics are included in circuit simulations, in order to predict voltage and current transient slopes, ringing, and spikes [14].

1) Resistive Switching Validation: For the resistive switching experiments the resistive load is 12Ω . Switching speeds and energy losses are dependent on gate resistance values. Different gate driver turn-ON and turn-OFF resistance values are tested. The top GaN HEMT device is OFF in this testing. The comparison between simulation and experiment is performed at room temperature. Comparisons between experimental and simulated waveforms are shown in Fig. 24 for turn-ON transient and in Fig. 25 for turn-OFF transient. The gate driver turn-ON resistance is 7.5Ω , and turn-OFF resistance is 3Ω . As seen from the figures, the simulation results are in good agreement with the experimental results.

Table IV shows EPC 2001 turn-ON and turn-OFF resistive switching performance with different gate resistance values. The fastest switching speeds obtained for the DPT are $dv/dt_{(on)} =$

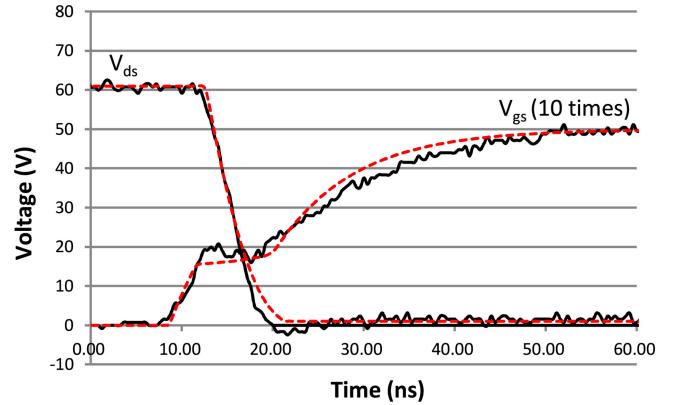


Fig. 24. Simulated (dashed) and experimental (solid) turn-ON voltage waveforms of resistive switching.

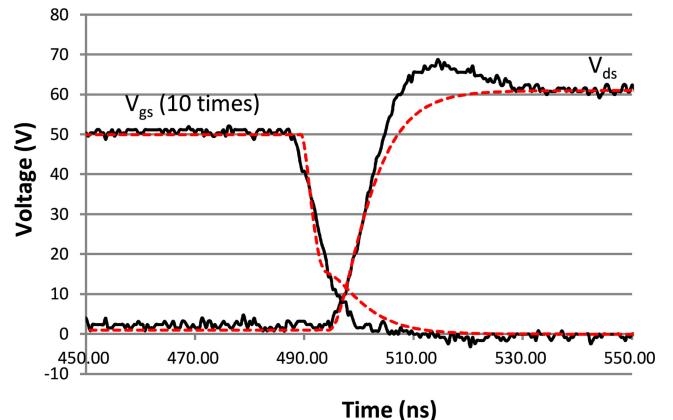


Fig. 25. Simulated (dashed) and experimental (solid) turn-OFF voltage waveforms of resistive switching.

TABLE IV
RESISTIVE SWITCHING RESULTS

Turn-on gate resistance $R_{on} (\Omega)$	Turn-off gate resistance $R_{off} (\Omega)$	Turn-on dv/dt (V/ns)	Drain-source voltage falling time (ns)	Turn-off dv/dt (V/ns)	Drain-source voltage rising time (ns)
15	10	5.42	8.9	2.84	16.9
15	7.5	5.42	8.7	3.29	14.6
15	3	5.51	8.7	4.98	9.6
10	3	7.42	6.5	5.00	9.6
7.5	3	9.34	5.2	5.17	9.3
0	0	16.2	3.0	26.6	1.78

16.2 V/ns and $dv/dt_{(off)} = 26.6\text{ V/ns}$. Fig. 26 shows the turn-ON speed dependence on turn-ON resistance, while Fig. 27 shows the turn-OFF speed dependence on turn-OFF resistance. As the gate resistance increases, switching speeds reduce as expected. As turn-ON gate resistance varies from 7.5 to 15Ω , the corresponding turn-ON dv/dt drops from 9.34 to 5.42 V/ns . As turn-OFF gate resistance increases from 3 to 10Ω , the corresponding turn-OFF dv/dt is reduced from 5.17 to 2.84 V/ns . The simulated results show a good matching with the experiment.

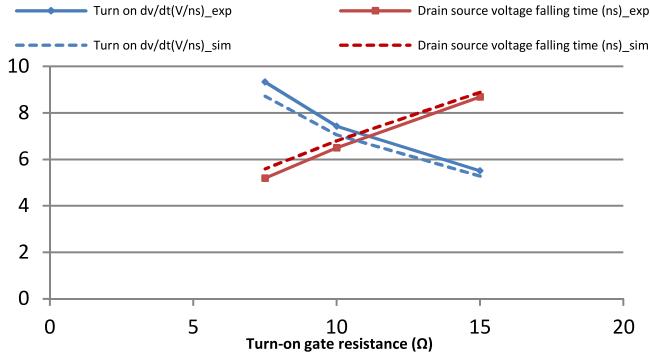


Fig. 26. Simulated (dashed) and experimental (solid) turn-ON dv/dt and drain source voltage falling time dependence on turn-ON gate resistance.

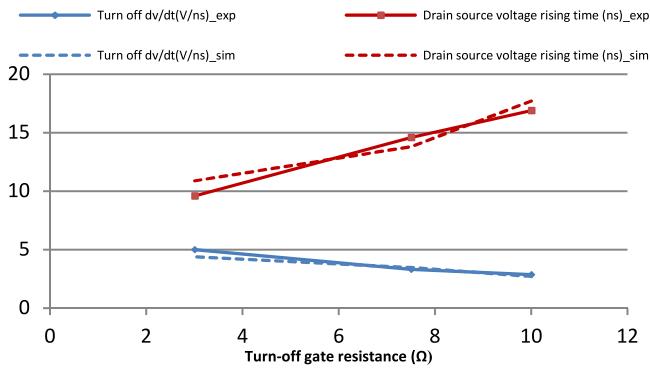


Fig. 27. Simulated (dashed) and experimental (solid) turn-OFF dv/dt and drain source voltage rising time dependence on turn-OFF gate resistance.

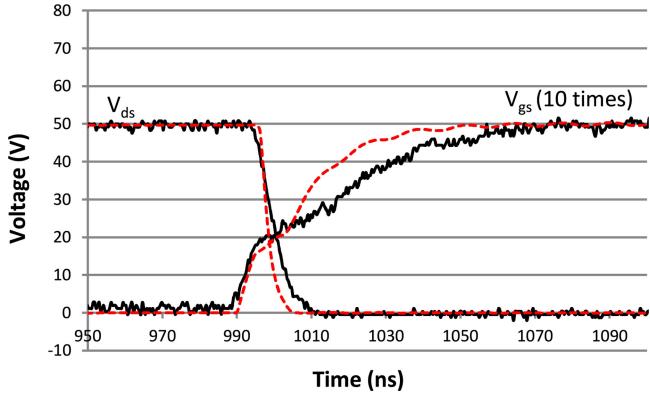


Fig. 28. Simulated (dashed) and experimental (solid) turn-ON transient under inductive switching.

2) *Inductive Switching Validation:* For the inductive switching test a $250 \mu\text{H}$ ferrite EE core inductor is used as an inductive load in the phase-leg tester topology. The inductor is modeled by adding to the main inductance an equivalent series resistance, an equivalent parallel capacitance, as well as an equivalent parallel resistance. By curve fitting, the measured inductor impedance measured with the network analyzer, these parameters of the load inductor can be extracted. Figs. 28 and 29 show the inductive switching transient for the turn-ON and turn-OFF of the

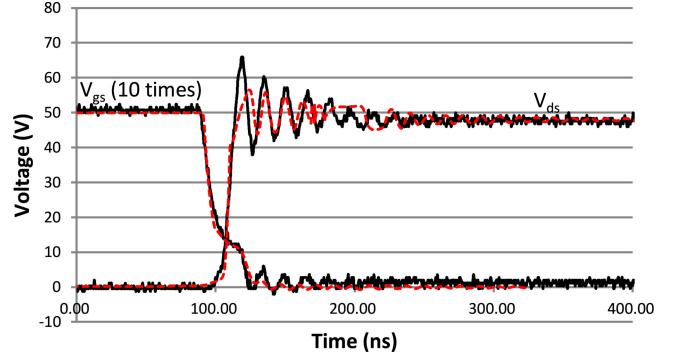


Fig. 29. Simulated (dashed) and experimental (solid) turn-OFF transient under inductive switching.

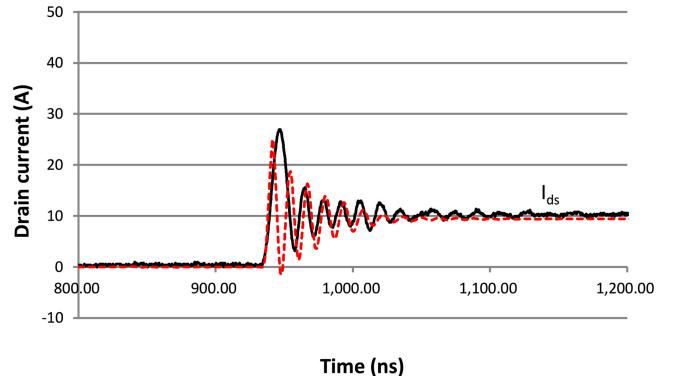


Fig. 30. Simulated (dashed) and experimental (solid) turn-ON current waveforms under inductive switching.

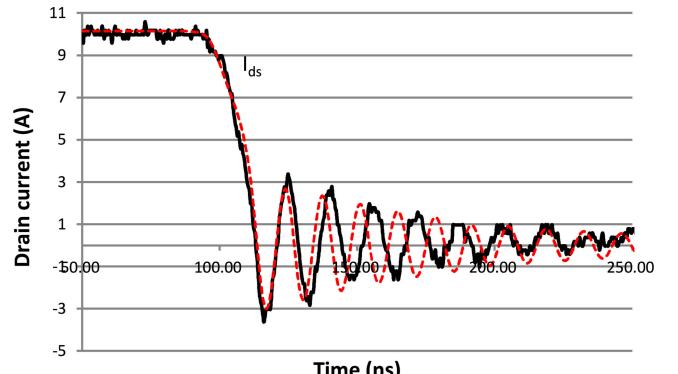
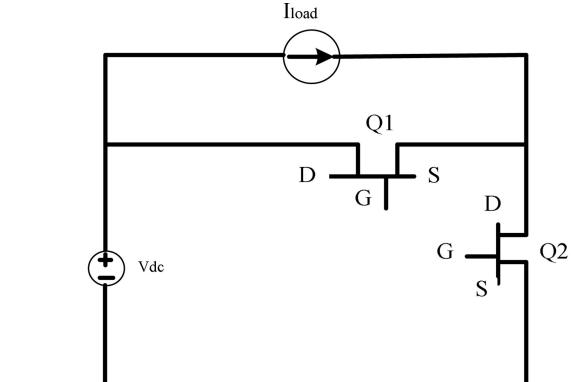


Fig. 31. Simulated (dashed) and experimental (solid) turn-OFF current waveforms under inductive switching.

low-side device under 48 V dc voltage and 10 A load current, with turn-ON resistance 15Ω and turn-OFF resistance 7.5Ω . A good matching between simulation and measurement voltage waveforms is observed.

Figs. 30 and 31 show the drain current waveforms during turn-ON and turn-OFF transient under 10 A inductive switching condition. Both turn-ON and turn-OFF drain current transient comparisons show fairly good agreement. A discrepancy between simulated and experimental results is found in drain



(a)

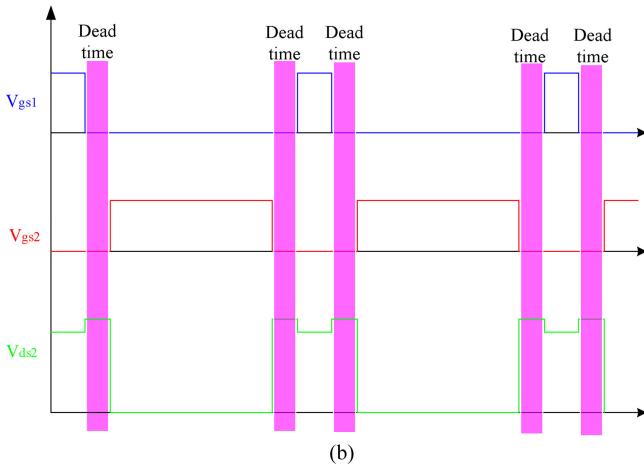


Fig. 32. (a) Double-pulse test schematic. (b) Gate drive signals showing the dead time introduced to prevent cross-conduction.

current ringing shown in Fig. 30. This might be due to the underestimated capacitances C_{gd} and C_{ds} at low voltage bias in device model parameter extraction shown in Figs. 11 and 12. There is a slight difference in ringing resonant frequency between simulated and experimental waveforms in Fig. 31. This is probably caused by the nonlinear capacitance model in the GaN HEMT model or the extracted parasitic inductances.

3) Validation of Third Quadrant Operation: Considering the double-pulse test circuit under inductive load, shown in Fig. 32(a), the top side GaN HEMT Q1 operates as a free-wheeling diode. One main difference between a GaN HEMT and a silicon MOSFET is that the GaN HEMT does not have a built-in body diode. When the GaN HEMT is used as a free-wheeling diode, it actually operates in the third quadrant. With zero gate-source voltage bias, the GaN HEMT has a voltage drop of almost 1.7 V for 10 A current as shown in Fig. 3. Therefore, it is desirable to reduce this conduction loss by turning ON the top HEMT similarly to synchronous rectifier operation for a MOSFET circuit [15]. A short 100 ns dead time between the two gate drive signals is introduced to avoid cross-conduction, as shown in Fig. 32(b).

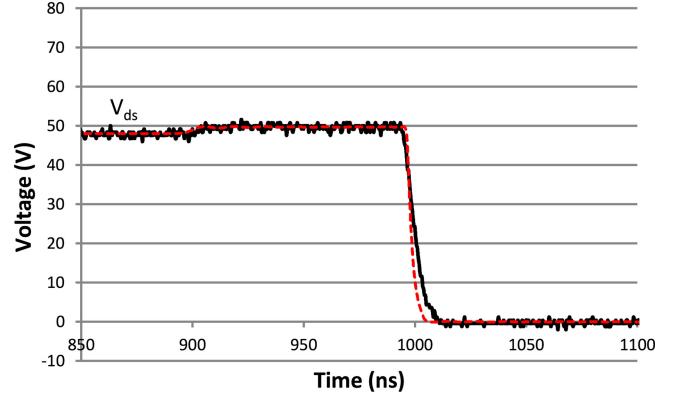


Fig. 33. Comparison of simulated (dashed) and experimental (solid) drain-source voltage waveforms of Q2 at turn-ON transition.

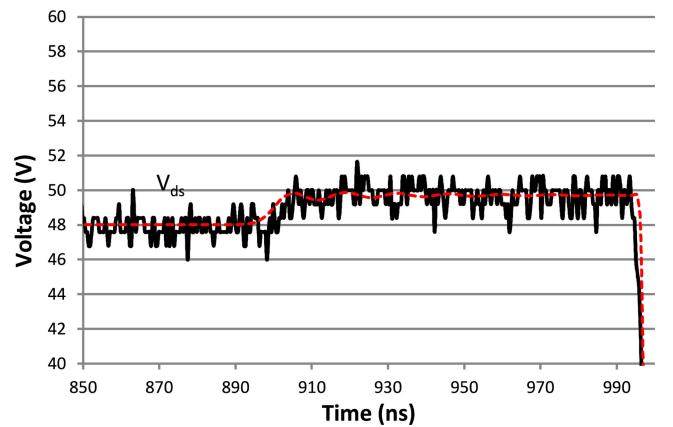


Fig. 34. Comparison of simulated (dashed) and experimental (solid) drain-source voltage waveforms of Q2 during dead time (zoom-in of prior figure).

Fig. 33 shows the drain-source voltage of the Q2 switch at turn-ON. From the figure it can be seen that the drain-source voltage increases by about 1.7 V during the 100 ns dead time. This is due to the increased voltage drop across switch Q1 during the dead time. Fig. 34 shows a zoom-in of the voltage during the dead time interval. Note that the simulation captures this effect and shows excellent agreement with the experiment.

V. CONCLUSION

In this paper, a simple and accurate circuit-simulator compact model for a normally off GaN HEMT device is developed. The model parameters can be easily extracted from static I - V characteristics and C - V characteristics. This model captures reverse channel conduction, which is a very important feature for circuit designers. To the authors' knowledge, this is the first GaN HEMT model that describes the complete static I - V characteristics for power electronics applications. A parameter extraction method is provided to allow easy extraction of model parameters using static I - V characteristics and C - V characteristics. The device model is validated under static conditions over a wide temperature range of 25 to 125°C. A double-pulse test-bench is built to test the switching behavior of GaN HEMT. In

order to simulate the parasitic ringing during very fast switching transient, gate-to-source driving loop and drain-to-source main switching loop parasitic elements of the PCB layout are extracted using a 3-D impedance extraction program. The extracted parameters are used with the GaN HEMT device models for resistive and inductive hard switching simulations in Pspice. The simulation results are compared with experimental results. The comparison shows good matching between simulated and experimental results under both resistive and inductive switching. The dynamic performance of the GaN HEMT in its reverse conduction region is also verified. However, some future work can be done to improve the proposed GaN HEMT model, such as dynamic $R_{ds(on)}$, which is not captured in this model.

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