

FABRICATION, MODELING AND
CHARACTERIZATION OF GaN HEMTs,
AND DESIGN OF HIGH POWER MMIC
AMPLIFIERS

A THESIS
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL AND
ELECTRONICS ENGINEERING
AND THE INSTITUTE OF ENGINEERING AND SCIENCES
OF BILKENT UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

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November 2009

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ABSTRACT

FABRICATION, MODELING AND
CHARACTERIZATION OF GaN HEMTs, AND DESIGN
OF HIGH POWER MMIC AMPLIFIERS

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November 2009

High power and high frequency requirements in advanced telecommunication systems become more stringent as faster and higher capacity wireless data transfer over long distances is getting a common need for both military and commercial applications. Present mature semiconductor technologies have already reached their performance limits in responding next generation needs of high power modules. Under these circumstances, further improvements seem to be possible via introducing more capable technology. GaN HEMT device technology promises high power performance in microwave and millimeter-wave regimes at least an order of magnitude better than any other current counterparts. Research and development processes of this technology require deep understanding of theoretical fundamentals of HEMT device formation and should be supported by efficient epitaxial wafer growth and microfabrication facilities, and accurate large-signal nonlinear modeling capability. After all, GaN HEMT technology can be transformed to real applications of monolithic microwave integrated circuit (MMIC) power amplifiers (PAs).

This work can be separated into three main parts. In the first part, we introduced bottom up approach to the GaN HEMT technology starting from GaN material properties, semiconductor physics and design of GaN HEMT devices, and MOCVD growth and characterization, completing with fabrication

processes and large-signal nonlinear modeling issues of the active devices. 2DEG sheet carrier concentrations in the order of $1 \times 10^{13} \text{ cm}^{-2}$ and electron mobility values between 1500-2000 $\text{cm}^2/\text{V}\cdot\text{s}$ are obtained from our GaN HEMT epiwafers. Furthermore, 900mA/mm of maximum drain current density, 32GHz of f_T , and 40 GHz of f_{\max} are achieved from a fabricated 6x150um GaN HEMT device. Large-signal nonlinear modeling is applied successfully for a 4x200um device with 1um gate length. In the second part, this model is used as a basis for two MMIC PA designs have center frequency of 2GHz and coplanar wave guide passive elements. ~2W and ~4W output power levels and ~42% and ~35% PAE values are generated from these MMIC PAs at 1dB compression point, respectively. In the final part, we applied our MMIC PA design experiences to a GaAs pHEMT process of UMS foundry. We introduced two-stage balanced PA topology in order to achieve wideband and high power response at the output. Aimed frequency range is 18-22GHz. According to the simulation results, output power of ~2W is obtained with 31%-35% PAE in this frequency band. S-parameter measurement data are quite in agreement with simulation results, even better. CW power measurement results are subjected to 1-2dB degradation in output power levels compared to HB simulation results since the design kit we used contains pulsed measurement based transistor models. The measurements results proved the efficiency and correctness of our design.

Keywords: GaN HEMT, MMIC PA design, MOCVD growth, microfabrication, large-signal nonlinear modeling, K-band balanced MMIC PA design, GaAs pHEMT.

ÖZET

GaN HEMT YAPILARININ ÜRETİMİ, MODELLENMESİ VE ÖLÇÜMÜ, VE YÜKSEK GÜÇLÜ MMIC YÜKSELTEÇLERİN TASARIMI

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Kasım 2009

Daha hızlı ve daha yüksek kapasiteli uzun mesafe kablosuz veri iletimi, askeri ve sivil uygulamalarda yaygın bir ihtiyaç haline geldikçe; ileri düzey telekomunikasyon sistemlerindeki yüksek güç ve yüksek frekans gereksinimleri çok daha zor ulaşılabilir hale gelmiştir. Günümüzün gelişimini tamamlamış yarıiletken teknolojileri, yüksek güç birimlerinde belirlenen ihtiyaçları karşılama noktasında kendi limitlerine ulaşmış durumdadır. Bu koşullarda, bahsedilen sorunların çözümü ve daha ileri hedeflerin gerçekleştirilmesi ancak daha yüksek kapasiteli bir teknoloji aracılığı ile mümkün görülmektedir. GaN HEMT aygit teknolojisi mikrodalga ve milimetre dalga frekanslarında diğer eşdeğer teknolojilere kıyasla en az 10 kat daha fazla çıkış güç performansı vaadetmektedir. Bu teknolojinin araştırma geliştirme süreci, HEMT aygit oluşumu altında yatan fiziksel prensiplere çok iyi derecede hakim olmayı gerektirmektedir; yine bu sürecin, elverişli epitaksiyel yapı büyütme ve mikrofabrikasyon ekipmanları, ve yüksek doğruluk derecesinde büyük-işaret modelleme becerileri ile desteklenmesi gerekmektedir. Bu şartlar yerine getirilip GaN HEMT teknolojisi oluşturulduktan sonra MMIC güç yükselteç uygulamaları gerçekleştirilebilir.

Bu çalışma üç ana başlık altında toplanabilir. İlk kısımda, GaN malzeme özellikleri, GaN HEMT aygitların yarıiletken fiziği ve epitaksiyel tasarımlı,

MOCVD büyütme ve karakterizasyonu, mikrofabrikasyon adımları ve büyük işaret modelleme konuları ele alınarak, GaN HEMT teknolojisine en temelden başlayan ve sonuç olarak modeli çıkarılmış aktif aygit noktasına kadar inceleyen bir yaklaşım ortaya konmuştur. GaN HEMT epitaksiyal yapılarımıza tipik olarak, iki boyutlu elektron gazı (2DEG) taşıyıcı yoğunluğu $1 \times 10^{13} \text{ cm}^{-2}$ mertebesinde ve elektron mobilitesi değerleri 1500 ila 2000 $\text{cm}^2/\text{V}\cdot\text{s}$ arasında elde edilmiştir. Fabrikasyonu tamamlanmış 6x150um'luk bir GaN HEMT aygitında, 900mA/mm maksimum drain akım yoğunluğu, 32GHz f_T , ve 40GHz f_{max} değerlerine ulaşılmıştır. Kapı uzunluğu 1um olan 4x200um'luk bir aygitin büyük-işaret modeli başarılı bir şekilde elde edilmiştir. İkinci kısımda, çıkarılan bu model, merkez frekansı 2GHz olan ve coplanar dalga kılavuzu yapısında pasif elemanlar içeren iki çeşit MMIC güç yükselteci tasarımında kullanılmıştır. Bu tasarımlarda 1dB kompresyon noktasında sırasıyla, ~2W ve ~4W çıkış gücü, ve ~%42 ve ~%35 güç kataklı verim (PAE) değerleri oluşturulmuştur. Son kısımda, tasarım tecrübelerimizi UMS firmasının GaAs pHEMT tasarım kitini kullanarak uygulamaya geçirdik. Hedeflenen geniş bant (18-22GHz) ve yüksek güç kapasitesine ulaşabilmek için iki aşamalı dengeli güç yükselteç topolojisi kullanılmıştır. Simülasyon sonuçlarına göre bu frekans bandında, yaklaşık 2W çıkış gücü ve %31 ila %35 arasında değişen PAE değerleri elde edilmiştir. Küçük işaret ölçümleri simülasyonlarla oldukça uyum içerisinde çıkmış hatta daha iyi sonuçlar vermiştir. CW çıkış gücü ölçüm sonuçları HB simülasyon sonuçlarının 1-2dB civarında altında kalmıştır. Bu durumun nedeni ise kullanılan tasarım kitinin atmalı ölçümlere dayalı transistor modelleri içermesidir. Ölçümler sonucunda yapılan MMIC PA tasarımının etkinliği ve doğruluğu ortaya konmuştur.

Anahtar kelimeler: GaN HEMT, MMIC PA tasarımı, MOCVD büyütme, mikrofabrikasyon, büyük-işaret modelleme, K-bant dengeli MMIC PA tasarımı, GaAs pHEMT.

Acknowledgements

I would like to thank my supervisor Prof. Ekmel Özbay, for his great support and encouragement during the course of this work. It was an honor and a remarkable experience to participate in various advanced projects under his invaluable guidance.

I would also like to express my deepest gratitude to Prof. Abdullah Atalar and Dr. Tarik Reyhan for their invaluable comments and advices on my MMIC PA designs. I learned a lot from their immense experiences. I am also grateful to Assoc. Prof. Oğuz Gülsen for reviewing this thesis.

I am thankful to Mustafa Öztürk, Başar Bölükbaş, Özgür Kelekçi, Bayram Bütin, Kamil Bora Alıcı, and other NANOTAM and BilUzay members for their generous helps and favorable discussions which form the critical milestones of this work.

Financial support of The Scientific and Technological Research Council of Turkey (TÜBİTAK) related to the National Scholarship Programme for MSc Students is cordially acknowledged.

Finally, my very special thanks belong to my sweetheart, my future wife, Sevgi, for making my life meaningful and enjoyable. Without her deep understanding, endless discretion and boundless love, I wouldn't be able to take any progress in my challenging studies. I hereby dedicate this labor to my soulmate.

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Chapter 1

Introduction

Invention of the solid-state transistor, in 1947, became a major milestone in evolution of modern electronics since transistor is the inevitable key component of almost all electronic circuits. Later on, semiconductor technology has been increasingly improved to achieve mass production and higher capacity transistors. Today, this trend still continues to have faster, powerful and reliable transistors. To do so, people try to explore and study on new material systems rather than conventional mature technologies.

One might ask why we need better transistors and say just be contented with today's mature technology since it is safe and cheap. There are two answers to this question, first one is logical and second one is technical. Logical one is that we wouldn't able to reach current mature technology if newer materials and technologies were not studied. In order to figure out the technical answer let's consider an explanatory example, that is telecommunication. Need for telecommunication is apparent since without it no one can configure and reestablish needs of humanity in modern world. Usage area of telecommunication covers everything from civil to military applications and transistor quality determines the limits of the telecommunication capacity. If we develop higher performance transistors, we can reduce the product volumes and weights, and built up more energy efficient and more reliable telecommunication systems compared to previous technologies. All these mean that we will achieve safer and cheaper electronic equipments.

Micro-electronics has been evolved with the usage of Germanium (Ge), Silicon (Si), Silicon Germanium (SiGe), and Gallium Arsenide (GaAs) semiconductor materials. In 1979, invention of the GaAs high electron mobility transistors (HEMTs) was very important breakpoint in the near electronics history [1]. Very high sheet carrier densities and mobility values were achieved with this invention.

GaAs HEMT structure is basically formed by a non-doped GaAs channel layer and a highly doped n-type AlGaAs donor-supply layer. This heterojunction of different band-gap materials constitutes a triangular-like quantum well on the GaAs side of the conduction band which allows electrons move freely parallel to the heterojunction plane without any impurity collision. This collection of high mobility electrons inside the quantum well is called two dimensional electron gas (2DEG). Basic epitaxial structure and band diagram of GaAs HEMT are shown in Figure 1.1a and Figure 1.1b, respectively. GaAs HEMT technology has reached its mature state after many improvements in the epitaxial structure and material quality. HEMT structure was transferred to Gallium Nitride (GaN) material system in order to seek for higher performance transistors.

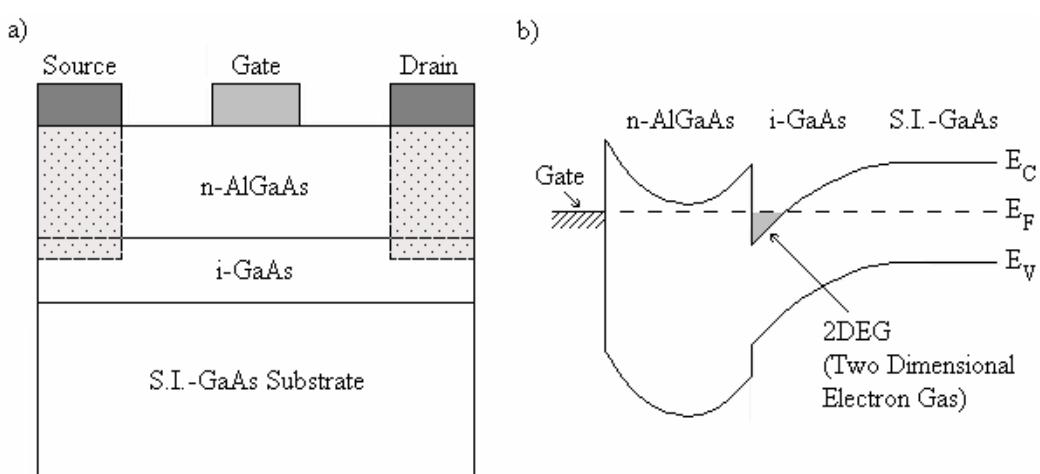


Figure 1.1 Cross section (a) and band diagram (b) of GaAs HEMT Structure.

GaN, which is wide band-gap III-V compound, is the latest semiconductor that has been extensively studied on for high power applications. In 1994, first AlGaN/GaN high electron mobility transistor (HEMT) is demonstrated by Khan *et al.* [2]. Researches on GaN indicate very promising results compared to other semiconductor technologies. This improvement belongs to the superior material properties of AlGaN/GaN material system. GaN HEMT structure is investigated comprehensively throughout next chapter. Table 1.1 lists fundamental application areas of GaN technology.

Field	Application
RF Power Transistors	Wireless Base Stations
High Frequency MMICs	Wireless Broadband Access
Military	Radar/Communication Links
Power Transmission Lines	High Voltage Electronics
Power Conditioning	Mixed-signal Integration
Switches	Plasma Display Panels
High-temperature Sensors	Engine Electronics
Hall Sensors	Automotive Applications
MEMS	Pressure Sensors

Table 1.1 GaN-based micro-electronics applications.

We focused on high power characteristics of transistors in this thesis. GaN is known to be the most suitable semiconductor for high power applications compared to other materials. Some figures-of-merit have been proposed to quantify the performance limits of the materials using their important parameters related to specific applications. Keyes' figure-of-merit describes the thermal limitations for switching behavior of high speed transistors used in integrated circuits. High frequency and high power operation capability of a material is estimated by Johnson's figure of merit. Baliga high-frequency figure of merit

predicts switching power loss of a material at high frequency. Baliga figure-of-merit defines the capacity of having minimum conduction losses in power transistors [3]. Table 1.2 lists Keyes, Johnson, Baliga high-frequency and Baliga figures-of-merit for Si, GaAs, 4H-SiC, 6H-SiC and GaN materials normalized to Si [4]. As can be seen from these figures-of-merit values, GaN proves its promising high power capacity.

Material	Keyes [$\kappa(v_{sat}/\varepsilon_r)^{1/2}$]	Johnson [($E_{cr} \cdot v_{sat}/\pi$) ²]	Baliga HF [$\mu_n \cdot E_{cr}^2$]	Baliga [$\varepsilon_r \cdot \mu_n \cdot E_{cr}^3$]
Si	1	1	1	1
GaAs	0.45	7.1	10.8	15.6
4H-SiC	4.61	180	22.9	130
6H-SiC	4.68	260	16.9	110
GaN	1.6	760	77.8	650

Table 1.2 Important figures-of-merit for GaAs, 4H-SiC, 6H-SiC and GaN relative to Si.

Growing IC market and increasing demand for stringent electronic circuit specifications pushed researchers to develop genius, effective and ‘all-in-one’ solution, monolithic microwave integrated circuit (MMIC). In 1975, R. S. Pengelly reported first MMIC which is GaAs FET based low noise amplifier [5]. As the name implies MMICs contain all circuit elements as planar on same substrate without any external interconnections and bonds. This nature of MMICs allows operation of higher frequencies with lower losses and makes it more feasible and reliable compared to previous hybrid technology. In terms of simple integrity to the outer electrical environment, MMICs are internally matched to 50 Ohm in general. Today, MMICs are the fundamental components of the microwave electronic systems e.g. cell phones, WiMAX applications, and satellite transceivers.

In this work, we pursued the steps of achieving MMIC power amplifiers from bare transistor investigation stage to extensive MMIC design phase. Firstly, GaN HEMT epitaxial structure was designed and grown using metal organic chemical vapor deposition (MOCVD) system. At next stage, transistor layout was defined and fabrication was carried out on epiwafers. Fabricated samples were characterized and selected to be modeled. Since we are interested in high power characteristics, we need nonlinear large signal modeling of transistors. For this purpose we used TOPAS software of IMST GmbH [6]. After obtaining the model of our GaN HEMTs, we designed 2W and 4W coplanar MMIC power amplifiers at 2GHz. Coplanar capacitors, inductors, transmission lines, and junctions were modeled using COPLAN software (from IMST) that is compatible with Advanced Design Software (ADS) [7]. In order to gain further experience in MMIC design at higher frequencies, we used UMS foundry service and designed K-band GaAs pHEMT MMIC balanced power amplifier.

Chapter 2 gives the background information on GaN HEMTs. First, GaN material properties and their influence on high power characteristics of GaN HEMTs are described. Then, principle of GaN HEMTs is explained including theory of 2DEG formation. Next, epitaxial structure of GaN HEMT is investigated. Finally, second chapter concludes with the illustration of MOCVD growth details of GaN HEMT structure together with data taken from MOCVD system, and characterization results of grown wafers.

Chapter 3 deals with fabrication technology and characterization of GaN HEMTs. First, mask design issue is covered. Then, lithography and metallization techniques which we have used in our fabrication process are explained. Next, GaN HEMT fabrication process is described step by step, namely, mesa etching, Ohmic contact metallization, Ohmic contact annealing, gate metallization using e-beam lithography system, SiN passivation, air-bridge post, seed layer of electroplating, air-bridge metallization, and seed layer

removal steps. This chapter concludes with the DC and RF characterization results of the fabricated GaN HEMT devices.

Chapter 4 starts with describing small signal linear modeling of the HEMT devices, and then continues with representing nonlinear large-signal modeling techniques i.e. physical models, analytical models and table-based models. Next, modeling of GaN HEMTs using TOPAS software (IMST GmbH) is explained. Nonlinear large signal model extraction from S-parameter measurements at multi-bias points is described in detail. Comparison of extracted model and measurement is given and accuracy of the model is discussed.

Chapter 5 contains detailed work on coplanar MMIC power amplifier design at 2GHz using our own GaN HEMT model and COPLAN software of IMST GmbH. Description of design methodology is given for two different designs. COPLAN software is investigated deeply in order to understand physical background and use it in more efficient way. Design steps including load pull simulations, DC bias circuits, input & output matching networks are explained. At the end of fifth chapter, simulation results of the designs are shown and commented.

Chapter 6 is devoted to K-band GaAs pHEMT MMIC balanced power amplifier design using UMS foundry design kit. First, information about the UMS foundry service is given. Then, balanced design methodology is introduced. Design details and critical considerations are explained. Wideband matching techniques are discussed. Electromagnetic coupling effect is investigated throughout the circuit especially for Lange couplers. 2.5D and 3D EM simulation results of critical parts are given. Simulation results of whole circuit are illustrated. Next, measurement board design for our MMIC is explained. Finally, on wafer measurement data are compared with simulation results.

Chapter 7 summarizes works done and results obtained in the thesis. Future work vision towards more powerful, efficient and reliable transistors and power amplifiers is described.

Chapter 2

GaN High Electron Mobility Transistors

This chapter provides general physical understanding of GaN high electron mobility transistors (HEMTs) starting from material properties of GaN. Then, principle of GaN HEMT operation including fundamental of two dimensional electron gas (2DEG) formation is given. Next, epitaxial structure behind the HEMT device is examined. Further, MOCVD growth of GaN HEMTs is described and characterization results of epiwafer are illustrated.

2.1 GaN Material Properties

Over the last decades, GaN has been very promising research topic and candidate for high power applications due to its superior material properties over conventional ones. Important material properties of GaN and some other semiconductors are listed in Table 2.1. GaN is a wide band-gap material so that it can stand at extreme environmental conditions such as high temperatures and voltages [8], [9], [10], [11]. Radiation hardness of the GaN is comparable with SiC and higher than GaAs [12]. This fact makes GaN very attractive for space applications. Thermal conductivity of GaN is significantly higher than that of GaAs. This is another measure that makes GaN more suitable for high power operation needs compared to GaAs power devices. Furthermore, saturated

electron drift velocity of GaN is higher than that of Si, SiC and GaAs. This puts GaN into better position for high saturation current and high frequency applications compared to its competitors.

Property	Si	GaAs	4H-SiC	6H-SiC	GaN
Bandgap, (eV)	1.12	1.42	3.27	3.02	3.4
Breakdown Electric Field, (MV/cm)	0.3	0.4	3	3.2	3.3
Relative dielectric constant	11.7	12.9	9.7	9.66	8.9
Thermal Conductivity κ , (W/cm·K)	1.3	0.55	3.7	4.9	1.3
Electron Mobility μ_n , (cm ² /V·s)	1400	8500	900	400	1000
Hole Mobility, (cm ² /V·s)	450	400	120	90	200
Saturated Electron Drift Velocity, ($\times 10^7$ cm/s)	1	1	2	2	2.5
Melting Point, K	1415	1238	2827		2791

Table 2.1 Important material properties of selected semiconductors [13], [14], [15].

On-resistance of an active device defines conduction losses during on-state operation. Thus, it is very important parameter for power capacity and efficiency criteria. On-resistance of vertical device structure with a uniform doping profile is represented as follows [16];

$$R_{on} = 4V_{br}^2 / \epsilon_r \mu_n E_{cr}^3 , \quad (2.1)$$

where V_{br} is the breakdown voltage, ϵ_r is the relative permittivity, μ_n is the electron mobility and E_{cr} is the critical electric field for breakdown. This equation gives 5 times lower on-resistance value for GaN compared to 4H-SiC considering same breakdown voltage. Actually, as an active device, GaN is used in HEMT structure that has lateral device configuration. On-resistance formula which is driven for GaN HEMT structure is [17];

$$R_{on} = V_{br}^2 / \xi \mu_n E_{cr} (E_{cr}^2 - E_p^2), \quad (2.2)$$

where E_p is the net polarization field in the GaN HEMT structure and ξ is the specific constant with a unit of (F/cm) which relates the critical electric field and sheet electron carrier density of the device channel. Revised formula for GaN HEMT results in 50 times better on-resistance values compared to SiC devices for the same breakdown voltage.

There are three available crystal structures for compound semiconductors GaN and its ternary alloys AlGaN and InGaN, which are wurtzite, zinc-blende and rock salt structures. In this work, we deal with wurtzite structure since it is thermodynamically more stable than other two structures and have strong polarization properties [18]. The GaN wurtzite structure can be grown with two polarities along the c-axis depending on the atomic order through growth direction, namely, Ga-face and N-face [19]. They have different piezoelectric properties and surface stability [20]. In Figure 2.1 two different growth directions of wurtzite crystal structure for GaN is shown.

GaN is very stiff material that makes it mechanically easy to handle. It is also electrically stable at very high temperatures up to 1200 °C under atmospheric pressures [21]. In addition, Ga-face GaN crystal has very robust chemical inertness against strong acids and bases [22].

Nitrogen is the smallest and the most electronegative Group V element. High electro-negativity of nitrogen makes III-nitrides special compared to other III-V

materials, i.e. strong ionicity of metal-nitrogen covalent bond causes microscopic polarization. This microscopic polarization results in a macroscopic polarization if the crystal has no inversion symmetry.

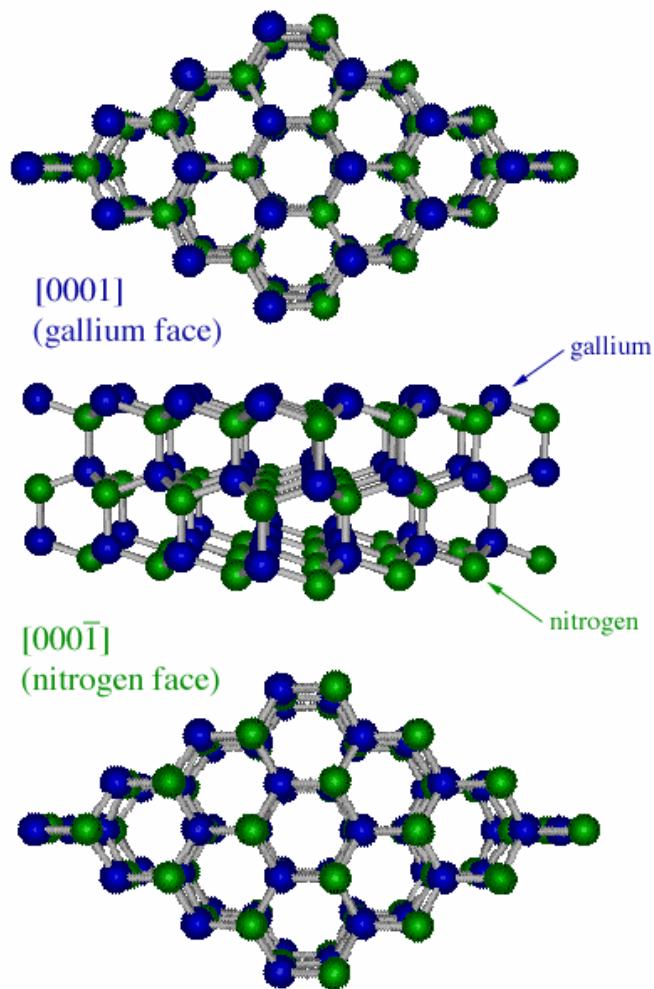


Figure 2.1 Schematic illustration of GaN wurtzite crystal structure. The blue and green spheres indicate Ga and N, respectively. GaN with Ga-face polarity is shown on the top and GaN with N-face polarity is shown on the bottom of the figure [23].

Hexagonal wurtzite III-nitride crystal structure has no inversion symmetry and therefore it has strong macroscopic polarization along growth direction. This kind of polarization occurrence is called spontaneous polarization because

no external intervention takes place on the structure hence crystal lattice stays in equilibrium position [24]. In Figure 2.2, spontaneous polarization in GaN and AlGaN compound semiconductors is shown for [0001] growth direction, which is also the common direction for MOCVD growths. This direction is also called Ga-face polarity for GaN as mentioned before.

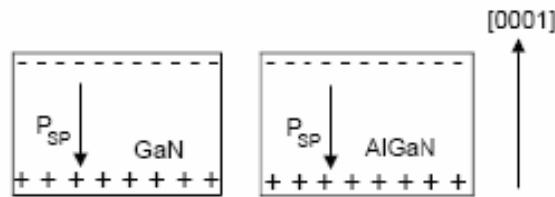


Figure 2.2 Spontaneous polarization fields and sheet charges occurred in GaN and AlGaN grown in [0001] direction.

As well as the ionicity of the crystal lattice, deviation from the ideal crystal lattice parameters also affects the magnitude of spontaneous polarization. Equilibrium lattice parameters for wurtzite crystal structure parallel and perpendicular to growth direction are called c_0 and a_0 , respectively. The c_0/a_0 ratio and the spontaneous polarization values of GaN and AlN are given in Table 2.2 [24], [25], [26], [27], [28], [29], [30]. Increment in discrepancy of c_0/a_0 ratio from the ideal value 1.633 causes enhancement in spontaneous polarization.

parameter	ideal	GaN	AlN
c_0/a_0	1.633	1.6266	1.6009
P_{SP} , (C/m^2)	-	-0.029	-0.081

Table 2.2 c_0/a_0 ratio and spontaneous polarization values of wurtzite crystal GaN and AlN.

In addition to the natural non-ideality of the crystal lattice, external interventions have also effect on lattice parameters. Heterostructure formation is a good practical example to this kind of change in crystal organization. Due to the lattice mismatch between the two materials, strain is occurred at the

heterostructure interface. Consequently, axial stress takes place on the plane of intersection. This stress is absorbed via the change in the lattice parameters a_0 and c_0 of the crystal structures. Quite similarly to the spontaneous polarization case new equilibrium state causes alteration in polarization strength in the materials. Aforementioned type of change in polarization is called piezoelectric polarization [24].

Let's consider wurtzite AlGaN/GaN heterostructure grown in [0001] direction. Since lattice parameters of AlGaN compound are slightly smaller than those of GaN, AlGaN layer is under tensile stress and inversely, GaN layer is under compressive stress. The tensile stress on AlGaN layer decreases c_0/a_0 ratio and therefore generates a piezoelectric polarization in AlGaN layer which has same direction with the spontaneous polarization as shown in Figure 2.3. For the case of thick enough GaN layer, the compressive stress is relaxed and absorbed by the whole GaN structure. As a result, no piezoelectric effects are observed in GaN buffer.

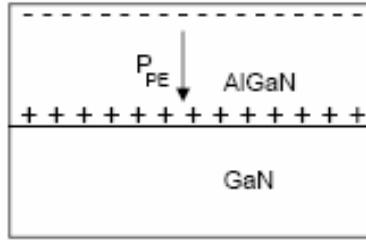


Figure 2.3 Piezoelectric polarization field and sheet charges in AlGaN layer.

Considering the piezoelectric effects, we ended up with higher polarization field in the AlGaN layer than in the thick GaN layer. Thus electric field becomes severely discontinuous at the heterostructure interface which leads to a very high positive sheet charge density at AlGaN side as shown in Figure 2.4. Owing to surface donor-like traps [31], [32], [37], piezoelectric polarization brings 2DEG idea, which is a sheet of electrons at the GaN side of the interface, into existence. Calculation of the density of this negative charge accumulation and more detailed work will be carried on under next subsection.

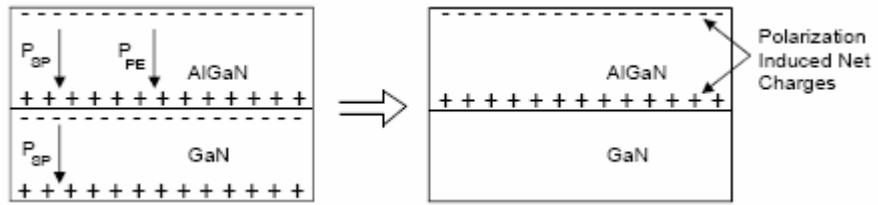


Figure 2.4 Illustration of piezoelectric and spontaneous polarization fields and sheet charges in AlGaN/GaN structure.

2.2 Principle of GaN HEMTs

For many years, active device need in microwave applications has been fulfilled by the metal-semiconductor field effect transistor (MESFET) technology; however, MESFET has already reached its performance limits. Higher capacity active devices are under investigation and HEMT is the current promising candidate due to its novel electron transport properties.

The HEMT is basically based on MESFET operation principle. It has three terminals, drain (D), source (S), and gate (G). Basic GaN HEMT schematic is illustrated in Figure 2.5. There is a conducting channel called 2DEG between drain and source contacts. The channel density is controlled by applied voltage on gate. Thus, HEMT acts as a voltage controlled current source in principle.

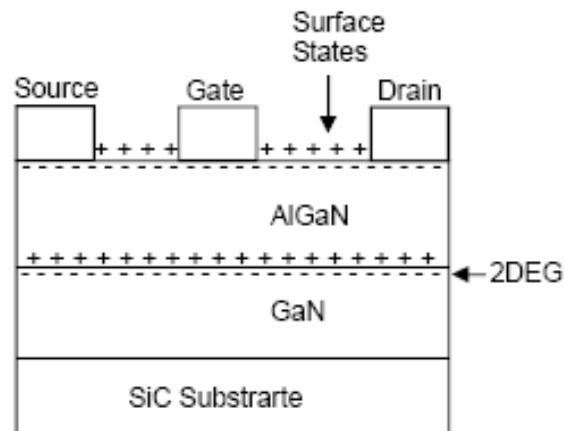


Figure 2.5 Basic GaN HEMT structure.

We have already investigated the properties of AlGaN/GaN heterostructure in previous subsection. Here, we will focus on derivation of 2DEG density. To do so, we need to know the physical properties of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ compound as a function of its aluminum (Al) mole fraction (x). Lattice parameters, piezoelectric constants, elasticity constants, and spontaneous polarization for GaN and AlN are given in Table 2.3 [33], [34]. As a first order approximation, the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ physical properties can be linearly extrapolated using corresponding values for GaN and AlN.

Parameter	GaN	AlN
a_0 , (\AA)	3.189	3.112
e_{31} , (C/m^2)	-0.49	-0.60
e_{33} , (C/m^2)	0.73	1.46
C_{13} , (GPa)	103	108
C_{33} , (GPa)	405	373
P_{SP} , (C/m^2)	-0.029	-0.081

Table 2.3 Required material properties of GaN and AlN for 2DEG calculations.

Let's consider there is no external electric field applied on the AlGaN/GaN heterostructure. The total macroscopic polarization (\mathbf{P}) of the system is represented by the addition of spontaneous polarization (\mathbf{P}_{SP}) and piezoelectric polarization (\mathbf{P}_{PE}). Since all polarization vectors are directed to z-axis for our case. We do not need to use vector notation any more. For AlGaN layer total macroscopic polarization is given by

$$\mathbf{P} = \mathbf{P}_{\text{SP}} + \mathbf{P}_{\text{PE}} . \quad (2.3)$$

As we explained earlier, thick GaN layer contains only spontaneous polarization. Based on Gauss' law, discontinuity of polarization at the interface causes a bound sheet charge density (σ_P) given by;

$$\sigma_P = P_{\text{PE,AlGaN}} + P_{\text{SP,AlGaN}} - P_{\text{SP,GaN}} . \quad (2.4)$$

Next step is the derivation of the piezoelectric polarization expression in order to calculate the sheet charge density. For our special case, piezoelectric polarization relationship is as follows;

$$P_{\text{PE}} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) . \quad (2.5)$$

where e_{33} (z-direction) and e_{31} (x and y directions) are piezoelectric constants, $\epsilon_z = (c-c_0)/c_0$ and $\epsilon_x = \epsilon_y = (a-a_0)/a_0$ are the strain along z-axis and the isotropic in-plane strain, respectively. In wurtzite crystal structure, the two strain expressions are related by elastic constants, C_{13} and C_{33} . This relation is given by;

$$\epsilon_z = -2 \epsilon_{x,y} \frac{C_{13}}{C_{33}} . \quad (2.6)$$

Using equations (2.5) and (2.6) the piezoelectric polarization in AlGaN layer can be expressed by;

$$P_{\text{PE}} = 2 \frac{a - a_0}{a_0} \left(e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right) . \quad (2.7)$$

Combining equations (2.4) and (2.7) the polarization induced sheet charge density σ_P at $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ interface can be calculated by;

$$|\sigma_P| = \left| 2 \frac{a - a_0}{a_0} \left\{ e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right\} + P_{\text{SP,AlGaN}} - P_{\text{SP,GaN}} \right| . \quad (2.8)$$

Calculations show that the sheet charge density increases with the increment of Al composition rate of AlGaN [35]. On the other hand, grown material quality puts practical limit to the Al mole fraction (x). According to equation (2.8), AlGaN/GaN heterostructure generates 10 times higher sheet charge

density compared to other counterparts [36], which promotes higher HEMT device performances.

Together with polarization properties, band offset at conduction band makes AlGaN/GaN heterostructure special for high current and high power microwave applications. After reaching a critical thickness of undoped AlGaN layer, aforementioned discontinuity at the conduction band forces energy level to fall below the Fermi level and forms a triangular-like quantum well at the AlGaN/GaN heterojunction interface as shown below in Figure 2.6.

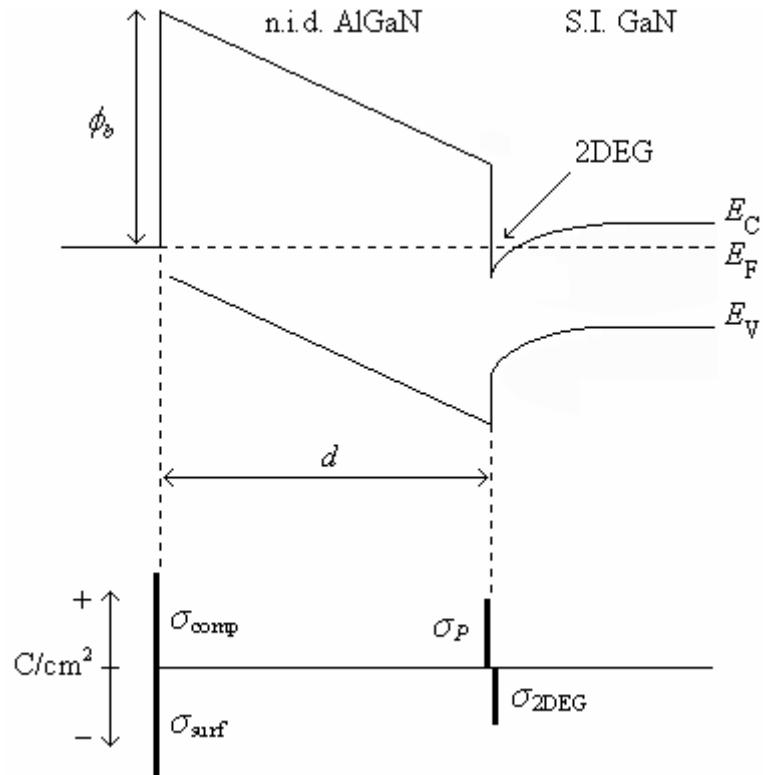


Figure 2.6 Band diagram of the AlGaN/GaN heterostructure and accumulated sheet charges in the system [35].

We can express this critical thickness of AlGaN layer using a straightforward solution of the Poisson equation neglecting the width of the Fermi distribution as follows;

$$d_{cr} = (E_D - \Delta E_C) \cdot \left(\frac{\epsilon_{AlGaN}}{e\sigma_P} \right), \quad (2.9)$$

which depends on the surface donor energy E_D and the band offset of the AlGaN/GaN heterojunction ΔE_C as well as the polarization induced sheet charge density σ_P and the dielectric constant of AlGaN ϵ_{AlGaN} . This equation has been validated by experimental studies. 35 Å critical thickness for the AlGaN layer and ~1.65 eV surface donor energy level below the conduction band was reported [37].

Beyond a critical thickness of AlGaN layer polarization fields become high enough to ionize surface donor states. These ionized electrons move toward the AlGaN/GaN interface under the effect of internal fields and fill the triangular like quantum well. This negative charge assembled at the interface called *two-dimensional electron gas*, 2DEG. Accordingly, the ionized surface donor states form a positive charge σ_{comp} at the surface of AlGaN layer as shown in Figure 2.6, which tends to compensate the negative sheet charge σ_{surf} generated due polarization induced sheet charge σ_P .

A simple semi-classical electrostatic analysis assuming charge neutrality in order to hold between the sheet charge densities at the surface and the interface, leads to the following analytical expression (2.10) for the 2DEG sheet carrier concentration (n_s) as a function of the Al alloy composition x of the AlGaN barrier layer;

$$n_s(x) = \frac{\sigma_P(x)}{e} - \left(\frac{\epsilon_0 \epsilon_{AlGaN}(x)}{de^2} \right) (e\phi_b(x) + E_F - \Delta E_c(x)), \quad (2.10)$$

where σ_P is the polarization induced sheet charge density at the interface of AlGaN/GaN heterojunction, e is the electron charge, ϵ_0 is the permittivity of free space, ϵ_{AlGaN} is the relative dielectric constant and d is the thickness of the AlGaN barrier layer, ϕ_b is the Schottky barrier height, E_F is the Fermi level at

the heterojunction with respect to the GaN conduction band edge, and finally ΔE_c is the conduction band offset at the AlGaN/GaN interface.

The most accurate and consistent model for 2DEG formation is the surface donor model [37] which asserts that surface donors are the source of electrons in the 2DEG channel as we explained before. Using critical distance d_{cr} expression (2.9) which is based on surface donor model we can write down n_s in close form as follows;

$$n_s = \frac{\sigma_p}{e} \cdot (1 - d_{cr}/d) . \quad (2.11)$$

According to surface donor model, formation of 2DEG and the effect of critical thickness are summarized in Figure 2.7. We do not observe 2DEG formation up to the critical thickness of AlGaN layer as shown in Figure 2.7. (a). On the other hand, 2DEG formation occurs for AlGaN layer thickness higher than d_{cr} as illustrated in Figure 2.7. (b).

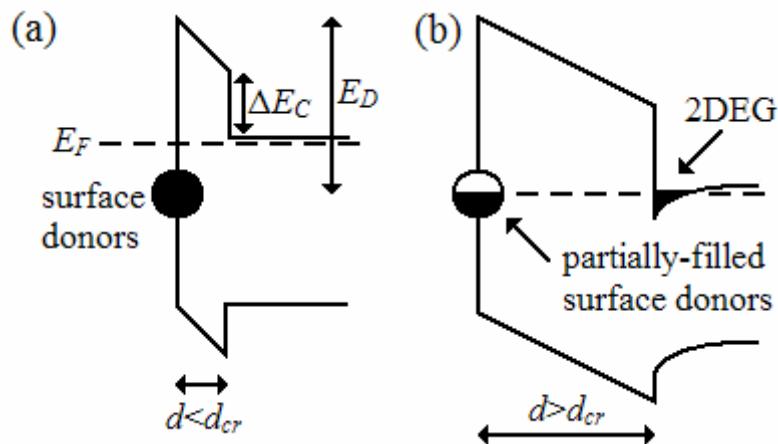


Figure 2.7 Illustration of surface donor model [37].

Conductivity of the 2DEG channel is crucial parameter for HEMT operation, which depends on sheet carrier concentration and mobility of the electrons in the channel. The conductivity σ can be expressed by following formula [38];

$$\sigma = e n_s \mu_n , \quad (2.12)$$

where e is the electron charge and μ_n is the mobility of electrons in the channel. There is a trade-off between the sheet carrier concentration and the electron mobility which should be carefully controlled. Increasing n_s deteriorates μ_n since additional scattering mechanisms come into the picture.

Surface quality of the HEMT structure is very important since 2DEG characteristic is based on surface donor-like states, which constitutes the core of the HEMT operation. Surface can be affected by several internal and environmental factors. Epitaxial structure is one of the basic factors that plays important role in determination of surface quality. Through the next subsection we will investigate epitaxial structure steps in detail and search for improvements in order to acquire better material quality.

2.3 Epitaxial Structure

Here, we will examine the epitaxial layer structure layer by layer, from bottom to top. Firstly, we will mention about substrate choices of the GaN HEMT structure. Unfortunately, GaN HEMTs are not grown on GaN substrates since growth of high quality GaN substrate is still under development and very expensive [39]. Although native substrate for GaN is not commonly available to date, several other substrate types are practically used in literature such as sapphire (Al_2O_3), semi-insulating (S.I.) silicon carbide (SiC), and silicon (Si). There is also a new developed substrate type SopSiC (Silicon on poly-crystalline Silicon Carbide) [40].

Sapphire substrate:

Traditionally, sapphire, single crystal Aluminum Oxide (Al_2O_3), is the most commonly used substrate for GaN hetero-epitaxy. At development stage of our GaN HEMT wafer growths we also mostly used sapphire as a substrate.

Sapphire is an interesting choice because it is semi-insulating, it can withstand the required high growth temperatures, and it is relatively cheap (\$40-\$50 for a 2-inch wafer). However, its very low thermal conductivity (0.47 W/cm·K at 300 K), large lattice mismatch (16%), and large thermal expansion coefficient (TEC) mismatch (34%) with the GaN epilayers make it the worst choice for high-power applications. Nevertheless, the power results for GaN HEMTs on sapphire substrates are surprising and are more than 10 times as high as can be achieved by GaAs HEMTs.

Silicon (Si) substrate:

Silicon preserves its importance and is still the most common and widely used semiconductor material for electronics applications. Despite the very large lattice mismatch (17%) and enormous TEC mismatch (56%), the advantages of low substrate cost, excellent availability of large substrate diameters, acceptable thermal conductivity (1.5 W/cm·K at 300 K), and integration possibilities with Si electronics make Si substrates interesting candidate for GaN hetero-epitaxy. Very promising results have been reported in literature for GaN HEMTs on silicon substrate [41], [42], [43], [44].

Silicon Carbide (SiC) substrate:

The high thermal conductivity (3.7-4.5 W/cm·K at 300 K), low lattice mismatch (3.4%), and relatively low TEC mismatch (25%) are the main reasons for the superior material quality of GaN epilayers grown on S.I. SiC compared to those grown on sapphire and silicon. As a consequence, the 2DEG transport properties of GaN epilayers on S.I. SiC are much better and it is very clear that at the moment S.I. SiC is the best substrate choice for GaN HEMT based microwave high-power applications. On the other hand, it is very expensive compared to its competitors (~4000\$ for a 75mm wafer). Increasing demand for high power GaN HEMTs will obviously push market to enhance mass production which in turn pulls down SiC substrate prices. Since we focused on

high-power applications, S.I. 4H-SiC is used as a substrate of our GaN HEMTs in this work.

Silicon on poly-crystalline Silicon Carbide (SopSiC) substrate:

Silicon on poly-crystalline Silicon Carbide substrate structure combines the advantages of Si and SiC materials [40]. Compared to the conventional SiC single crystal approach, this approach offers a larger diameter substrate and a lower cost solution. The SopSiC is expected to show thermal capabilities close to those of polycrystalline SiC. Compared to bulk silicon, this substrate exhibits a major improvement in terms of heat dissipation. SopSiC substrates are fully compatible with the compounds semiconductor device manufacturing. SopSiC material is expected to be the solution to bring low cost approach and high performances necessary for high power and high frequency devices [45], [46], [47].

Nucleation layer:

After completing the substrate types we can move on to the nucleation layer stays between the substrate and GaN buffer layers. Nucleation layer can be made of GaN, AlN, AlGaN or graded AlGaN layers. This layer is required due to the high mismatch in lattice constant and dissimilarity between GaN and the substrate materials which results in low-quality material with high surface roughness. Nucleation layer reduces the density of threading dislocations in the GaN buffer layer. GaN buffer should be highly resistive; nucleation conditions also influence the GaN buffer resistivity.

For different substrate types, different materials are chosen for nucleation layer and they have different optimization values such as growth temperature and thickness. For instance, low temperature GaN or AlN nucleation layers can be used for sapphire and SiC substrate. In Figure 2.8, sample epitaxial structure containing low temperature AlN nucleation layer is shown. In practice, low

temperature GaN is preferable because the large lattice mismatch between the low-temperature AlN nucleation layer and the following GaN buffer layer can cause defect generation.

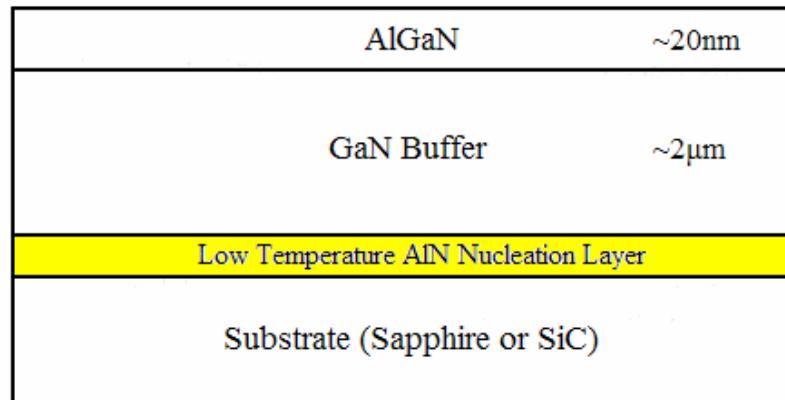


Figure 2.8 Sample epilayer structure with low temperature AlN nucleation layer.

On the other hand, step-graded AlGaN nucleation layer can be used for Si substrates. Compared to single nucleation layer, step-graded structure allows smoother transitions between different lattice dimensions which result in better GaN buffer quality with lower dislocation density.

GaN buffer layer:

In this part, we will examine the GaN buffer layer as the next layer in the structure. In order to achieve optimal device performance it is crucial that the GaN buffer layer is of a very high quality, i.e. low defect density and high resistivity (semi-insulating behavior) to avoid both charge trapping of 2DEG electrons, which causes drain current collapse and hence output power reduction, and high buffer leakage, which makes it very difficult or even impossible to pinch-off a device and achieve a high breakdown voltage. The inability of effectively pinching-off a device also reduces the available current swing and therefore the achievable microwave output power. In addition, buffer

leakage can cause interaction between active devices on the same chip even if they are isolated by mesa structures.

Furthermore, the surface of the GaN buffer layer should be smooth to render a good interface between itself and the AlGaN barrier layer. A smooth and sharp interface is required to obtain a high mobility and good confinement of the 2DEG electrons. Good carrier confinement also enables effective device pinch-off.

Increasing GaN buffer thickness provides improvements including smoother growth fronts (improved interface roughness of the heterostructure), reducing dislocations, and further removal of the active regions of the device from the defective nucleation layers and substrate. 2DEG mobility values also increase with buffer layer thickness due to improvements in the AlGaN/GaN interface quality [48].

Spacer layer:

In the epitaxial design of GaN HEMT structures, there is a thin improvement layer, between GaN buffer layer and AlGaN supply layer, which is called spacer layer. This layer can be made of AlN or non-intentionally doped (n.i.d.) AlGaN usually with the same Al alloy composition as AlGaN supply layer is inserted. Spacer layer strongly decreases Coulomb scattering between the 2DEG electrons and their ionized parent atoms in the supply layer. Hence the mobility of the 2DEG electrons is significantly increased to typical values ranging from 1200 - 2000 cm²/Vs at room temperature (RT).

Thickness of the spacer layer has a critical importance on the 2DEG properties and sheet resistance so it needs to be very well controlled. It is reported that the growth duration of AlN spacer layer is resulted in 10 seconds under approximately 0.5 nm/s growth rate condition, in order to achieve optimum 2DEG mobility and sheet resistance levels [49].

AlGaN supply layer:

AlGaN layer is used to supply sufficient electrons to the 2DEG and it is usually Si-doped. Al alloy concentration and thickness of AlGaN layer affect sheet carrier concentration. As we increase Al alloy concentration, 2DEG density also increases. Moreover, as the thickness of the supply layer increases, 2DEG density increases slower than the previous case.

Therefore, to achieve a high 2DEG density it should be tried to incorporate as much aluminum as possible without causing relaxation of the AlGaN layer. An additional restriction on the maximum thickness of the AlGaN layer is imposed by a very important device structural design concept, which is known as the high-aspect-ratio design concept that puts a limit on the maximum AlGaN thickness.

For microwave high-power applications the most important device figures-of-merit are the unity current gain frequency or cut-off frequency (f_T), and the unity power gain frequency or maximum oscillation frequency (f_{max}). Under the assumptions that all electrons in the 2DEG travel at the saturation velocity and that any intrinsic feedback due to the gate-drain capacitance (C_{gd}) can be neglected, cut-off frequency is inversely proportional to the effective gate length, i.e. including lateral depletion between the gate and drain regions. The aspect ratio in the aforementioned design concept is the ratio of the effective gate length and the distance between the Schottky gate metal and the 2DEG. It has been shown that for good microwave device performance this ratio should not drop below 10. According to this design concept, corresponding thickness is typically around 25nm.

Theoretically, there is also a lower limit for AlGaN supply layer thickness that we have mentioned under previous subsection. Up to the critical thickness there is no formation of 2DEG. Figure 2.7 should be addressed to see that 2DEG

formation begins at the AlGaN/GaN heterostructure interface after surface donor states reach Fermi level.

Cap layer:

In order to reduce gate leakage and increase the Schottky barrier height, thin GaN cap layer can be introduced to the structure. The conduction band profile of HEMT structures with and without a GaN cap is shown in Figure 2.9. The enhanced barrier height increases the flat-band voltage.

Experimental results show that if we use thick cap layer then we will not need surface passivation [50]. Alternatively, in order to accommodate lattice mismatch between AlGaN and GaN, we can use graded AlGaN cap layer instead of GaN. Furthermore, AlGaN can sustain larger electric fields and has higher Schottky barrier than GaN.

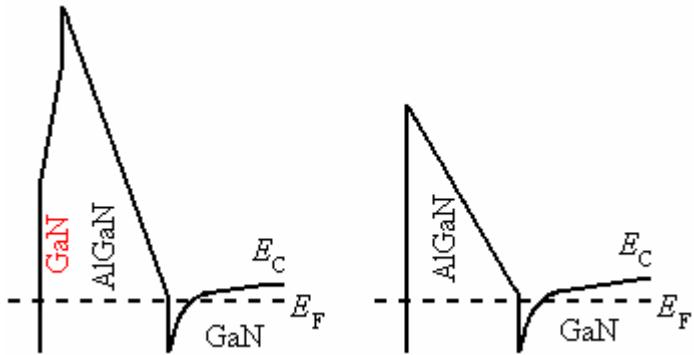


Figure 2.9 Conduction band profiles with and without a GaN cap layer [48].

Current research results introduce novel piezoelectric-induced cap structure consists of a thin GaN/AlN/GaN triple-layer [51], [52]. With this new advancement lower sheet resistance and higher gate-to-drain breakdown voltages could be achieved.

The bottom thin GaN layer in the aforementioned cap structure has a duty of Schottky gate contact formation just like classical AlGaN/GaN HEMTs with GaN cap layer. The thin AlN layer increases 2DEG density by conduction band bending caused by strong polarization-induced electric field between AlN and GaN layers. The top GaN layer is added in order to have a smooth surface morphology and lower sheet resistance.

Surface Passivation layer:

There are several options for surface passivation layer such as Si_3N_4 , SiO_2 , SiON , Sc_2O_3 , MgO , Ni , NiO and Ozone. Among this list, Si_3N_4 is the most commonly used one for passivation. Sample structure of AlGaN/GaN HEMT with SiN passivation layer is shown in Figure 2.10. Proper surface passivation prevents the surface states from being neutralized by trapped electrons and therefore maintains the positive surface charge and prevents the formation of virtual gate. Consequently, better transport properties, higher peak value of transconductance, higher peak drain current, higher gate-to-drain breakdown voltage, reduced DC-RF dispersion, and higher output power density have been achieved using passivation techniques compared to unpassivated devices [53], [54] [55] [56], [57], [58], [59], [60], [61], [62].

On the other hand, passivation technique critically depends on the deposition conditions of the dielectric, as well as on surface cleaning techniques. Care must be taken to reproduce the same surface condition, with varying $\text{Al}_x\text{Ga}_{1-x}\text{N}$ contamination levels resulting from different processing steps, exposure to air, etc. If the passivation process is imperfect, then electrons, leaking from the gate metal under the influence of a large electric field present during high power operation, can get trapped.

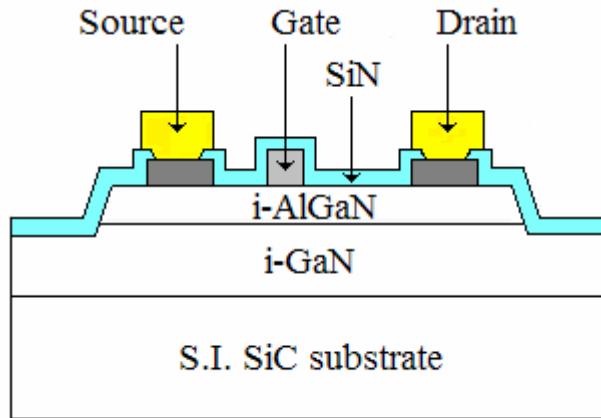


Figure 2.10 Epilayer structure with surface passivation layer of Si_3N_4 .

The AlGaN/GaN HEMT epitaxial design is basically completed up to this point. Every layer in the structure is explained according to the literature works reported. Now, MOCVD growth details will be explained in the next subsection.

2.4 MOCVD Growth

In this subsection, we will mention about epitaxial structure design parameters and MOCVD growth steps of AlGaN/GaN HEMTs on sapphire substrate for two samples labeled as B-1540 and B-1545. MOCVD growths were carried out in Bilkent University Nanotechnology Research Center (NANOTAM) using AIXTRON RF200/4 RF-S MOCVD system which is shown in Figure 2.11. Photograph of the reactor of this MOCVD system is given in Figure 2.12.

As we mentioned before, sapphire has a 16% lattice mismatch with GaN which causes high dislocation density and a 34% thermal expansion coefficient (TEC) mismatch with GaN which is the source of cracks in the epiwafer. Moreover, very low thermal conductivity of the sapphire (0.47 W/cm·K at 300K) requires finely optimized nucleation layer implemented between sapphire substrate and GaN in order to heal the effects of lattice mismatch and TEC

mismatch and provide high resistive and high quality GaN buffer layer with acceptable dislocation density. Besides low thermal conductivity, high stiffness and high chemical and thermal stability of sapphire make it suitable for cleaning at high temperatures (1000 °C-1200 °C) under hydrogen flow. Substrate cleaning is very important pretreatment step before the growth.



Figure 2.11 AIXTRON RF200/4 RF-S MOCVD system.

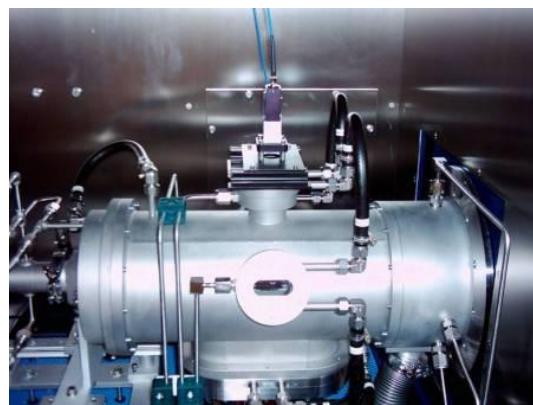


Figure 2.12 Reactor of the MOCVD system in NANOTAM.

Nucleation layer is vital for achieving required surface roughness and 2DEG formation. Optimized nucleation layer and whole epitaxial design structures for B-1540 and B-1545 are given in Figure 2.13.

B-1540	B-1545
GaN cap layer ~ 3 nm	GaN cap layer ~ 3 nm
AlGaN ~ 30 nm	AlGaN ~ 30 nm
AlN interlayer 1-2 nm	AlN interlayer 1-2 nm
GaN Buffer Layer (4) ~ 160 nm	GaN Buffer Layer (4) ~ 160 nm
GaN Buffer Layer (3) ~ 160 nm	GaN Buffer Layer (3) ~ 480 nm
u.i.d.-GaN Layer (2) ~ 100 nm	u.i.d.-GaN Layer (2) ~ 860 nm
u.i.d.-GaN Layer (1) ~ 1,13 µm	u.i.d.-GaN Layer (1) ~ 290 nm
GaN Buffer Layer ~ 150 nm	HT AlN Buffer Layer ~ 320 nm
LT GaN NL (250 sec.)	AlN NL (90 sec.)
Sapphire	Sapphire

Figure 2.13 Optimized epitaxial design of AlGaN/GaN HEMTs on sapphire.

Before the growth of B-1540 wafer, sapphire substrate is kept under hydrogen flow at 1100 °C for 10 minutes. Then, temperature is decreased to 500 °C after 60 seconds nitridation step. At that temperature and 200mbar pressure, GaN nucleation layer is grown for 250 seconds under 1500sccm NH₃ and 5sccm trimethylgallium (TMGa) flows. Next, temperature is raised to 1030 °C while pressure is kept constant and 150nm GaN layer, which is the first high temperature GaN layer, is grown under 1350sccm NH₃ and 10sccm TMGa flows. For the second high temperature GaN layer, temperature is further increased to 1050 °C, TMGa flow is kept constant and NH₃ flow is defined as 1600sccm. This GaN layer is comparatively thick, 1.13µm. Next, temperature is gradually increased from 1060 °C to 1100 °C for the next 3 GaN buffer layers grown under 1800sccm NH₃ and 17sccm TMGa flows, and 200mbar pressure. Increasing GaN crystal quality from bottom to surface is aimed with the steps explained above.

After completing GaN buffer layers, 1-2nm AlN interlayer is grown under 50mbar pressure, 200sccm NH₃ and 10sccm trimethylaluminum (TMAl) flows. This layer is intended to increase barrier energy level which in turn improves device performance measures e.g. higher saturation drain current, unity current gain frequency f_t and maximum oscillation frequency f_{max} are obtained. Then, 30nm thick AlGaN layer is grown under 500sccm NH₃, 10sccm TMAl, and 5sccm TMGa flows while other conditions are the same as the previous layer. Finally, just by cutting down TMAl flow, 3nm GaN cap layer is grown which is adopted to have lower sheet resistance.

During MOCVD growth, epitaxial layer parameters such as growth rate, layer thickness, composition of ternary compounds, and surface properties should be accurately tracked in real-time. Optical reflectance method is the usual choice for calibrating, monitoring and controlling MOCVD growth processes since it allows direct access to the epitaxial layers and has an appropriate structure for implementation in MOCVD systems. This system has an adjustable monochromatic light source directed to the wafer surface. The light impinged on to the epitaxial layer under investigation is partly reflected. The reflected light intensity is measured by a CCD array or a photodiode. Ratio of the reflected and incident light intensities is called reflectance. Transients of the reflectance measurements are examined to gain information from interference effects occurred due to multiple internal reflections as shown in Figure 2.14. Interference of the reflected beams leads to an intensity modulation of the total reflectance. This fact is known as Fabry-Perot oscillations. Period of the modulation gives information about the growth rate and thickness of the epitaxial layer. Besides, amplitude of the modulated reflectance carries material property related information such as composition of ternary compounds and surface roughness. Optical reflectance graphs taken by the MOCVD system for B-1540 wafer are shown in Figure 2.15. Reflectance transient graph of B-1540 wafer indicates high quality epitaxial growth and surface properties.

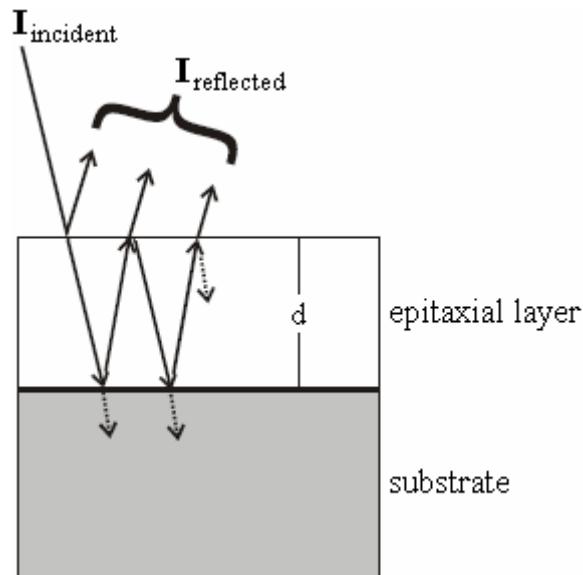


Figure 2.14 Illustration of incident and reflected beams of the optical reflectance measurements.

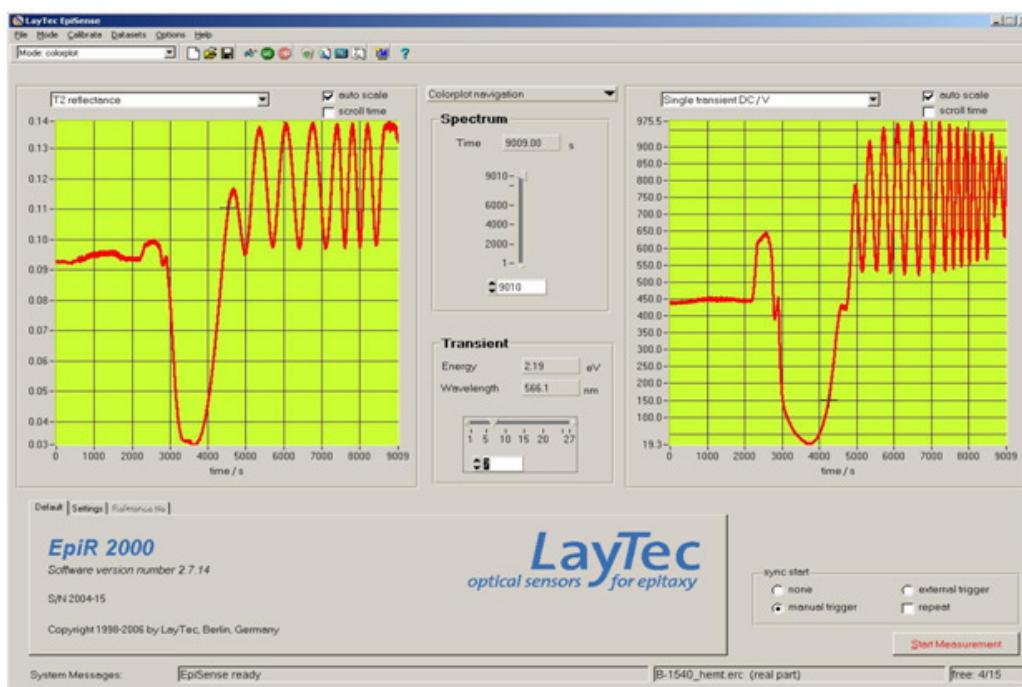


Figure 2.15 Optical reflectance graphs of B-1540 wafer.

Same pretreatment of sapphire substrate is carried out for B-1545 growth. In this case, low temperature (LT) AlN and high temperature (HT) AlN layers are

grown between substrate and GaN buffer layer. To do so, first, temperature and reactor pressure are pulled down to 750 °C and 50mbar, respectively. Then, nitridation step is done under 300sccm NH₃ flow. Next, with the addition of 15sccm TMAl flow LT-AlN nucleation layer is grown for 90 seconds. This layer is a preparation step for the next HT-AlN layer and responsible for low dislocation density in HT-AlN layer. After LT-AlN nucleation layer growth, temperature is raised to 1130 °C in 4 minutes. This process provides annealing of LT-AlN layer which has dominant amorphous character. Eventually, shift to single crystal character is intended for LT-AlN layer. Also, possible parasitic reactions in the reactor are prevented. After annealing step, 320nm HT-AlN layer is grown under 25mbar pressure, 25sccm TMAl flow and 150sccm NH₃ flow which is gradually decreased to 40sccm in 60 seconds and kept constant for the rest of the HT-AlN growth. In other words, V/III ratio is decreased from 307 to 82 during the HT-AlN growth.

Since mobility of the Al atoms on the surface of the substrate is very low, high growth temperature is needed for high crystal quality. Moreover, 50sccm trimethylindium (TMIn) flow is given during HT-AlN growth. Existence of In atoms increases mobility of the Al atoms, however, In atoms cannot penetrate into AlN crystal structure at that temperature.

HT-AlN layer has also a barrier function against the Oxygen (O) atoms in the sapphire substrate. O atoms passing through GaN buffer layer change electronic properties of GaN material and make it less resistive. HT-AlN layer helps the formation of high resistive (HR) GaN buffer layer by preventing O atoms penetrating GaN layers.

After HT-AlN layer, 300nm first GaN layer is grown under 200mbar pressure, 1300sccm NH₃ and 10sccm TMGa flows at 1000 °C. Then, in 5 minutes, temperature and NH₃ flow are increased to 1050 °C and 1500sccm, respectively. So, V/III ratio is changed from 1315 to 1515. Under these

conditions 860nm second GaN layer is grown. Next, fast growth step is started for the third GaN layer, which is 480nm thick, by shifting temperature to 1060 °C, NH₃ flow to 1800sccm, and TMGa flow to 17sccm. Optical reflectance oscillations are dense and smooth under these conditions. After this layer, only temperature parameter is changed to 1075 °C and 160nm GaN layer is grown. Then, reactor process conditions are changed for 1-2nm thick AlN interlayer growth. Reactor pressure and NH₃ flow is decreased to 50mbar and 200sccm, respectively. Temperature is kept constant and 10sccm TMAI flow is given. For 30nm AlGaN barrier layer growth, 5sccm TMGa flow is inserted to previous conditions and NH₃ flow is raised to 500sccm. Finally, TMAI flow is interrupted keeping the other conditions constant and GaN cap layer is grown for 15 seconds. Optical reflectance graphs taken by the MOCVD system for B-1545 wafer are shown in Figure 2.16. Reflectance transient graph of B-1545 wafer indicates high quality epitaxial growth and surface properties.

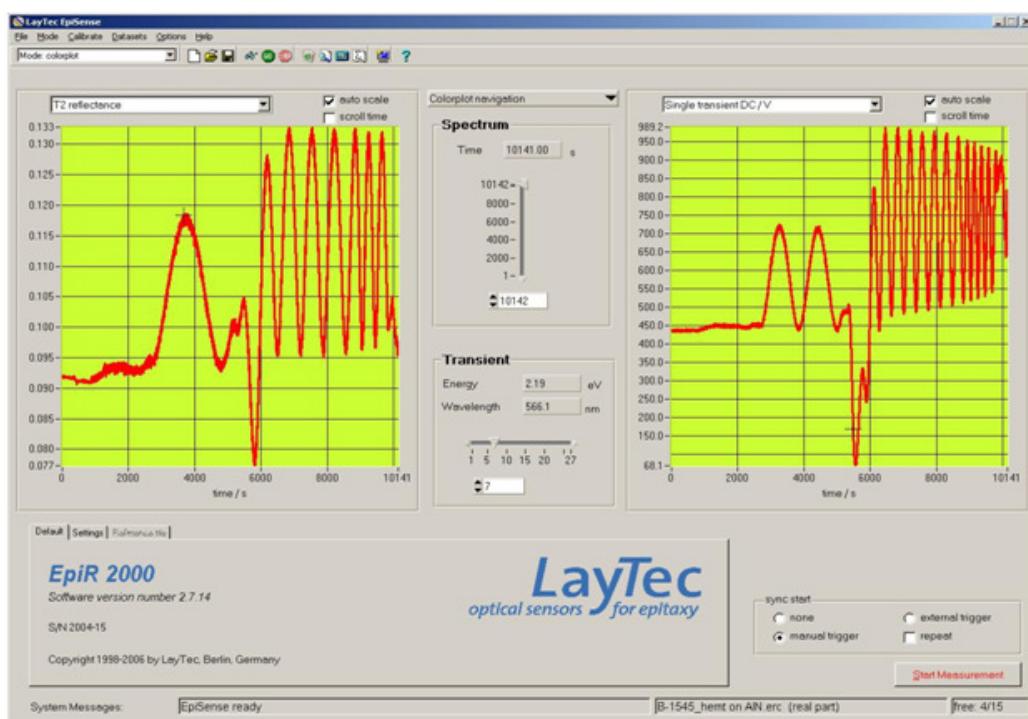


Figure 2.16 Optical reflectance graphs of B-1545 wafer.

2.5 Wafer Characterization

Photoluminescence (PL) measurements are used as a characterization measure of GaN material quality. In Bilkent University NANOTAM building, we have a Jobin Yvon Triax 550 CCD photoluminescence system, which is shown in Figure 2.17, with two different lasers for excitation of samples: 1- 325 nm HeCd, 2- 246 nm NeCu70 DUV laser. Also, it has a cryostat system for low temperature measurements (4K). The photoluminescence system has a fully automatic motorized stage for sample mapping.

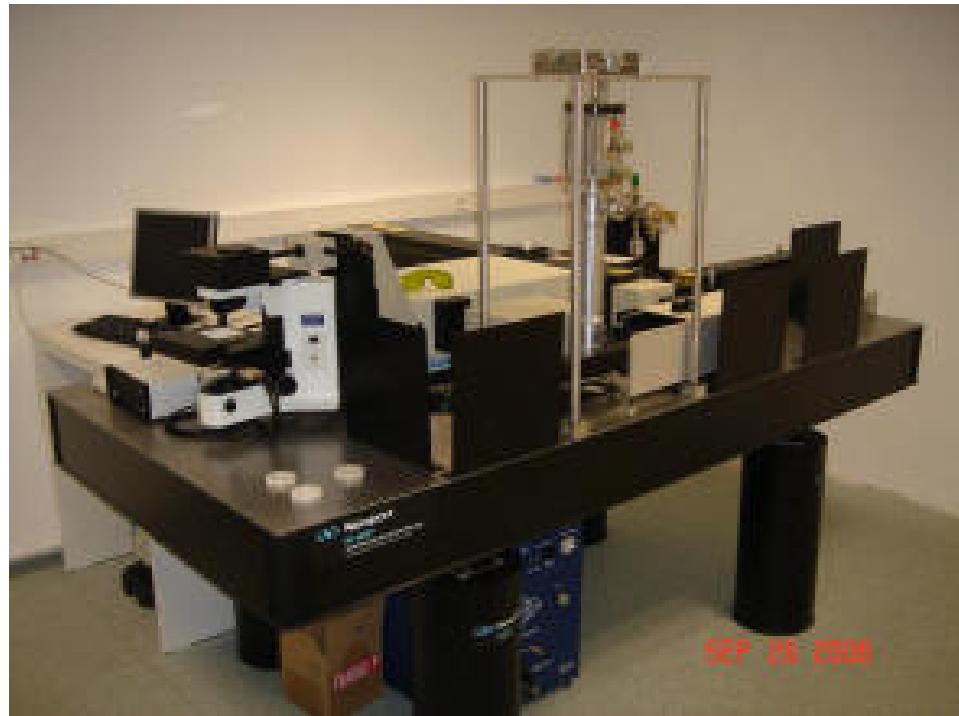


Figure 2.17 Photograph of Jobin Yvon Triax 550ccd Photoluminescence System in NANOTAM.

Figure 2.18 gives the graph of the PL measurement data taken from GaN layer of B-1545 sample. Signal peak is at 362nm and full width at half maximum (FWHM) is 4.15nm. 362nm wavelength corresponds to direct bandgap of GaN, 3.4eV. Measurement shows high peak intensity and narrow FWHM that are indications of high crystal quality of GaN.

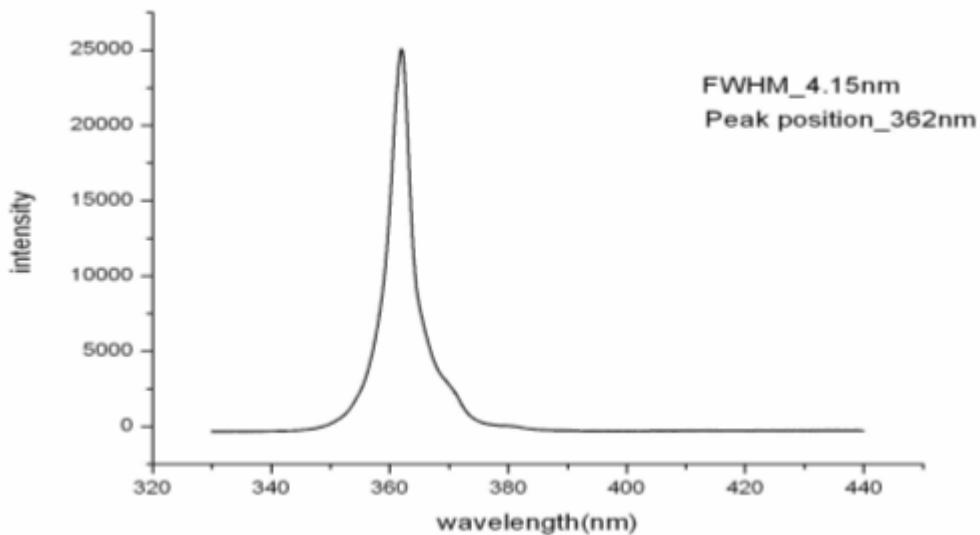


Figure 2.18 PL measurement graph of GaN layer of the B-1545 epiwafer.

AlGaN layer optimizations were done before the whole HEMT structure growth. AlGaN layer were grown on sapphire substrate with AlN buffer layer and optical transmission measurements were taken using Ocean Optics [63] USB4000-UV-VIS miniature fiber optic spectrometer and USB-ISS-UV-VIS integrated sample system. These modules are shown in Figure 2.19.



Figure 2.19 Ocean Optics USB4000-UV-VIS and USB-ISS-UV-VIS modules.

Optical transmission measurement results are shown in Figure 2.20. Transmission starts at 320nm wavelength approximately which corresponds to 3.87eV. Bandgap equation of AlGaN as a function of aluminum concentration (x) is given below [64];

$$E_g^{(Al_xGaN_{1-x})} = E_g^{(GaN)} \cdot (1 - x) + E_g^{(AlN)} \cdot x - b \cdot x(1 - x), \quad (2.13)$$

where b is the bowing parameter of bandgap calculation which is equal to 1.0eV, $E_g^{(GaN)}$ and $E_g^{(AlN)}$ are the bandgap values of GaN and AlN, and they are defined as 3.42eV and 6.13eV at room temperature, respectively. According to equation (2.13) aluminum concentration is calculated to be 23%.

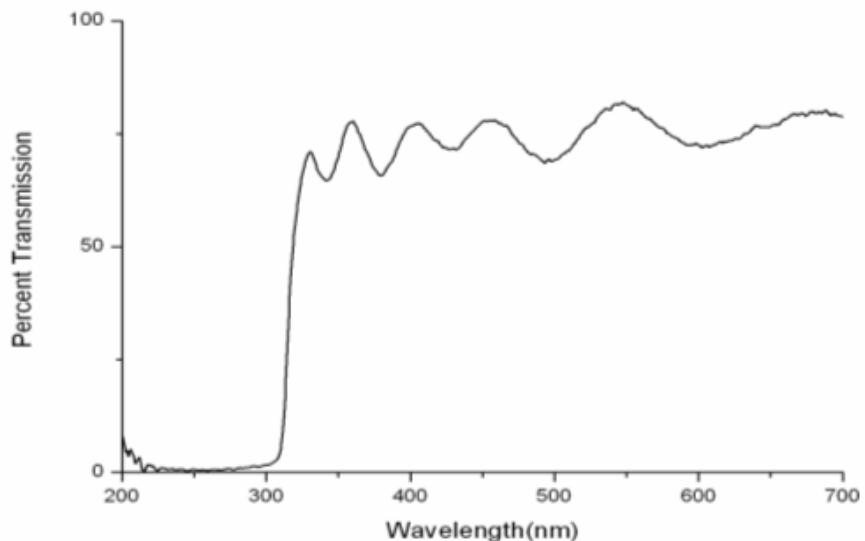


Figure 2.20 Optical transmission measurement of AlGaN barrier layer.

Atomic force microscope (AFM) is used for surface morphology characterization of the epiwafers grown. In Bilkent University NANOTAM building, we have a Veeco di CP-II multi mode AFM system with a 5um x 5um scanner stage and a motorized z stage. CP-II has maximum application flexibility. Accurate measurements are performed with a closed-loop scan-linearization system. 20 bit DACs are utilized for ultra low-noise piezoelectric positioning control. Photograph of our AFM system is given in Figure 2.21.



Figure 2.21 Photograph of Veeco di CP-II multi mode AFM system in NANOTAM.

Contact-mode AFM scan result of B-1545 epiwafer is given in Figure 2.22. Low RMS value, ~0.3nm, indicates that sample has good surface characteristics.

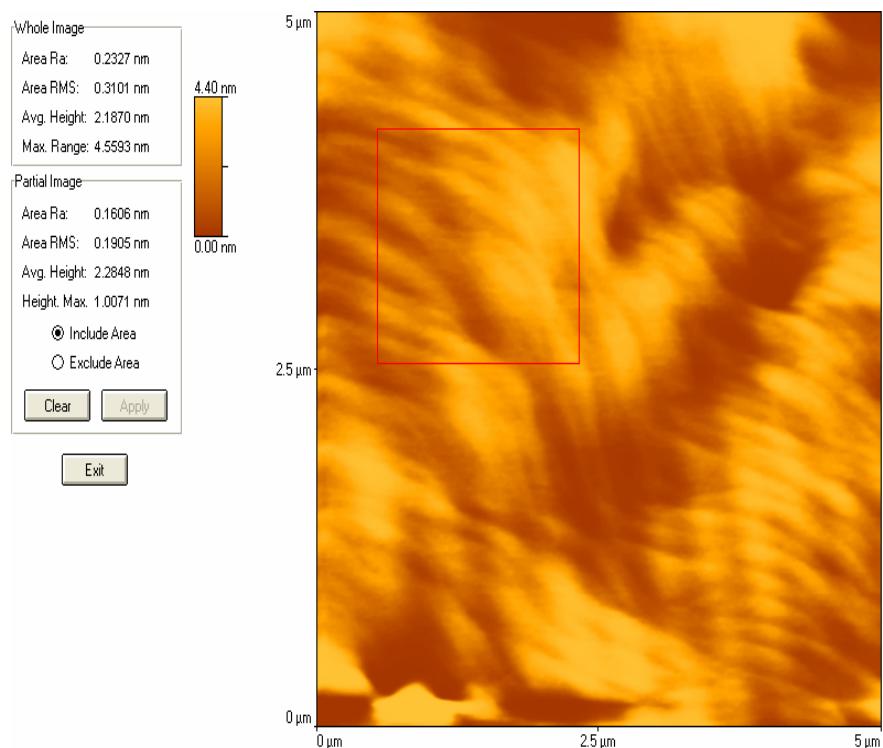


Figure 2.22 Contact-mode AFM scan graph of B-1545 epiwafer.

After the MOCVD growth of B-1540 and B-1545 HEMTs, Hall Effect measurements are taken in order to obtain 2DEG sheet carrier concentration (n_s) and channel mobility (μ_n) levels using our EGK HEM-2000 Hall Effect measurement system in NANOTAM electrical measurements laboratory shown in Figure 2.23.



Figure 2.23 EGK HEM-2000 Hall Effect measurement system in NANOTAM.

Preparation of samples before the measurements is carried out as follows. Samples are diced as 6mm x 6mm squares. In order to be able to pass electric current through the sample with low contact resistance, Ohmic contacts are plated on the corners as shown in Figure 2.24. E-beam evaporator is used for coating Ti/Al/Ni/Au metals with corresponding thicknesses 200Å/2000Å/400Å/500Å. Then samples are annealed in rapid thermal annealing (RTA) oven for Ohmic contact formation by allowing metals diffuse into the structure.

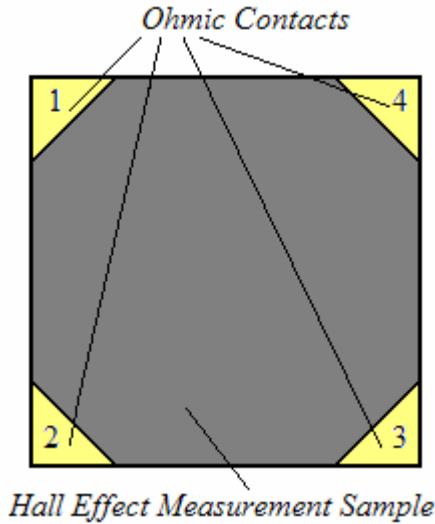


Figure 2.24 Illustration of a sample prepared for Hall Effect measurement.

The measurements can be divided into two parts. First one is determination of n_s based on the Hall Effect. Second one is calculation of μ_n based on the van der Pauw resistivity measurement technique. In the first part, input current I is driven between the opposing pair of contacts 2 and 4 under magnetic field B perpendicular to the sample surface. Then, voltage between the remaining pair of contacts 1 and 3, which is called Hall voltage (V_H), is measured. Consequently, n_s is calculated using following equation;

$$n_s = \frac{IB}{e|V_H|}. \quad (2.14)$$

In the second part, the van der Pauw resistivity measurement technique is applied. Two characteristic resistances, $R_A = V_{34}/I_{12}$ and $R_B = V_{41}/I_{23}$, are measured. The R_S is related to these resistances by the van der Pauw formula;

$$e^{\left(-\pi \cdot \frac{R_A}{R_S}\right)} + e^{\left(-\pi \cdot \frac{R_B}{R_S}\right)} = 1. \quad (2.15)$$

The R_s is solved numerically using equation (2.15) and μ_n is calculated by;

$$\mu_n = \frac{1}{e n_s R_s}. \quad (2.16)$$

Hall Effect measurement results of B-1540 and B-1545 epiwafers are given in Figure 2.25 and Figure 2.26, respectively. Under 0.5mA input current, mobility of electrons is turned out to be $1500 \text{ cm}^2/\text{V}\cdot\text{s}$ and 2DEG sheet carrier concentration is found as $1.14 \times 10^{13} \text{ cm}^{-2}$ for B-1540 epiwafer. The measurements indicate that electron mobility and 2DEG sheet carrier concentration of B-1545 epiwafer are $1748 \text{ cm}^2/\text{V}\cdot\text{s}$ and $1.04 \times 10^{13} \text{ cm}^{-2}$, respectively, under 2mA input current.

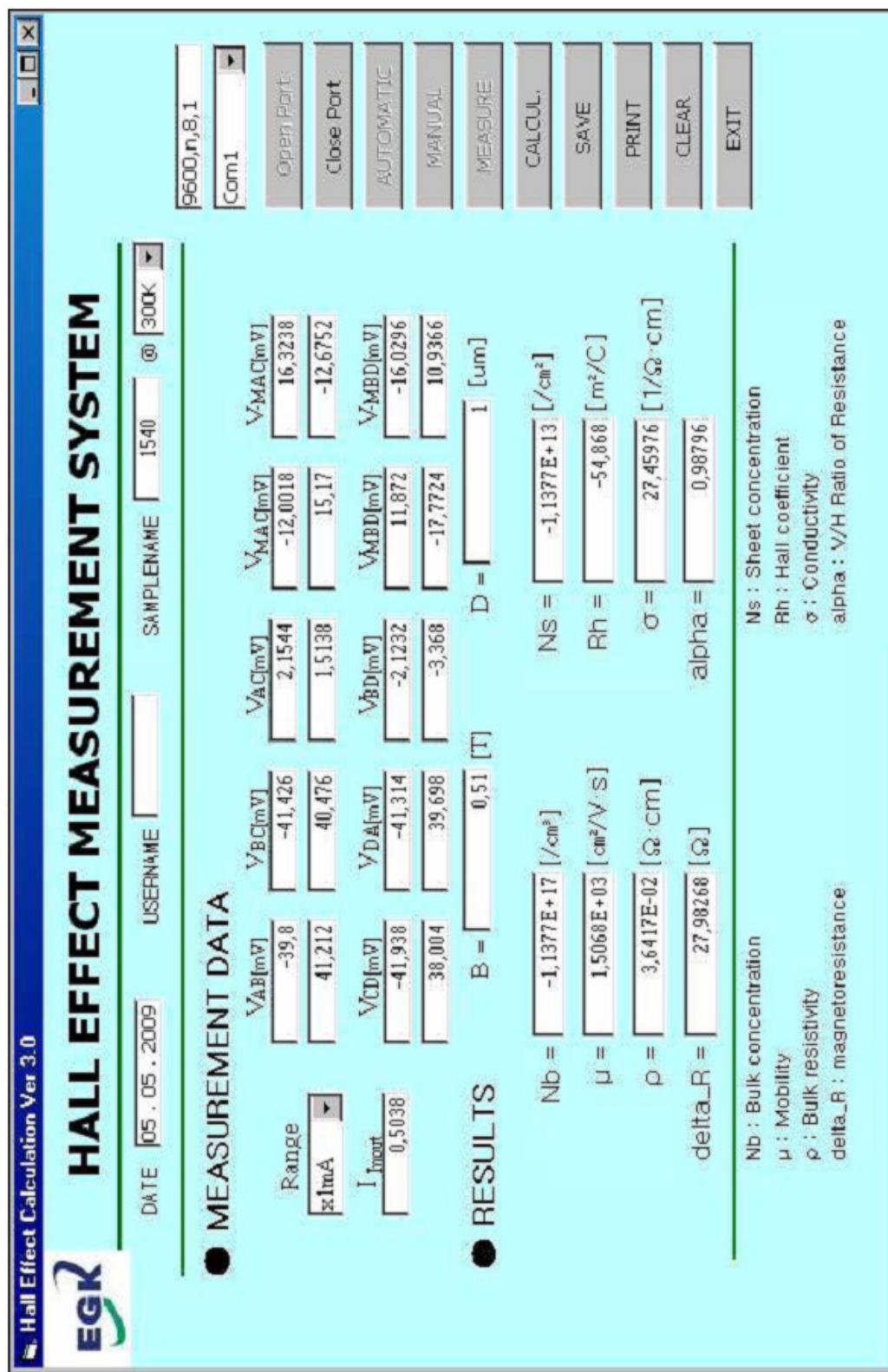


Figure 2.25 Hall Effect measurements of B-1540 epiwafer.

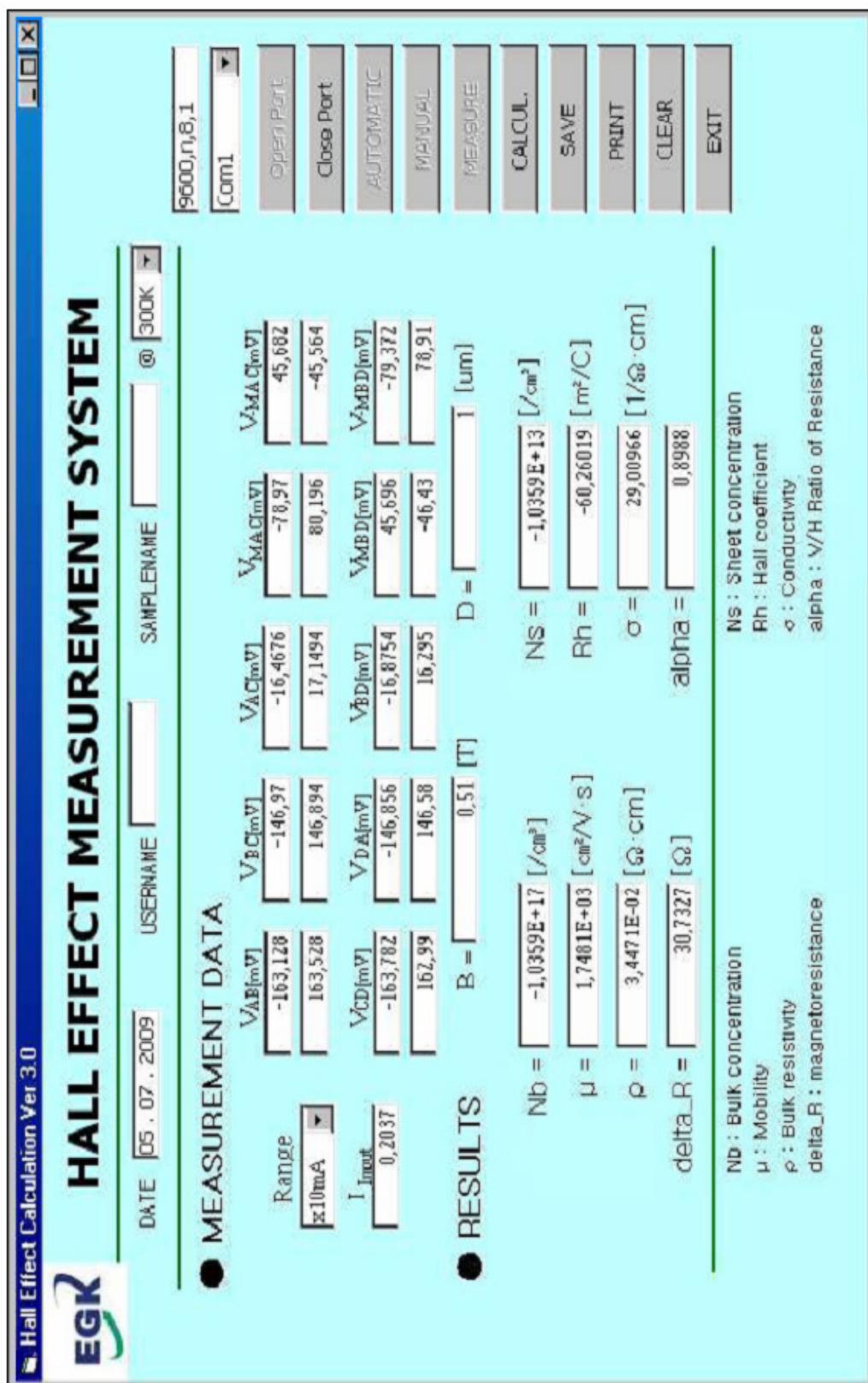


Figure 2.26 Hall Effect measurements of B-1545 epiwafer.

Chapter 3

Fabrication Technology and Characterization of HEMTs

We have already given the details of the AlGaN/GaN HEMT epitaxial structure. In order to build a connection between semiconductor domain and electronics domain, and have an electrical control over semiconductor behavior, we need to fabricate a device properly on top of the epitaxial wafer. In this chapter, fabrication steps and characterization issues of our AlGaN/GaN HEMTs are covered. NANOTAM class-10000 clean room, Bilkent University Advanced Research Lab (ARL) class-100 clean room and NANOTAM electronics characterization lab are used during the whole fabrication and characterization processes. First, photolithography mask design for fabrication is mentioned. Next, lithography and metallization techniques used are explained. Then, fabrication steps are given. The chapter concludes with the presentation of the characterization results of the fabricated devices.

3.1 Mask Design

We developed various coplanar wave guide (CPW)-type HEMT layouts including small and large periphery devices having different unit gate width, gate length and number of comb-shaped gate fingers. Important aspects that need to be considered in the layout design are the gate length (L_g), unit gate

width (W_{gu}), total gate width (W_g) drain-source spacing (L_{ds}), gate-source spacing (L_{gs}), gate-drain spacing (L_{gd}), and gate-to-gate pitch (L_{gg}).

The cut-off frequency of a device is inversely proportional to the gate length as given in (3.1) under the assumptions that all electrons in the 2DEG travel at the saturation velocity and that any intrinsic feedback due to the gate-drain capacitance (C_{gd}) can be neglected.

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{v_{sat}}{2\pi L_g} , \quad (3.1)$$

where g_m is transconductance and C_{gs} is gate-source capacitance of the active device, and v_{sat} is the saturation velocity of the electrons in the channel. Hence, as we decrease the L_g , f_T increases so that we are able to operate the transistor at higher frequencies. In our fabrication process, E-beam lithography workstation is used to be able to define sub-micrometer gate lengths. Moreover, shorter L_g leads to the increase in the drain current that is proportional to the gate width over gate length (W_g/L_g) ratio. According to this statement, W_g should also be increased for high power applications; however, unit gate width needs to be electrically small at operation frequency. As a solution to the limited W_{gu} dimension problem, the total gate width can be increased using several parallel gates. There is also an upper limit for the number of parallel gates related to the same reason that we have limitation in W_{gu} . The gate-to-gate pitch should be kept as short as possible in order to have maximum number of gates in parallel and still conserve the lumped element approximation. As the gates get closer, channel temperature interference rises and device performance is degraded. Consequently, an L_{gg} controlled trade-off occurs between the channel temperature effects consideration and achieving high power devices.

The drain-source spacing should be kept as short as possible since it is proportional to the drain-source resistance R_{ds} . The gates are preferred to be placed closer to the source than to the drain side in order to improve breakdown

properties and average electron speed in the channel. In our mask design, we considered both symmetric and asymmetric gate devices in order to have a deeper understanding of the device behavior with respect to the gate position.

Designed layouts are layer by layer transferred to a photolithography mask using Wavemaker™ software. The mask set contains alignment marks for optical and E-beam lithography, and transmission line model (TLM) patterns for Ohmic contact resistance determination. Our latest HEMT photo-mask layout is given in Figure 3.1. In Figure 3.2, an 8x75 μm HEMT layout, which has 3 μm drain-to-source spacing, SiN passivation layer and air-bridges at gate-source intersections, is shown.

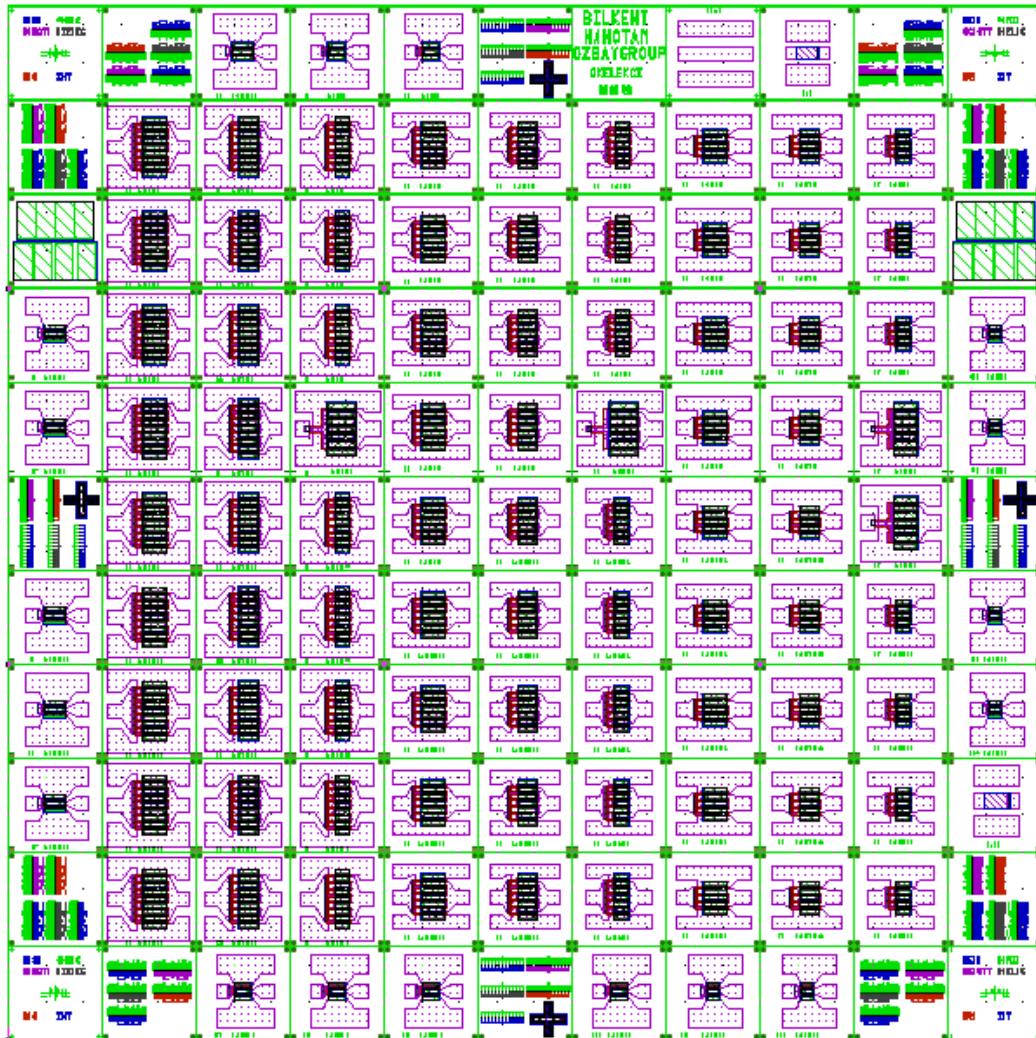


Figure 3.1 HEMT photo-mask layout.

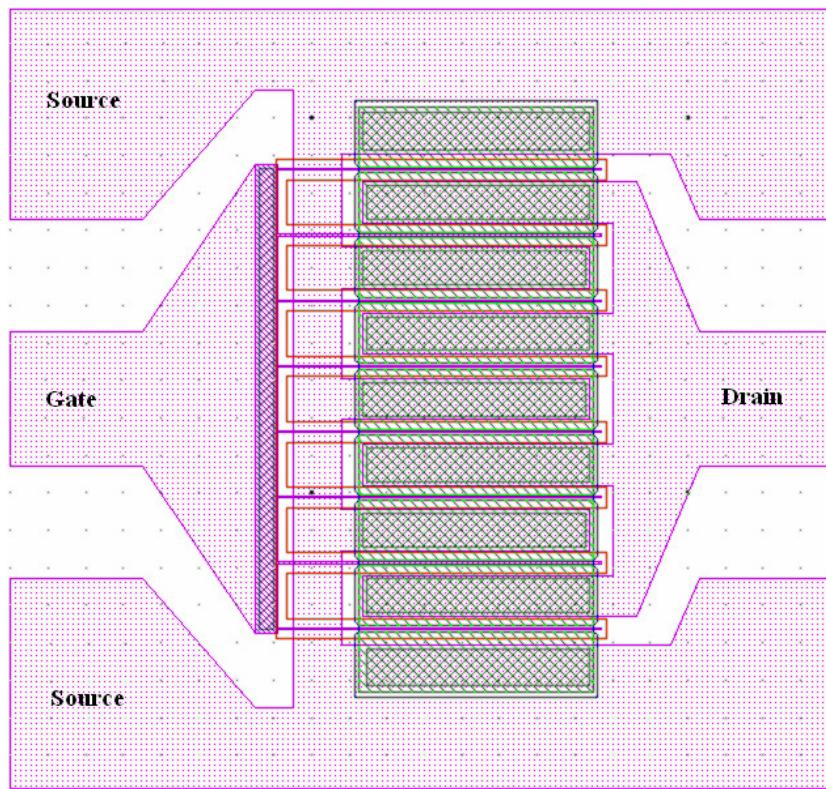


Figure 3.2 An $8 \times 75\mu\text{m}$ HEMT layout.

3.2 Lithography Techniques Used

Lithography is the fundamental and most critical process in semiconductor fabrication which allows us to form geometric shapes on the surface of the wafer. A specific chemical solution called “resist” is required for every lithography method. In our fabrication process, we use two lithography techniques, namely, photolithography and E-beam lithography. We will explain each technique in the following paragraphs.

Photolithography

In photolithography technique, resist sensitive to UV light called “photoresist” is used for pattern formation. Photolithography process steps are surface preparation, photoresist coating (using spinner), soft-bake treatment,

photo-mask alignment, UV exposure, development, hard-bake treatment, processing using the photoresist as a masking film, stripping, and post processing cleaning. Prior to photoresist coating, samples are subjected to standard wafer cleaning steps which will be explained later. For sufficiently long spin time, thickness of the coated resist in microns is given as follows;

$$t = k \cdot \frac{p^2}{w^{1/2}}, \quad (3.2)$$

where **k** is the spinner constant which is typically 80-100, **p** is the resist solids content in percent, and **w** is the spinner rotational speed in rpm/1000. Spin-coating steps are illustrated in Figure 3.3. We use programmable spin coater of Specialty Coating Systems™ shown in Figure 3.4.

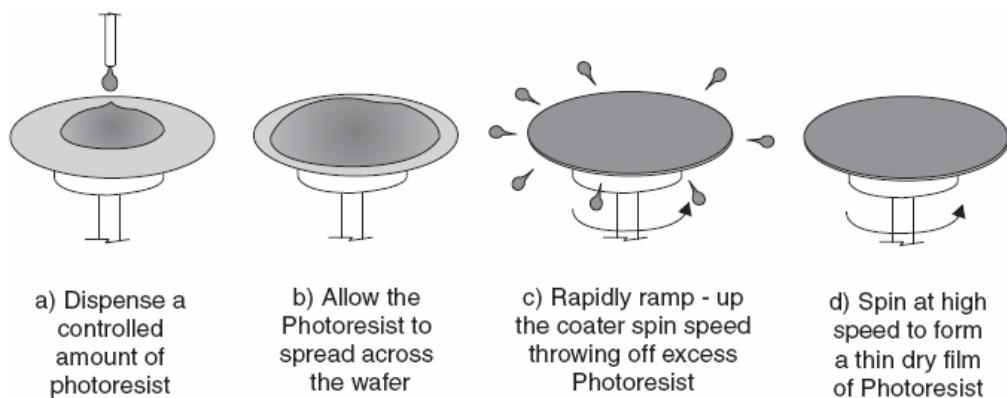


Figure 3.3 Spin-coating steps.



Figure 3.4 SCS Spincoat System.

Soft-bake on a hot plate (at 80-100°C for 30-60 sec.) is done in order to condense the resist after spin coating. Chrome coated fused quartz substrate photo-mask is used for applying selective area exposure on the sample surface. Then, alignment of the mask to the previous fabrication step on the sample is done using alignment marks on the mask and the sample. Figure 3.5 illustrates possible mask alignment scenarios. Correct alignment of the mask is vital for fabrication yield. We use Karl Suss MA6 mask aligner system shown in Figure 3.6. In this system, UV exposure in two modes, contact (soft, hard, vacuum) and proximity printing, are possible. Pattern resolutions starting from 2.5um (in proximity mode) and down to submicron values (in vacuum contact mode) can be achieved depending of the optical wavelength.

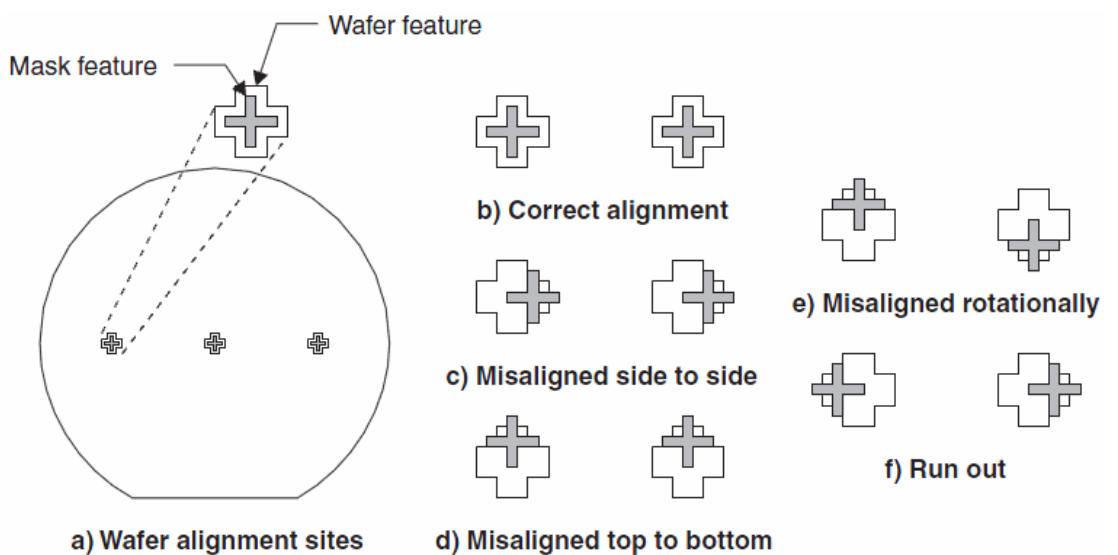


Figure 3.5 Illustration of mask alignment scenarios.

There are two types of photoresists which are positive tone and negative tone. Positive resists become more soluble in developer solution when exposed to UV radiation. In contrast to positive resists, UV exposed negative resist portions are rendered insoluble to developer solution. Opposite resist profiles occur for positive and negative photolithography and they serve for different purposes. For instance, positive resist is more appropriate for mesa etching step in order to have continuity of interconnect metals, and negative resist is required in

metallization steps for easy lift-off process. In Figure 3.7, UV exposure and development steps of negative and positive photolithography are summarized and patterned resist profiles are shown for both cases.



Figure 3.6 Photo of a Karl Suss MA6 Mask Aligner System.

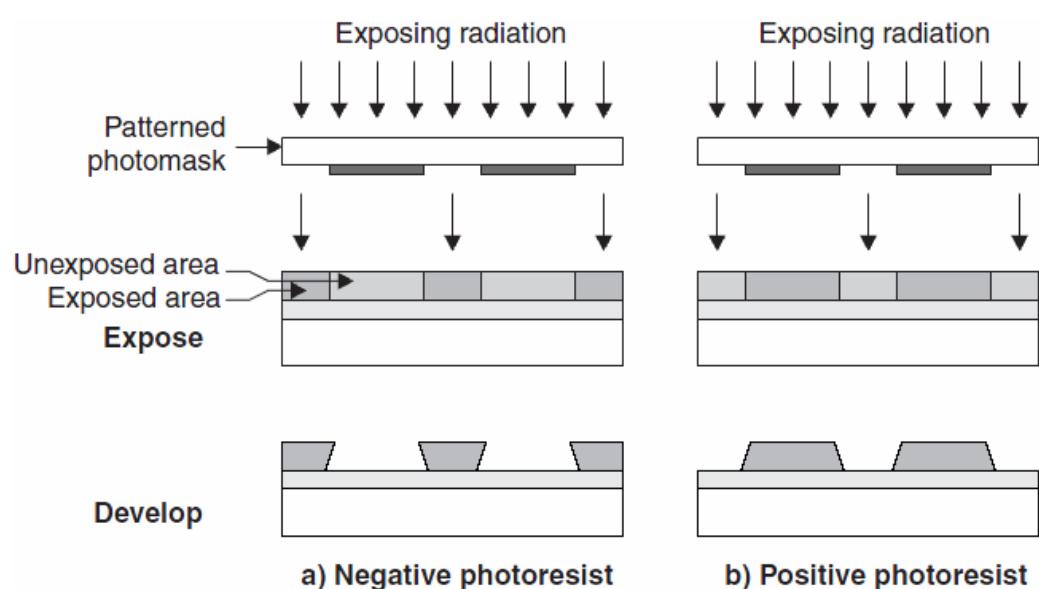


Figure 3.7 Schematic illustration of negative (a) and positive (b) photolithography.

Next step of the photolithography after the development is hard-bake treatment. Hard-baking is done at temperatures between around 120 °C for 10 minutes using hot plate. This treatment is used to stabilize and harden the photoresist and to evaporate any remaining residue of the coating solvent and developer so that solvent burst effects are avoided in vacuum processing. On the other hand, hard-bake improves adhesion of the resist to the sample surface and makes the resist removal step more difficult.

Need for hard-bake treatment depends on the processing step type. There are two primary patterning techniques. First one is etch-back where photoresist pattern is applied on the sample and open parts are etched away. Main steps of this technique are given in Figure 3.8. Etch-back process requires hard-baked resist coating.

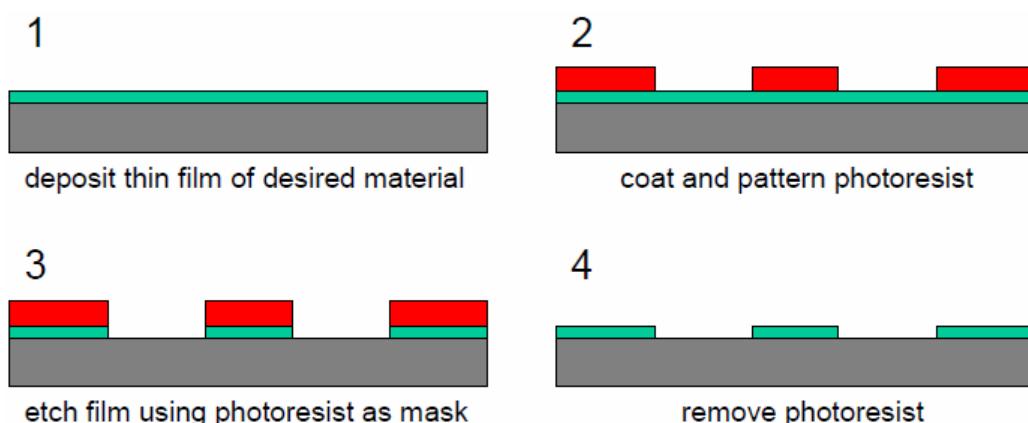


Figure 3.8 Steps of etch-back process.

The other technique is lift-off which consists of photolithography pattern coating, material deposition all over the sample surface and finally removing the resist together with unwanted portion of the deposited material. Lift-off steps are summarized in Figure 3.9. Since soft resist is required for this technique, hard-bake treatment is not applied usually.

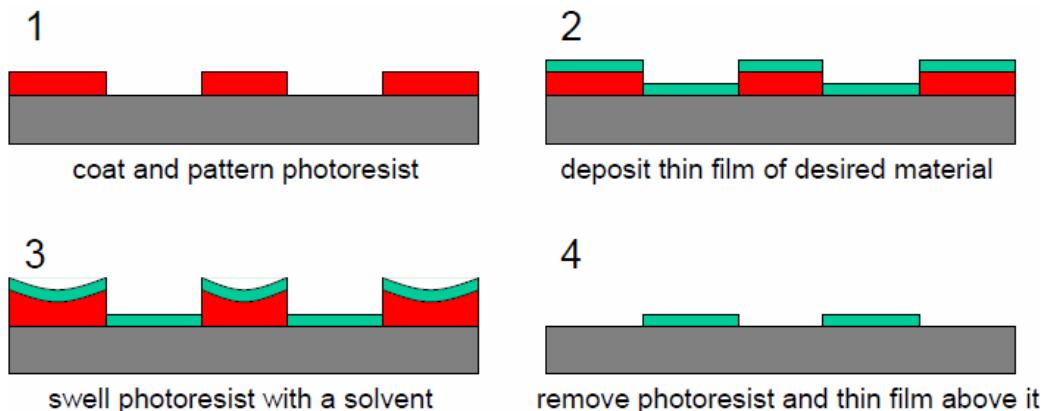


Figure 3.9 Steps of lift-off process.

The photoresist should be removed after all process steps. There are various solvents used for resist removal process. We use simply acetone (CH_3COCH_3) to remove both positive and negative tone resists. An ultrasonic cleaner that generates ultrasound waves is used to assist and ease the resist removal process in case the resists tend to stay on the sample surface.

E-beam lithography

Resolution of the optical lithography (r) is limited by the UV exposure wavelength as stated by the Rayleigh criteria given below;

$$r = k_1 \cdot \frac{\lambda}{\text{NA}} , \quad (3.3)$$

where k_1 is a constant specific to the applied process, λ is the wavelength of the exposure, and NA is the numerical aperture of the system. In order to overcome the resolution limit for submicron patterning down to 100nm, electron beam lithography is used as one the effective high resolution methods by the very small de-Broglie wavelength of electrons compared to optical UV wavelengths. E-beam lithography systems are direct write systems that means no physical mask is required in this process, however, lithography patterns have to be transferred as a software code to the E-beam control unit. These systems contain electron source, electron accelerator unit, electron beam focusing unit, and beam

deflection and stage translation components. Likewise in the case of optical lithography process, resist material is required for pattern printing in E-beam lithography. Most commonly used E-beam lithography resist is polymethyl methacrylate (PMMA) which forms positive images. The developer of PMMA is typically a solution of methylisobutyl ketone (MIBK) and isopropanol (IPA). Photo of the E-beam lithography workstation used in NANOTAM is shown in Figure 3.10.



Figure 3.10 Photo of an E-beam lithography system.

3.3 Metallization Techniques Used

Two metallization methods are used throughout our GaN HEMT fabrication process. First one is “electron beam evaporator system” which is very effective tool for Ohmic and Schottky contacts formation. Wide variety of metals such as Ti, Al, Ni, Au, Ag, Ge, and Pt can be evaporated in appropriate metal crucibles by focusing accelerated electron beam on to the target metal. System pressure is kept close to the vacuum condition in order to acquire highly pure metal vapor. Evaporated metal is deposited on the samples attached to the ceiling of the

system. Deposited metal thickness is controlled by a sensor at the same level with the samples. Photograph of Leybold Univex-350 e-beam evaporator system in NANOTAM Class-10000 clean room is shown in Figure 3.11.



Figure 3.11 Photo of the Leybold Univex 350 E-beam evaporator in NANOTAM.

Electroplating is the other metallization technique that we used in our fabrication process. This method is appropriate for thick Au coating ($2\text{-}4\mu\text{m}$) which is required for interconnect and air-bridge metallization. As the interconnection metal thickness gets higher resistive loss decreases and mechanical endurance of the contacts against probing the device several times increases. When it comes to air-bridges, high metallization thickness levels which cannot be achieved by e-beam evaporator system become more inevitable. Air-bridge height is very critical parameter which should be kept as

high as possible in order to minimize the parasitic capacitance effects. Consequently, air-bridge metal must be thick enough to carry its own load and resistant to possible mechanical intervention during fabrication process.

The sample surface is required to be made conductive prior to electroplating process. To do so, Ti/Au metals are deposited as much as $500\text{\AA}/1500\text{\AA}$, respectively, using e-beam evaporator system. This metal layer is also called seed layer. Then, thick metal pattern is defined by photolithography. Next, electroplating of Au metal is done in electrolyte solution kept at $50\text{ }^{\circ}\text{C}$ such that the sample is connected to the cathode and Au source is connected to the anode of the electroplating circuit. Current flow through the circuit carries Au ions up to the sample surface and deposition occurs. Thickness of the plated Au increases in time. Schematic of our home-made electroplating setup is shown in Figure 3.12. After completing electroplating process, the seed layer should be removed using proper etching techniques since electroplated contacts are short circuited to each other by the seed layer.

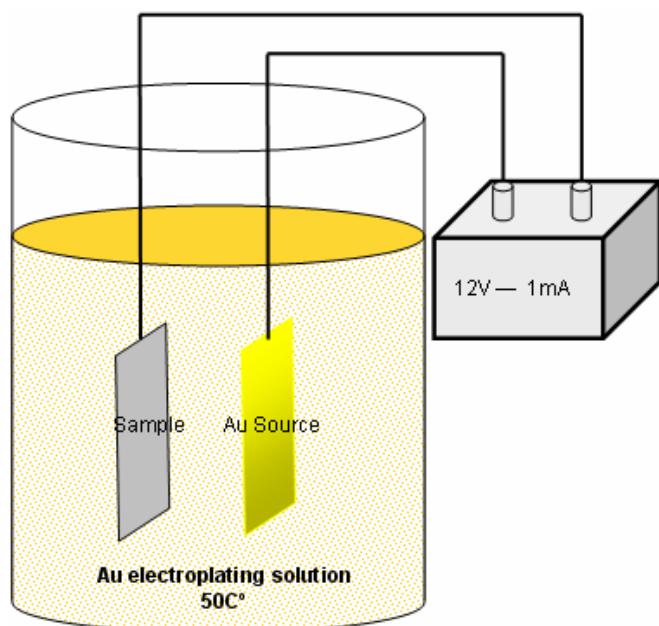


Figure 3.12 Schematic of our Au electroplating setup.

3.4 Fabrication Steps

Now, we will continue with the details of the fabrication steps. Before going through, we will remark a common point for all steps, that is sample cleaning. Device quality and fabrication yield have strong positive dependence on epiwafer surface cleanliness. Any organic and inorganic dust on the sample surface can cause unwanted results such as mechanical failures and improper device operation. Therefore, samples are needed to be cleaned right before every main fabrication step. In order to realize sample cleaning, we keep the samples diced 8mm by 8mm under acetone (CH_3COCH_3), isopropyl alcohol ($\text{CH}_3\text{CHOHCH}_3$) and pure water flows, in turn. Then, samples are dried using pressured nitrogen (N_2) gas. Finally, a short soft baking can be applied to evaporate possible water remainder on the surface.

Fabrication process consists of mesa etching, Ohmic contact for drain and source connections, Schottky contact for gate metallization, SiN passivation, air-bridge post, seed layer, air-bridge metallization, and seed layer and air-bridge post removal steps, respectively. We will explain each step in the following paragraphs.

Mesa Etching

Each HEMT device should be electrically isolated from neighboring devices. This isolation is acquired by mesa etching. We use reactive ion etching (RIE) technique to etch the openings on the sample defined by photolithography. We use Freon (CCL_2F_2) gas for plasma formation. Flow rate is 20sccm and chamber pressure is $8\mu\text{bar}$. We obtain approximately 1nm/sec. etch rate under 200W RF power. Etch depth should be larger than the 2DEG depth for proper electrical isolation. Typical 2DEG depth is around 30-60nm. 100nm etch depth is formed in 100 seconds which is appropriate for our fabrication process. In Figure 3.13, schematic illustration and a photo of the sample after mesa etching are shown. After mesa etching step, the samples should be cleaned well to remove possible

particles attached to the surface during RIE etching process. For the following steps cleaning of the samples requires extra care since there will be metal contacts to be considered.

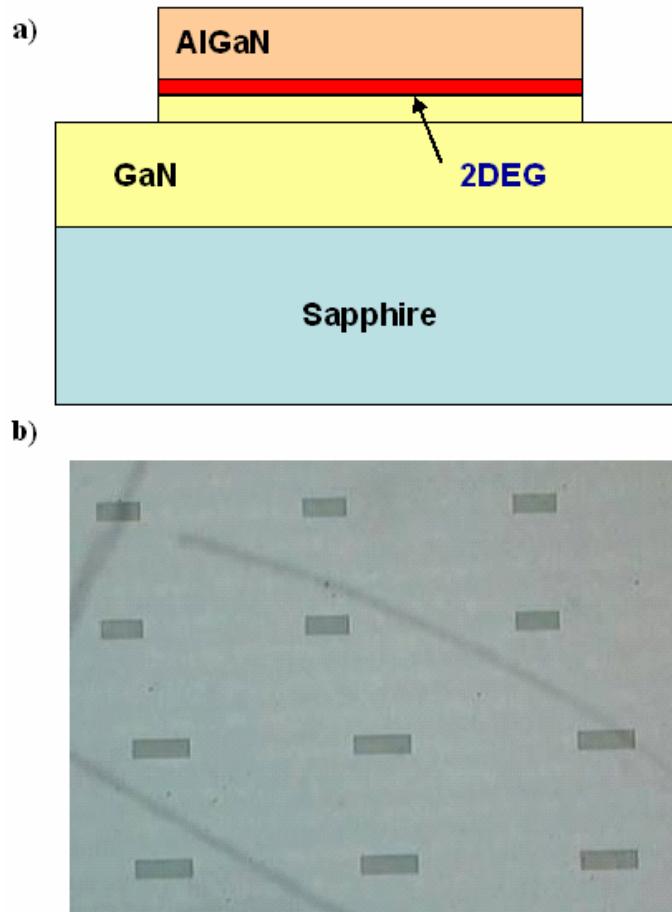


Figure 3.13 Schematic illustration (a) and a photo (b) of the sample after mesa etching step.

Ohmic Contacts

In HEMT device, Ohmic contact is required to form an electrical connection to the channel from the upper surface. This connection is supposed to be low-loss since resistance occurred by the Ohmic contacts remarkably degrades the performance of the HEMT device. As a physical explanation of this fact, extrinsic transconductance (g_m) in dependence of the intrinsic transconductance (g_{m0}) and the source resistance (R_s) is given in (3.4). Hence, it is obvious that

parasitic resistances coming from Ohmic contact formation have to be decreased to have better device performance.

$$g_m = \frac{g_{m0}}{1 + R_s \cdot g_{m0}} . \quad (3.4)$$

In order to achieve low-loss Ohmic contacts, the contact metal should have low work-function which allows electrons pass easily through the metal-semiconductor crossing. Titanium is found to be an efficient metal for being used as the first metal layer of the Ohmic contact due to various reasons. Titanium atoms interact with the N atoms on the semiconductor surface to form TiN which has very low work-function (3.74eV) [65]. Moreover, formed TiN leaves donor-like N vacancies which make the electron flow easier [66], [67]. Additionally, this first metal layer provides good mechanical stability and dissolves the native oxide on the semiconductor surface [68], [69]. Aluminum is used as a second metal layer of the Ohmic contact. This layer prevents oxidation of the Ti layer via forming an Al₃Ti alloy layer. After annealing process, Al diffuses through the Ti layer and forms an Ohmic contact. Additional two metal layers (Ni/Au) are deposited in order improve the contact quality. Au layer improves conductivity of the overall Ohmic contact. Ni layer acts as a barrier between Al and Au layers which prevents highly resistive Al/Au mixing called “purple plague”. Oxidation of the Al layer is also prevented by Ni/Au layers. Ohmic contact formation is completed by annealing of the deposited metal stack at high temperatures around 800-900 °C as long as optimized time duration. Line definition of the contacts can be kept stable with the existence of the Ni/Au layers.

In our fabrication process, drain and source Ohmic contact regions are defined by negative photolithography technique using corresponding mask step aligned to the mesa etching alignment marks. Then, e-beam evaporator is used for metallization of the Ohmic contacts. Ti/Al/Ni/Au metal stack is deposited as much as 150Å/1500Å/400Å/700Å, respectively. As a next step of the Ohmic

contact metallization, standard lift-off process is applied to remove unwanted metal parts coated on the photoresist. Negative profile of the photoresist facilitates the lift-off process. Finally, rapid thermal processor (RTP) is used for annealing Ohmic contacts at 850 °C. Annealing process carried out in forming gas (combination of 95% N₂ and 5% H₂) ambient. Ramp time is 30 seconds from room temperature to 850 °C. Temperature stays at 850 °C for 30 seconds. Then samples are cooled down to room temperature in one minute. Schematic illustration and photos of the Ohmic contacts before and after the annealing process is shown in Figure 3.14. Photo of the SSI Solaris 75 RTP system in NANOTAM is given in Figure 3.15. Temperature versus time graph taken from the RTP during annealing of the samples is given in Figure 3.16.

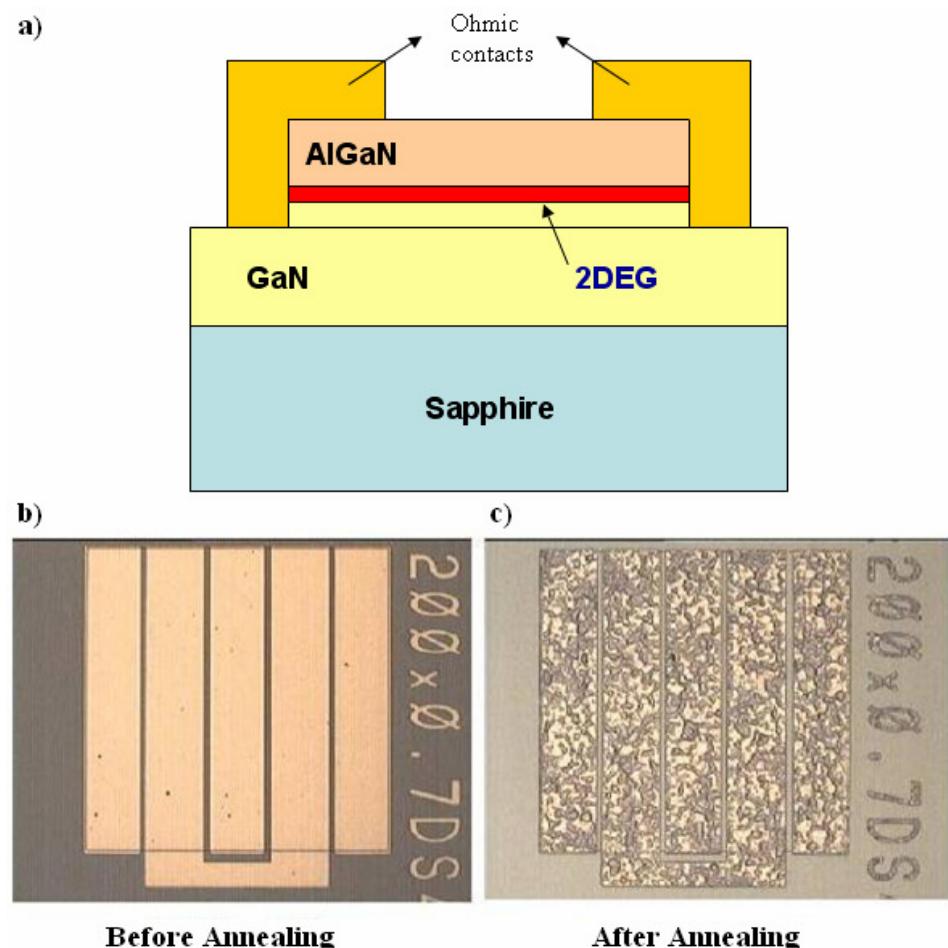


Figure 3.14 Schematic illustration (a) and photos of the Ohmic contacts before (b) and after (c) the annealing process.



Figure 3.15 Photo of the SSI Solaris 75 RTP system in NANOTAM.

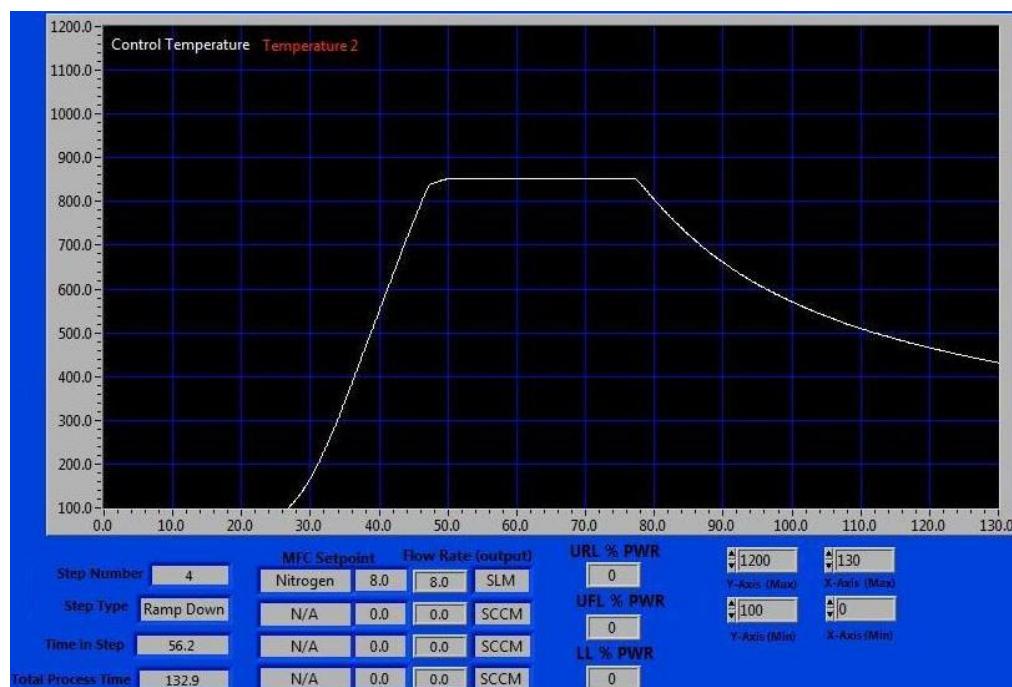


Figure 3.16 RTP temperature vs. time graph.

The contact resistance is a measure of Ohmic contact quality and can be determined by TLM resistance measurement technique. A series of rectangular Ohmic contacts with various spacing between them is fabricated to form TLM pattern. We applied four point TLM measurement method in order to eliminate the parasitic resistance introduced by the probes, and evaluate the contact resistance by fitting the resistance measurements taken between all TLM contact couples with the following expression (3.5);

$$R_{\text{meas}} = 2 \cdot \frac{R_c}{w} + R_s \cdot \frac{d}{w} , \quad (3.5)$$

where R_{meas} (Ω) is the measured resistance between two contacts, R_c ($\Omega\text{-mm}$) is the Ohmic contact resistance, R_s (Ω/square) is the sheet resistance of the semiconductor structure, w is the width of the contacts, and d is the inter-contact spacing. Schematic illustration of the TLM pattern we used is shown in Figure 3.17.

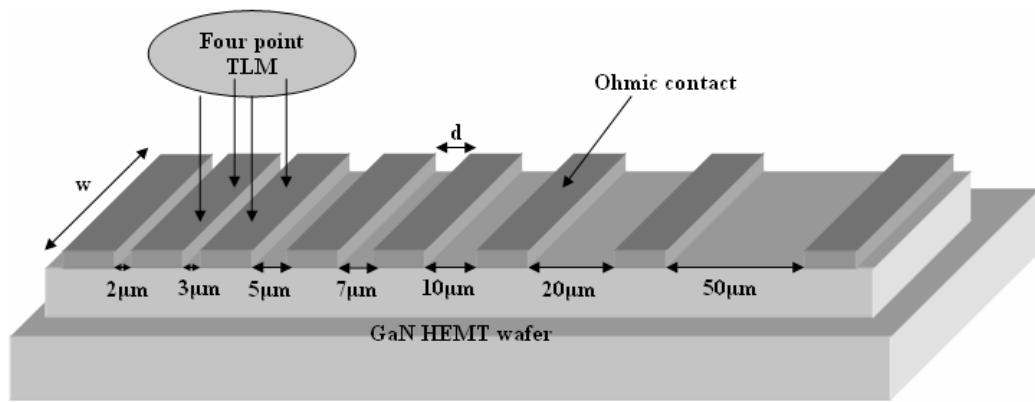


Figure 3.17 Schematic illustration of the TLM pattern.

Measurement and parameter fitting results of a typical Ohmic contact we fabricated are given in Figure 3.18. The contact resistance is found to be 0.5 ($\Omega\text{-mm}$) which corresponds to a highly conductive Ohmic contact.

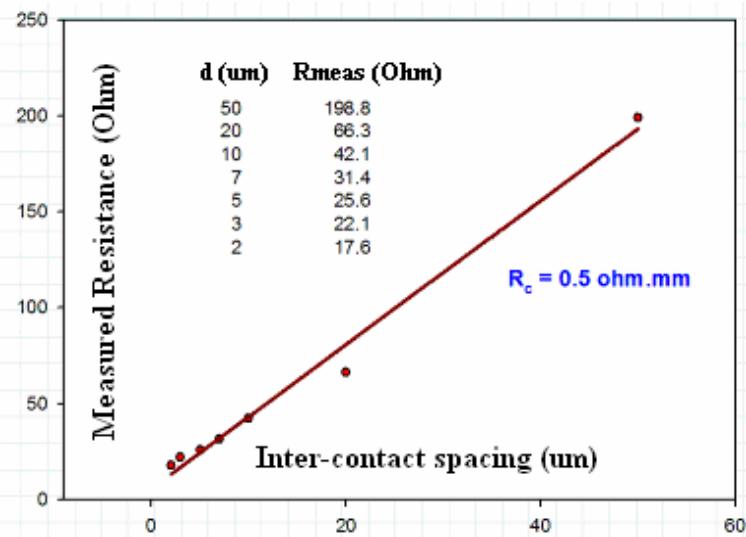


Figure 3.18 TLM measurement data and corresponding graph.

Schottky Contacts

Schottky contacts are vital for gate formation in HEMTs. The most important parameter in Schottky contacts is energy barrier height between the semiconductor surface and contact metal. Band diagrams of the Schottky contact before and after the metallization are shown in Figure 3.19. High Schottky barrier height is required to obtain low gate leakage current and high breakdown voltage. This can be achieved by a metal with high work function. Furthermore, contact metal should have good thermal stability at high channel temperature levels of GaN HEMTs, and good adhesion to the AlGaN/GaN material system which is very important to acquire enough mechanical strength of the gate contacts during device processing. As a matter of fact, input resistance of the HEMT device is determined by the resistance of the Schottky gates. We need to improve conductivity of the Schottky contacts in order to have as low as input resistance which has a strong influence on the HEMT device performance.

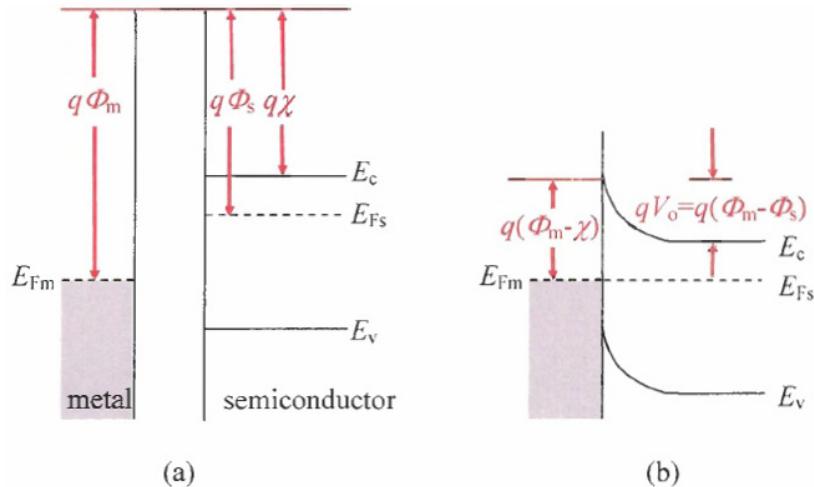


Figure 3.19 Band diagrams of a metal and a semiconductor (a) and Schottky contact after connection (b).

Nickel is found to be a good candidate for high quality Schottky contacts due to its high work function (5.15eV), good adhesion, and thermal stability properties. On top of Ni, Au is used as a second metal layer in Schottky contact

formation which enhances conductivity of the connection and prevents the oxidation of Ni.

In order to fabricate submicron gates, we used E-beam lithography workstation in our fabrication process. PMMA resist is used in gate pattern definition. Thickness of the resist must be higher than that of the contact metal. After the resist coating, Ni/Au metal stack is deposited using e-beam evaporator system. Thickness of the Ni and Au metals are $500\text{\AA}/2500\text{\AA}$, respectively. In Figure 3.20, schematic illustration of the device fabricated up to this point and corresponding device photos are given. We have fabricated HEMT devices with gate lengths in $0.2\text{-}0.4\mu\text{m}$ range.

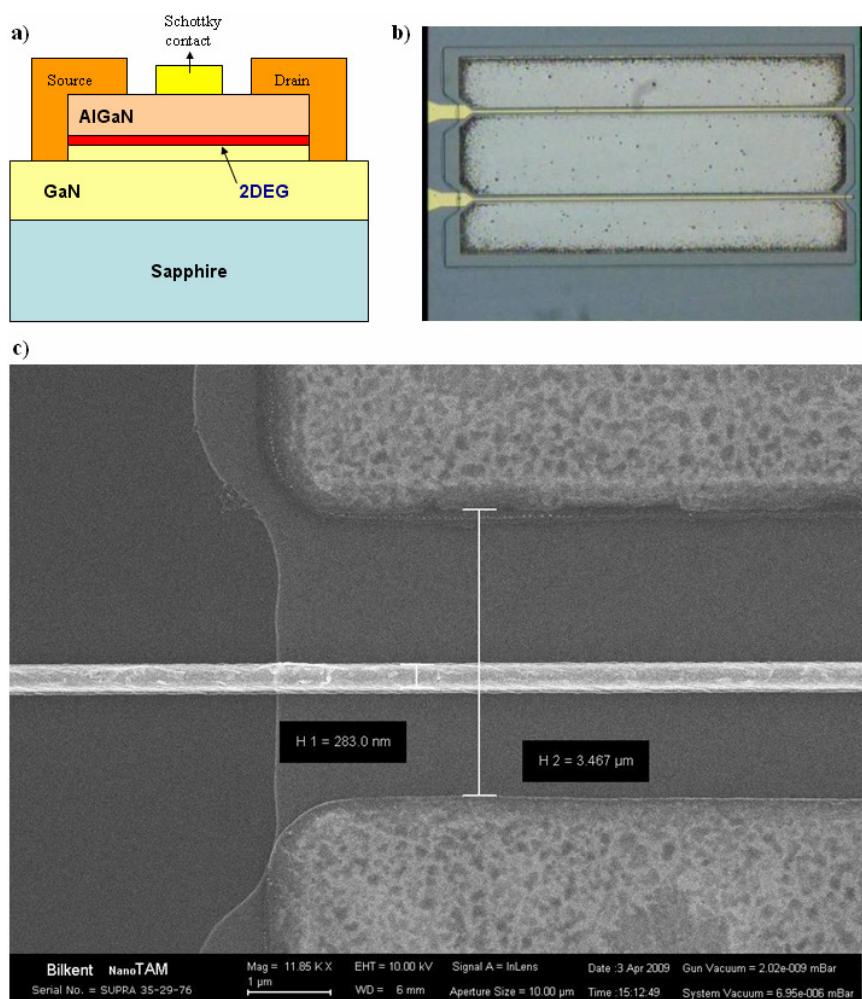


Figure 3.20 Schematic illustration (a) and photos (b-c) of the device after gate metallization.

SiN Passivation

As we mentioned before in Chapter 2, surface passivation topic has been extensively examined by researchers in parallel with the AlGaN/GaN HEMT device progress. Surface passivation has an important role on both electronic transport properties, and mechanical and/or chemical damage protection of the device. Latter one is obvious, however, physical understanding of the relation between the device performance and surface passivation has not been fully made clear yet. Very confusing and contradictory literature works have been published on this issue [53], [54], [70], [71]. On the other hand, there is widely accepted hypothesis on surface passivation which is related to virtual gate formation [72], [73], [74], [75]. In Figure 3.21 virtual gate formation is illustrated schematically. According to this hypothesis, surface states neutralization due to trapped electrons is prevented and positive surface charge is maintained by appropriate surface passivation therefore virtual gate formation does not occur. As a result, better device performance measures such as reduction in current slump and microwave power degradation, lower gate leakage, higher sheet carrier concentration, and higher breakdown voltage are achieved by introducing surface passivation layer.

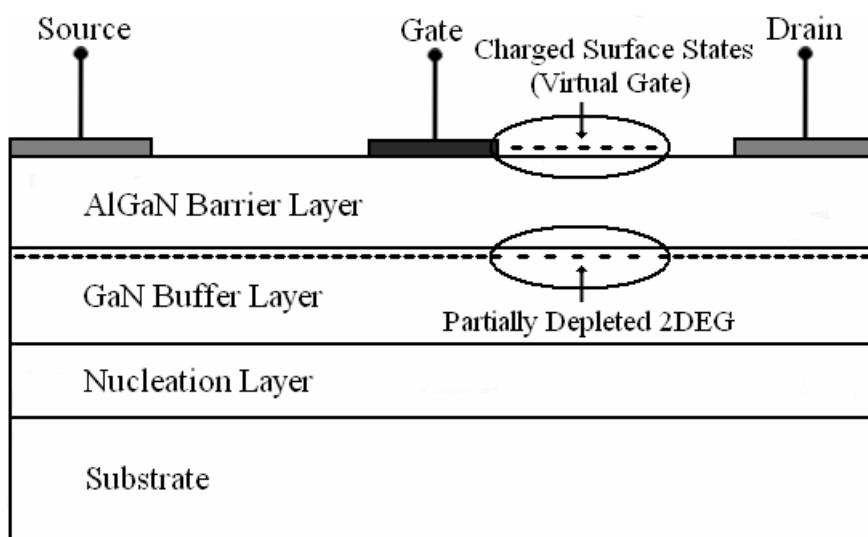


Figure 3.21 Schematic illustration of virtual gate formation in GaN HEMT devices.

In our fabrication process, SiN is used as a passivation material. Plasma enhanced chemical vapor deposition (PECVD) system is used to deposit SiN layer on our samples. Under 180sccm SiH₄ and 45sccm NH₃ process gases flow, 100nm thick Si₃N₄ is coated using 20W RF power.

Air-Bridge Post

Air-bridge fabrication starts with air-bridge post material lithography step. We use Su1828 photoresist for this photolithography process. Then, resist reflow process is applied at 150 °C for 10 minutes in order to achieve appropriate resist profile which is required for mechanically stable air-bridge formation. DekTak profilometer measurement results of an air-bridge post before and after the reflow process are given in Figure 3.22.

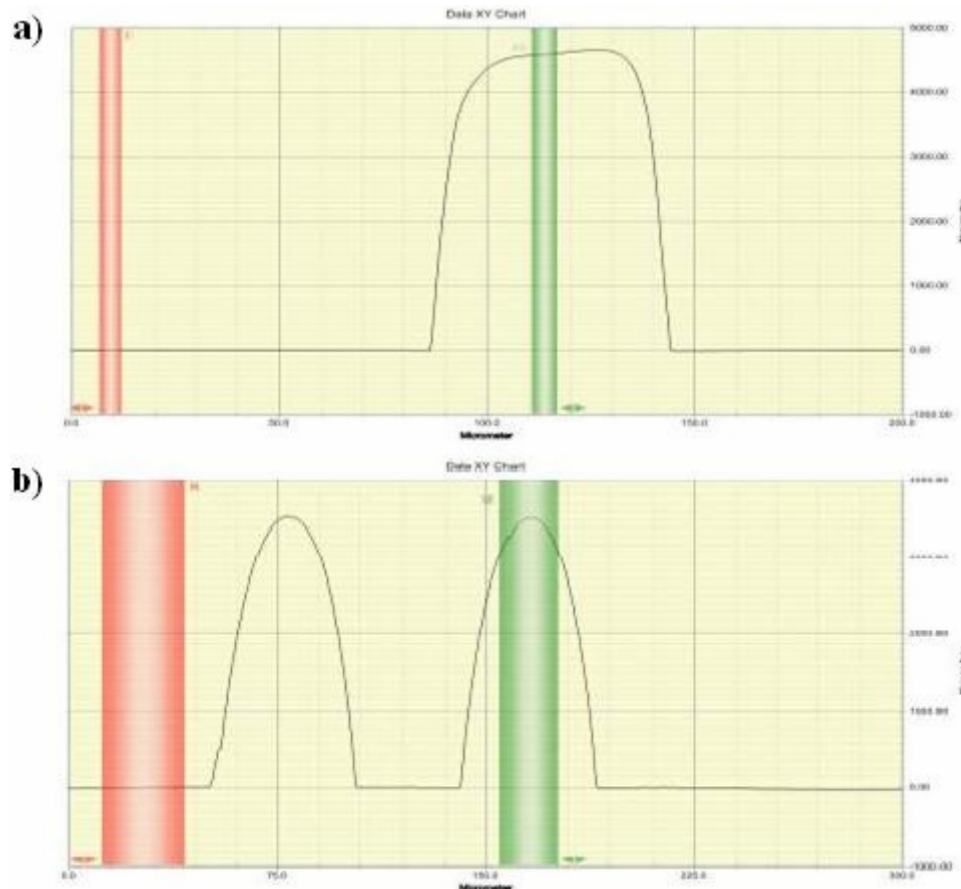


Figure 3.22 An air-bridge post profile before (a) and after (b) reflow process.

In Figure 3.23, some device photographs taken after air-bridge post step are given.

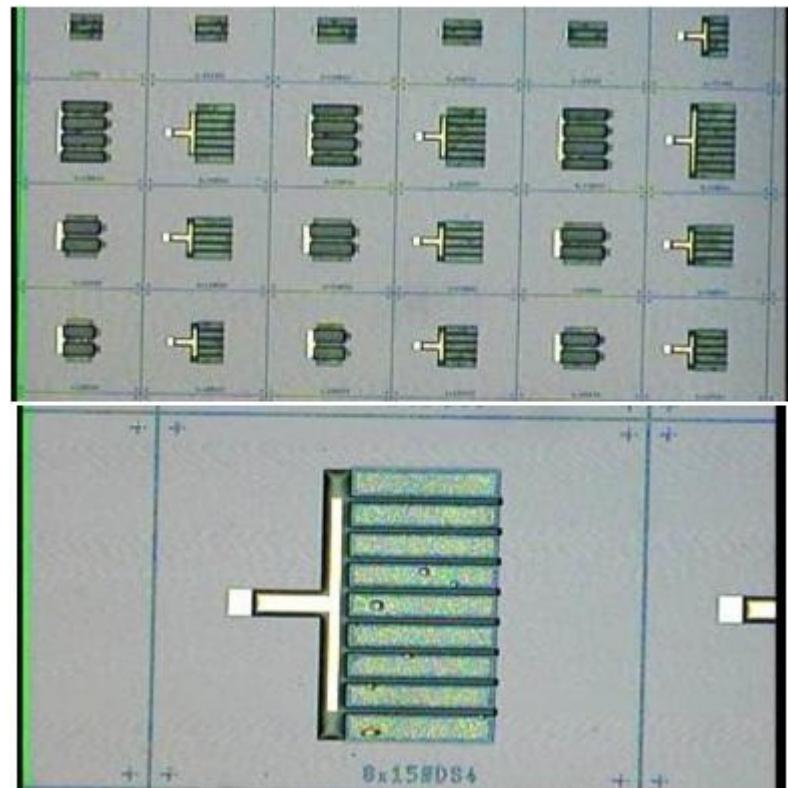


Figure 3.23 Some device photos after the air-bridge post step.

Seed Layer

As we explained before, seed layer is formed by evaporating Ti (500\AA) and Au (1500\AA) metals, respectively, in order to form a conductive sample surface which is required in electroplating process.

Air-Bridge

At this step, lithography process is done using TI35ES photoresist to form interconnect metallization patterns. Next, $\sim 2\text{um}$ thick Au electroplating is carried out.

Removal of the seed layer and air-bridge post

The seed layer is removed by HF wet etching technique after depositing 500Å thick Ti protection layer on top of the interconnect metallization. Removal of the seed layer is one of the most critical steps of the HEMT fabrication process. Photo of a device after this step is given in Figure 3.24. Air-bridge post material can be clearly seen in this photo.

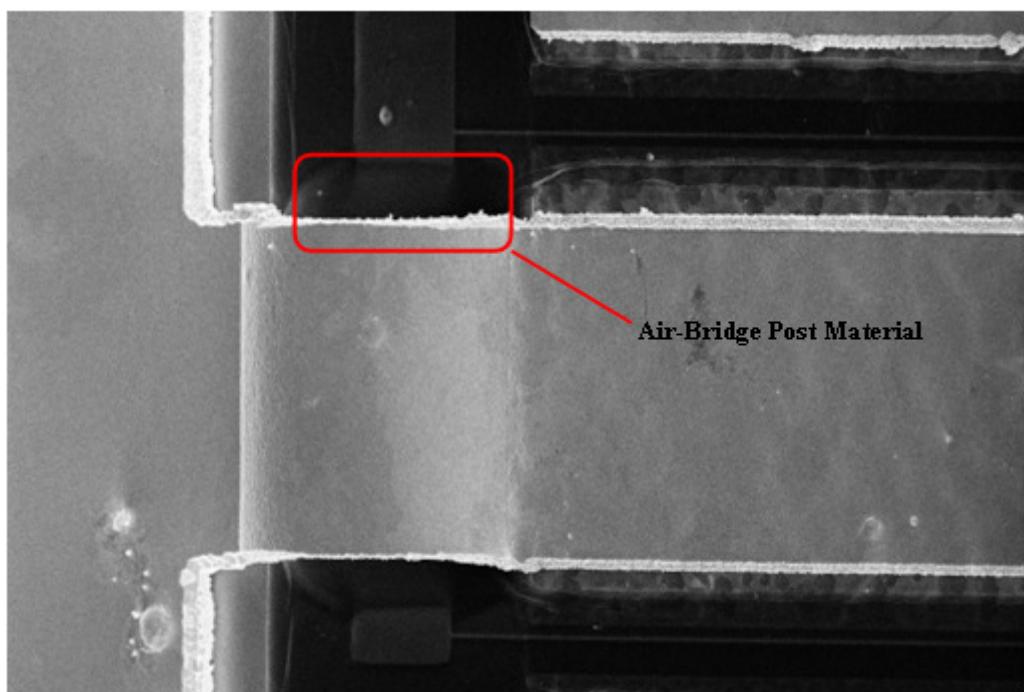


Figure 3.24 Photo of a device after the seed layer removal step.

Finally, air-bridge post is removed by keeping the samples in acetone. Additionally, ultrasonic cleaner assists the process for 10-15 seconds. After this step, the air-bridges are formed and our HEMT fabrication is completed. SEM photos of the air-bridges are given in Figure 3.25 and a microscope photograph of a fabricated 6x150µm HEMT device is shown in Figure 3.26.

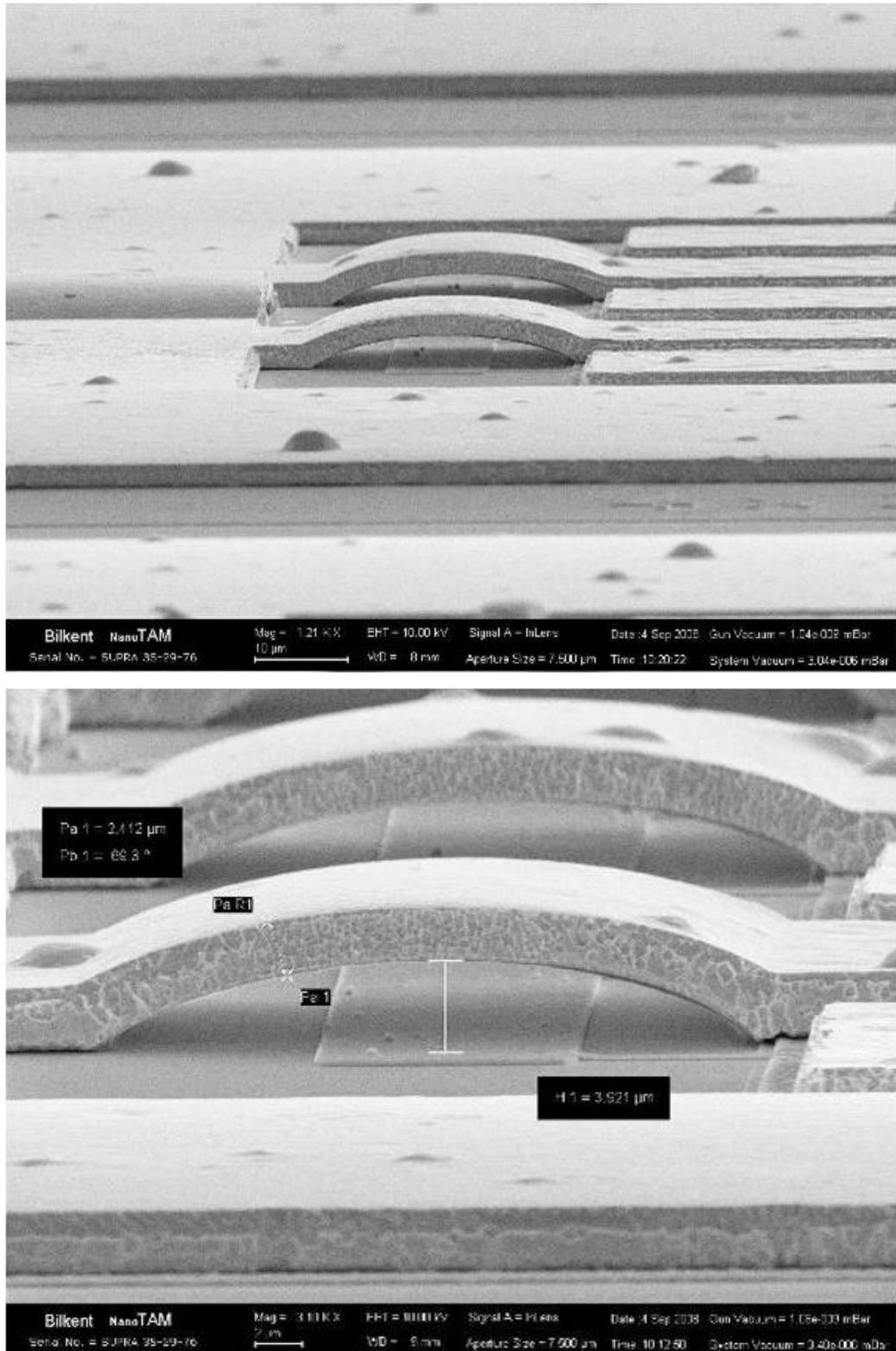


Figure 3.25 SEM photos of the fabricated air-bridges.

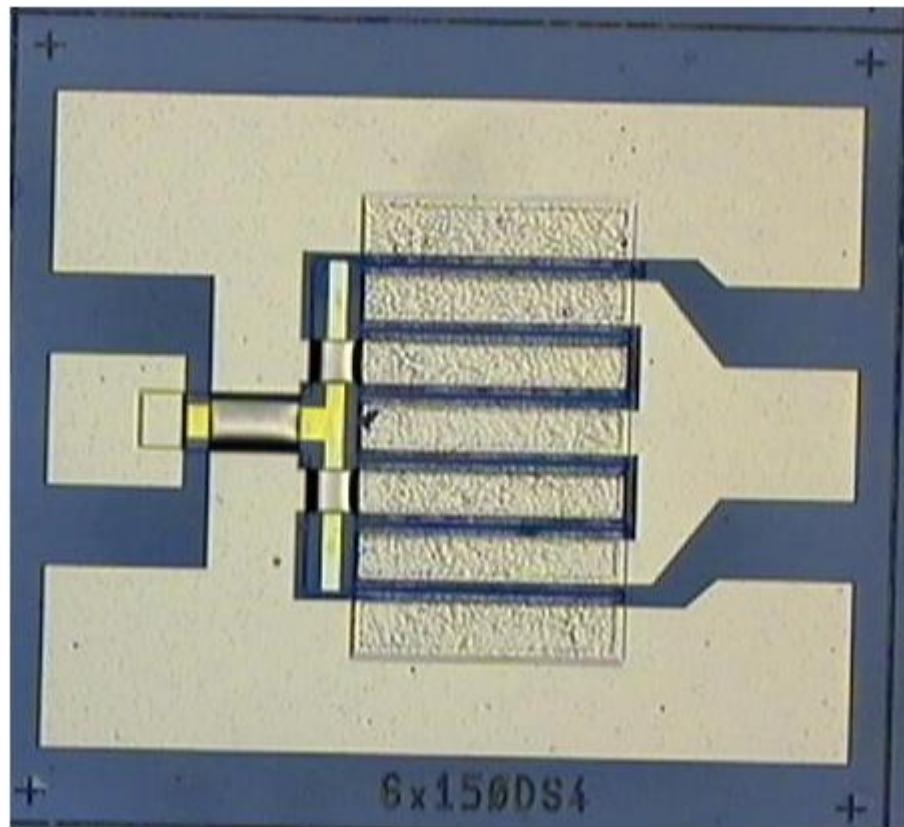


Figure 3.26 A photo of a fabricated HEMT device taken by microscope.

3.5 Characterization of the Fabricated GaN HEMTs

There are two main characterization techniques that we use for fabricated GaN HEMT devices. First one is DC characterization and second one is AC characterization. We cannot perform large-signal characterization since we do not have load-pull measurement setup in our labs.

Important device measures such as Pinch-off voltage, Knee voltage, maximum drain current, breakdown voltage, and DC transconductance are determined by DC characterization. We use a HP4142B modular DC source/monitor instrument and a probe station for performing DC characterization. Schematic of our DC measurement setup is shown in Figure

3.27. Drain, source and gate contacts of the transistor are probed in probe station and connected to corresponding ports of the HP4142B system. Using a GPIB connection, computer control over the setup is provided.

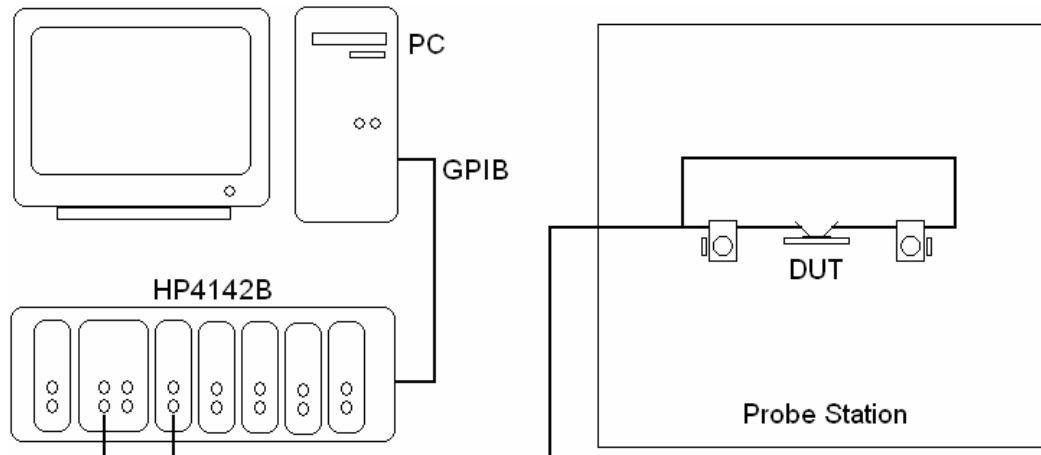


Figure 3.27 Schematic view of our DC characterization setup.

DC measurements are automated by a computer code. Gate and drain voltage ranges and number of measurement points are entered to the software. Gate bias is applied first and drain current is measured during drain voltage sweep between predefined values. This procedure is repeated for every gate bias step. A typical DC I-V graph is given in Figure 3.28.

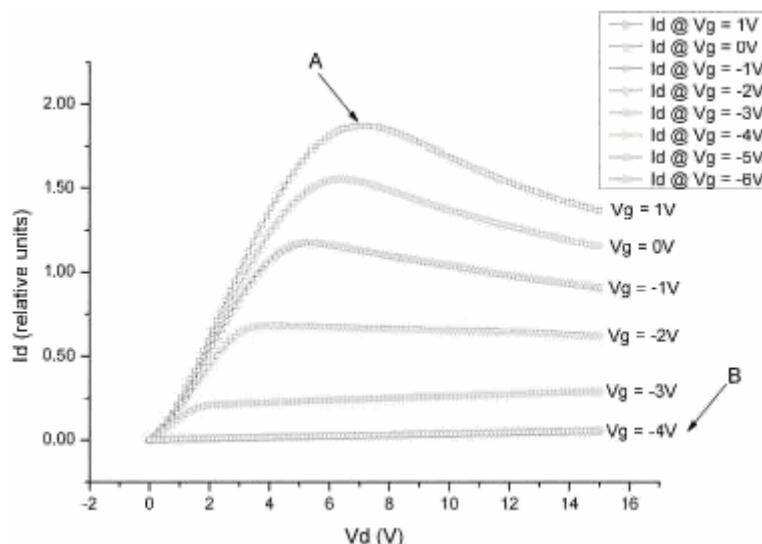


Figure 3.28 A typical DC-IV graph of GaN HEMT device.

Important DC characterization points are marked on Figure 3.28. Maximum drain current and knee voltage are read from point A which is located at the intersection of linear and saturation regions. Pinch-off gate voltage is determined from point B where the drain current is approximately equal to zero. The drain current changes negligibly at gate bias voltages less than the pinch-off voltage which indicates that 2DEG channel is totally depleted.

Breakdown voltage characterization is done while keeping the gate voltage less than the pinch-off voltage. Then, the drain voltage is increased until 10mA/mm drain current density is reached. At this point, recorded drain voltage corresponds to breakdown voltage by conventional definition.

DC transconductance ($g_{m,DC}$) is one of the important characterization measures and it is defined as follows;

$$g_{m,DC} = \frac{\Delta I_{DS}}{\Delta V_{DS}} \Big|_{V_{DC}=cons.}. \quad (3.6)$$

During the DC transconductance measurements, drain voltage is kept constant usually around the knee voltage, then; gate voltage is swept and corresponding drain current values are enrolled.

DC characterization results of 6x150μm and 4x150μm sample devices are given in Figure 3.29 and Figure 3.30, respectively. 902mA/mm maximum drain current density, breakdown voltage higher than 80V, 6.2V knee voltage, -4V pinch-off voltage, and 224mS/mm transconductance density are obtained from a 6x150μm device. 897mA/mm maximum drain current density, breakdown voltage higher than 60V, 5.5V knee voltage, -4V pinch-off voltage, and 230mS/mm transconductance density are obtained from a 4x150μm device.

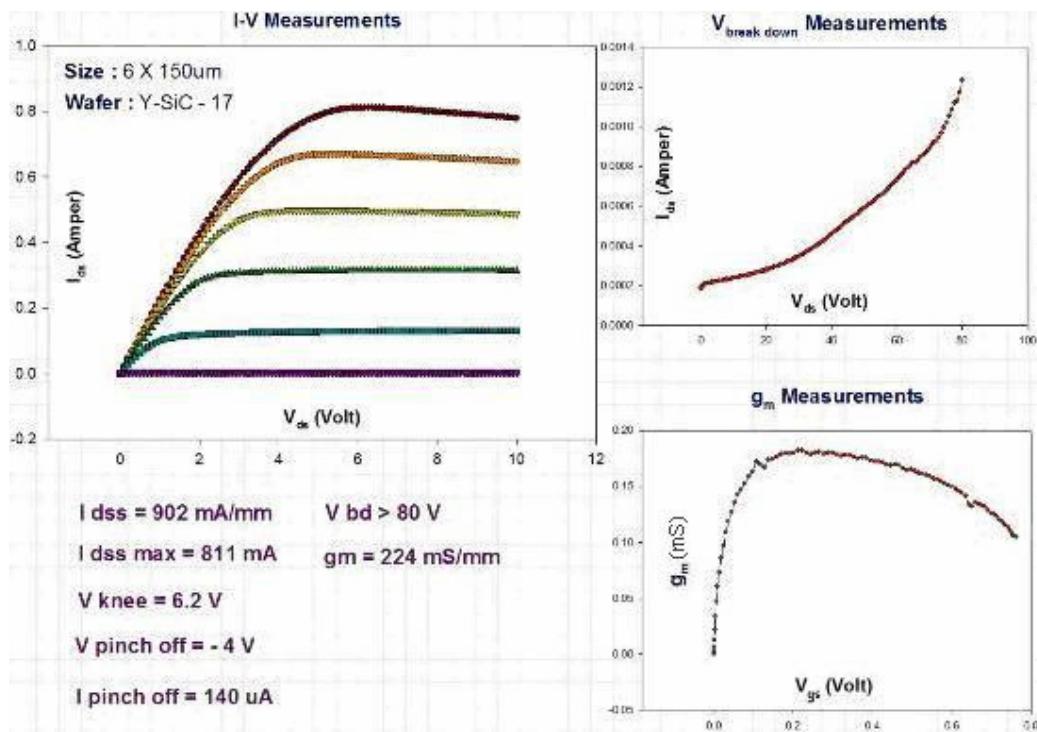


Figure 3.29 DC characterization results of a 6x150μm GaN HEMT device.

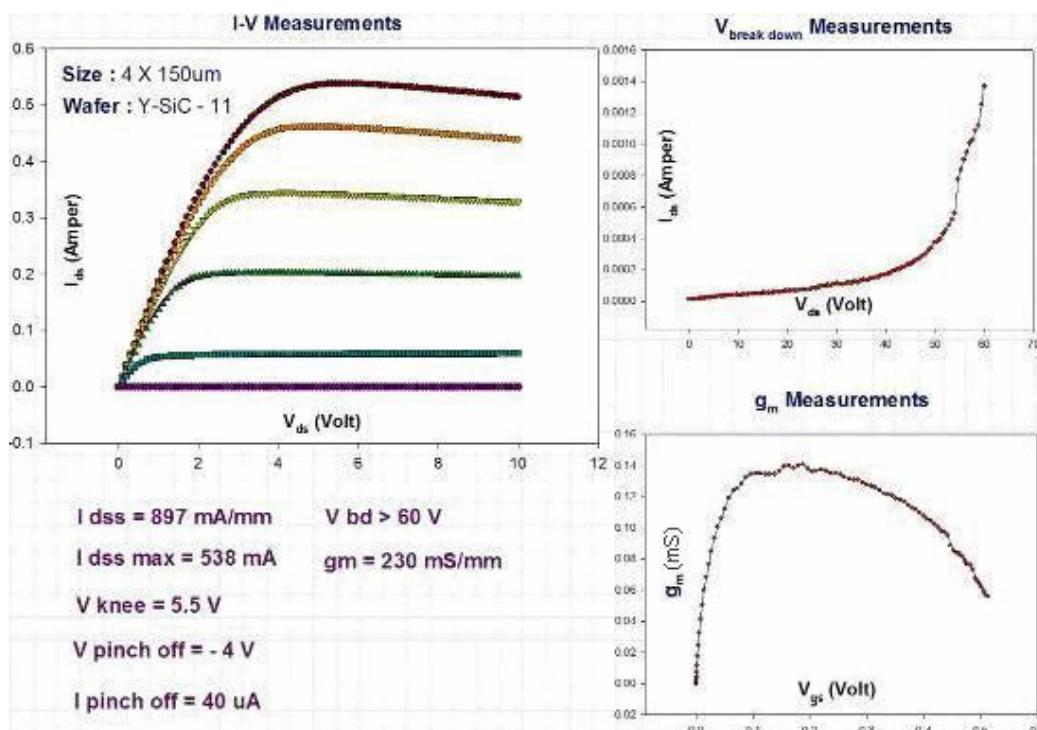


Figure 3.30 DC characterization results of a 4x150μm GaN HEMT device.

AC characterization is performed to determine current gain cut-off frequency (f_T) and power gain cut-off frequency (f_{max}) of an active device. AC characterization requires a Network Analyzer, a dual output DC power supply, and a probe station. Schematic view of an AC measurement setup is shown in Figure 3.31.

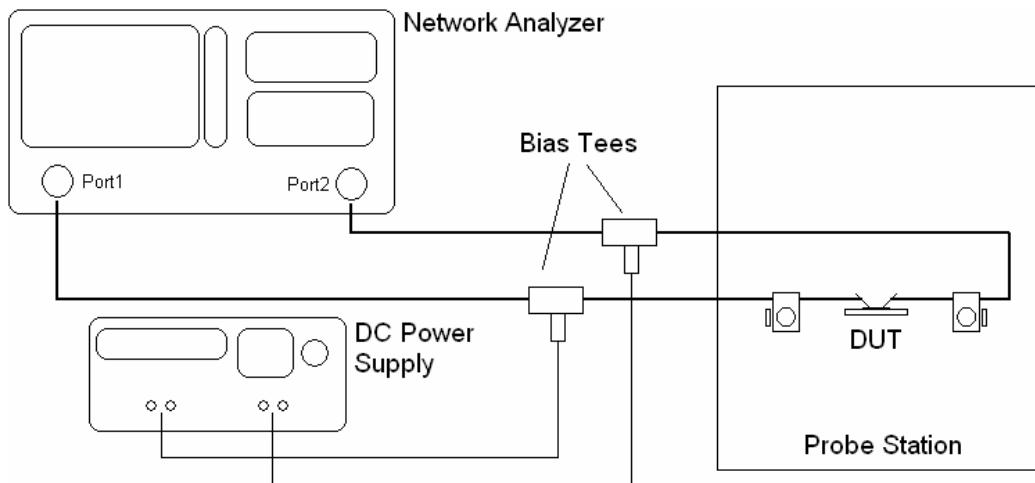


Figure 3.31 Schematic view of an AC measurement setup.

Network analyzer measures two port S-parameters for each frequency point in the range given. This process is repeated at all bias voltages of interest. Bias voltages are controlled by the dual port DC power supply and connected to the active device via bias tees.

H_{21} parameter is calculated from measured S-parameters in order to determine f_T of an active device. H_{21} formula with respect to S-parameters is given in (3.7) [76]. Calculated H_{21} parameter is plotted against frequency in dB scale and linear region at considerably lower frequency points of this plot is extrapolated to higher frequencies with an appropriate linear fit. Then, f_T is determined from 0 dB crossing of H_{21} parameter.

$$H_{21} = \frac{-2 \cdot S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}}. \quad (3.7)$$

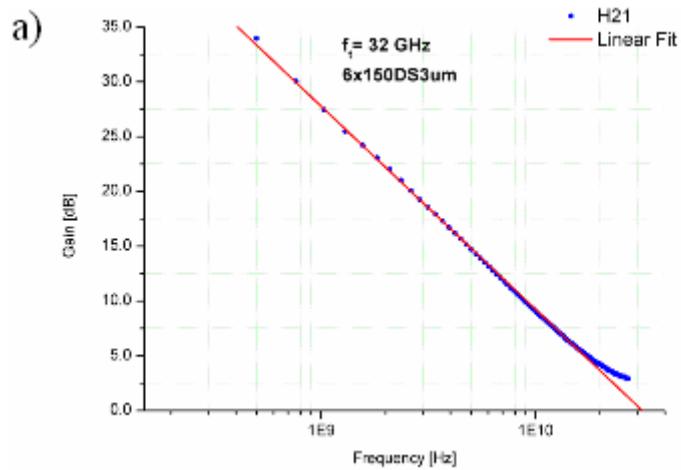
“ f_{\max} ” is defined as a frequency at which unilateral power gain (G_U) is equal to 1. The unilateral power gain is calculated with respect to the measured S-parameter as given in equations (3.8) and (3.9) [77]. Similar to H_{21} parameter case, calculated G_U is plotted against frequency in dB scale and linear region at considerably higher frequency points of this plot is extrapolated to higher frequencies with an appropriate linear fit. Then, f_{\max} is determined from 0 dB crossing of the unilateral power gain.

$$G_U = \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{2k \cdot \left| \frac{S_{21}}{S_{12}} \right| - 2 \operatorname{Re} \left(\frac{S_{21}}{S_{12}} \right)}, \quad (3.8)$$

where k is given as follows;

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2 |S_{12}| \cdot |S_{21}|}. \quad (3.9)$$

AC characterization results of the same $6 \times 150\mu\text{m}$ and $4 \times 150\mu\text{m}$ devices are given in Figure 3.32 and Figure 3.33, respectively. For the $6 \times 150\mu\text{m}$ GaN HEMT, 32GHz f_T and 40GHz f_{\max} are obtained. For the $4 \times 150\mu\text{m}$ GaN HEMT, 30.7GHz f_T and 49.7GHz f_{\max} are obtained.



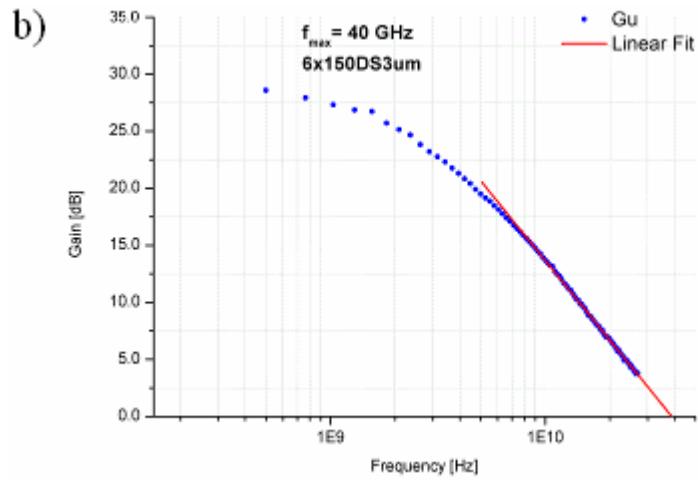


Figure 3.32 Current gain (a) and unilateral power gain (b) graphs of a 6x150 μm GaN HEMT.

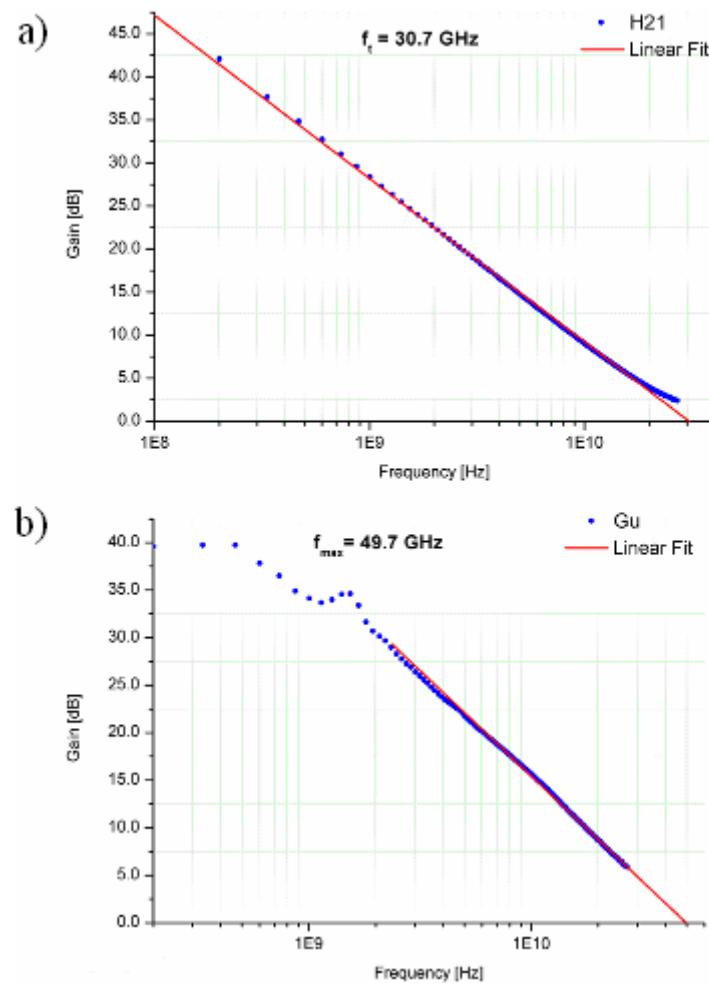


Figure 3.33 Current gain (a) and unilateral power gain (b) graphs of a 4x150 μm GaN HEMT.

Chapter 4

Compact Modeling Issues of HEMT Devices

In previous chapters we introduced the details of AlGaN/GaN HEMTs starting from semiconductor engineering details to fabrication steps and device characterization. Ultimate goal of developing AlGaN/GaN HEMTs is being able to acquire high performance MMICs which require accurate modeling of active devices. In this work, particularly, we deal with high power amplification which means transistors operate under large-signal conditions promoting nonlinear behavior. In order to design MMIC PAs, we need nonlinear large-signal model of AlGaN/GaN HEMT devices which contains nonlinear behavior of the transistor precisely at high power levels and for all possible operation conditions such as bias points and environment temperature.

Before going into details of nonlinear large-signal modeling, it is worth to mention about small-signal linear modeling which forms the basis of nonlinear modeling. Furthermore, small-signal model provides information about gain, bandwidth, stability and noise characteristics of the active device. On the other hand, limitations of this model should be kept in mind. For instance, small signal model reflects the behavior of the transistor for very low signal levels so that the load line stays in the vicinity of the DC bias point.

4.1 Small-Signal Linear Modeling of HEMTs

The small-signal linear models are based on the S-parameter measurements taken under various bias conditions. In order to have a connection between the measurements and the electrical properties of the active device, electrical equivalent circuit (EEC) of the small-signal model is proposed based on typical HEMT device characteristics as illustrated in Figure 4.1. EEC contains bias independent parasitic inductances, capacitances and resistances which are called extrinsic elements of the transistor. Elements in the dashed rectangle define the bias dependent transistor behavior and they are called intrinsic elements.

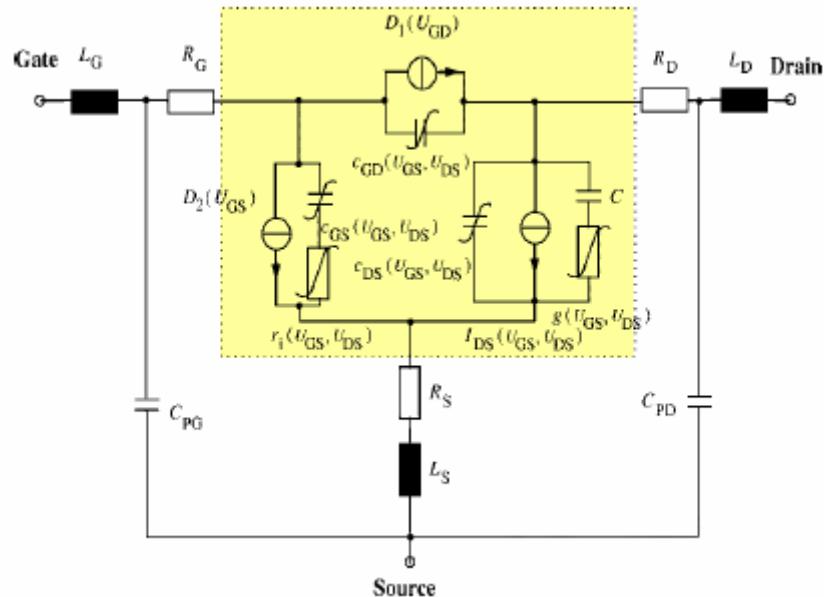


Figure 4.1 The bias dependent small-signal equivalent circuit of the HEMT device.

These EEC elements need to be extracted systematically using the S-parameter measurements as follows: Extraction methodology starts with determination of the extrinsic elements using two S-parameter measurements under “*cold*” conditions ($V_{DS}=0V$). For the extraction of parasitic capacitances “*pinched cold*” S-parameters ($V_{GS} < V_{pinch-off}$, $V_{DS}=0V$) are used. Specific form of the EEC under this bias condition is shown in Figure 4.2a. Due to the resulting “ Π ” shape

configuration, imaginary parts of the Y-parameters of this EEC are considered. Consequently, at low frequency, parasitic capacitances can be determined by linear fitting since resistances and inductances are eliminated under these conditions. Next step is the extraction of parasitic inductances and resistances under “*gate forward cold*” conditions ($V_{GS} > 0V$, $V_{DS} = 0V$). Corresponding EEC is given in Figure 4.2b. In this case, Z parameters are taken into account due to the “T” shape nature of the EEC. Imaginary parts of the Z parameters are used to determine inductances. We have 4 unknown resistances and 3 resistance equations from real parts of the Z-parameters. Additional required information about parasitic resistances is taken from real part of the Z_{22} under “pinched cold” condition. As a result all the extrinsic elements could be extracted based on simple S-parameter measurements.

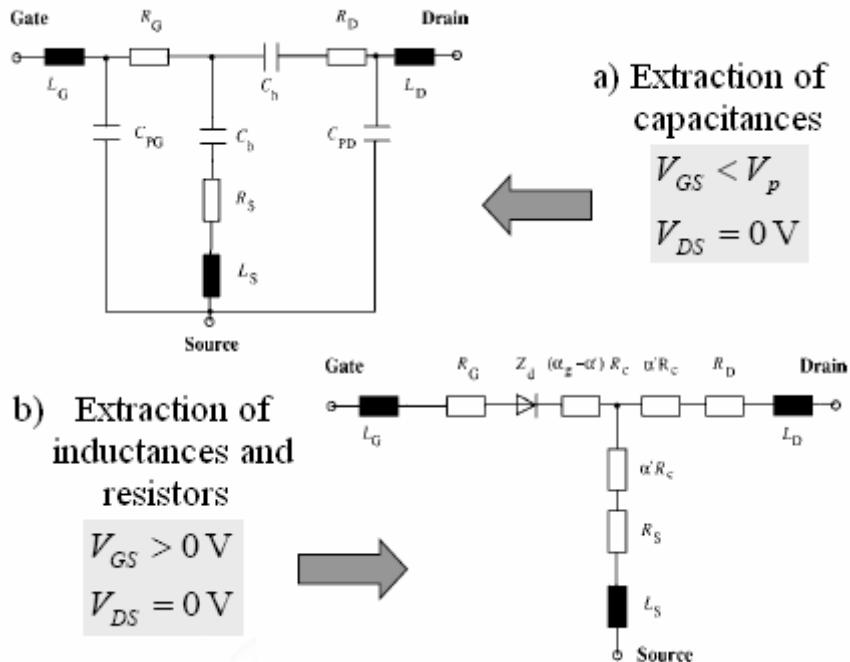


Figure 4.2 Summary of extrinsic element extraction procedure, and corresponding EECs under (a) “pinched-cold” and (b) “gate forward cold” conditions.

Before proceeding to the intrinsic parameter extraction step, extrinsic elements need to be de-embedded properly from the S-parameter measurements starting

from outer extrinsic elements to inner ones as summarized in Figure 4.3. First, S-parameters are converted Z-parameters and series elements L_G and L_D are subtracted. Then, resulting Z-parameters are converted to Y-parameters and parallel elements C_{PG} and C_{PD} are subtracted. Finally, updated Y-parameters are converted back to Z-parameters and series elements R_G , R_D , R_S and L_S are subtracted.

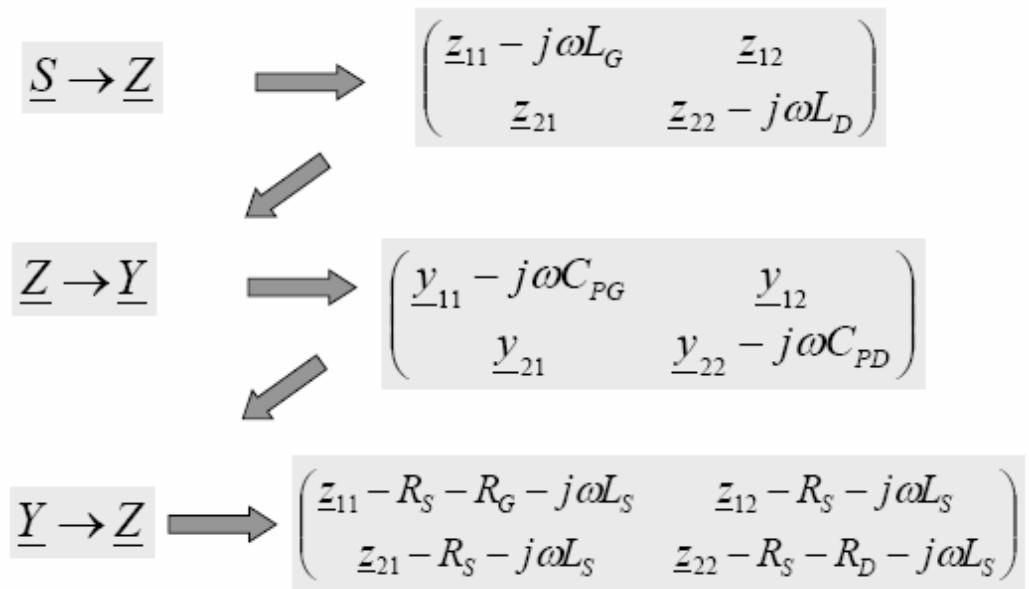


Figure 4.3 Steps of extrinsic elements de-embedding.

Now we can start bias dependent intrinsic parameter extraction by converting the final form of Z-parameters to Y-parameter since intrinsic EEC has “ Π ” topology. Similar to determination of extrinsic elements, intrinsic elements are extracted by parameter fitting. Additionally, this process is repeated for all measured bias conditions in order to determine bias dependent intrinsic parameters. As a result, broadband bias dependent small-signal model is completed. This kind of model requires optimization process for each element during extraction steps which allows the model simulation results fit best to the measurement data. Small-signal modeling is very important issue and will be addressed in the large signal modeling part which will be explained next.

4.2 Large-Signal Nonlinear Modeling of HEMT Devices

There are several methods of large-signal nonlinear modeling, namely, physical models, analytical models and table-based models. We will explain each technique shortly.

Physical models:

The best and proper way of understanding the HEMT device operation principles rely on physical properties of semiconductor materials used in epitaxial structure, carrier transport properties of 2DEG, and the device geometry. Physical models require the data mentioned above (e.g. density of states and dislocations, bandgap energies, polarization properties, doping concentrations, saturated electron velocity and electron mobility in the channel, material growth and fabrication process parameters, and dielectric constants) in order to estimate the overall device performance [78], [79], [80], [81], [82], [83], however, these information about the active device need to be very accurate that can be obtained by using sophisticated measurement methods. Nevertheless, physical modeling can be very effectively used for improving immature device technology including epitaxial design and fabrication processes.

Self consistent solution of Schrödinger and Poisson's equations are the basic tools of physical modeling. Analytical formulas and/or numerically solved nonlinear partial differential equations, describing the internal field distribution, charge transport, current continuity and energy conservation, are used in physical equations in order to obtain the model [84], [85], [86], [87].

Physical models are very time consuming in terms of computation complexity and their results are not directly compatible with circuit simulators. Hence, physical models are generally not appropriate for the circuit design purpose.

Analytical models:

Contrary to physical models, analytical models are based on measurement data of active devices. On the other hand, transistor physics related analytical functions representing measured quantities are used to form the model; however, these functions are not always directly related with the physical properties of the transistor. Hence, some physical effects are not considered compared to physical models. Moreover, there are severe limitations on proposing global analytical functions which accurately represents nonlinear behavior of the active device for all operation points.

The measurement data consist of DC or “pulsed” I-V and CW or “pulsed” S-parameters under various bias points. These data are interpreted by using electrical equivalent circuit as explained in small signal linear modeling. Nonlinear model is constructed using extracted intrinsic elements and corresponding analytical functions.

This modeling approach is compatible with circuit simulators and able to simulate beyond the measurement range conceivably due to the analytical function behavior of the model. On the other hand, this technique is technology dependent and requires some understanding in the device modeling process for circuit designers to have effective design cycle. Furthermore, analytical models have limited accuracy and difficulty in extraction of the model fitting parameters having no physical meaning.

Table-based models:

Table-based models are solely based on measurement data. Unlike analytical models, there is no need for predefined equations describing the transistor behavior which means this type of modeling is more accurate and technology independent. Measured data are interpolated and smoothed by using

multidimensional spline functions. Table-based nonlinear model is represented by large signal electrical equivalent circuit as shown in Figure 4.4. First small signal counterparts of the circuit elements are extracted. Then, nonlinear element functions are derived by integrating over bias dependent differential equations determined from measurement data. In this modeling technique, charge conservation and model consistency between the large signal and the small signal conditions are the critical issues that are needed to be handled carefully. Table-based modeling approach is first proposed by Root [88]. Later on it was improved by the use of time delay in charge formulation [89].

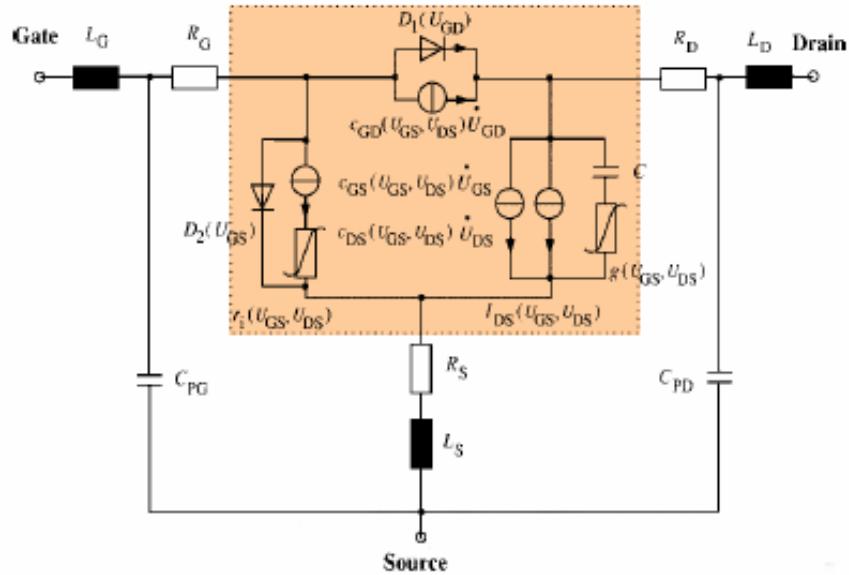


Figure 4.4 The large-signal electrical equivalent circuit of the HEMT device.

In this thesis we followed the table-based modeling technique in order to obtain a nonlinear large-signal model of our 4x200umx1um AlGaN/GaN HEMT on sapphire substrate. To do so, TOPAS (Transistor Parameter Scalable model) software developed by IMST GmbH is used. TOPAS is a kind of table based model which produces very promising results compared to other modeling techniques. There are various advantages of this type of nonlinear modeling: no need for time consuming very complex and expensive large signal

characterization tools, fast implementation, every measured characteristic of the device can be transferred into the model accurately without having physical interpretation of the device behavior, extracted model is directly compatible with circuit simulators, small-signal excitation of large-signal simulations are consistent with S-parameter measurements. Based on our GaN HEMT model extraction, details of the nonlinear large-signal table-based modeling using TOPAS software are given in the next subsection.

4.3 Large-Signal Nonlinear Model Extraction of Our GaN HEMT Using TOPAS Software

We have already mentioned about electrical equivalent circuit phenomena and extraction of extrinsic and intrinsic elements based on S-parameter measurement data taken at various bias points in small-signal linear modeling section. We will further explain step by step how to build a table-based large signal model.

First, we will focus on measurement requirements for appropriate large-signal modeling. For devices suffer from excessive self heating effects and high channel temperature such as GaN HEMTs, “pulsed” I-V and “pulsed” S-parameter measurements are vital for appropriate large-signal modeling. Temperature variation should be discarded from measurements in other words measurements have to be taken under isothermal conditions in order to correctly determine the nonlinear element functions with respect to bias voltages so that these functions can be integrated over large-signal path. CW isothermal measurements can be taken at points on constant power curves; however, measurement data taken over a single constant power curve is not enough to evaluate the compact device model for broad range of use. Moreover, CW measurements can be taken at only limited portion of the I-V region due to the thermal constraints of the device. Fortunately, “pulsed” measurement technique is an efficient solution to all of these problems faced in CW case. In pulsed measurement system bias voltages are kept at quasi bias points between

consecutive pulses such that device is in “pinched-off” or “cold” state. Power consumption is nearly zero at quasi bias points. Correspondingly, channel temperature of the device can be assumed to be equal to the ambient temperature.

Two types of pulsed measurements are possible, namely, dual-pulse type and single-pulse type. In dual-pulse type system both gate and drain voltages are pulsed. This technique is very effective for AlGaN/GaN HEMT modeling since it allows considering the gate and drain related trapping effects in addition to the temperature effects. The quasi gate bias has the control over surface state trapping effects. On the other hand, buffer trappings effects are examined by sweeping the quasi drain bias while keeping the quasi gate bias less than pinch-off point. Single-pulse type instrument applies pulses only on gate side and adjusts drain voltage to the corresponding I-V point. Since the drain side is biased continuously in this system, the quasi gate bias is kept under pinch-off voltage in order to get rid of thermal variations. Unfortunately, single-pulse type measurements are not appropriate for devices having significant trapping behavior; however, they are still convenient for temperature dependent large signal modeling. We performed measurements of our devices in IMST GmbH.

They have single-pulse type measurement setup as illustrated in Figure 4.5.

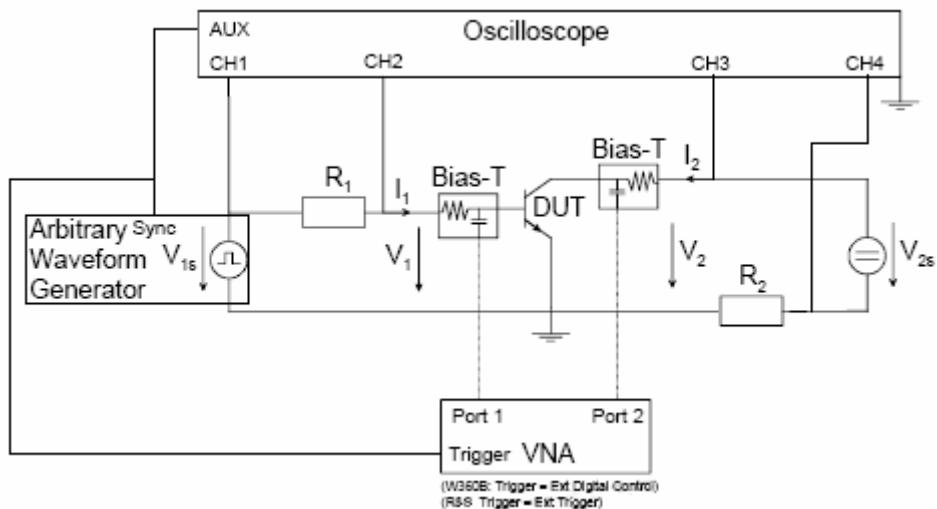


Figure 4.5 Schematic illustration of the single-pulse type measurement setup in IMST GmbH.

We selected our best devices in hand at that time showing negligible trapping effects for consistent nonlinear large-signal model extraction. We could not perform temperature dependent measurements due to the limited visit time we had in IMST GmbH. Instead, “pulsed” I-V and “pulsed” S-parameter measurements were taken under 1155 bias points at room temperature. In order to take measurements faster than temperature time constants we need comparably short pulse duration. Measurement instant versus voltage and current values should be accurately monitored so that measurement quantities have already settled to their steady-state positions and temperature effects have not come into the picture during the measurement interval which is down to 100ns using high speed VNA of Rohde & Schwarz ZVA with option ZVA-K7 in IMST GmbH RF measurement lab. Figure 4.6 shows the photo of this high speed VNA. Also, duty cycle of the pulses is adjusted according to recovery time of the thermal states. In our measurements, pulse width and duty cycle are taken around 1 μ s and 1%, respectively. Moreover, having dense measurement points on I-V domain increases model accuracy and results in better representation of nonlinear characteristics of the device.

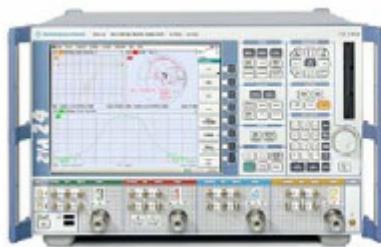


Photo: Rohde & Schwarz

Figure 4.6 Photo of the Rohde & Schwarz ZVA high speed VNA used in IMST GmbH

Next step is extraction of the small-signal equivalent circuit elements as basically explained in the beginning of this chapter. TOPAS software is used for every step of the model extraction. The software has a user friendly interface which guides the user throughout the model generation. First, extrinsic elements

are extracted and optimized using linear optimizer tool of the TOPAS. Corresponding screenshot is shown in Figure 4.7.

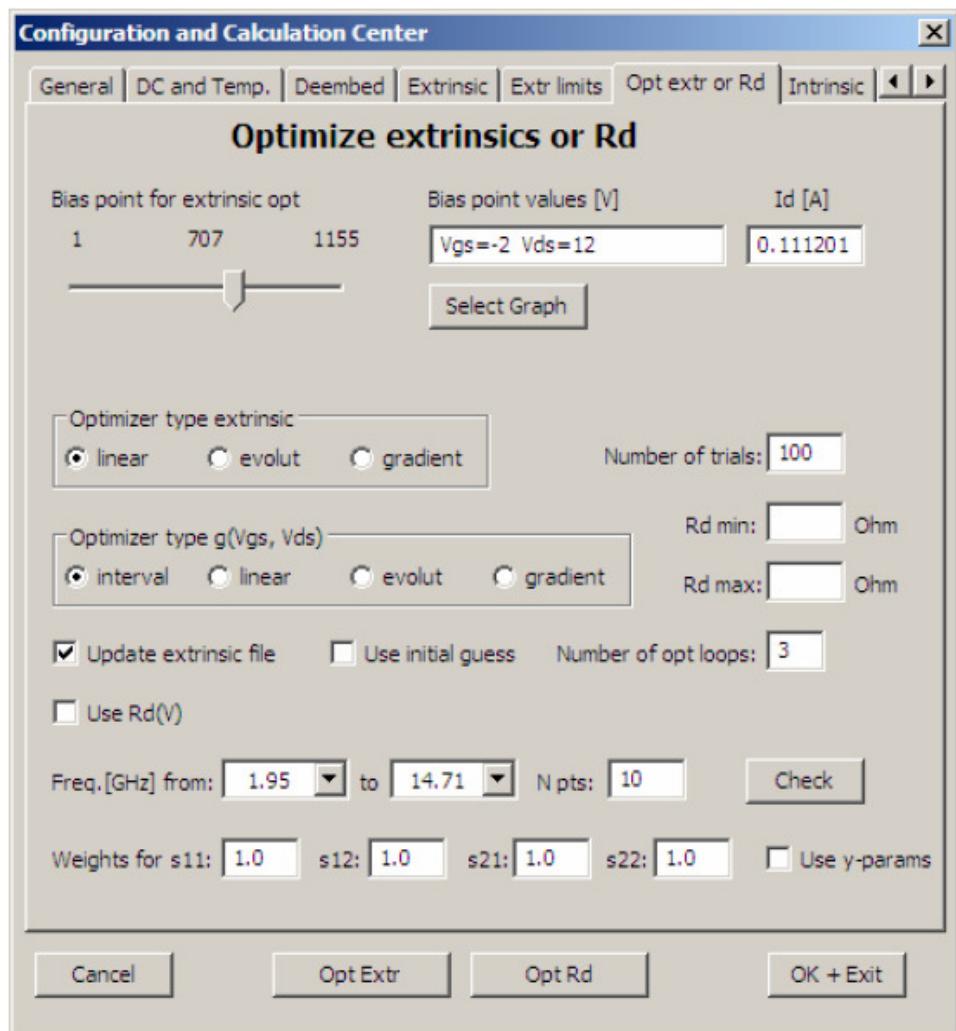


Figure 4.7 Screenshot of the extrinsic element optimization window on TOPAS.

Before proceeding to the intrinsic element extraction, extrinsic elements are automatically deembedded from the measurement data. Next, extrinsic elements are extracted with respect to bias voltages after required settings are adjusted as shown in Figure 4.8. Here we apply iterative approach for the intrinsic element extraction process. Frequency intervals in the settings window are updated by considering extracted results beforehand in order to obtain better fit to

measurement data at all bias points. Then, optimization of the intrinsic elements is carried out in the software.

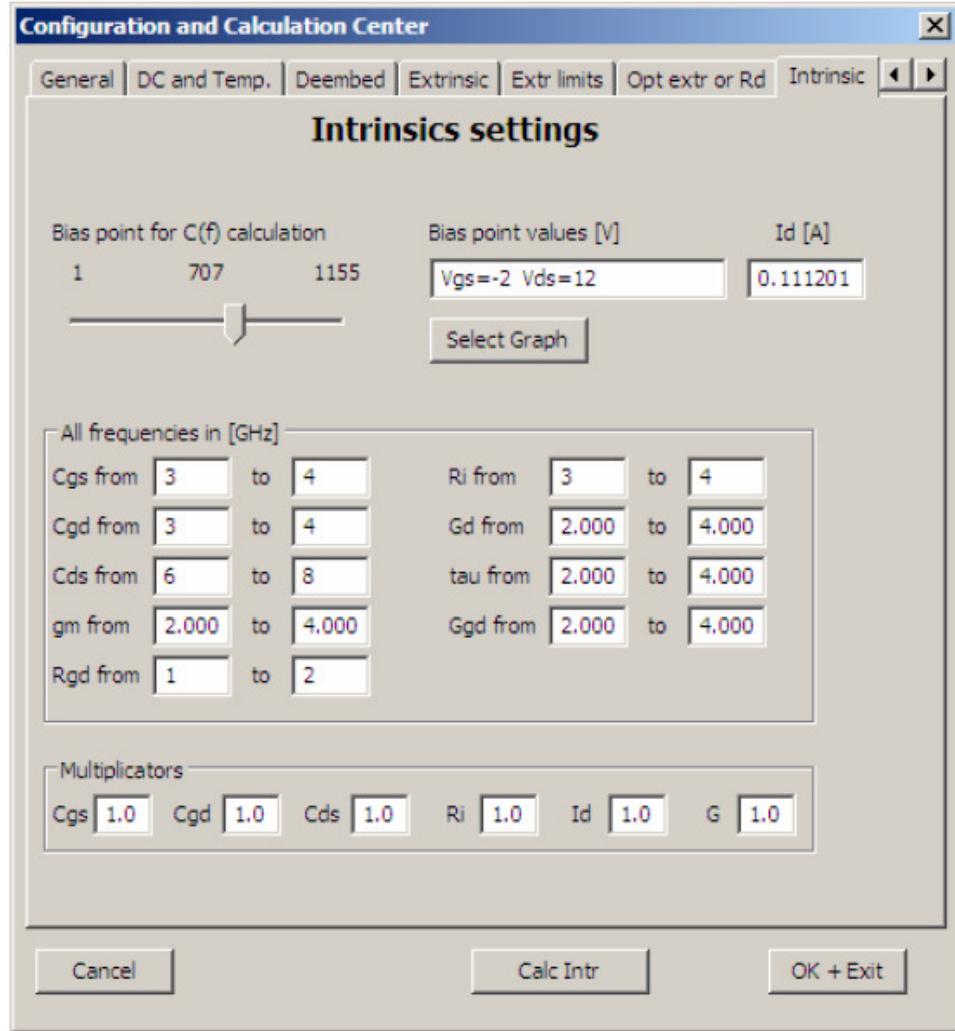


Figure 4.8 Screenshot of the intrinsic elements settings window on TOPAS.

One final step remains that is relating intrinsic parameters with inner (actual) bias voltages via voltage de-embedding ignoring gate current I_G before the calculation of the nonlinear model parameters. Equations of the inner voltages with respect to the outer voltages and drain-source current I_{DS} are given as follows [90];

$$V_{GS}' = V_{GS} - I_{DS}(V_{GS}, V_{DS}) \cdot R_S, \\ V_{DS}' = V_{DS} - I_{DS}(V_{GS}, V_{DS}) \cdot (R_D + R_S). \quad (4.1)$$

For the sake of completeness of the large-signal model, bias dependent continuous nonlinear function of each intrinsic element is generated using spline interpolation technique carried out in the TOPAS software. We should make a remark on an important point here. Spline calculations require equidistant input data, however, resulting inner bias voltages calculated from (4.1) have non equidistant grid. This problem is solved by using two one-dimensional spline interpolations for gate and drain bias voltages so that equidistant grid is formed.

In the next step, nonlinear model parameters are calculated based on the intrinsic element functions dependent on the bias voltages. As we mentioned earlier, in general integral method is used in these calculations. In TOPAS, an easier way is followed to make these calculations by converting the charge sources into their equivalent current sources. Need for transcapacitances in the small-signal equivalent circuit is avoided with the usage of this technique since a charge source calculation by integrating over a capacitance depending on two bias voltages is not required. Resulting equations representing the large-signal current sources caused by the charges on the large-signal capacitances c_{GS} , c_{GD} and c_{DS} are given as follows [91];

$$I_{GS} = c_{GS}(V_{GS}, V_{DS}) \cdot \dot{V}_{GS}, \quad (4.2)$$

$$I_{GD} = c_{GD}(V_{GS}, V_{DS}) \cdot \dot{V}_{GD}, \quad (4.3)$$

$$I_{DS} = c_{DS}(V_{GS}, V_{DS}) \cdot \dot{V}_{DS}. \quad (4.4)$$

The large-signal capacitances are related to their small-signal counterparts using Taylor series expansion. In addition to the current sources mentioned above, drain current source is extracted by the measured “pulsed” I-V curves, $I_D(V_{GS}, V_{DS})$.

During the large-signal nonlinear model calculations charge conservation and model consistency issues are considered so that TOPAS model does not generate unphysical results and inconsistency problems in circuit simulators. Furthermore, better harmonic balance simulation convergence behavior is

obtained owing to conservative extrapolation techniques used for regions out of the measurement data. At the final stage of the TOPAS model generation, information obtained about the equivalent circuit is saved in a simulation file that can be read by Agilents' Advanced Design Simulator (ADS).

4.4 Validation of the Large-Signal Nonlinear GaN HEMT Model

Large-signal nonlinear model validation process consists of two main steps. The first one is model consistency check, and the next one is large-signal behavior control using load-pull measurements.

The extracted model consistency is validated by comparison of measured and simulated S-parameters. Our nonlinear large-signal AlGaN/GaN HEMT model shows very good agreement with the measurements under low signal levels. This consistency holds for every measured bias point.

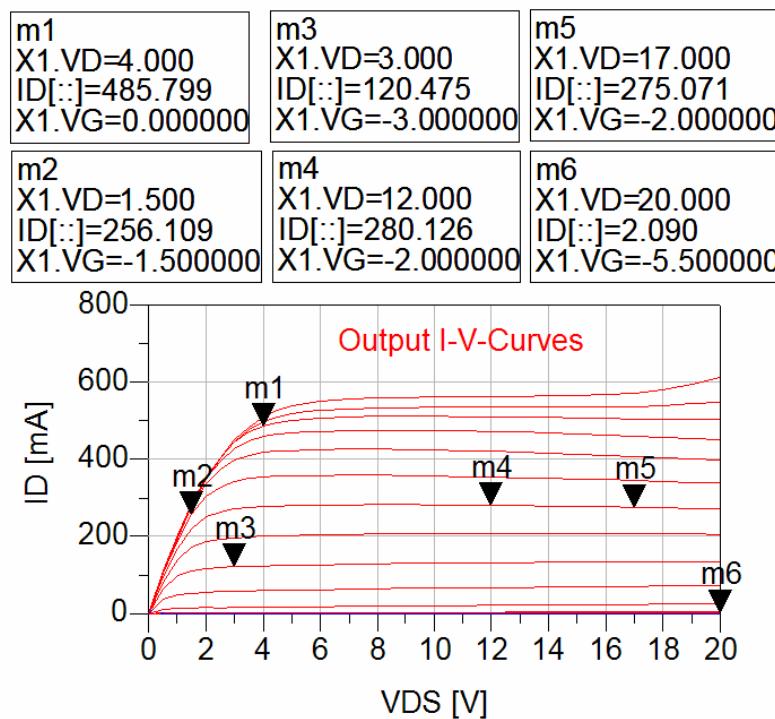


Figure 4.9 Output I-V Curves of the modeled GaN HEMT

We will demonstrate our model consistency for various bias points. Output I-V graph is given in Figure 4.9. Six bias points are indicated on this graph in purpose. In the following Figures 4.10-15, S-parameter comparison of the model and measurements is given for each highlighted bias point, respectively.

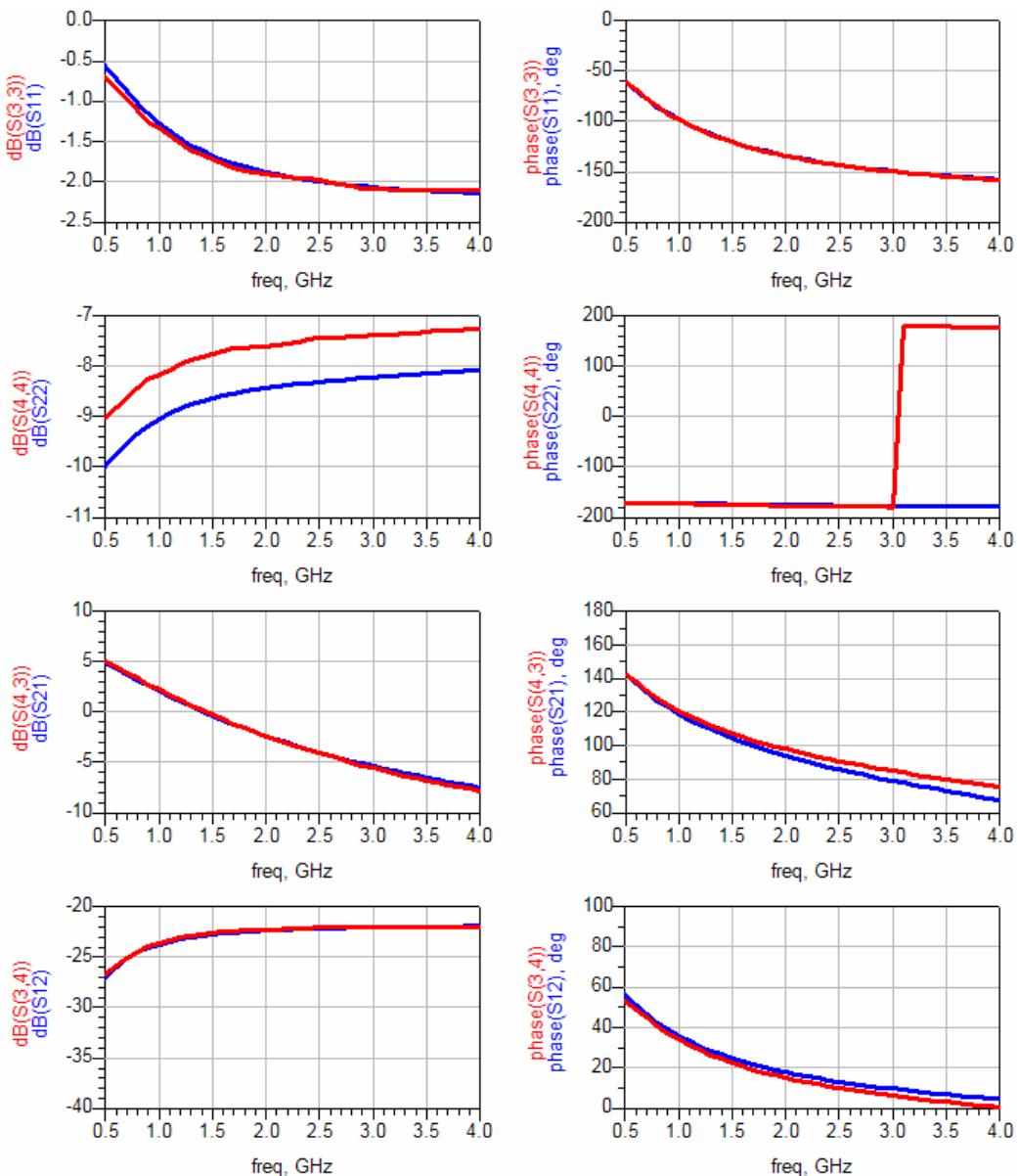


Figure 4.10 Comparison of measured (red curves) and simulated (blue curves) (using nonlinear TOPAS model) S-parameters at bias point “m1” ($V_{GS}=0V$, $V_{DS}=4V$).

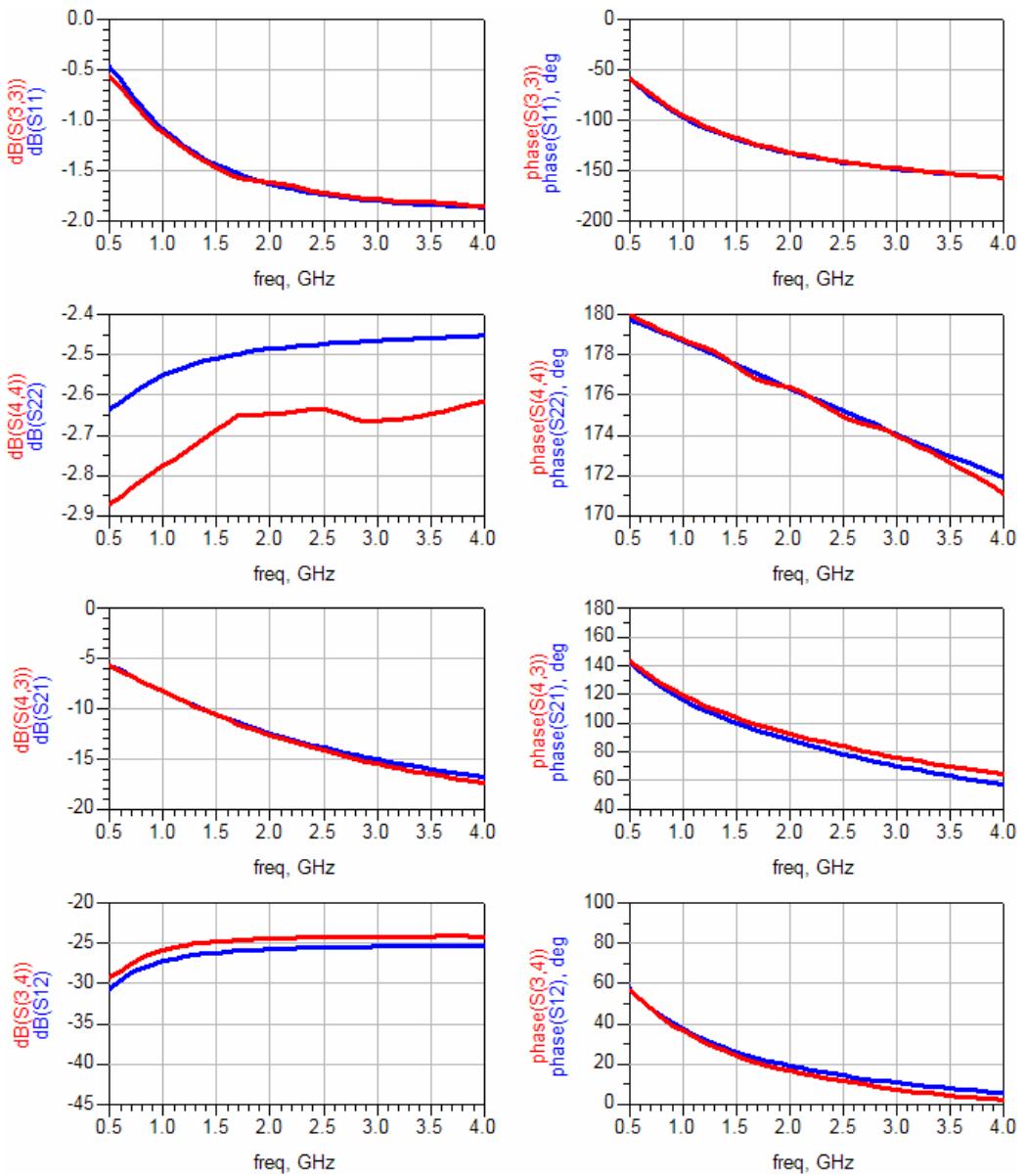


Figure 4.11 Comparison of measured (red curves) and simulated (blue curves) (using nonlinear TOPAS model) S-parameters at bias point "m2" ($V_{GS}=-1.5V$, $V_{DS}=1.5V$).

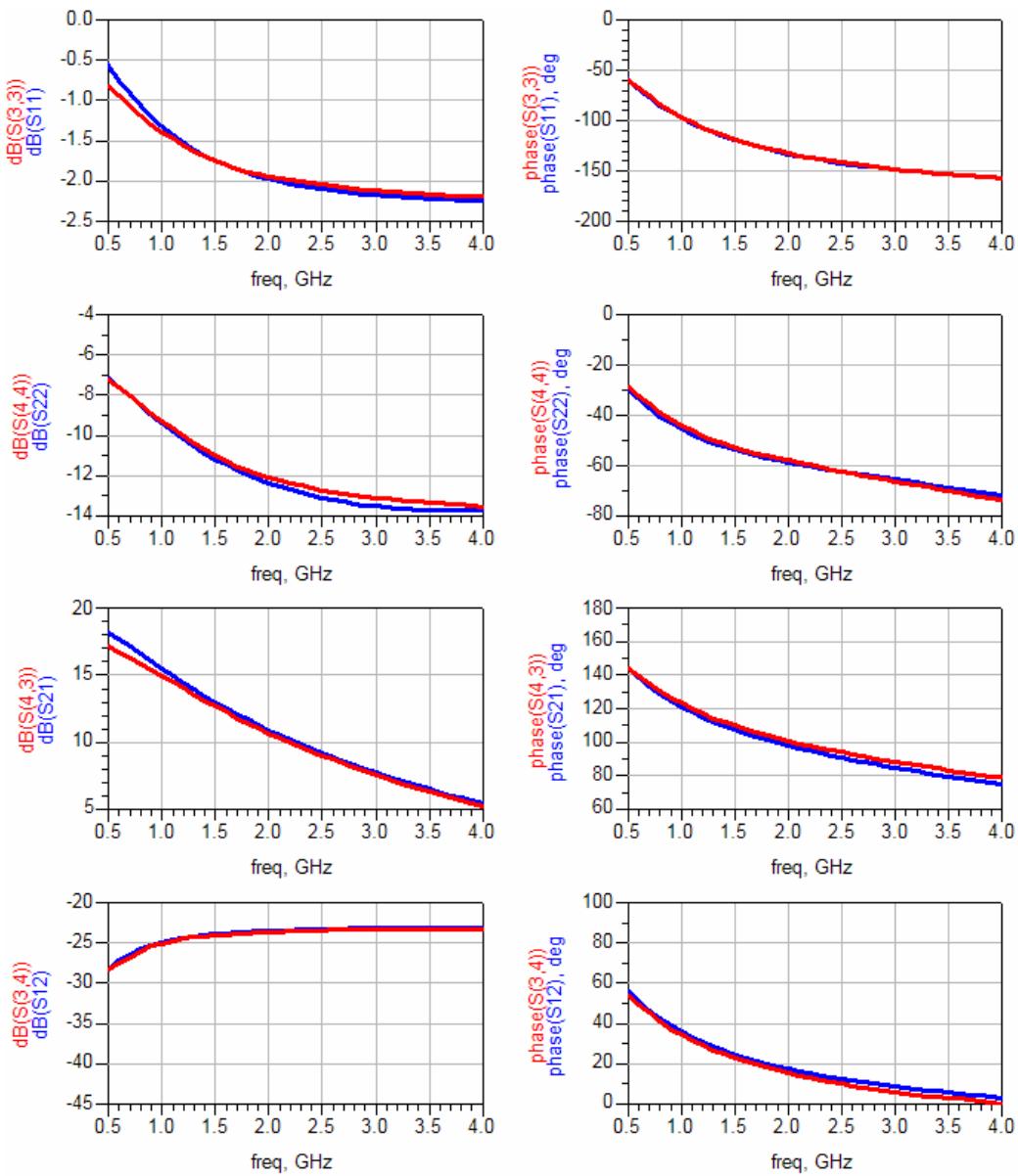


Figure 4.12 Comparison of measured (red curves) and simulated (blue curves) (using nonlinear TOPAS model) S-parameters at bias point “m3” ($V_{GS}=-3V$, $V_{DS}=3V$).

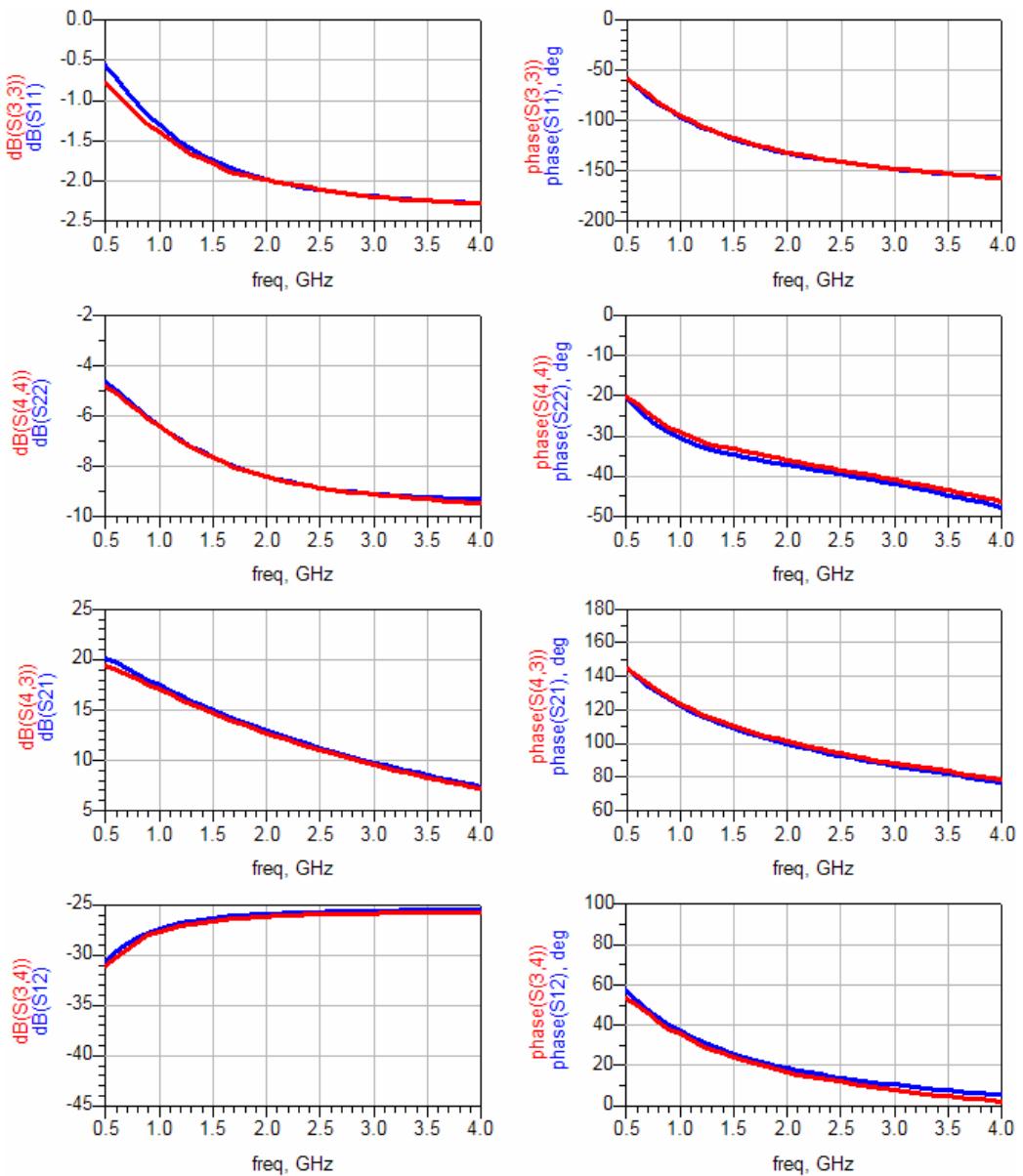


Figure 4.13 Comparison of measured (red curves) and simulated (blue curves) (using nonlinear TOPAS model) S-parameters at bias point “m4” ($V_{GS}=-2V$, $V_{DS}=12V$).

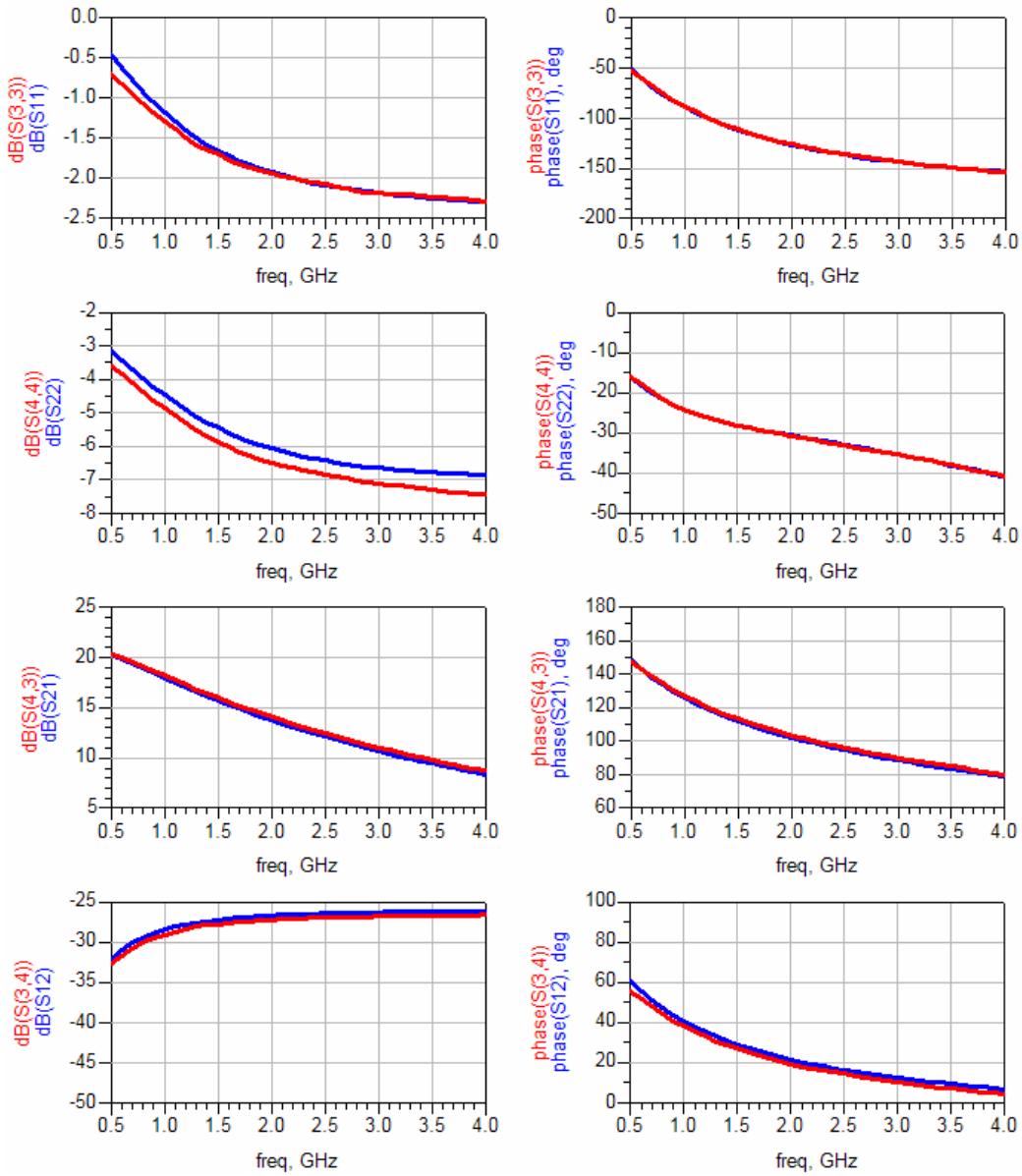


Figure 4.14 Comparison of measured (red curves) and simulated (blue curves) (using nonlinear TOPAS model) S-parameters at bias point “m5” ($V_{GS}=-2V$, $V_{DS}=17V$).

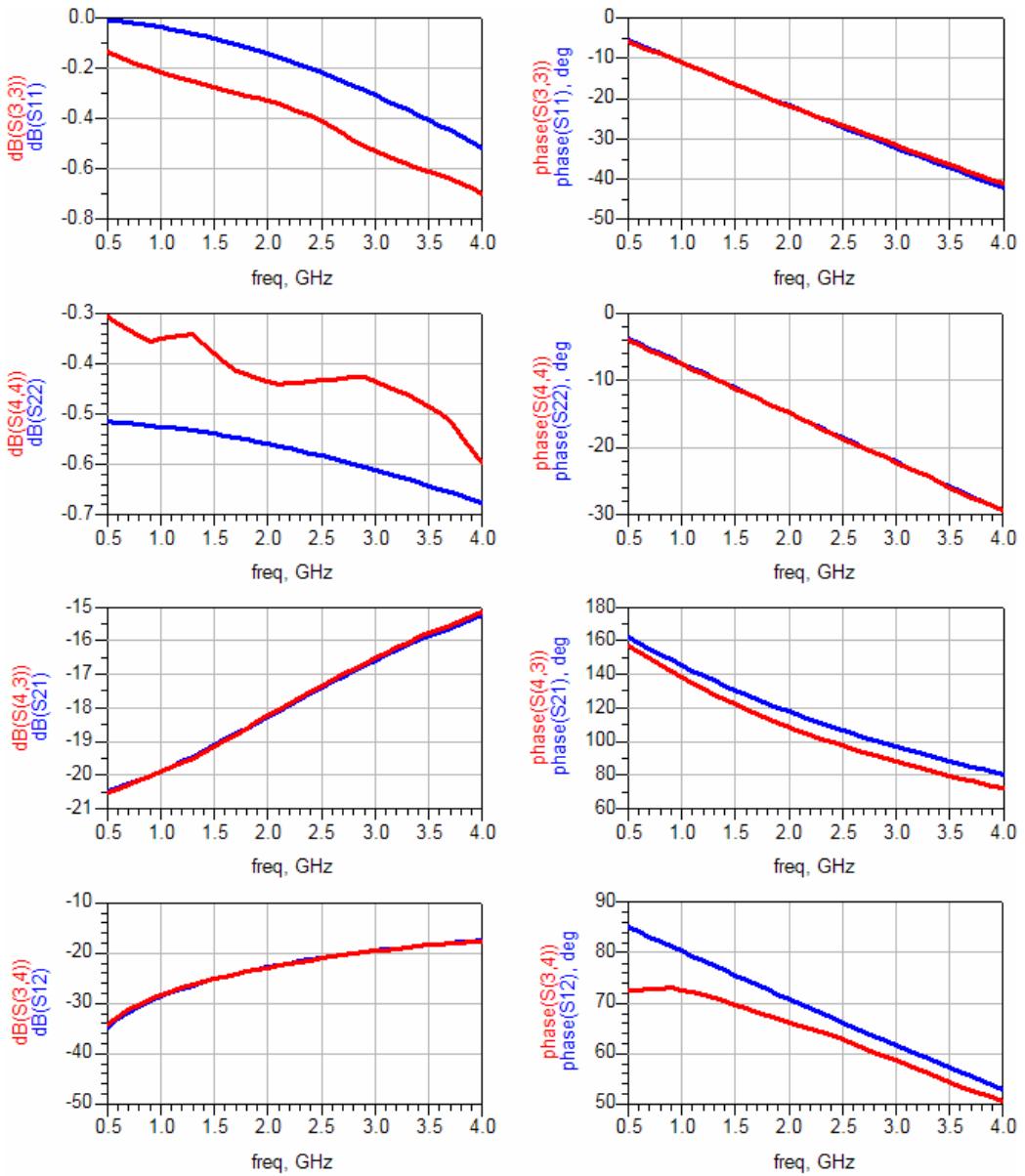


Figure 4.15 Comparison of measured (red curves) and simulated (blue curves) (using nonlinear TOPAS model) S-parameters at bias point “m6” ($V_{GS}=-5.5V$, $V_{DS}=20V$).

These S-parameter measurement and model simulation comparison results show that our model matches very well with the S-parameter measurements under low-signal levels. Hence, the model consistency is validated.

In order to check the model correctness under large-signal levels, we performed load-pull measurements in IMST GmbH and at the same time harmonic balance simulations were carried out using the model under the same conditions with the measurements.

Load-pull measurements were taken at 2GHz and under CW conditions due to the measurement limitations of the setup. Bias voltages were adjusted as $V_{GS} = -2V$, $V_{DS} = 10.1V$. Optimum power load and source impedances were found to be $(89.69 + j50.12)$ Ohm and $(17.90 + j34.01)$ Ohm, respectively, from the measurements. Load-pull and source-pull simulations of the large-signal model give similar results for the optimum power load and source impedances. This fact shows that our model can predict large signal impedances with fair accuracy which is an indication of good nonlinear behavior representation of the device. Based on this agreement, we simply used the impedance values determined from the measurements as load and source terminations in the harmonic balance simulation.

At this point, we should keep in mind that our model is based on the pulsed S-parameter measurements taken at only one ambient temperature (room temperature) and does not contain self heating effects. On the other hand, CW large signal measurements are subjected to excessive heat generation in the channel which in turn causes current collapse and degradation in output power. As a result, we do not expect that harmonic balance simulations of our model can correctly represent the CW large-signal measurements. The measurement and simulation results of output power and power gain are plotted in Figure 4.16. As we explained above, we observe mismatch in power gain around 2-4dB between the measurement and simulation results.

As a conclusion, our model is not totally valid for CW circuit design; however, it can still represent the large-signal impedances correctly and can be

used for CW circuit design if overestimation of output power is considered carefully. On the other hand, even if we do not have pulsed large-signal measurement results in hand, we can safely conclude that our model is valid for circuit designs under pulsed bias conditions. In the next chapter, we will give the details of coplanar MMIC power amplifier designs at 2GHz using our GaN HEMT model.

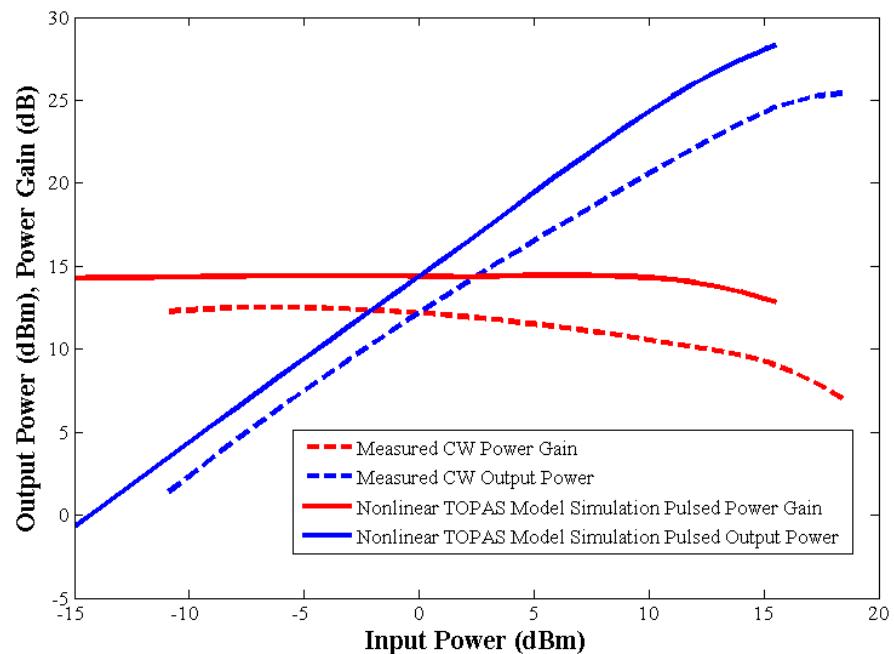


Figure 4.16 Output power and power gain comparisons between our GaN HEMT “pulsed” large-signal model and CW power measurements.

Chapter 5

2GHz GaN HEMT Coplanar MMIC Power Amplifier Designs

This chapter contains coplanar waveguide (CPW) MMIC power amplifier (PA) design steps based on our applications using our own GaN HEMT large-signal model which we derived in previous chapter and COPLAN software of IMST GmbH. We will demonstrate two designs that are single stage. The first one has a single transistor and the other one has two transistors in parallel in order to obtain as twice as output power compared to first design. According to simulation results, at 2GHz, ~2W and ~4W output powers, and ~42% and ~35% power added efficiencies are obtained for aforementioned designs, respectively. We will start with the explanation of general PA design considerations and continue with our specific design steps. Finally, simulation results will be given and discussed.

5.1 PA Design Considerations

There are various PA design approaches called classes of operation which are dependent on the bias voltages and the output termination impedance of transistor [92], [93], [94]. Class-A, Class-AB, Class-B, and Class-C PAs are analog-mode classes of operation defined in terms of conduction angle, that is, the portion of the RF signal cycle corresponds to which the transistor is in the

conduction state. The conduction angle is a function of the quiescent bias point and input drive level. Output load impedance is determined according to the maximum output power condition for all analog-mode classes of operation. Transfer characteristics, conduction angles and active load-lines of analog-mode PAs are shown in Figure 5.1. Additionally, active load-lines of Class E and Class F PAs which will be explained later are illustrated in the same figure.

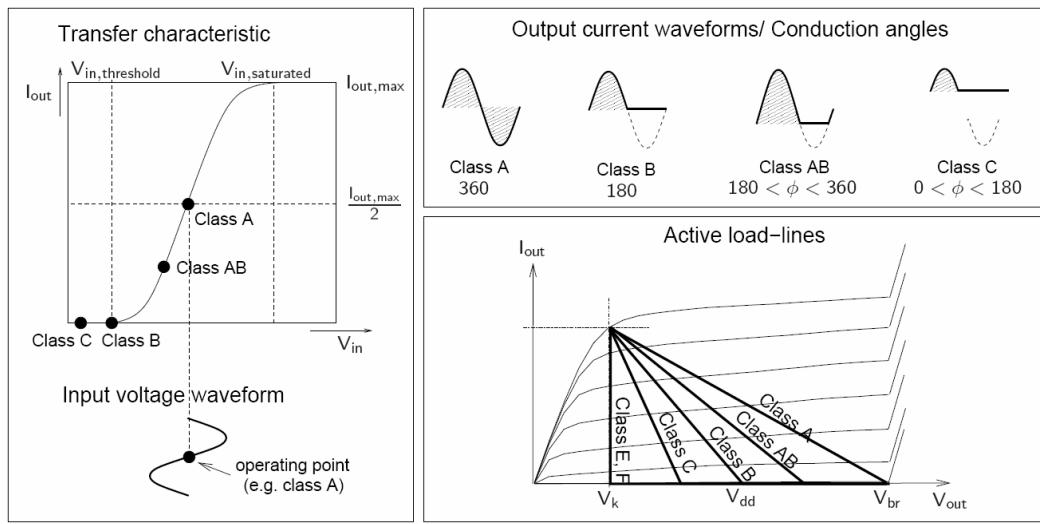


Figure 5.1 Important properties of various PA classes of operation.

Other classes of operation such as Class D, Class E and Class F are switch-mode designs. Although very high power added efficiency (PAE) levels can be reached using these PA designs, they exhibit low power gain, narrow frequency band, and strong nonlinearity. Hence, switch-mode PA designs are not considered in this work.

Among all analog-mode PA design techniques, Class A operation is selected for our designs. First of all, highest large signal gain and most linear output signal are attained with Class A configuration. Moreover, Class A operation is appropriate for wideband applications and the only possible mode able to work at frequencies which are significant fractions of f_{max} . This technique is relatively simple in terms of design and construction. Drawbacks of this class of operation

are 50% theoretical PAE limit and consequent heat dissipation. Input and output signal swings and load-line for Class A operation are illustrated in Figure 5.2 in more detail.

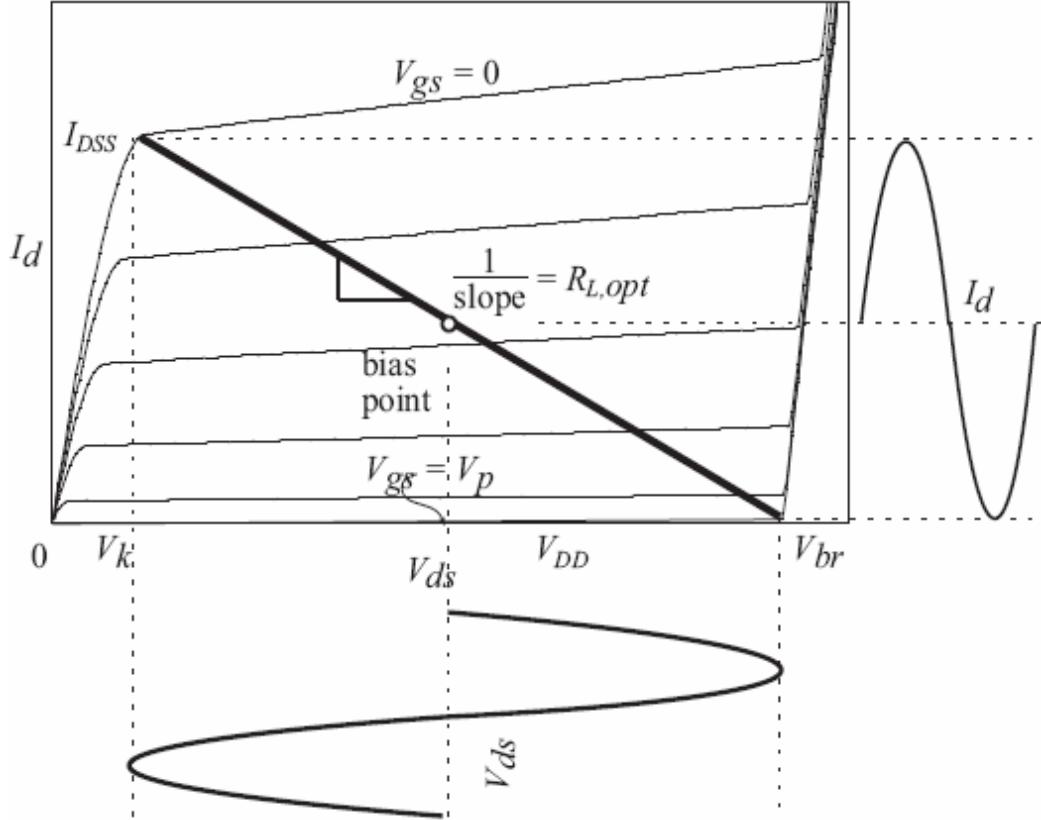


Figure 5.2 Illustration of input and output signals and load line for Class A PA.

After determination of PA operation mode, large-signal output and source impedances of the device are established by load-pull and source-pull simulations in order to obtain maximum output power from the device. This is an iterative approach such that load-pull simulations are affected by source impedance termination and source-pull simulation results are dependent on load impedance termination since the device has limited isolation between input and output ports. Initially, we set the source impedance to a low value as expected to be. Then, we start first load-pull simulation and get optimum load impedance of this case. Next, the output impedance is fixed at that final value and source-pull simulation is carried out. Using extracted source impedance value we repeat the

same steps starting from load-pull simulation until no significant improvement point is reached in output power. Final values of output and source impedances, PAE and output power are recorded as a reference for next steps of the design.

In RF and microwave electronic systems reference impedance is selected as 50Ω according to well known reasons [95], [96]. Predefined optimum output and source impedances should be transformed to 50Ω environment by output matching network (OMN) and input matching network (IMN), respectively. DC feeds of the PA are supplied via gate bias network (GBN) and drain bias network (DBN). Bias networks reject RF signals at frequency band of interest and carry DC voltages and currents. DC blocking capacitances are used at both input and output paths in order to prevent DC current flows out of the device. Besides, stability of the amplifier should be guaranteed over all frequencies independent of any source or load impedance variation. This requirement is called unconditional stability and should be met with additional lossy network if necessary. Sample schematic of single stage amplifier is shown in Figure 5.3.

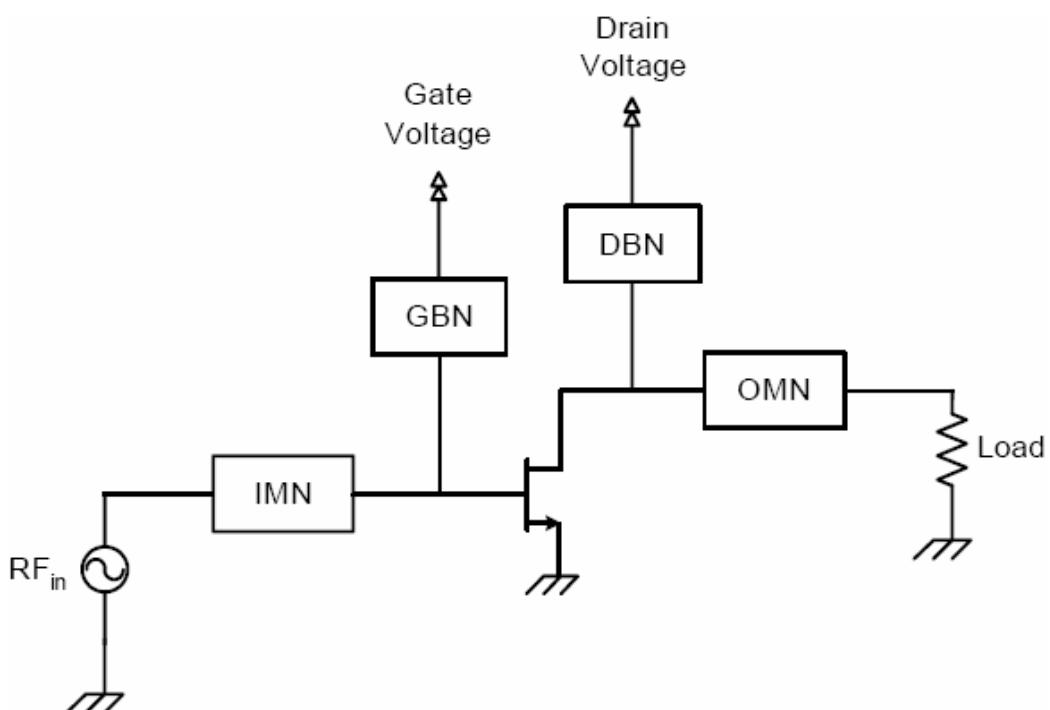


Figure 5.3 Basic schematic of single stage amplifier.

5.2 COPLAN Software for CPW Design

Coplanar waveguide (CPW) design technique allows more flexible layout generation compared to microstrip techniques. Moreover, for CPW designs, circuit sizes become less and there is no need for expensive and problematic via-hole and backside metallization processes. All this leads to remarkable cost reduction in the fabrication of MMICs. In our GaN HEMT MMIC fabrication process, we followed CPW approach due to the aforementioned reasons. We used COPLAN software for this purpose. We have attended CPW MMIC PA design training in IMST GmbH. COPLAN software is examined in more detail during this training.

COPLAN is a design and simulation tool for CPW circuits within ADS. An efficient and sophisticated quasi-static finite difference method (FDM) is implemented in this tool in order to carry out 3D electromagnetic (EM) simulations of the CPW structures. Since COPLAN can handle 3D solutions, all important effects such as metallization thickness, air bridge structure, internal coupling are taken into account during the CPW element simulation. Owing to a smart cache management included in FDM, very fast 3D EM simulation times are achieved in the order of seconds. This allows an efficient CPW MMIC design process.

The simulation steps followed in COPLAN are as follows: First, broadband equivalent circuit model is determined for each CPW elements. This model should represent physical characteristics of the corresponding structure in wide frequency range. Accurate broadband model can be formed only if all parasitic effects are taken into account in the equivalent circuit. Model of CPW spiral inductor is shown in Figure 5.4 where each turn of the inductor is represented by a Π -network and electrical coupling between the turns is considered by the

capacitance between the ports. Next, capacitive and inductive model parameters are calculated by the field distributions solved by a quasi-static 3D FDM. The solutions of a Laplace's differential equation for electric and magnetic potentials lead to the electric and magnetic field distributions, respectively. Capacitive model parameters are determined by the electric field distribution and charge distribution on the metallization. Similarly, inductive model parameters are determined by the magnetic field distribution and surface current distribution. A summary of these steps are shown in Figure 5.5.

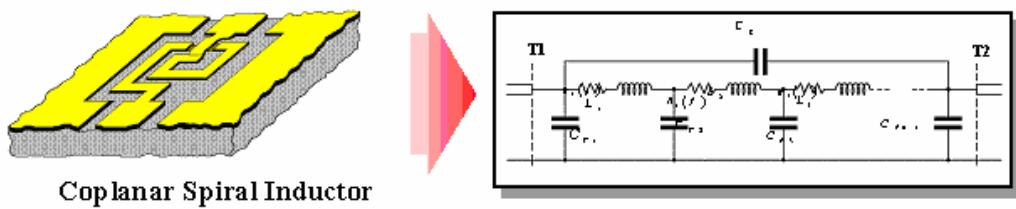


Figure 5.4 Broadband equivalent circuit model of coplanar spiral inductor implemented in COPLAN software.

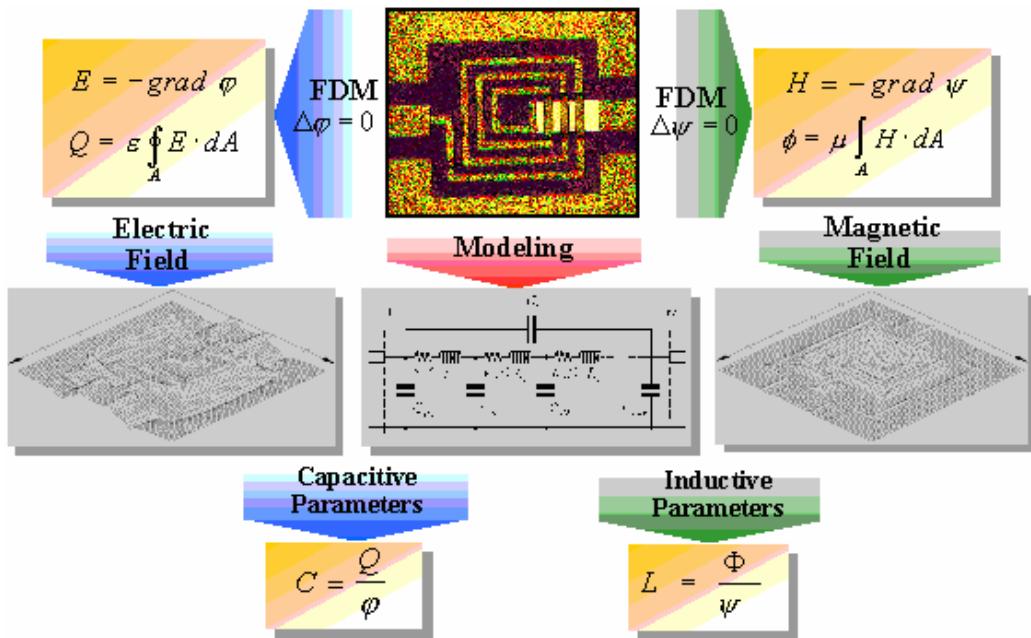


Figure 5.5 Modeling steps of coplanar structures used in COPLAN software.

Dispersion effects are not taken into account in this modeling approach due to the quasi-static solution nature. Moreover, only TEM mode excitation is considered in the solution process which means other modes are not included.

COPLAN coplanar element library contains CPW lines, various coplanar discontinuities of one-port, two-ports and four-ports, three types of air-bridges, rectangular inductors, MIM and interdigitated capacitors and thin film resistors.

5.3 GaN HEMT CPW MMIC PA Design Steps

Drain bias voltage of 17V and gate bias voltage of -2V are selected in our designs as indicated with marker “m4” in Figure 4.9. Load-pull and source-pull simulation results which show load and source impedances for maximum output power are given in Figure 5.6 and Figure 5.7, respectively. According to these results maximum output power of 33.62dBm can be obtained with 43.81% PAE for impedance terminations of $Z_{\text{Opt,LOAD}} = (68.90 + j15.83\Omega)$ and $Z_{\text{Opt,SOURCE}} = (5.67 + j23.66\Omega)$.

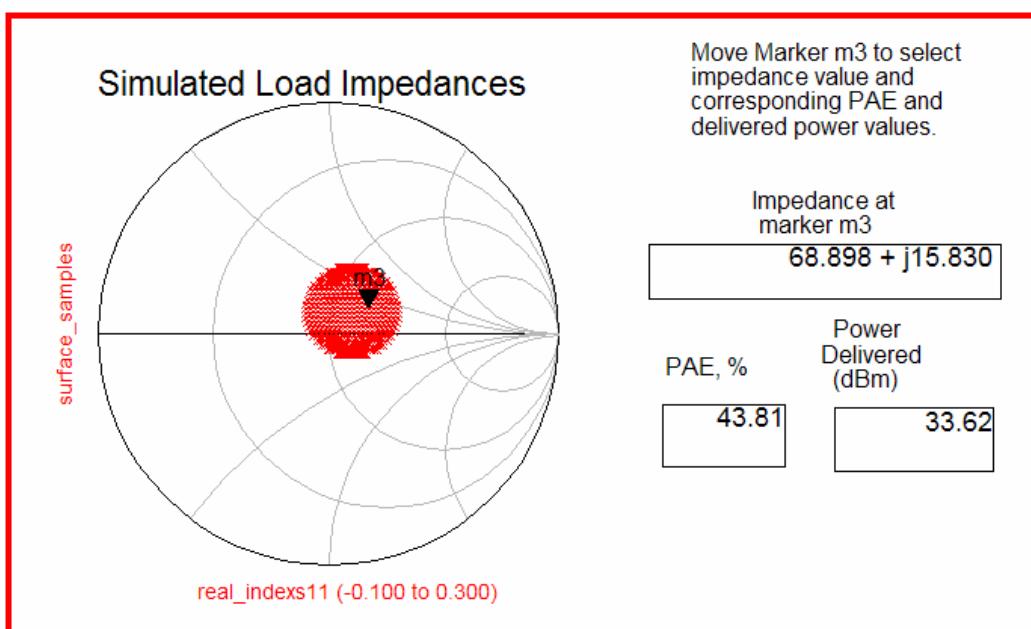


Figure 5.6 Load-pull simulation result of our GaN HEMT model.

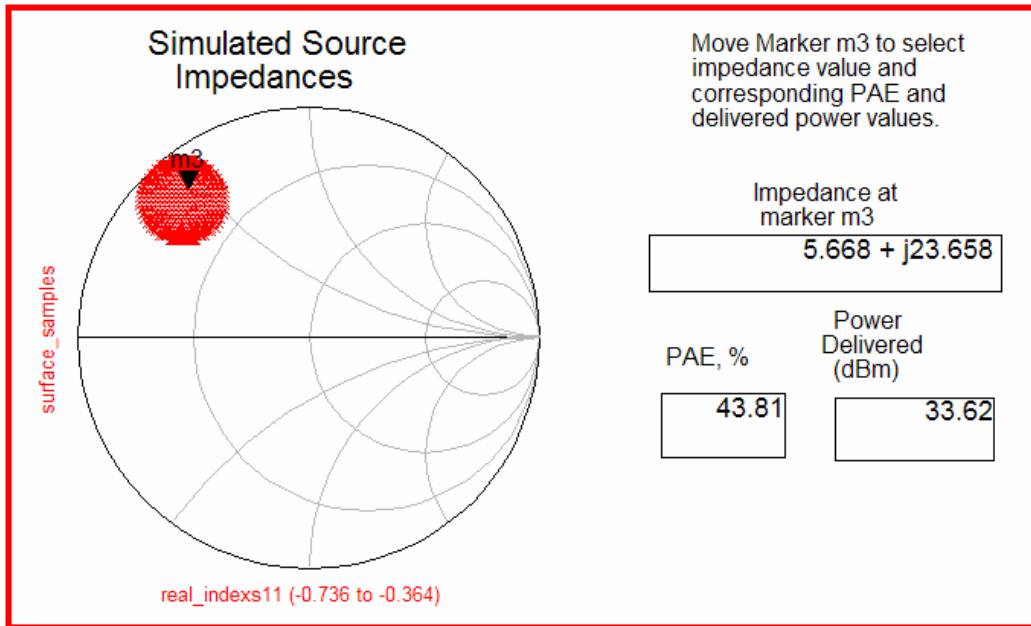


Figure 5.7 Source-pull simulation result of our GaN HEMT model.

In the beginning, design of the CPW MMIC PA with single GaN HEMT will be explained step by step. First, the optimum impedance values are used as a reference for matching network designs. Using Smith Chart tool of ADS, matching networks for input and output are determined with ideal elements. Two low-pass L-C branches and single low-pass L-C branch topologies are selected for IMN and OMN, respectively. Then, ideal elements of IMN and OMN are replaced with their COPLAN element counterparts. Since optimization of COPLAN inductor takes long time when all parameters are subjected to optimization, CPW line is used for initial calculations instead of inductor. After expected responses of matching networks are achieved, CPW lines are replaced with COPLAN inductors by intuition and some iteration are carried out for fine tuning. Next, CPW bias networks are designed in such a way that RF leak through DC path is avoided as much as possible. High value inductance is used for this purpose; same procedure is followed for inductance optimization as explained in matching network case. By-pass capacitor is added in order to provide good RF short before the DC source. Layout of GBN and

DBN are shown in Figure 5.8 and Figure 5.10, respectively. S-parameter simulation results of GBN and DBN are shown in Figure 5.9 and Figure 5.11, respectively. Finally, DC blocking capacitors are added to RF input and output ports. Effects of these capacitances are embedded to matching networks.

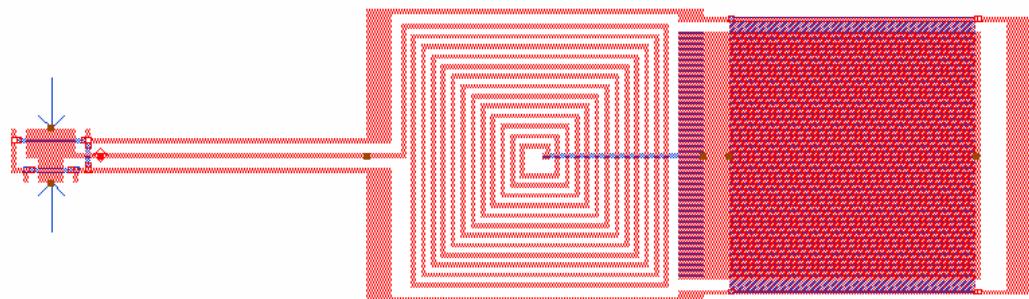


Figure 5.8 GBN layout of the first design.

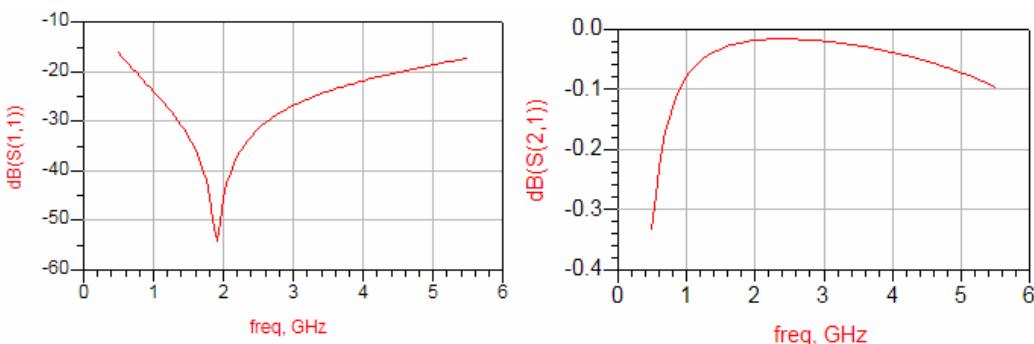


Figure 5.9 S-parameter simulation results of the GBN.

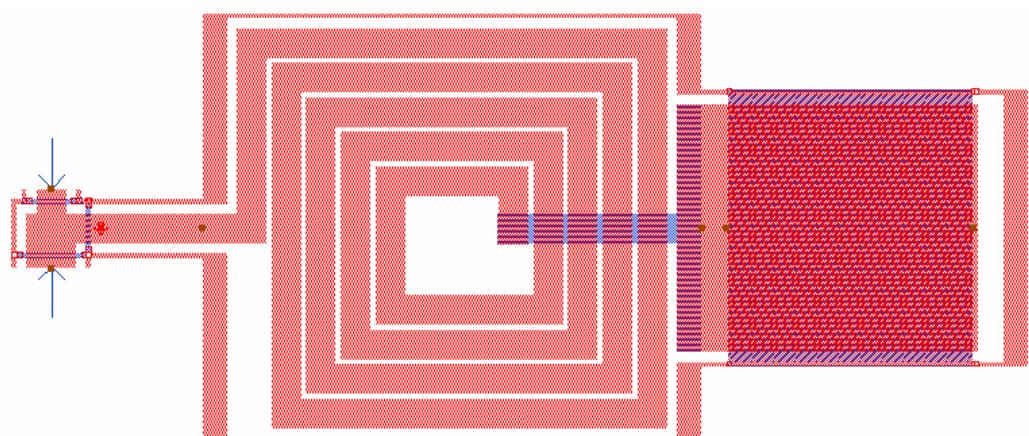


Figure 5.10 DBN layout of the first design.

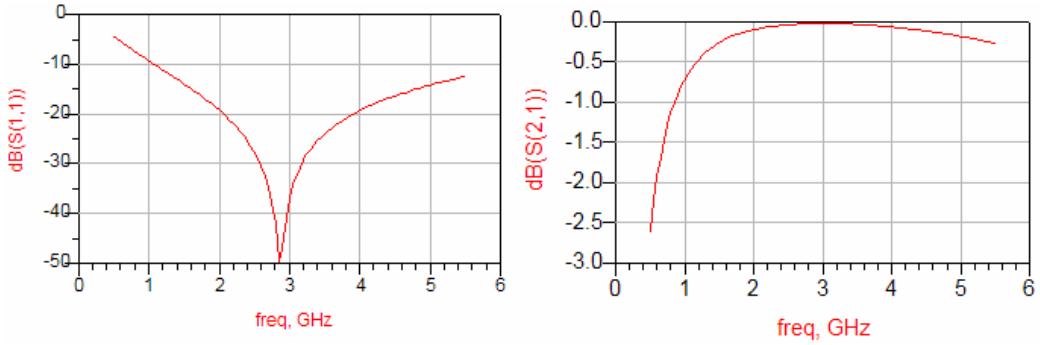


Figure 5.11 S-parameter simulation results of the DBN.

Overall design is optimized under harmonic balance simulations for maximum output power and checked with S-parameter simulations in terms of gain and stability conditions. Simulation results will be shown in the next subsection. Schematic of the first design is shown in Figure 5.12. Layout of the first design is shown in Figure 5.13.

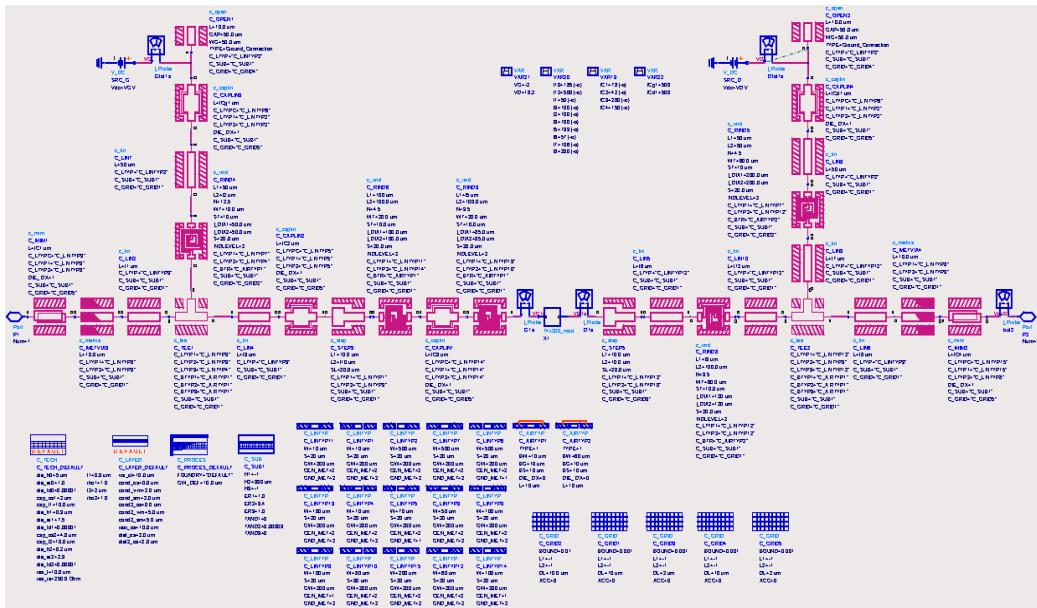


Figure 5.12 Schematic of the first CPW GaN HEMT MMIC PA.

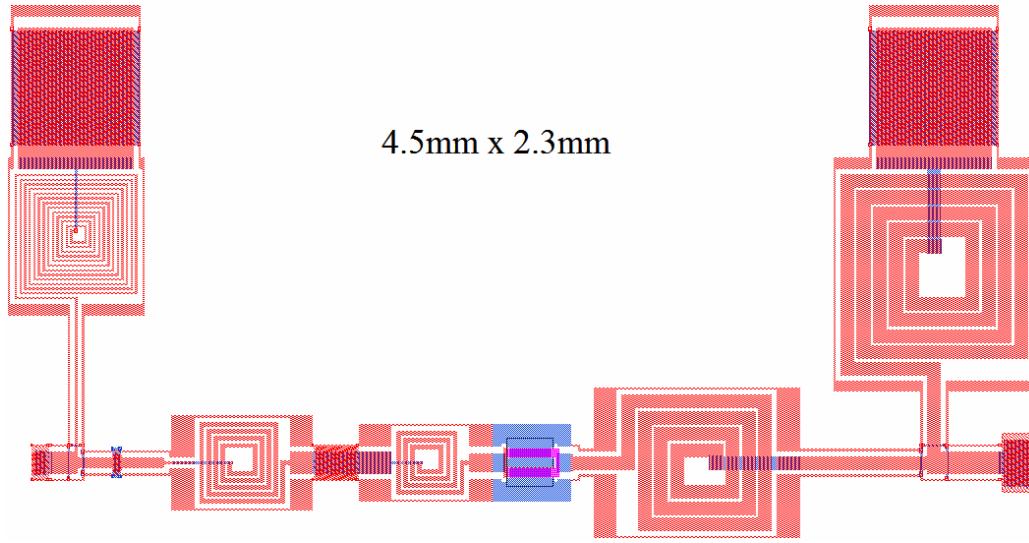


Figure 5.13 Layout of the first CPW GaN HEMT MMIC PA.

Second design with two GaN HEMTs in parallel has exactly the same procedure with the first one we explained above. Main difference between these two designs is the required impedance transformation ratio of matching networks since optimum impedances are theoretically divided by 2 in consequence of having two HEMTs in parallel. Simulation results of this design are also given in the next subsection. Schematic of the second design is illustrated in Figure 5.14. Total layout of the second design is shown in Figure 5.15.

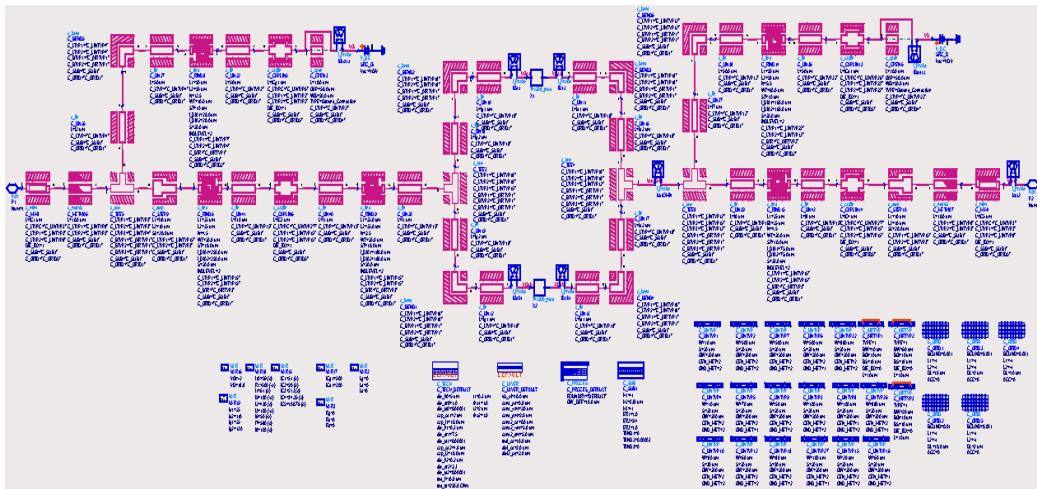


Figure 5.14 Schematic of the second CPW GaN HEMT MMIC PA.

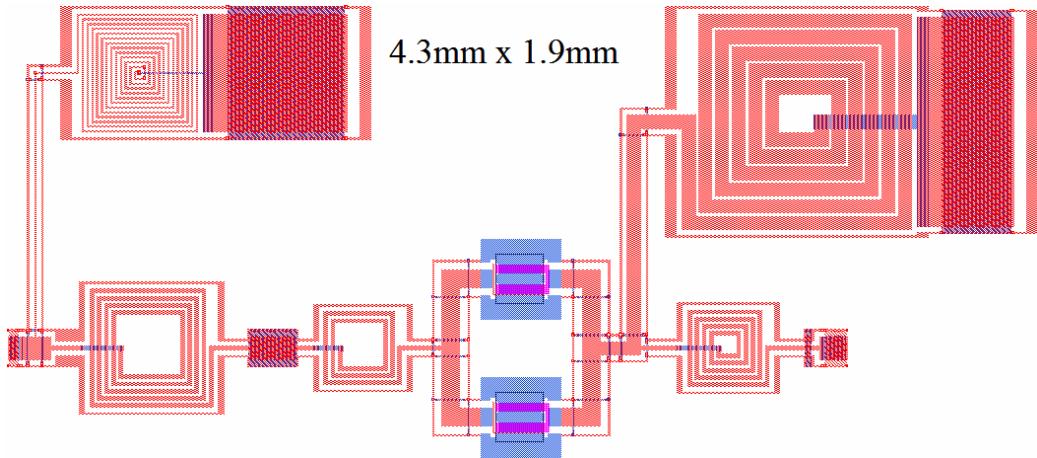


Figure 5.15 Layout of the second CPW GaN HEMT MMIC PA.

Fortunately, unconditional stability requirement is met with internal losses of the matching and bias networks for both designs. Hence, additional lossy networks are not implemented. By that way, design complexity and area of the total layout are reduced significantly.

Electromagnetic coupling effects between the circuit elements have not been taken into account in our GaN HEMT MMIC PA designs. Huge bias inductors and matching network inductors are the most critical elements in terms of electromagnetic coupling potential. As a figure of merit, distance between these electromagnetically sensitive elements should be kept at least 5 times the substrate thickness in order to get rid of significant effects of electromagnetic coupling. According to this figure of merit, layouts of our designs are subjected to be expanded to much larger areas; however, our substrate thickness is around $330\mu\text{m}$ which makes the above criteria unfeasible. Reasonable solution is the handling of electromagnetic effects using appropriate EM simulation tools such as Momentum (2.5D) and EMDS (3D) EM solvers implemented in ADS. Unfortunately, this kind of design process is very time consuming and we did not go through it. There is an alternative clever approach that is the inclusion of the bias networks into the matching networks so that we do not need to isolate

RF and DC paths and large RF choke inductors are not required any more. In this method bias network is used as a shunt inductor embedded in matching network if the impedance transformation and frequency band requirements allow such a topology. Although we could not implement this method in our GaN HEMT MMIC PA designs, we applied it in GaAs pHEMT balanced MMIC PA design which is introduced in Chapter 6.

5.4 Simulation Results of the MMIC PA Designs

Large-signal and S-parameter simulation results of the MMIC PA designs we have covered in this chapter are presented in the following paragraphs. Due to the limited time constraints of this work and repeatability problems of our GaN HEMT devices at that time, fabrication process of these MMIC PAs has not been started. Instead, more detailed studies and very much effort have been carried out through the way of GaN HEMT device improvement in NANOTAM labs. As a result, unfortunately, we could not compare the simulation results with measurement results of the designed MMIC PAs.

In Figure 5.16 and Figure 5.17, HB simulation results of the first design are given, namely, output power, power gain, and PAE. Markers in these figures approximately indicate 1dB compression point which corresponds to 18dBm input power. At aimed frequency of 2GHz, 2.14W output power, slightly higher than 15dB power gain and 42.26% PAE are obtained under 1dB compression point. These results almost reach the load-pull simulation limits. This is an indication of good design performance.

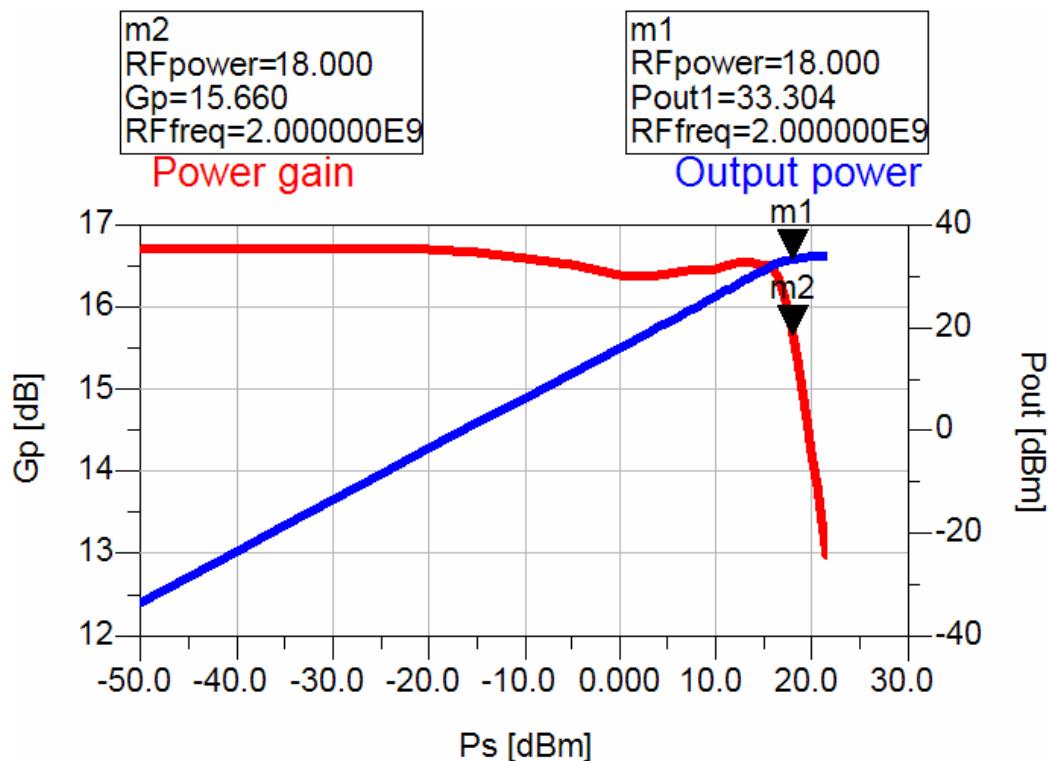


Figure 5.16 Power gain (red) and output power (blue) vs. input power sweep for the first design.

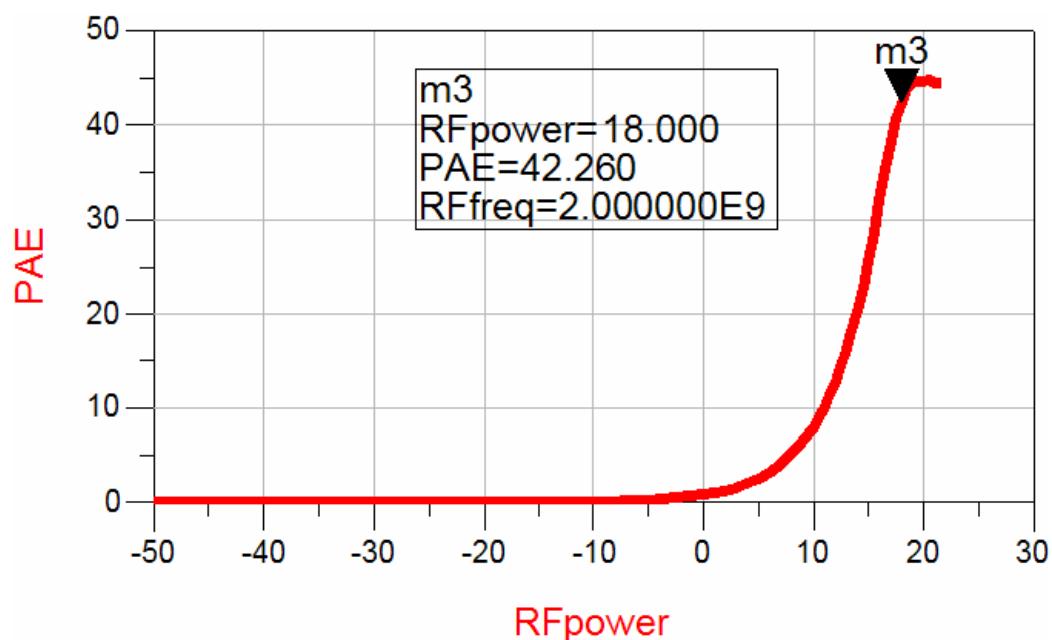


Figure 5.17 PAE vs. Input power sweep for the first design.

S-parameter simulation parameters of forward transmission (S21), input/output reflection coefficients (S11&S22), and stability factor (K) are shown in Figures 5.18, 5.19, and 5.20, respectively.

Markers “m7” and “m8” indicate 3dB cut-off frequency points in Figure 5.18. More than 1 GHz bandwidth is achieved in the first design. Small signal gain at 2GHz is approximately 16.5dB. Besides, -24dB of reverse isolation (S12) is observed at the center frequency.

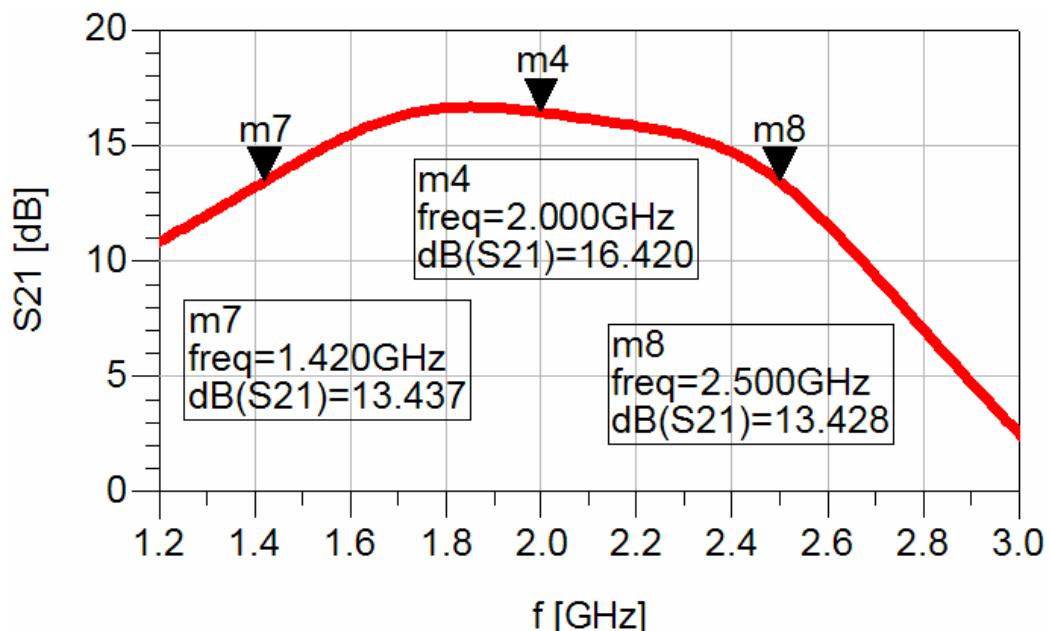


Figure 5.18 Forward transmission (S21) of the first design.

Moderate input and output matching performance is obtained from the first design. -12dB input reflection and -10dB output reflection at 2GHz are attained as shown in Figure 5.19. Since optimum output power matching condition is followed for output matching, relatively poor output reflection coefficient is inevitable compared to conjugate matching technique. Moreover, output matching response can be improved by adding extra poles to the OMN at the expense of additional losses coming from the extra circuit elements which is not accepted for PA design usually.

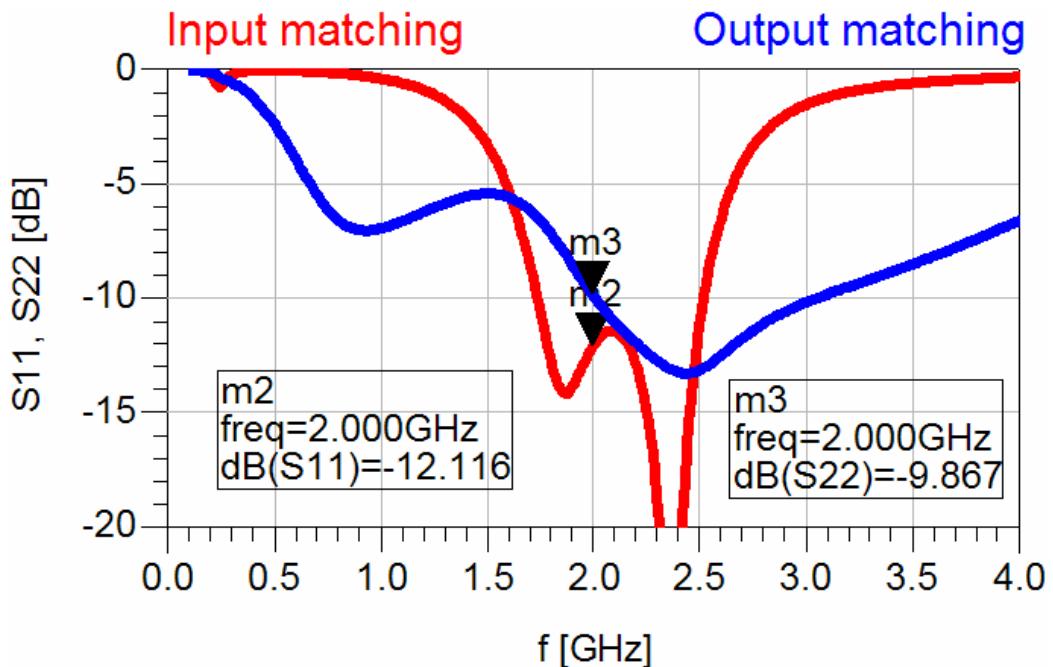


Figure 5.19 Input and output matching of the first design.

Unconditional stability is achieved for the first design without any additional stability network. Stability factor (K) is greater than 1 for all frequencies as shown in Figure 5.20.

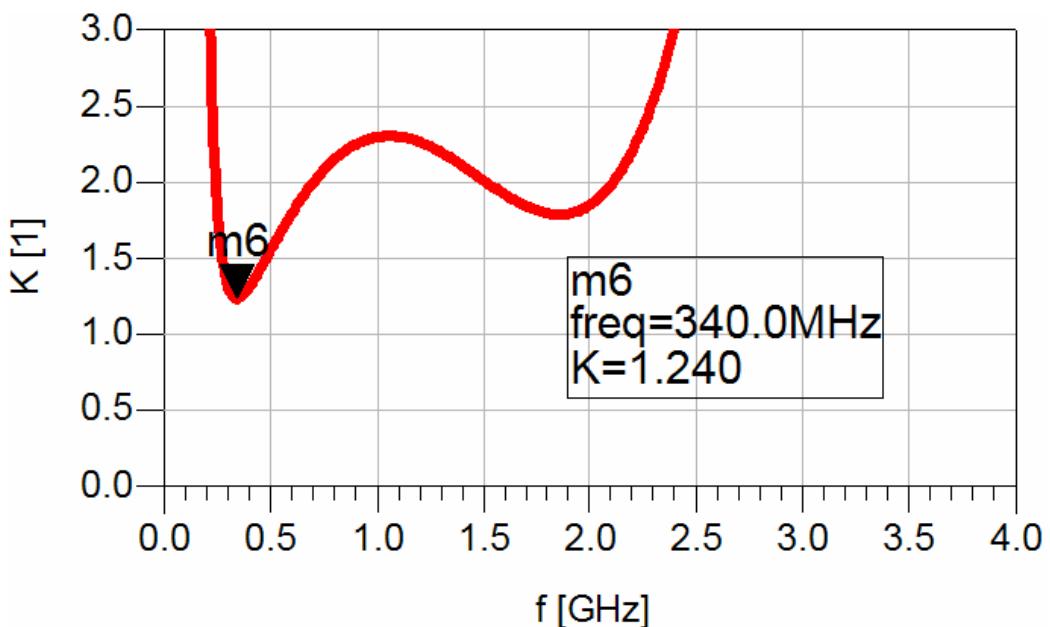


Figure 5.20 Stability factor of the first design.

In Figure 5.21 and Figure 5.22, HB simulation results of the second design are given, namely, output power, power gain, and PAE. Markers in these figures approximately indicate 1dB compression point which corresponds to 22dBm input power. At aimed frequency of 2GHz, 3.82W output power, 14dB power gain and 35.27% PAE are obtained under 1dB compression point. Aim of the second design was to get as twice as much output power by using double active device area compared to the first design. Resulting output power ratio of the second design to the first one is close to 1.8. This is an indication of good design performance considering power combining losses in the CPW lines and severe impedance transformation ratios of the second design.

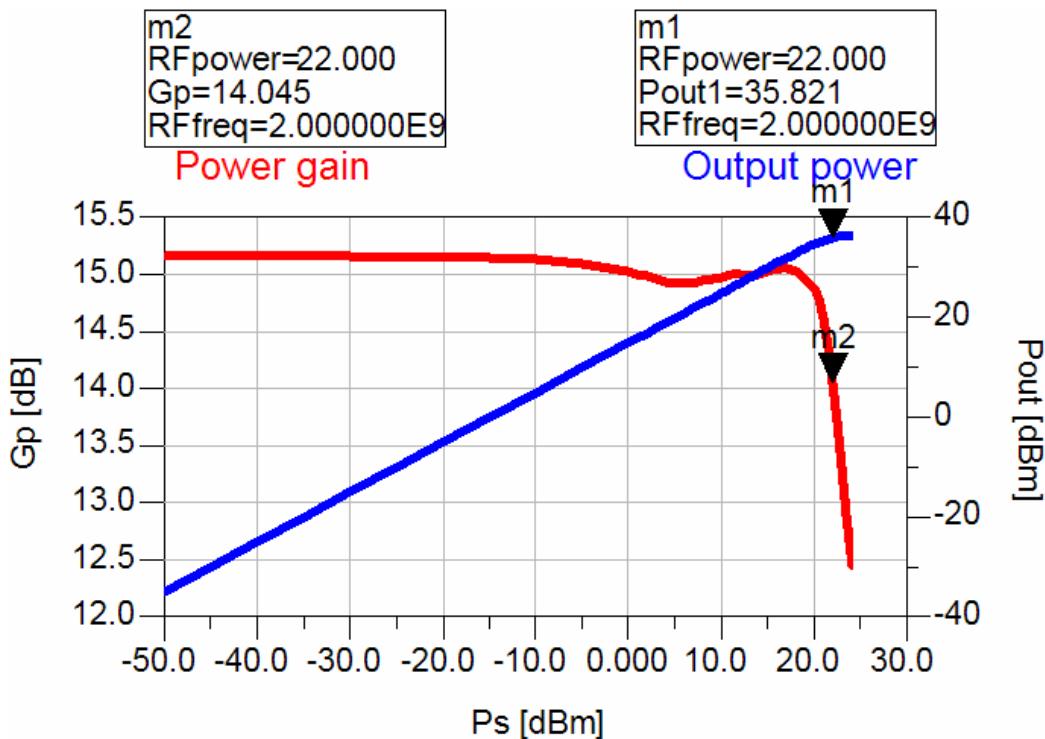


Figure 5.21 Power gain (red) and output power (blue) vs. input power sweep for the second design.

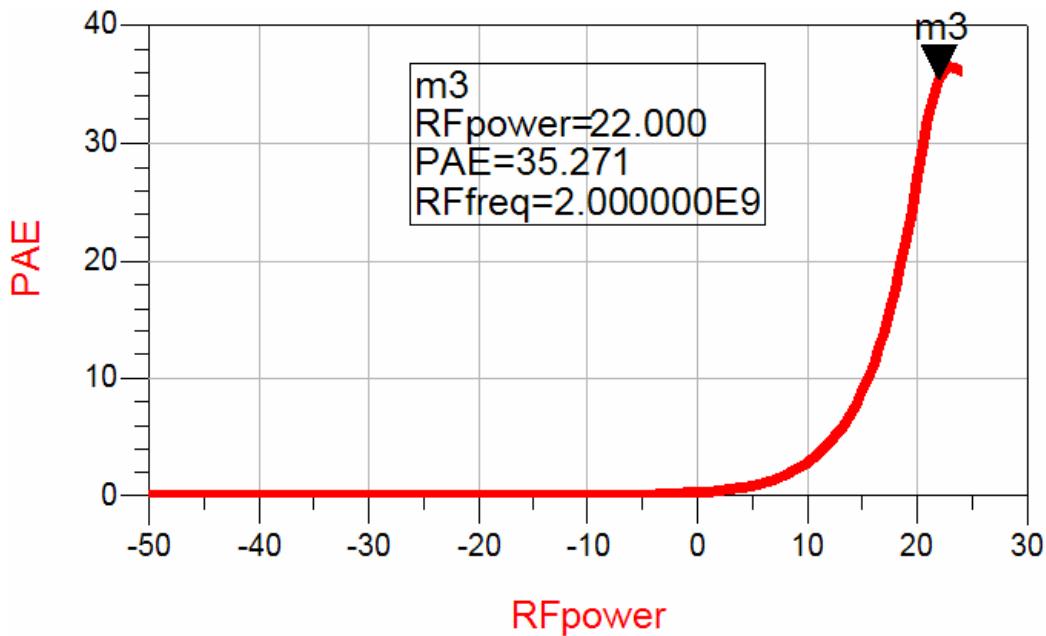


Figure 5.22 PAE vs. input power sweep for the second design.

For the second design, S-parameter simulation parameters of forward transmission (S_{21}), input/output reflection coefficients (S_{11} & S_{22}), and stability factor (K) are shown in Figures 5.23, 5.24, and 5.25, respectively.

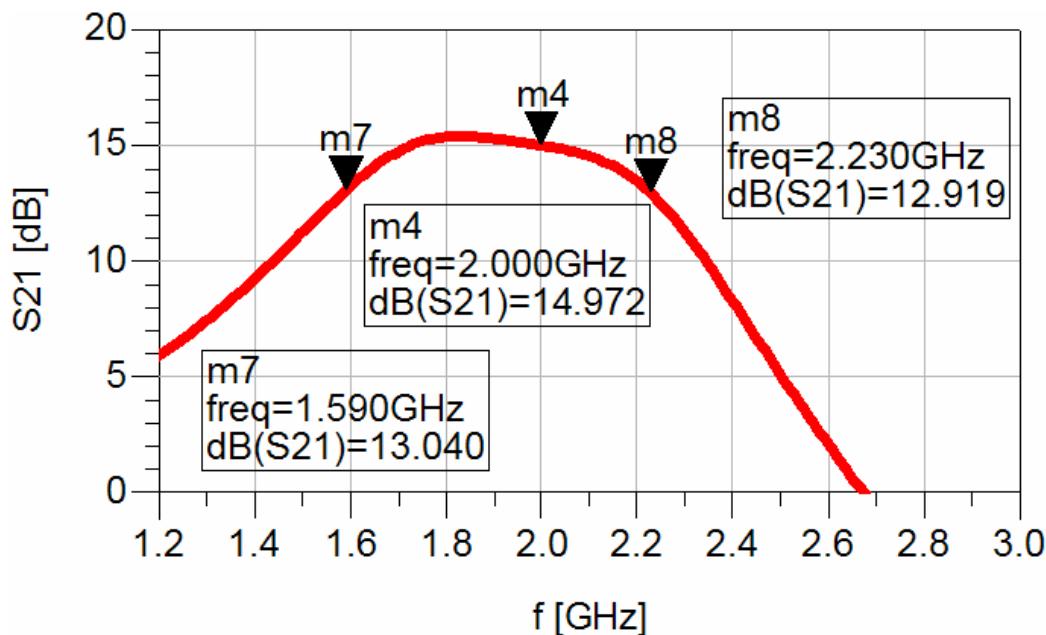


Figure 5.23 Forward transmission (S_{21}) of the second design.

Markers “m7” and “m8” indicate 3dB cut-off frequency points in Figure 5.23. 640MHz bandwidth is achieved in the second design. We observed less bandwidth compared to first design. Reason of this narrower frequency response is basically due to higher impedance transformation ratios of the second design. Small signal gain at 2GHz is approximately 15dB. We have 1.5dB reduction in small-signal gain at center frequency compared to the first design. Difference in gain comes from higher design complexity of the second design. Besides, -25.5dB of reverse isolation (S_{12}) is observed at the center frequency.

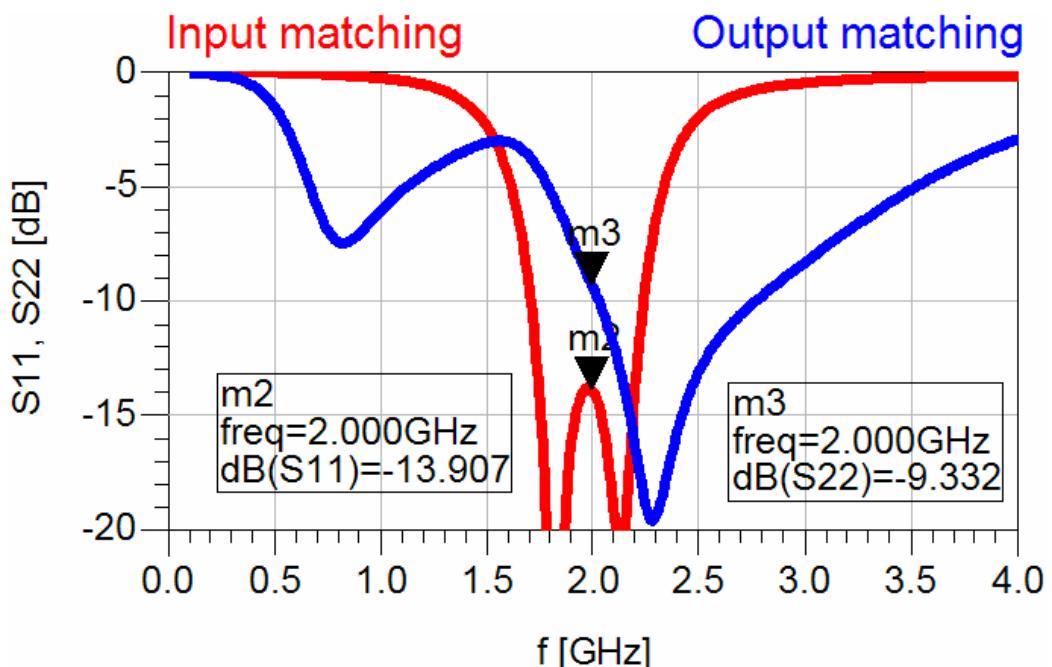


Figure 5.24 Input and output matching of the second design.

Moderate input and output matching performance is obtained from the second design. -13.9dB input reflection and -9.3dB output reflection at 2GHz are achieved as shown in Figure 5.24. Since optimum output power matching condition is followed for output matching, relatively poor output reflection coefficient is inevitable compared to conjugate matching technique. Moreover, output matching response can be improved by adding extra poles to the OMN at the expense of additional losses coming from the extra circuit elements which is not accepted for PA design usually. Instead, balanced design techniques can be

interpreted to improve input and output reflection coefficients. These balanced termination techniques also allow over octave bandwidth designs. We applied balanced design approach using two Lange couplers in our K-band design explained in the next chapter.

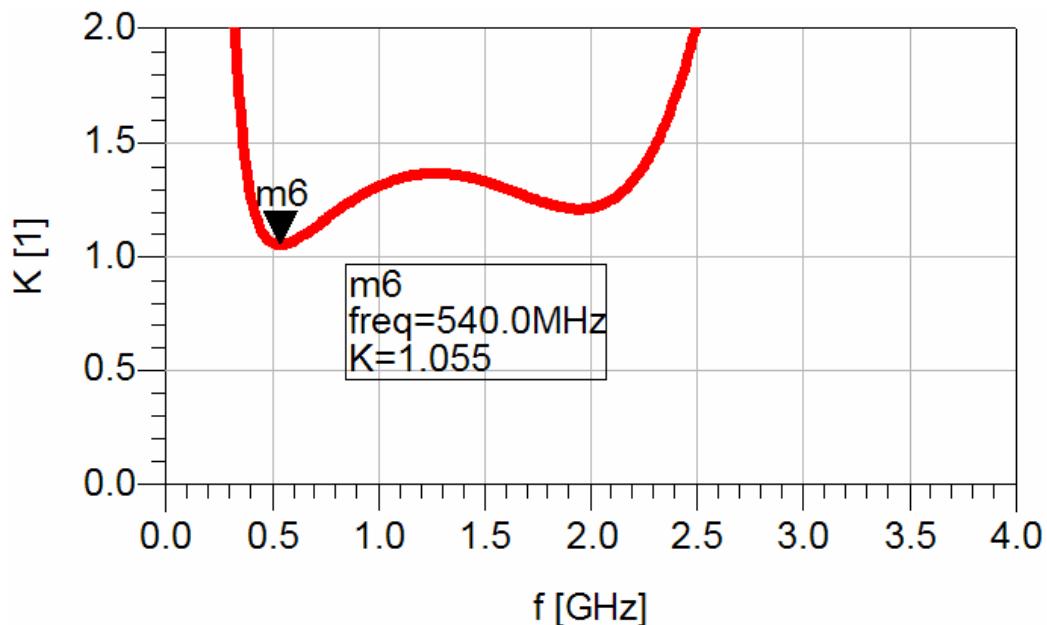


Figure 5.25 Stability factor of the second design.

For the second design, unconditional stability is achieved without any additional stability network. Stability factor (K) is greater than 1 for all frequencies as shown in Figure 5.25.

Chapter 6

K-Band GaAs pHEMT Balanced MMIC Power Amplifier Design

Power amplifier units are the key elements of the transmitter systems. Based on application and usage purpose, appropriate power levels at the transmitter output should be reached together with required bandwidth and linearity specifications.

In this work, we wanted to illustrate high frequency and high power MMIC PA design which includes several tricky design techniques. Bandwidth is chosen between 18-22GHz in K-band. Output power goal is defined as 2W. In order to achieve these stringent specifications, balanced design methodology is introduced. In this technique, wideband matching up to one octave bandwidth, stability improvement, and input power splitting and output power combining of two mirror-symmetrical PAs are handled at the same. Lange coupler is used as a 90° hybrid coupler in our balanced circuit topology. Mirror-symmetrical PAs consist of two stages. The first stage called gain block elevates the input power up to moderate power levels and the second stage takes that moderate power signal as an input via interstage matching network. High power amplification occurs at latter stage which is also named power block. Schematic of our balanced MMIC PA design is given in Figure 6.1.

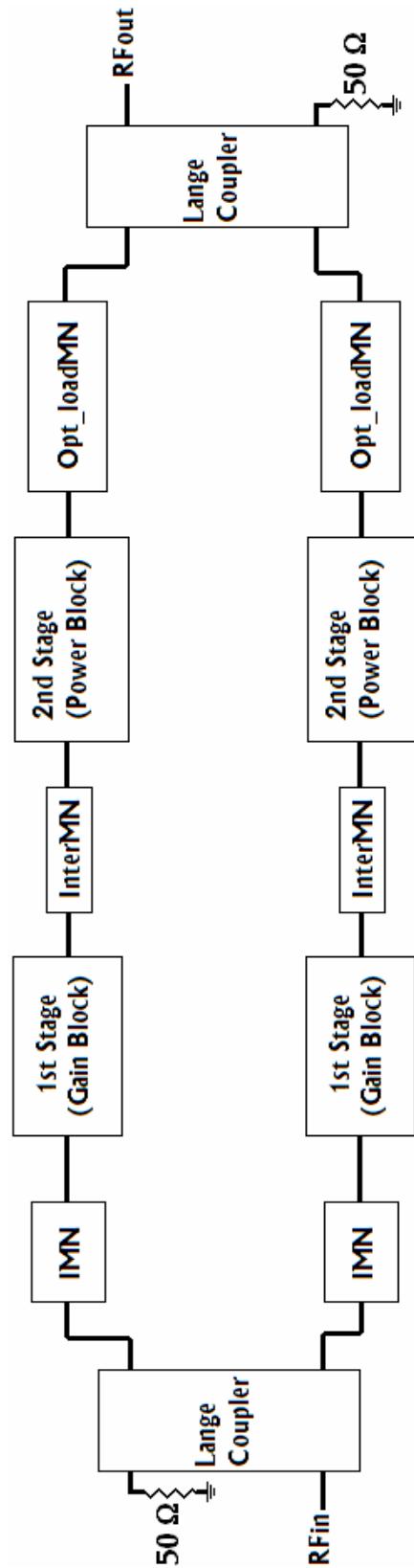


Figure 6.1 Block diagram of the balanced MMIC PA design.

Input matching network is used before the gain block in order to achieve the bandwidth requirement at the input side, and optimum load matching network is placed after the power block. Optimum load corresponds to complex conjugate of the large signal impedance value at the output similar to small-signal conjugate matching. We will go into details of the design steps in later subsections. First, we will mention about the foundry service choice for our design based on GaAs pHEMT.

6.1 Foundry Service

We searched through semiconductor foundries which provide multi-project wafer (MPW) run opportunity since only justification of our design is aimed in the scope of this work and no great number of chips are required for this purpose. Besides, sufficient active device performance that meets our design specifications is another important measure in our foundry choice criteria.

After consideration of issues mentioned above together with cost of the foundry service, we selected PPH25X high power pHEMT process offer of United Monolithic Semiconductor (UMS) [97] foundry. This process has $0.25\mu\text{m}$ gate length, 45GHz cut-off frequency, $>18\text{V}$ breakdown voltage, -0.9V pinch-off voltage, 400mS/mm maximum transconductance, 450mA/mm saturated drain current, and 900mW/mm output power density. In order to have an idea and for comparison purposes, the characteristics and parameters of open processes of UMS foundry is summarized in Table 6.1. PPH25X process is marked as blue in this table.

There are several steps of overall foundry service together with customer duties. Initially, UMS offers optional training courses and technical consultancy against significant amount of payment. We did not select this choice and determined to cope with the design based on our own knowledge, experience

and forthcoming long working days including weekends. In Figure 6.2, main process steps are given starting from foundry course, design kit delivery, design rule check (DRC) and foundry design reviews (FDR), and wafer fabrication (around 12 weeks), continuing with optional on wafer test and sorting, and ending at chip picking and delivery. We planned to test our MMIC PA chips in NANOTAM microwave characterization labs. Details of this test plan will be explained later in this chapter. Therefore, we did not ask UMS to carry out on-wafer test and sorting steps for us.

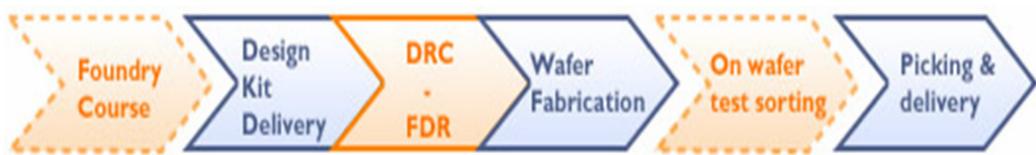


Figure 6.2 Typical UMS foundry service steps in order. Steps surrounded with dashed lines are optional.

At the beginning of the design cycle, design kit of the PPH25X process compatible with Agilent's ADS and AWR's Microwave Office [98] circuit simulators is received from UMS and the design manual is read in detail in order to handle our design according to design rules and process limitations. This preliminary phase of the design can be called as studying the PPH25X process of UMS foundry and has a vital importance on reliability of the design process. Furthermore, significant time saving is obtained with this approach since no big DRC problems are faced and no FDR iterations are required.

Small-signal and large-signal models of the active devices and accurate passive device models directly linked to automatic layout generation and library options are embedded in the design kit. Passive element scaleable models for inductors, capacitors, lines and resistors are provided. We are left with the pure design considerations after that point. In the next subsection, details of the balanced MMIC PA design will be presented.

Process	PH25 Low Noise	PH15 Low Noise	PPH25 Power	PPH25X Power	PPH15 Power	HB20P Power	HB20S High Power	HB20M VCO	HP07	BES
Active device	pHEMT	pHEMT	pHEMT	pHEMT	pHEMT	HBT	HBT	HBT	MESFET	Schottky
Power Density	250mW/mm	300mW/mm	700mW/mm	900mW/mm	600mW/mm	3500mW/mm	5000mW/mm	2000mW/mm	400mW/mm	-
Gate Length	0.25µm	0.15µm	0.25µm	0.25 µm	0.15µm	2µm	2µm	2µm	0.7µm	1µm
$I_{ds}(\text{gm max})$ $I_{ds \text{ sat}}/I_c$	200mA/mm 500mA/mm	220mA/mm 550mA/mm	200mA/mm 500mA/mm	170mA/mm 450mA/mm	300mA/mm 600mA/mm	0.3mA/µm ²	0.2mA/µm ²	0.3mA/µm ²	300mA/mm 450mA/mm	-
V_{BDS} / V_{BE}	> 6V	> 4.5V	> 12V	> 18V	> 8V	> 16V	> 35V	> 14V	> 14V	< 5V (Anode/ Cathode)
Cut off freq.	90GHz	110GHz	50GHz	45GHz	75GHz	25GHz	12GHz	30GHz	15GHz	3THz
V_{pinch}	-0.8V	-0.7V	-0.9V	-0.9V	-0.9V	-	-	-	-4.0V	-
Gm max / β	560mS/mm	640mS/mm	450mS/mm	400mS/mm	550mS/mm	70	50	60	110mS/mm	-
Noise / Gain	0.6dB / 13dB @10GHz 2dB / 8dB @40GHz	0.5dB / 14dB @10GHz 1.9dB / 6dB @60GHz	0.6dB / 12dB @10GHz	1.6dB / 7dB @40GHz	-	-	-	-	-	-

Table 6.1 Important properties of UMS processes.

6.2 K-band Design Considerations

During development cycle of the design, we have gone through several drafts. Technical and practical problems faced at each cycle are solved and the design is improved until all possible considerations are taken into account within our time constraints due to MPW run schedule of the foundry. Design steps and important considerations towards realization of practical MMIC PA at K-band are explained on final form of the design.

According to our power specification, transistor sizes and bias voltages are determined using DC simulations and very well known Cripps' method [99] which is a simple and effective tool for predicting maximum output power and optimum load impedance of a transistor based on load-line analysis at first glance. We focused on Class AB operation while determining output power and bias points. Later on, HB load-pull and source-pull simulations are carried out for more detailed and accurate analysis. Since we need 2W power at the output, 1W is ideally enough from single PA branch of balanced design. Hence, 8x125um active device is chosen as the second stage transistor. Design kit large signal models are valid under specific bias conditions which are 7V to 9V for drain bias and -0.5V to -0.3V for gate bias. Drain bias voltage of 9V and gate bias voltage of -0.4V are selected in this case. Load-pull and source-pull simulation results of this HEMT are given in Figure 6.3 and Figure 6.4, respectively. According to these results maximum output power of 30.26dBm can be obtained with 47.57% PAE from a 8x125um pHEMT device for impedance terminations of $Z_{\text{Opt,LOAD}} = (11.16 + j12.53\Omega)$ and $Z_{\text{Opt,SOURCE}} = (2.43 - j0.59\Omega)$ under 21dBm input power level.

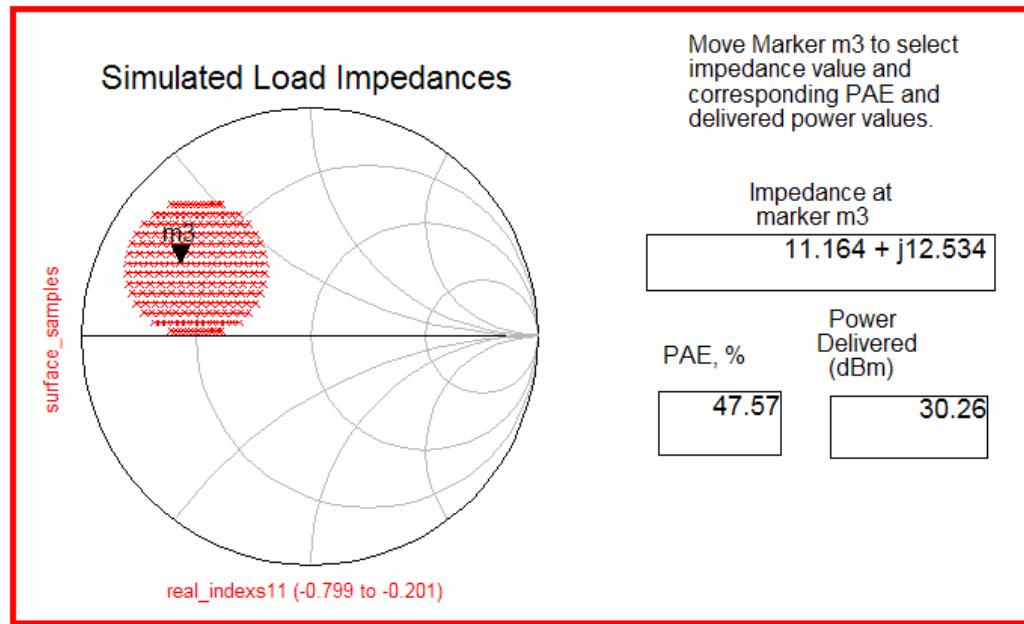


Figure 6.3 Load-pull simulation result of an 8x125um UMS GaAs pHEMT device.

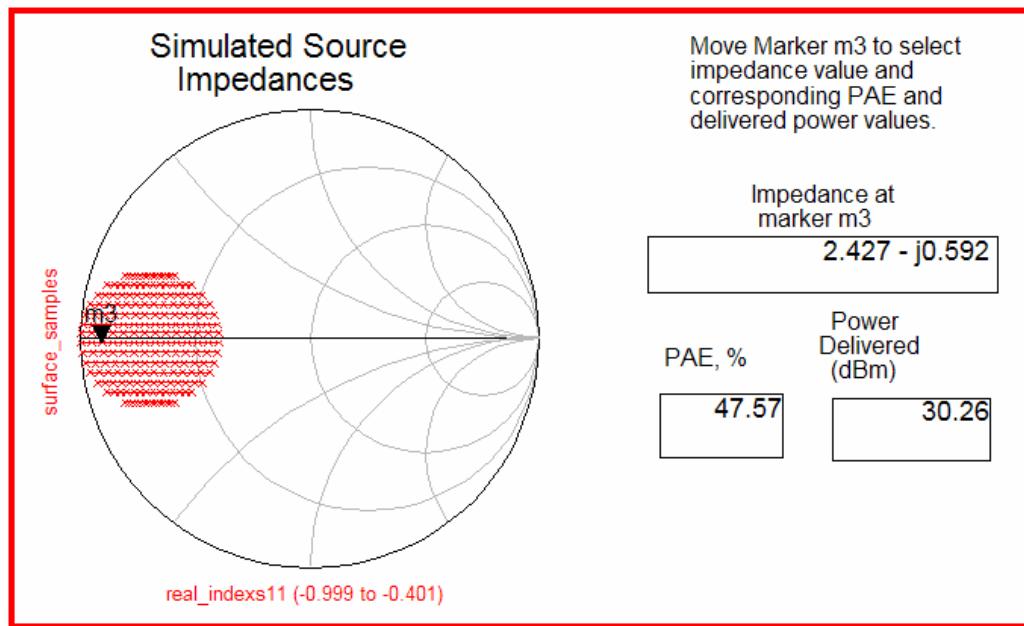


Figure 6.4 Source-pull simulation result of an 8x125um UMS GaAs pHEMT device.

In order to have more power gain we need gain stage as we explained before. First stage transistor dimensions and bias points are assigned in a similar way with the second stage transistor. Class of operation is chosen same as the second stage to assure consistency between the stages. Common choice of the gain

stage transistor has half total gate length of the power stage transistor, in our case that would be 500um since we have 1mm active device at second stage. In order to increase PAE of the system, total gate length of the first stage can be decreased as long as other design specifications can be still met.

In our design, we have stringent bandwidth requirement so that total gate length of the first stage transistor should be increased sacrificing from the PAE. Larger device in the first stage makes wideband interstage matching network more feasible since impedance transformation ratio between the drain of the first stage and the gate of the second stage gets lower.

Another important point is linearity issue of the first stage. In correct form of the multi-stage PA design, final stage should go into compression first. In other words, other stages should still perform in their linear regions while the final stage gets saturated. Under the light of these considerations above, we selected 6x100um device as the first stage transistor with drain bias of 8V and gate bias of -0.3V.

All bias networks of the design are embedded in RF networks so that significant layout area saving is achieved. On chip by-pass capacitance is designed to act electrically short at operation frequency band. Layout and S-parameter simulation results of this capacitor are given in Figure 6.5 and Figure 6.6, respectively. Capacitance value is 1.15pF.

Low frequency instability problems are solved by introducing series resistors on gate bias networks, between DC pad and by-pass capacitor, of each stage. Unconditional stability of the stages and overall design is assured without need for any other lossy networks that complicate the layout and decrease reliability of the design.

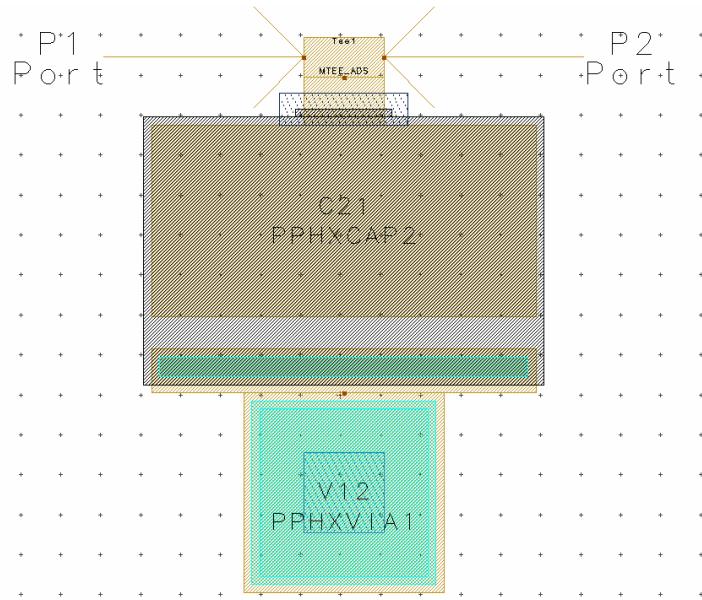


Figure 6.5 Layout of on chip MIM by-pass capacitor with via hole.

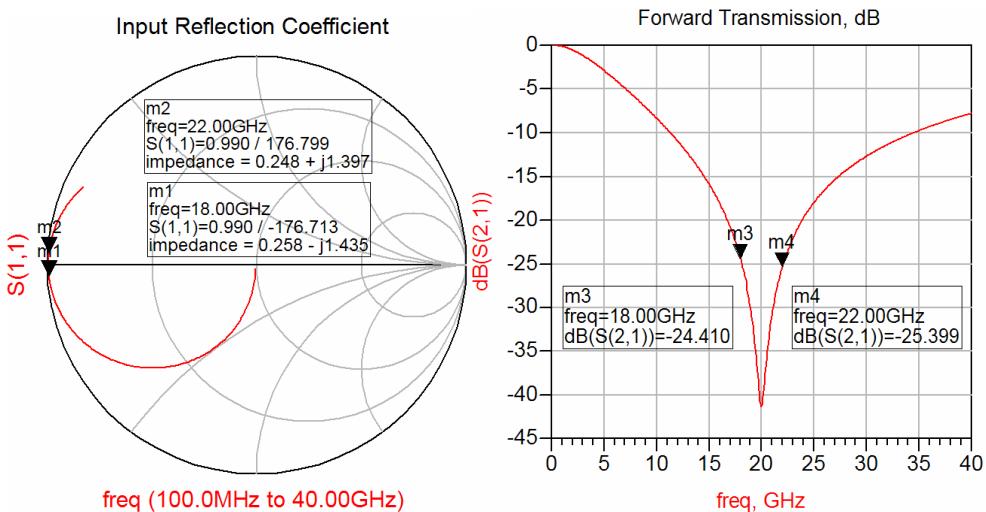


Figure 6.6 S-parameter simulation results of the shunt by-pass capacitor.

The design is started from the second stage stabilization with gate bias network and output matching network including drain bias circuit. First, optimum load matching topology is determined using ideal elements. Then, it is converted to real microstrip elements and design kit capacitances. We should remark that design kit inductances are not needed in our design since at K-band bare microstrip lines of reasonable length do the job well. Next, first stage

stabilization issue and input matching are handled. Input matching network is also designed as we explained above.

After all, we are left with the connection step of the two stages which is called interstage matching network. Now, we are faced with real problem. Let's describe the situation in more detail to understand difficulty of the problem clearly. On one side, we have drain port of the first stage transistor. Impedance of this port is frequency dependent and needs to be determined under large signal conditions since we reach high signal levels considering size of the first stage transistor. On the other side, interstage matching network should be terminated with the gate port of the second stage transistor. Source impedance of the second stage is also a large signal parameter and frequency dependent. As a result, we need a matching network which transforms frequency dependent large signal impedances to other frequency dependent large signal impedances in our frequency band of operation which is quite wide, 18-22GHz. Since we have multidimensional matching problem, variable impedances on both side, no straightforward solution is possible using circuit simulators. We proposed an alternative technique to deal with this matching problem. First, appropriate circuit topology is introduced with ideal elements using Smith Chart Matching tool of ADS. Then, it is converted to real elements and S-parameter response of the total branch of two stages is optimized with interstage matching parameters so that first order solution is completed. Finally, power characteristics of the connected two stages are improved and fine tuned iteratively using optimization tool of HB large-signal simulator. In this technique, we handled with interstage matching problem in an indirect way so that it is embedded in the whole system and overall response is taken into account.

Final schematic and layout forms of the two stage MMIC PA design is shown in Figure 6.7 and 6.8, respectively. We have three DC blocking capacitances, one in the input side, one in the output side, and one in the middle of the interstage matching network. Widths of the bias microstrip lines are determined

according to current ratings. Maximum mean current density is given as $7.5\text{mA}/\mu\text{m}$ in the PPH25X design manual.

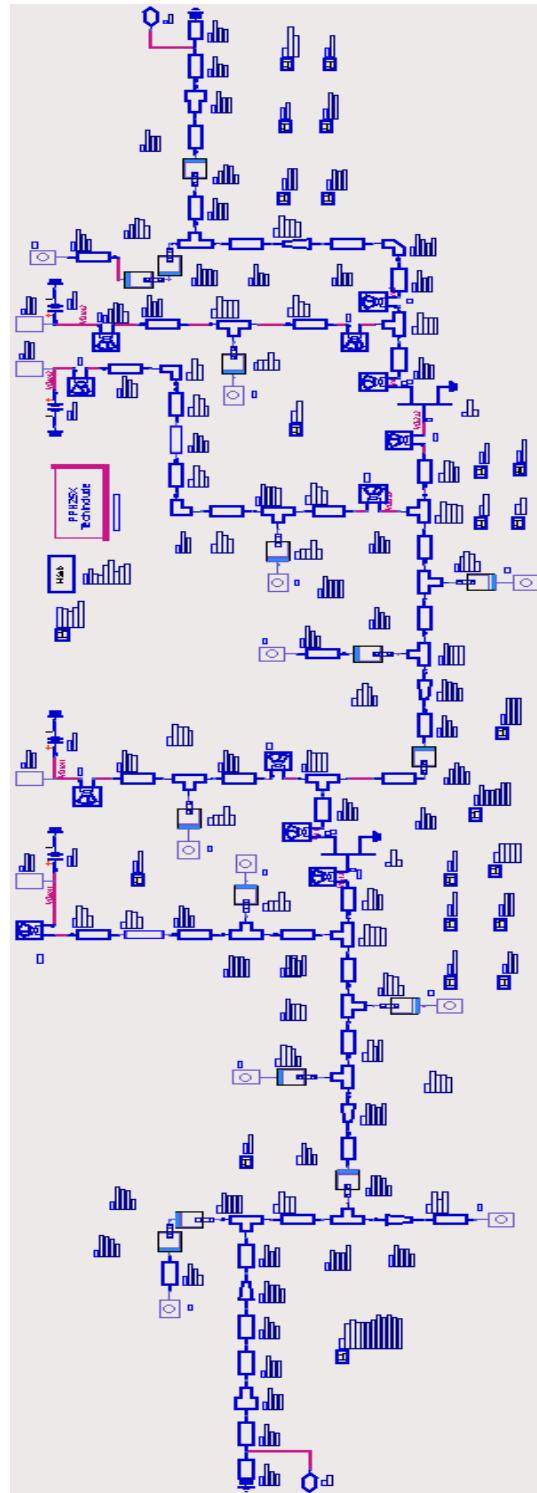


Figure 6.7 Schematic of the single branch of our balanced MMIC PA.

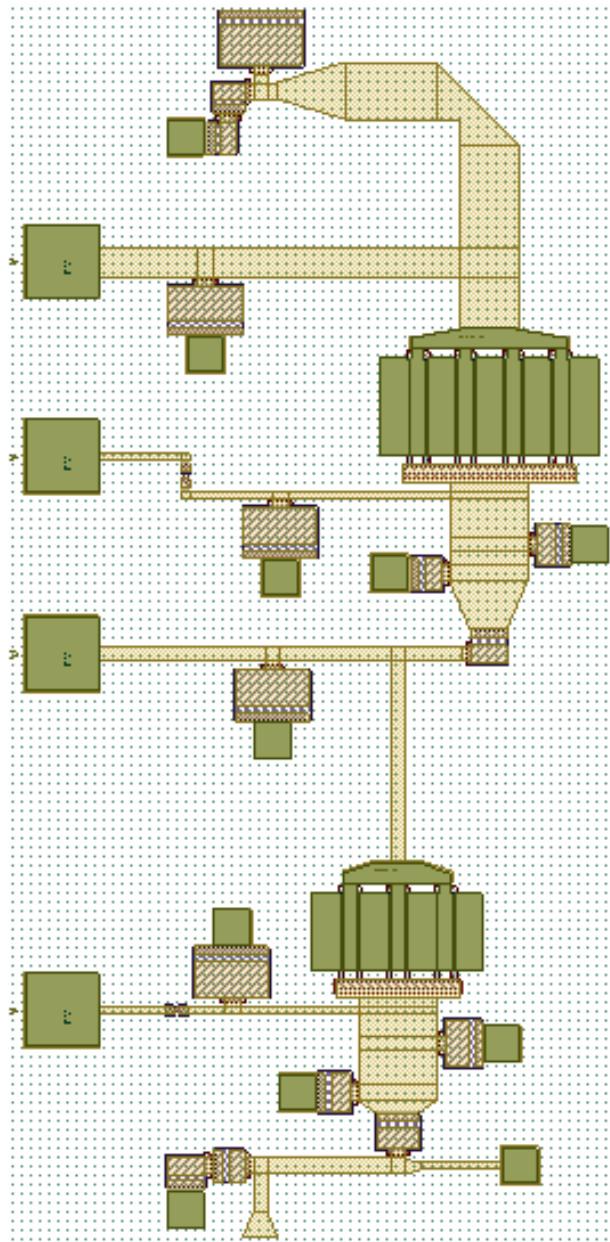


Figure 6.8 Layout of the single branch of our balanced MMIC PA.

During the layout design, unwanted electromagnetic coupling risk is considered. Enough spacing ($>2 \times$ substrate height ($\sim 70\mu\text{m}$)) is left between elements which have radiation potential. Momentum simulations of microstrip lines of the output matching network are carried out and compared with S-parameter block simulations in order to check if there is any significant

electromagnetic coupling effect. Results show that we have very good match between these two simulations which proves that our cautious approach works quite well. Moreover, we get rid of time consuming and complex EM simulations for the rest of the design after achieving these consistent results. Layout of the test structure is shown in Figure 6.9. Comparison of S-parameter schematic simulation and Momentum simulation results of microstrip lines of the output matching network are given in Figure 6.10.

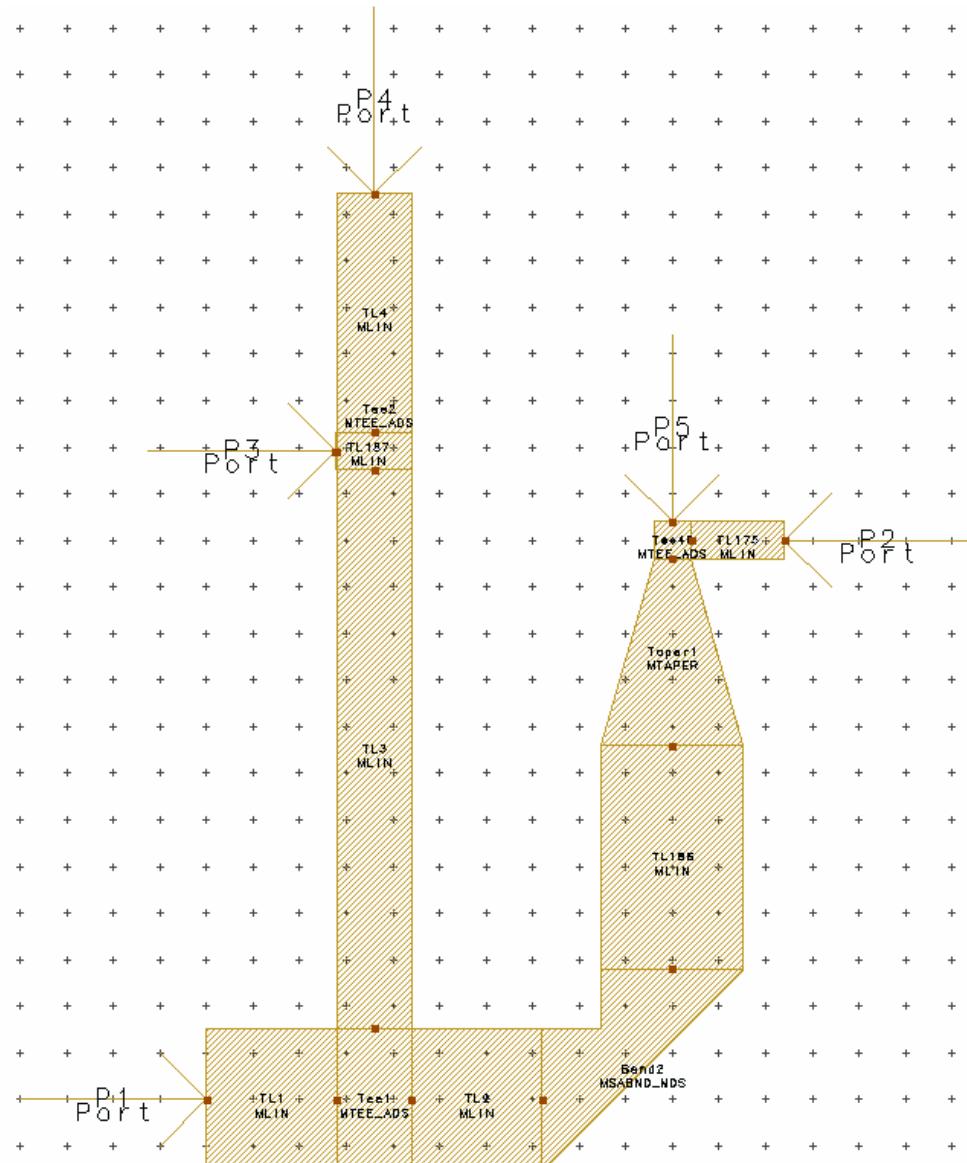


Figure 6.9 Layout of the Momentum test structure.

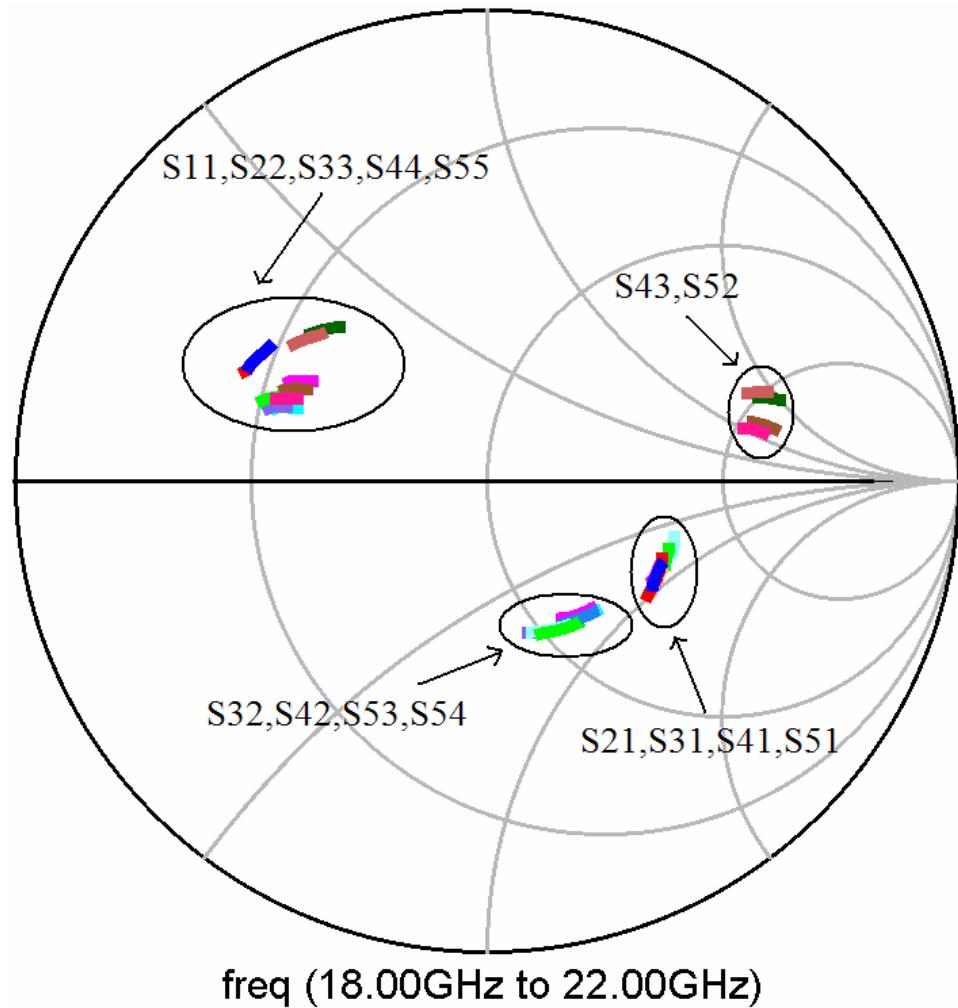


Figure 6.10 S-parameter comparison of schematic and Momentum simulations of the test structure with 5 ports.

6.3 Lange Coupler Design

Lange coupler is a kind of 3dB quadrature coupler invented by Julius Lange in 1969 [100]. This is a four port device which can be used for power splitting and combining purposes up to one octave bandwidth. Typical Lange coupler geometry with four fingers is given in Figure 6.11. Port names are indicated as input, coupled, direct and isolated. In ideal case, the coupled port has -90° phase shift compared to the direct port and both ports have equal signal magnitude

which is 3dB below the input signal level. Moreover, as the name implies, no signal is expected at the isolated port.

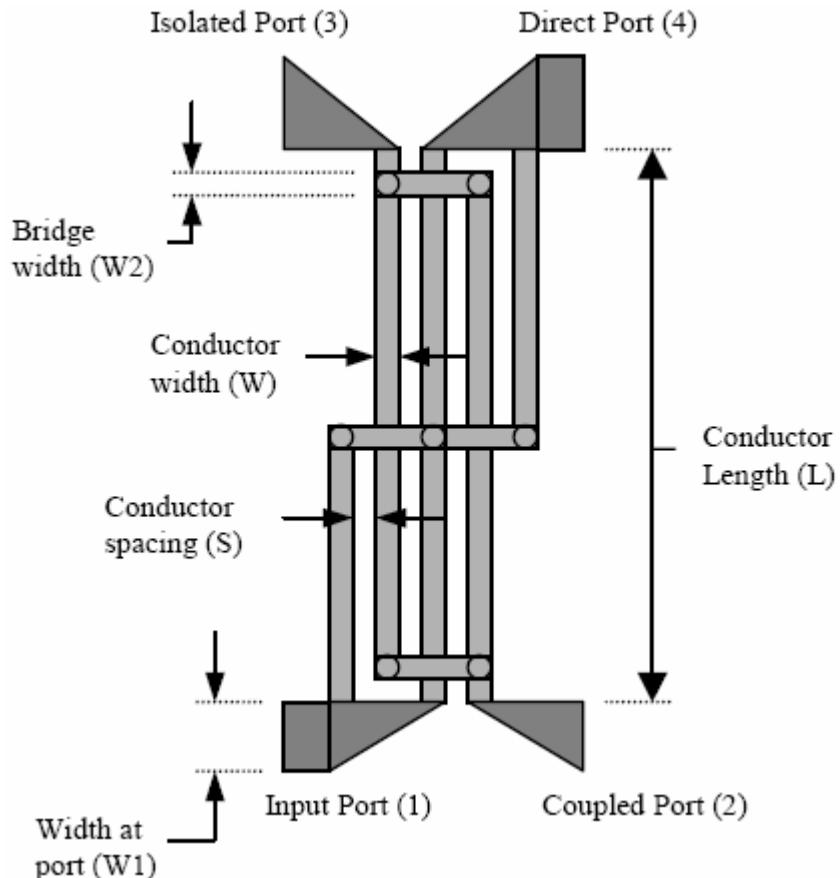


Figure 6.11 Typical Lange coupler geometry with four fingers.

Port width (W_1) is adjusted as the 50 Ohm microstrip line width on the substrate. In our case, W_1 is close to 50 μm . Conductor width (W) and spacing (S) are optimized using EM simulation tools. Bridge width (W_2) is determined according to design rules of the manufacturer; however, behavior of the Lange coupler is almost insensitive to this parameter. Finally, conductor length (L) can be chosen as the quarter wavelength at the center frequency as a starting point and should be optimized through EM simulations.

We started to design Lange coupler using ADS's built-in Lange coupler model in order to have first order approximate information about the

dimensions. Next, we generated more realistic layout for EM simulations and carried out manual optimization process. First draft of the Lange coupler structure is shown in Figure 6.12. Finger width and spacing are $10\mu\text{m}$ and $8\mu\text{m}$, respectively. Length of the Lange coupler is around 1.2mm. Since we used $3.3\mu\text{m}$ thick top metal layer for fingers, we had to use $1.1\mu\text{m}$ thick bottom metal layer as underpass connections instead of forming air-bridges. According to foundry design rules, we added air-bridges at intercept points of the two metal layers.

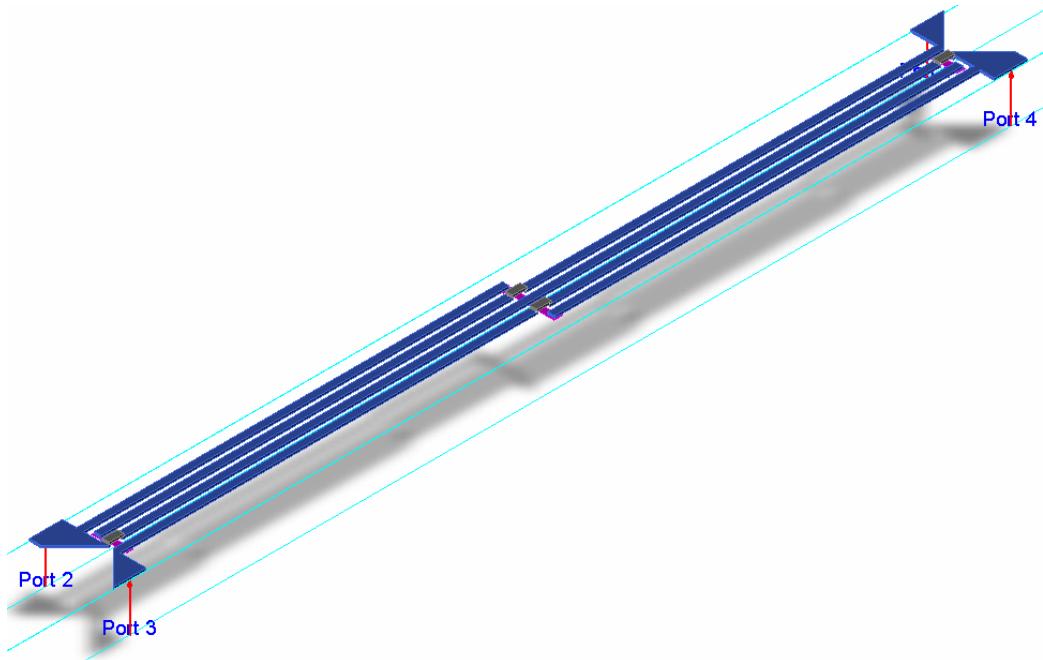


Figure 6.12 First draft layout of the Lange coupler

We used Momentum (2.5D) and EMDS (3D) simulators of ADS [101], and Ansoft HFSS [102] (3D) software for EM simulations of the Lange coupler. Simulation results are given in Figure 6.13 and 6.14. EMDS and HFSS simulation results are quite similar. On the other hand, Momentum simulation results show less coupling that is caused by the 2.5D nature of the Momentum solver. According to these results, appropriate coupling rate between the Lange coupler fingers cannot be reached by using this layout configuration while considering design rules.

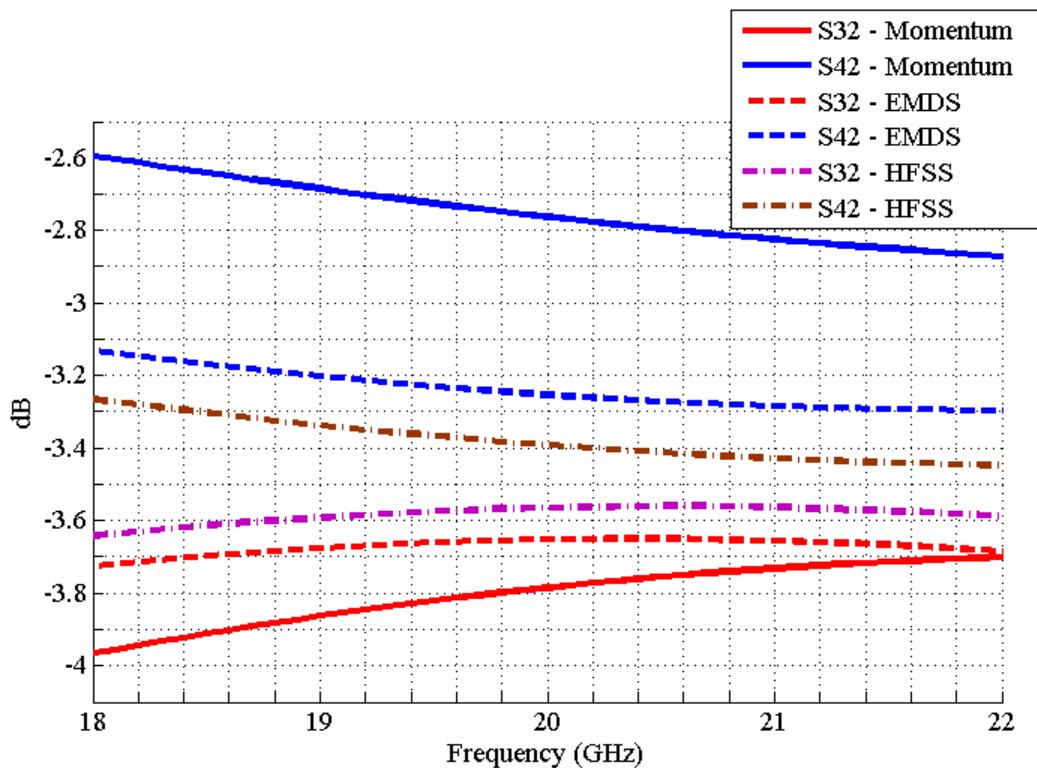


Figure 6.13 Various simulation results of the S-parameter magnitudes at direct and coupled ports.

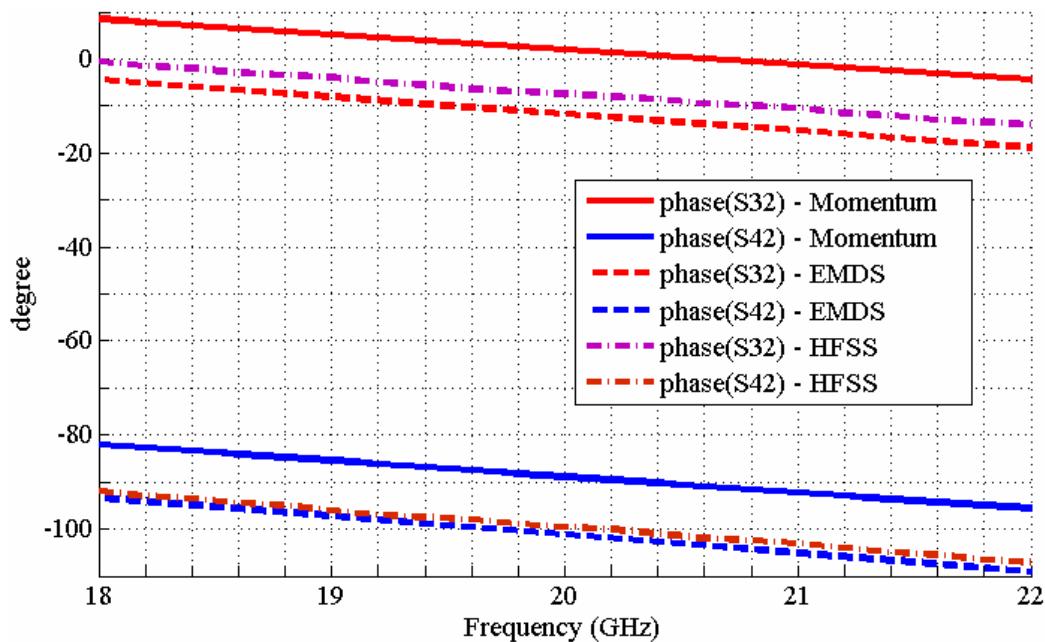


Figure 6.14 Various simulation results of the S-parameter phase values at direct and coupled ports.

We decided to continue with new Lange coupler design in order to increase the coupling rate. In this case, the fingers are formed by bottom metal layer so that they stay closer to the substrate compared to previous design, and top metal layer is used for air-bridge and port connections. Updated layout of the Lange coupler structure is shown in Figure 6.15. Final Lange coupler dimensions used in our MMIC PA are as follows: total length is around 1.2mm, finger width and spacing are 8 μ m and 5 μ m, respectively, and air-bridge width is 10um.

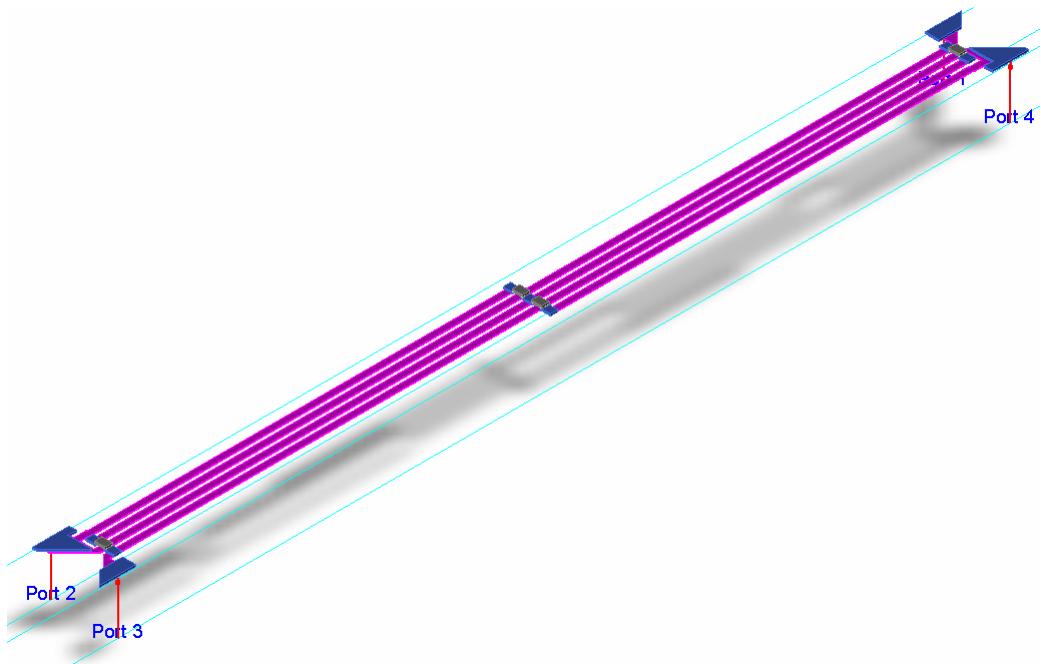


Figure 6.15 Final layout of the Lange coupler

Due to the limited time we had before the MPW run, we carried out only Momentum simulations for this design. Substrate definition tool of the Momentum software has some limitations since it is a 2.5D EM simulator; however, we did some pre-calculations to simplify the substrate definition. Bottom metal layer is partly surrounded by SiN layer and the left is simply air. We considered this dielectric composition as one dielectric material with corresponding dielectric constant. This artificial dielectric constant is calculated by the total capacitance between adjacent fingers filled by 255nm SiN and

845nm air. SiN and air portions of the gap act as parallel capacitances and average dielectric constant is calculated accordingly. Momentum simulation results of our Lange coupler design is given in Figure 6.16.

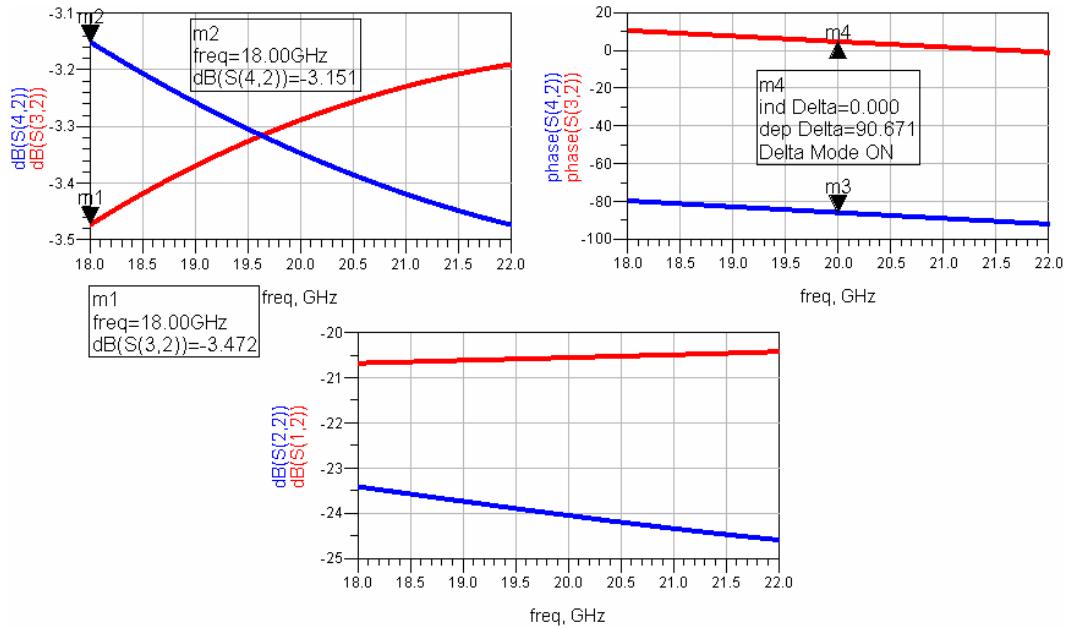


Figure 6.16 Momentum simulation results of the final Lange coupler design

After completing the Lange coupler design, overall layout of the K-band balanced MMIC PA is generated. Figure 6.17 shows the total layout which is going to be fabricated including several test structures on the left side. In MMIC PA part, 50 Ohm termination resistors of the Lange coupler are designed to work under almost all unwanted conditions such as open or short loading of the output port, and failure of one branch of the balanced structure. Testing part of the chip contains $6 \times 100\mu\text{m}$ and $8 \times 125\mu\text{m}$ transistors with RF input and output pads, one shunt capacitor with one RF pad, and a Lange coupler with two RF pads at input and direct ports and two 50 Ohm loads at coupled and isolated ports. With this Lange coupler test structure we can only measure S22 and S42 additional Lange coupler is required to test other parameters. Unfortunately, we don't have enough space to put one more. Dicing street is located between the actual chip and the test region. Total chip dimensions are 1.8mm x 3.3mm.

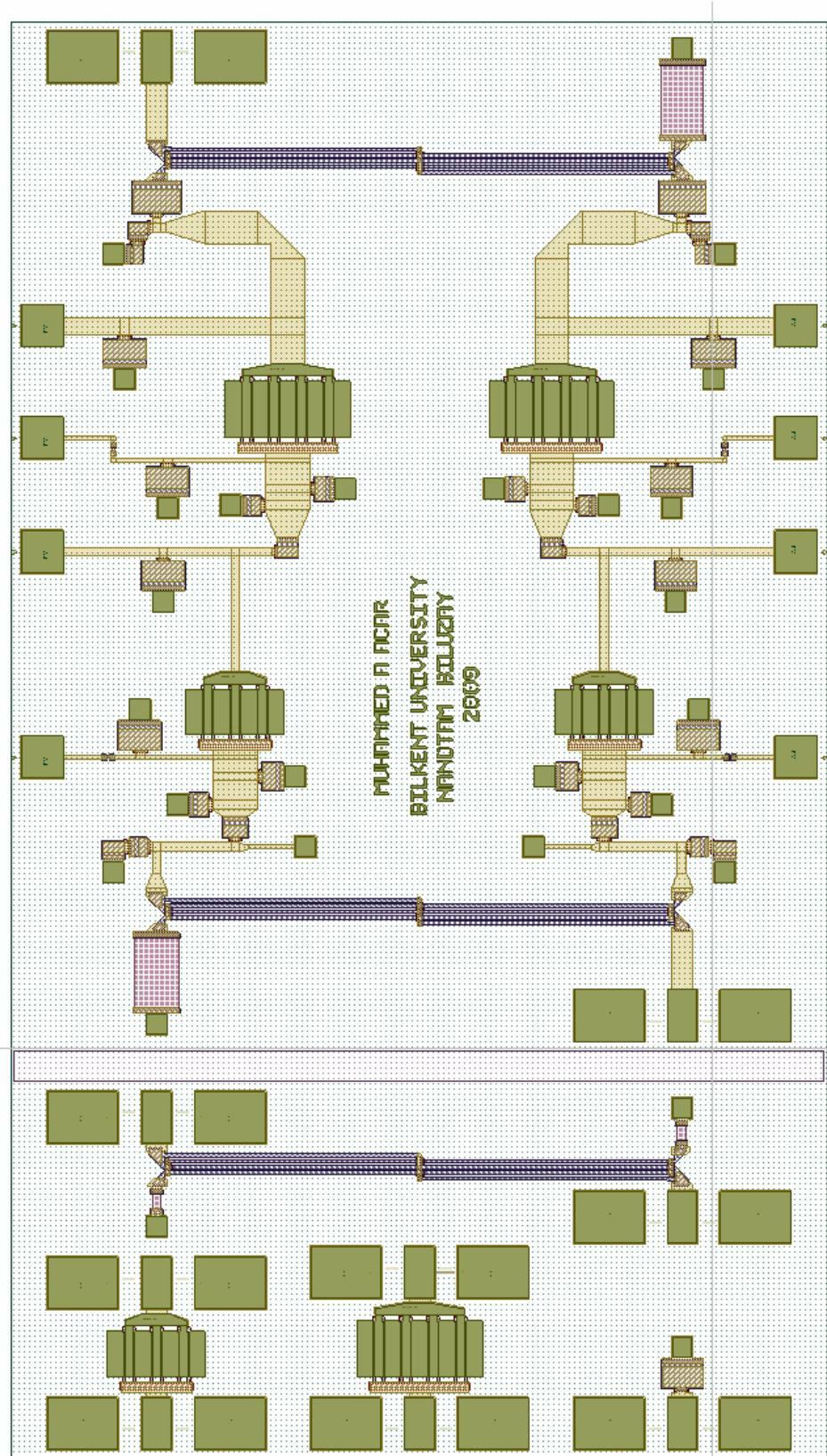


Figure 6.17 Final layout of the K-band GaAs pHEMT balanced MMIC PA.

6.4 Simulation and Measurement Results of the K-band Balanced MMIC PA

In this subsection, we will first illustrate S-parameter simulation results of the single branch two-stage MMIC PA shown in Figure 6.7. Next, we will introduce our measurement setup and show measurement data together with overall simulation results of our balanced MMIC PA. Finally, we will comment on comparison of simulation and measurement.

S-parameter simulation results of the single branch two-stage MMIC PA are given in Figure 6.18.

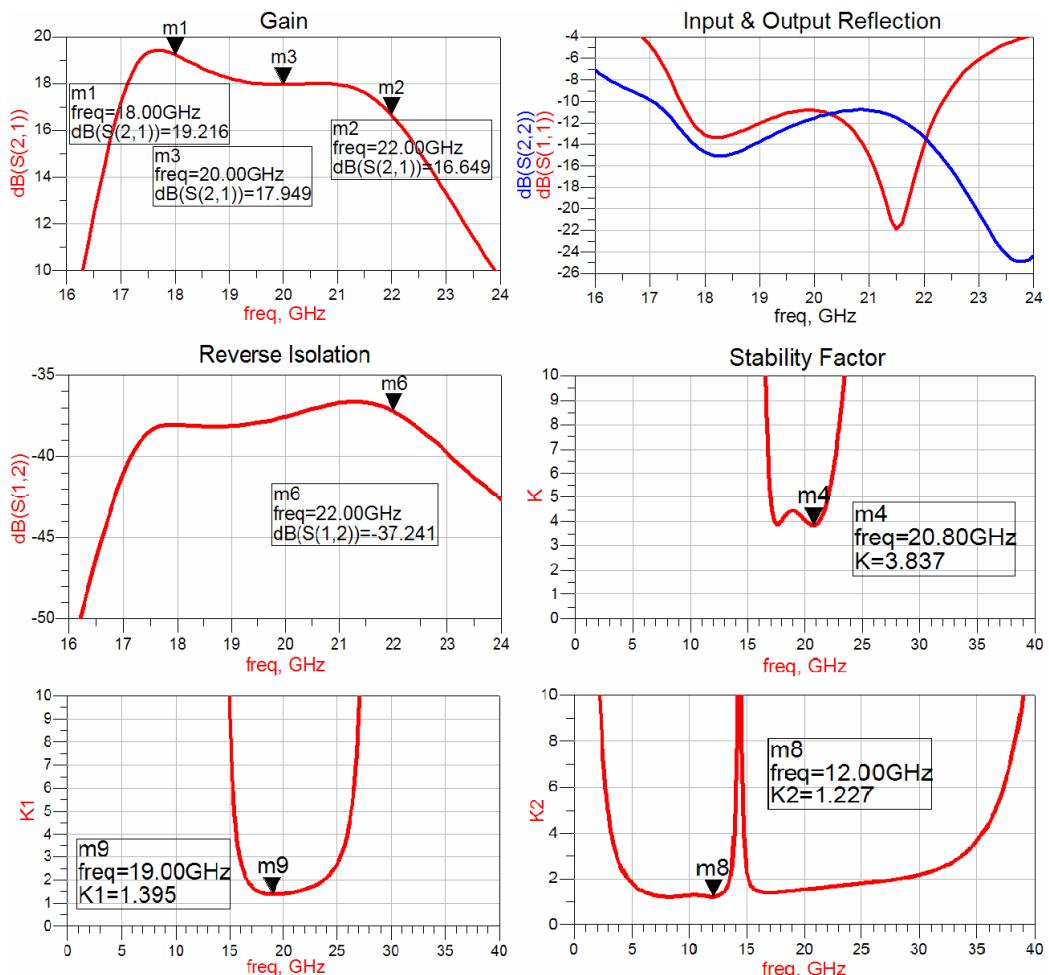


Figure 6.18 S-parameter simulation results of the single branch two-stage MMIC PA.

Unconditional stability is assured for each stage and overall PA. Better than -11dB input and output reflection and -37dB isolation are obtained in 18-22GHz operation band. Gain of the amplifier stays between 16.7dB and 19.2dB throughout aimed frequency band.

0.4mm thick FR4 PCB is designed for DC supply lines. Layout of this PCB is shown in Figure 6.19, dimensions are 6cm x 8cm. 1nF, 10nF, 100nF SMD capacitances and 1uF tantalum capacitance are placed on every DC supply line in order to avoid oscillation possibility over wide range of frequencies. In order to assure appropriate RF grounding at operation frequencies 100pF single layer capacitances are placed as close as possible to the DC pads on the MMIC chip. Furthermore 3mm thick copper block is produced. This metal block is used as a mechanical base, electrical common ground and very efficient passive heat sink for the MMIC chip, single layer capacitors and the DC board.

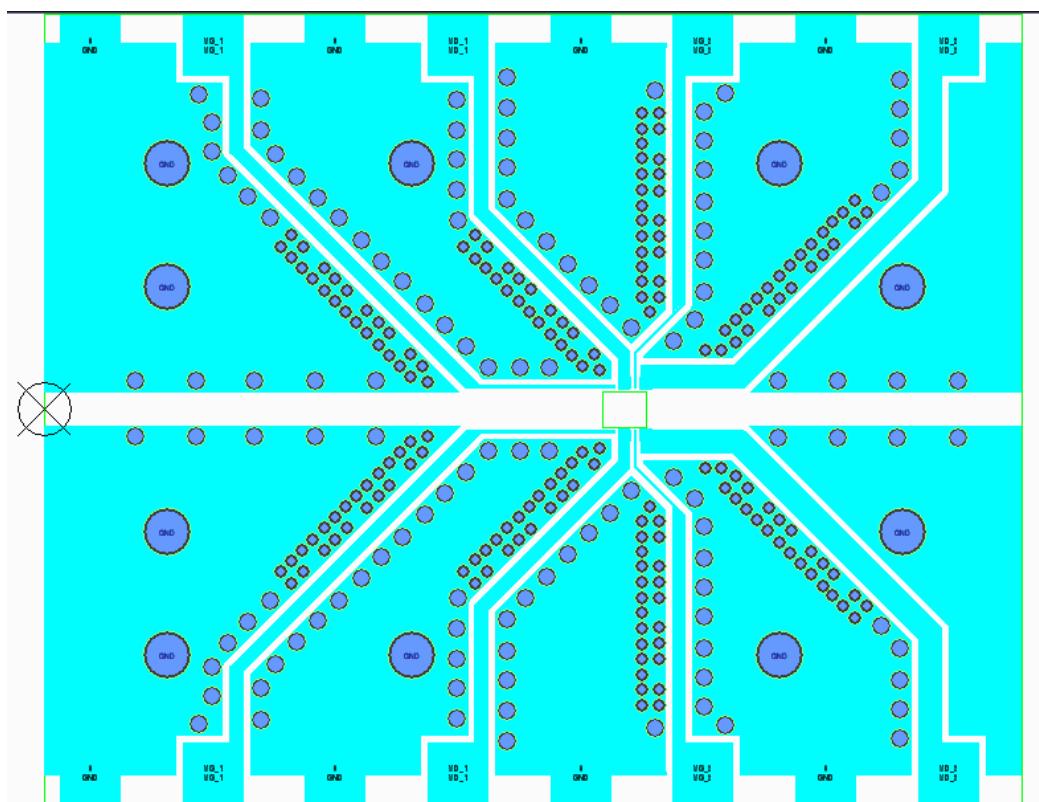


Figure 6.19 Layout of the DC board of the MMIC chip.

We have two measurement setups. First one is for S-parameter measurements. Second one handles CW power measurements. Photograph of our S-parameter measurement setup is given in Figure 6.20. This setup contains Agilent E8361C (10MHz-67GHz) PNA network analyzer, Cascade Microtech RF-1 Microwave probing station, Agilent U8001A single output (0-30V, 3A) DC power supply, and Agilent E3631A triple output (0-6V, 5A / 0±25V, 1A) DC power supply. Before taking the S-parameter measurements, on wafer calibration of the PNA is carried out so that reference planes of the measurements are assigned to tip of the probes.

S-parameter measurement data and simulation results are given in Figures 6.21-24. We need to focus on the frequency range between 18GHz and 22GHz for simulation results since our Lange coupler EM simulation covers only this band. Measurement results are obviously better than simulation results. This fact shows our cautious design approach worked quite well.

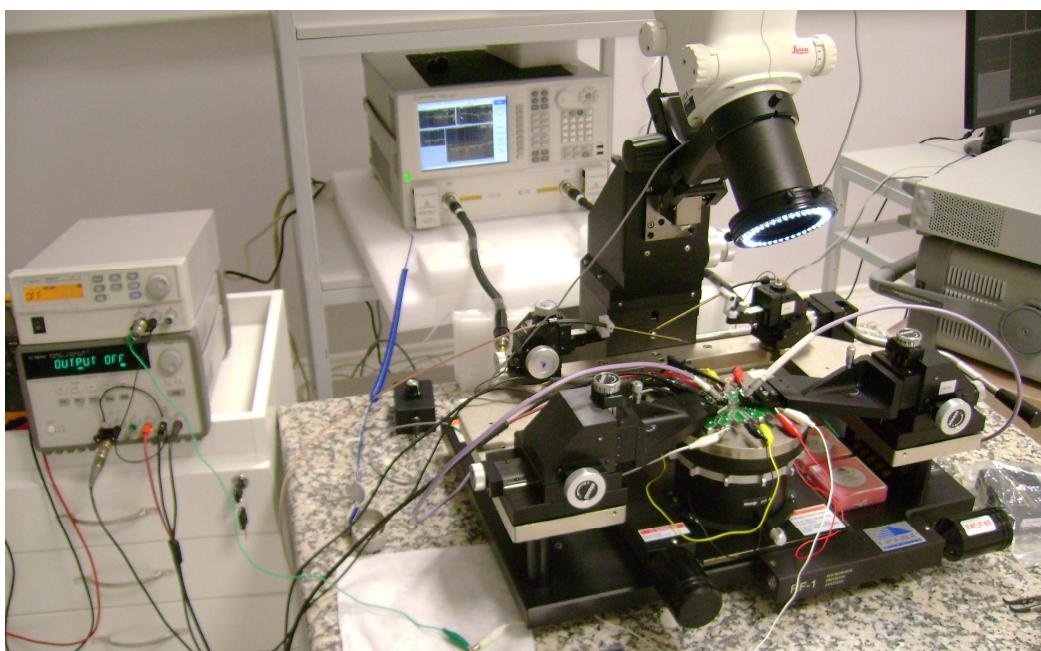


Figure 6.20 Photo of our S-parameter measurement setup.

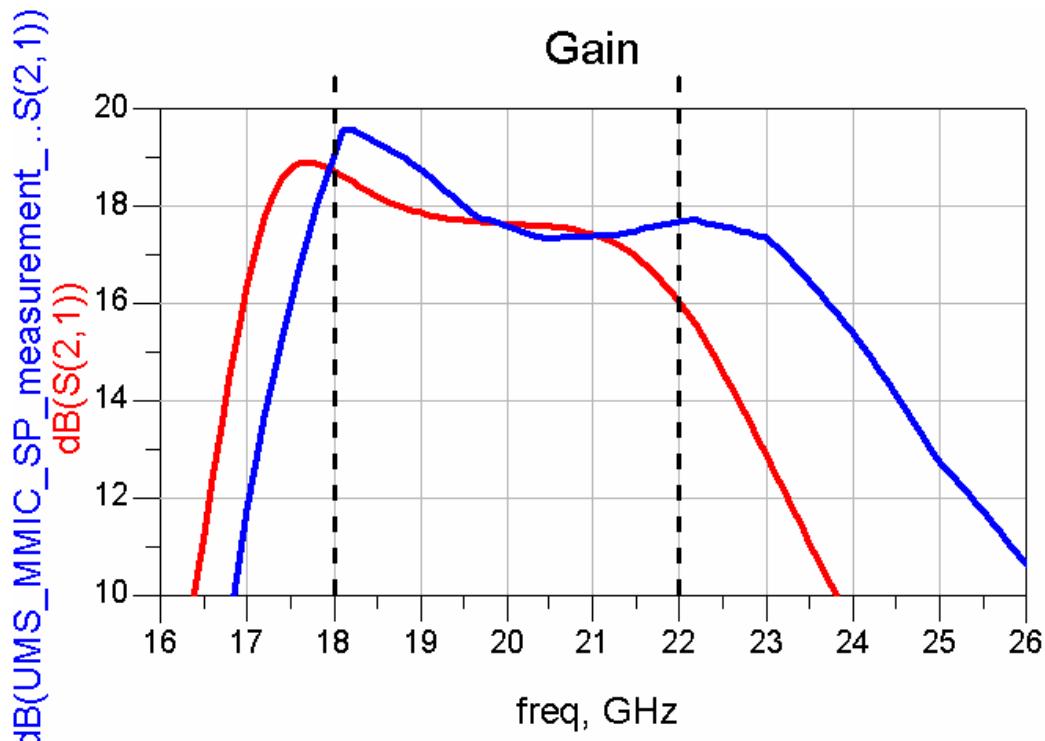


Figure 6.21 Gain comparison between measurements and simulations.

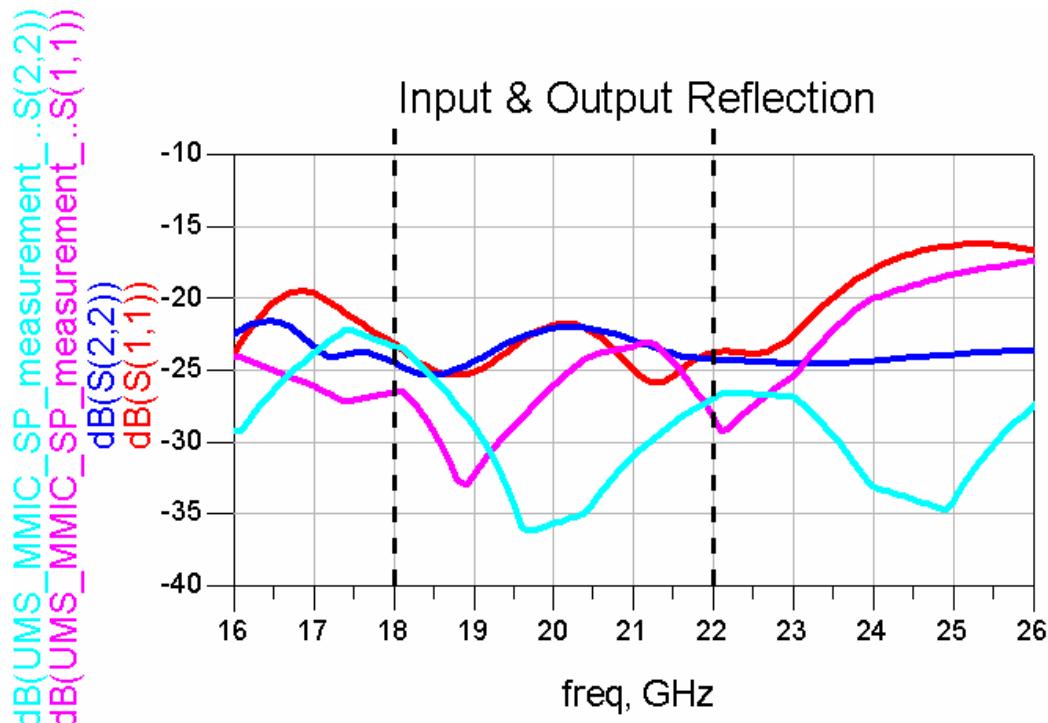


Figure 6.22 I/O Reflection comparison between measurements and simulations.

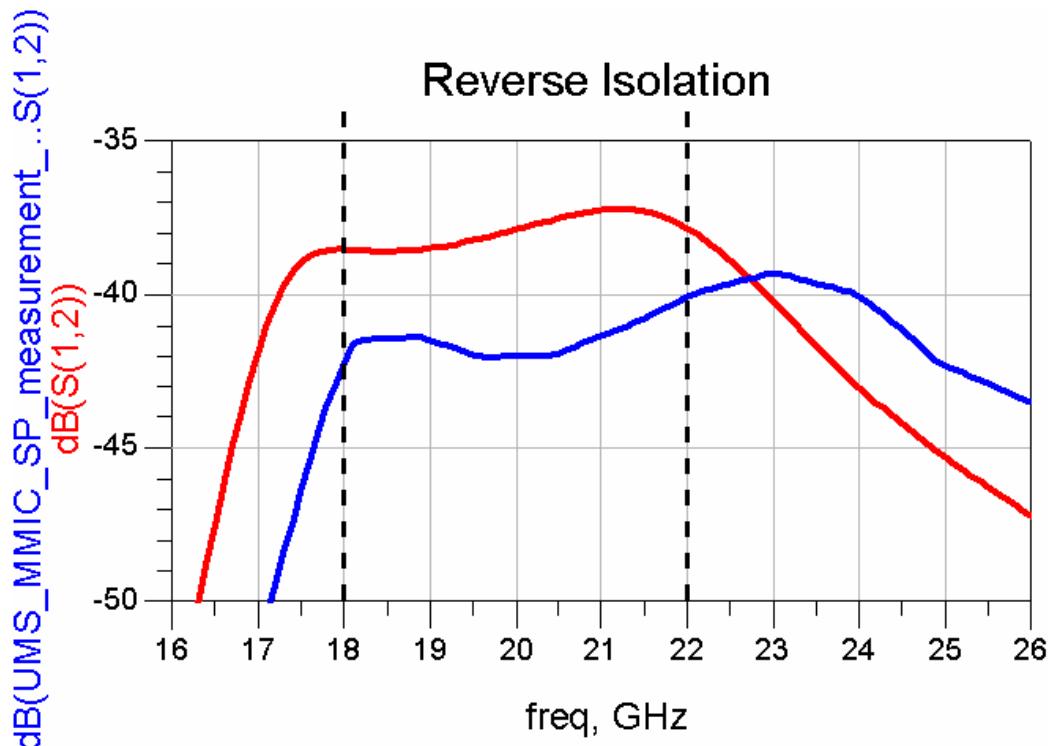


Figure 6.23 Reverse isolation comparison between measurements and simulations.

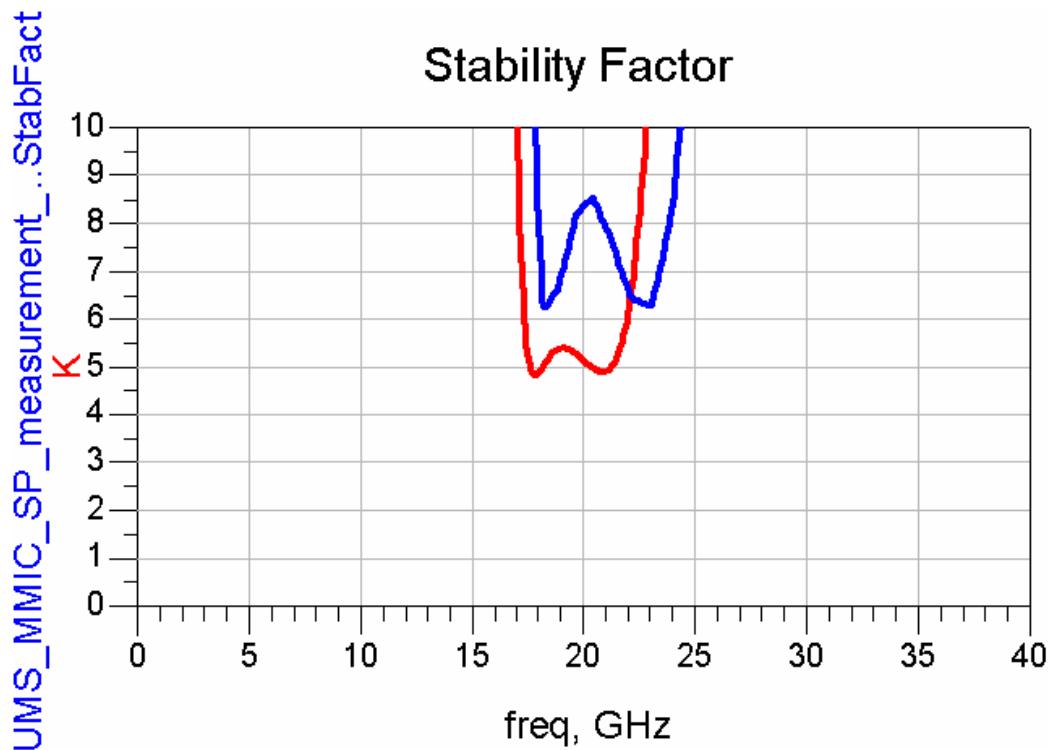


Figure 6.24 Stability factor comparison between measurements and simulations.

Photograph of our CW power measurement setup is given in Figure 6.25. This setup contains Agilent N5183A MXG (100kHz-32GHz) analog signal generator, Agilent 83020A power amplifier, Agilent 87422A power supply, Cascade Microtech RF-1 Microwave probing station, Agilent U8001A single output (0-30V, 3A) DC power supply, Agilent E3631A triple output (0-6V, 5A / 0- \pm 25V, 1A) DC power supply, Agilent E4407B ESA-E Series (9kHz-26.5GHz) spectrum analyzer, and Maury 20dB attenuator. Before taking the CW power measurements, through calibration is carried out so that reference planes of the measurements are determined to be at I/O RF pads of the MMIC chip.



Figure 6.25 Photo of our CW power measurement setup.

Harmonic balance (HB) simulation results under 16dBm input signal level is given in Figure 6.26. Output power levels between 32.6dBm and 32.9dBm, and PAE values between 31.4% and 35.2% are obtained at 18-22GHz operation band. Amount of power dissipated at input and output Lange coupler 50 Ohm resistors are given in Figure 6.27. Under normal operation conditions, very low power loss levels are obtained both at input and output 50 Ohm isolation terminations.

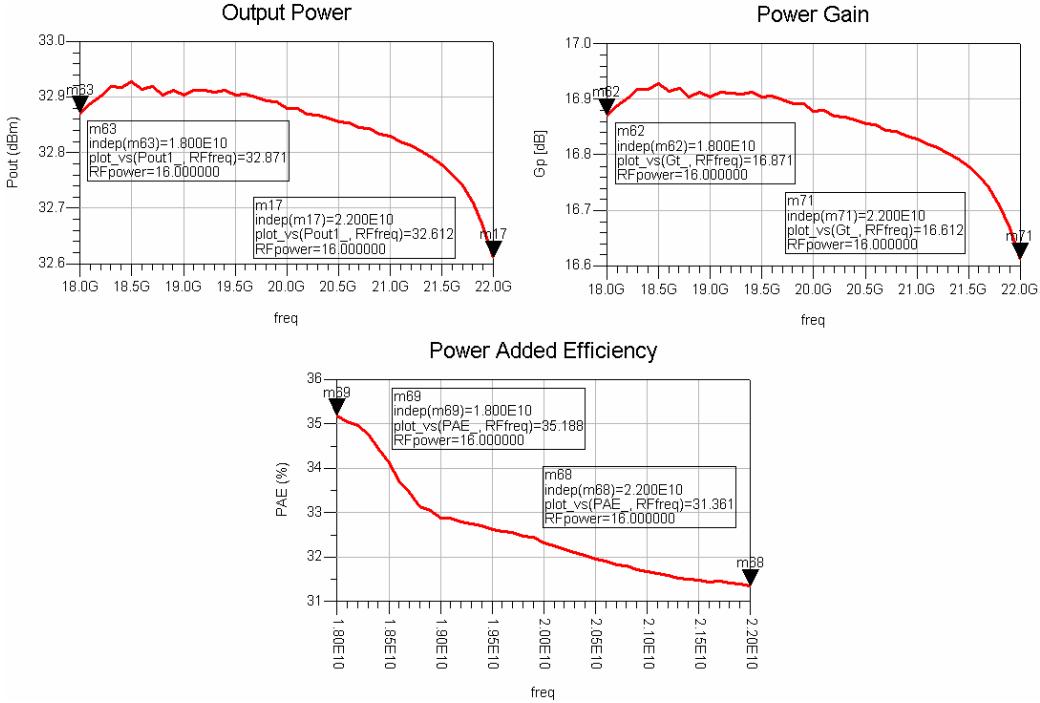


Figure 6.26 HB simulation results of our MMIC chip under 16dBm input signal level.

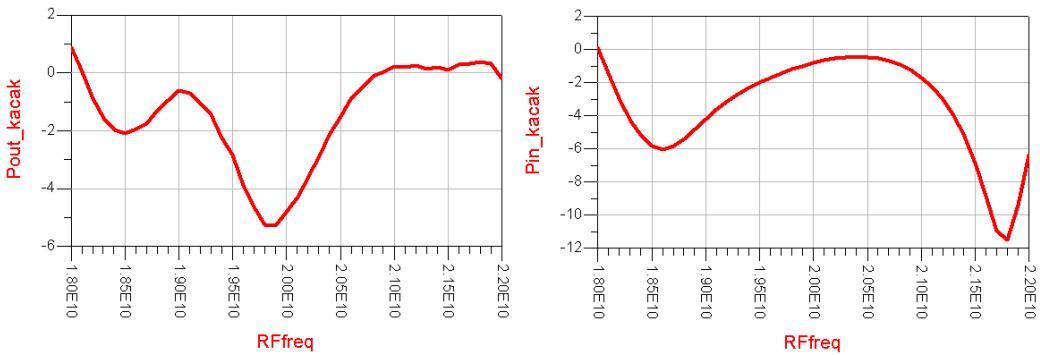


Figure 6.27 Power dissipation at input and output Lange coupler 50 Ohm resistors.

CW output power measurement data are given together with input power sweep simulation results in Figures 6.28-30 at 18GHz, 20GHz, and 22GHz, respectively. Since UMS PPH25X design kit contains pulsed measurement based transistor models, we expect to have output power degradation at CW case up to 1-2dB. Considering this criteria, our CW power measurement data are in agreement with simulation results. Moreover, power gain converges to measured small-signal gain at low input power levels. Unfortunately, we could

not carry out pulsed measurements due to lack of measurement equipments compatible for pulsed measurements at K-band. As a result, we successfully validated our K-band MMIC PA design with consistent measurement results.

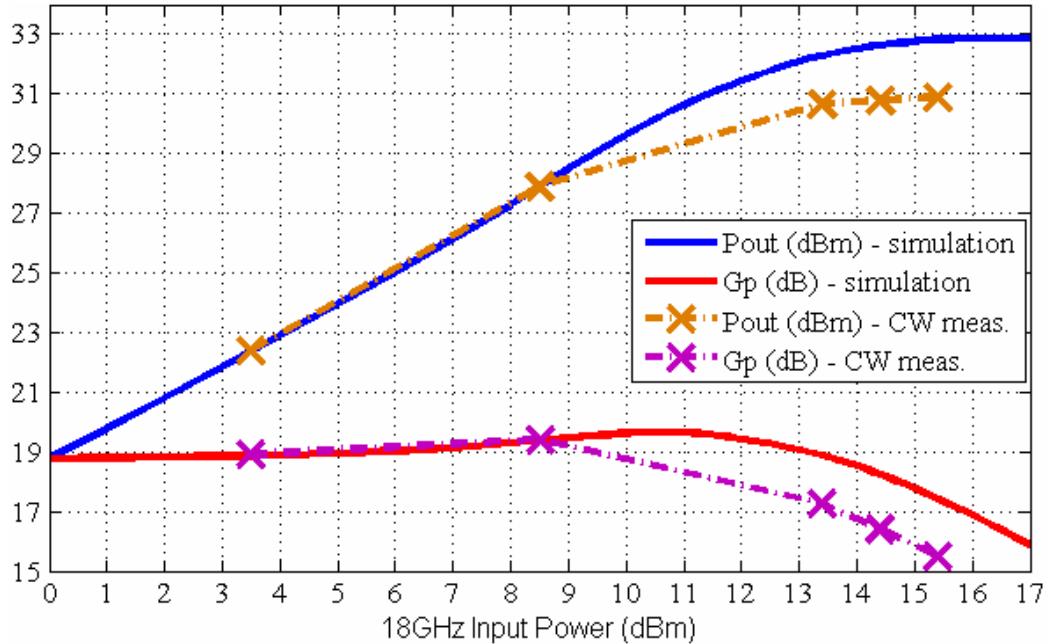


Figure 6.28 Output power and power gain simulation and measurement results at 18GHz.

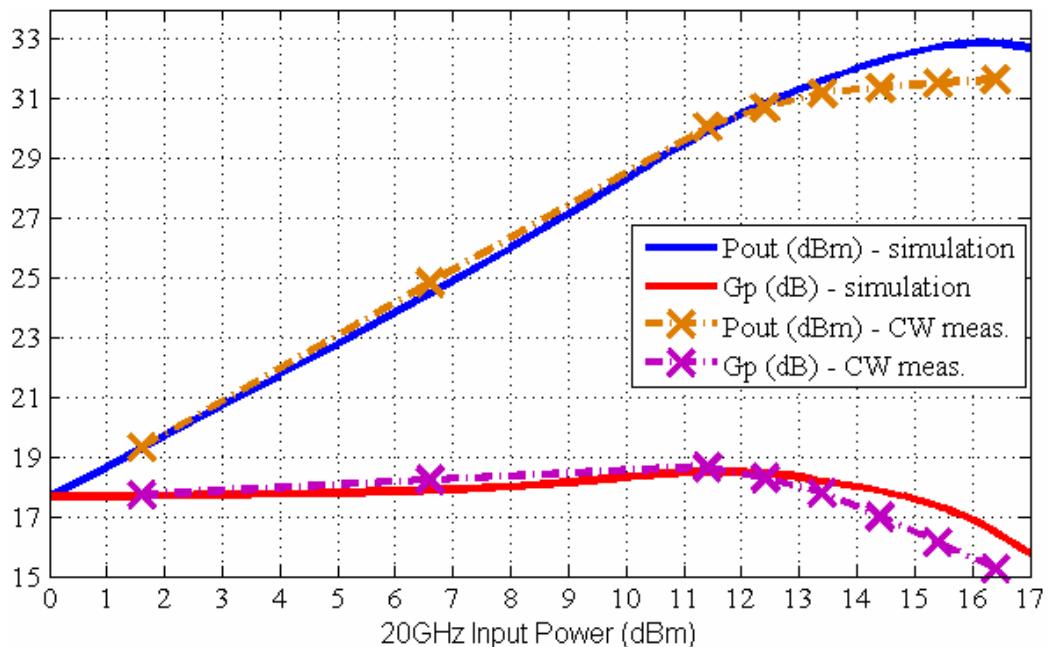


Figure 6.29 Output power and power gain simulation and measurement results at 20GHz.

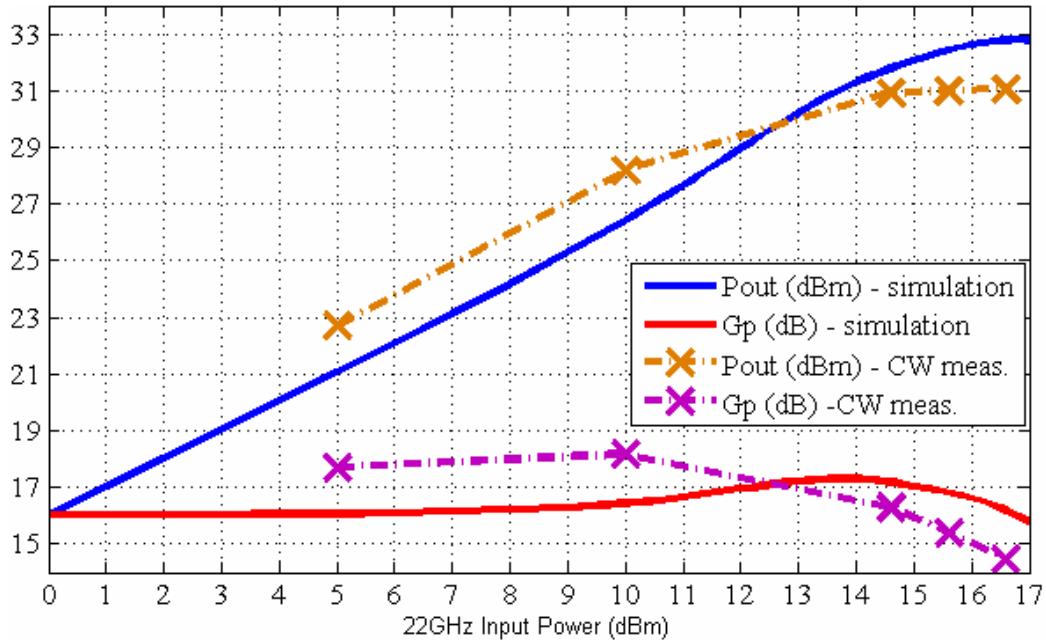


Figure 6.30 Output power and power gain simulation and measurement results at 22GHz.

To summarize S-parameter measurement results of our MMIC chip, 17.5dB to 19dB small-signal gain, less than -25dB input and output reflection, less than -40dB reverse isolation and unconditional stability are observed. When it comes to CW output power measurements, 31dBm at 18 GHz, 31.7dBm at 20 GHz, and 31dBm at 22 GHz maximum output power levels are obtained.

Two microscope images and a photograph of the MMIC PA chip are given in Figures 6.31-33.

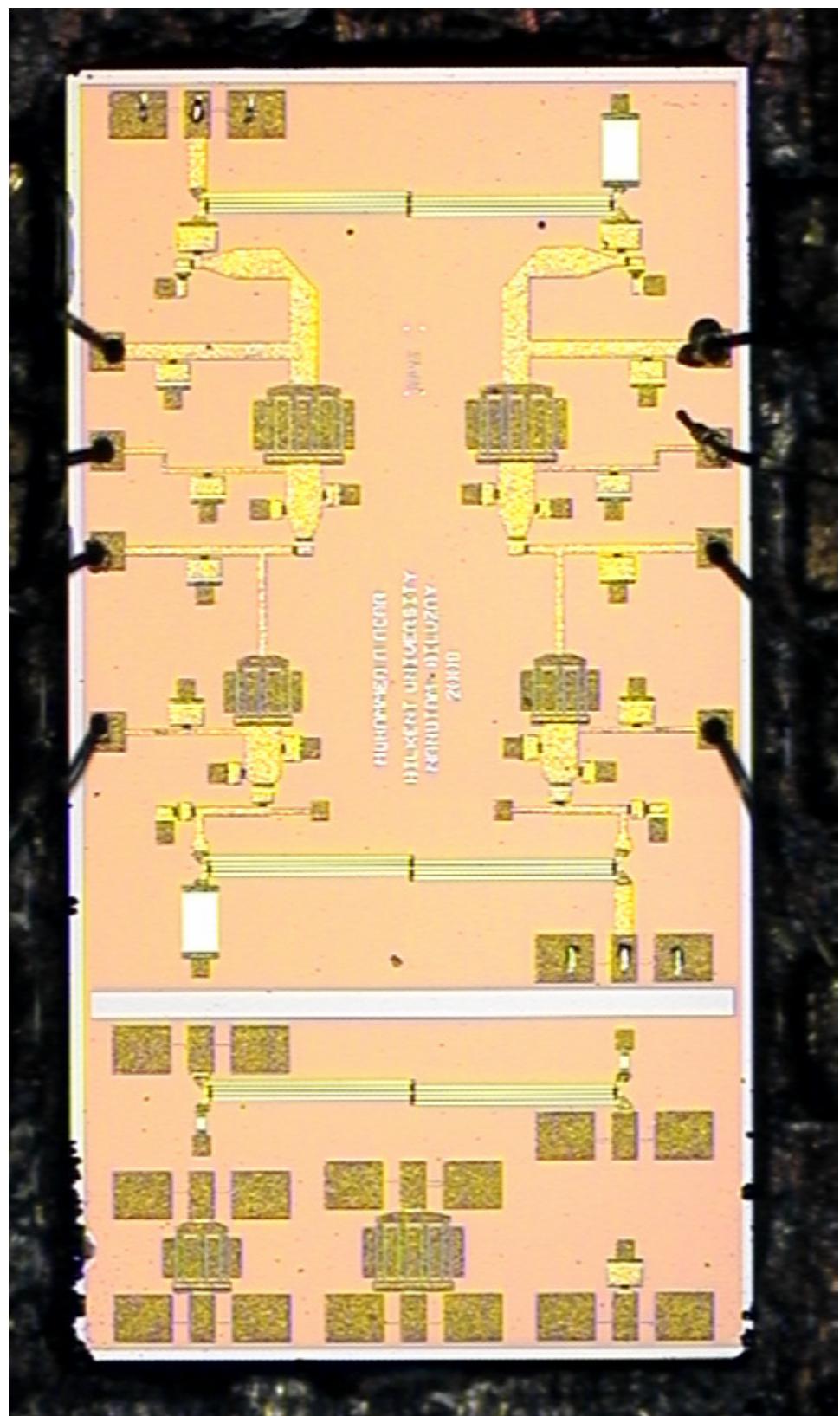


Figure 6.31 Microscope image of the GaAs MMIC PA chip.

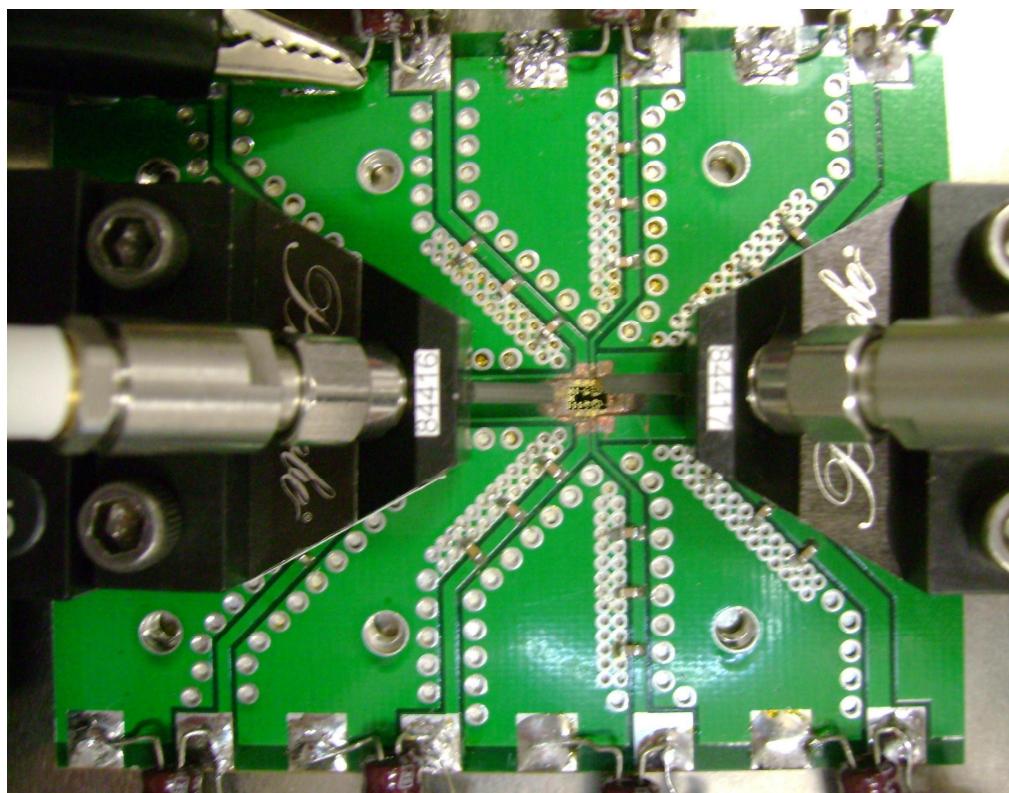


Figure 6.32 Photo of the MMIC chip on the DC board under probe station.

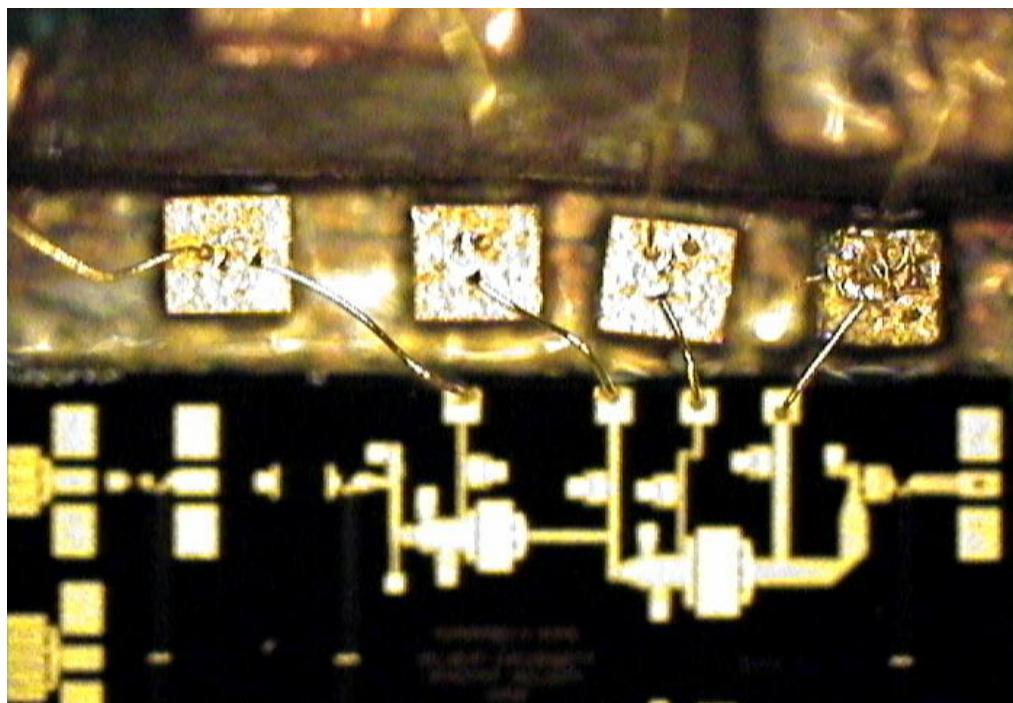


Figure 6.33 100pF single layer by-pass capacitors next to the MMIC chip.

Chapter 7

Summary & Future Work

During this work, we have dealt with wide range of subjects on GaN HEMT technology and MMIC PA designs. GaN HEMT concept is introduced starting from the physical basics and expanded to realization and modeling of the devices through the MOCVD growth, microfabrication process and characterization steps. Then, CPW GaN MMIC PA design works are explained step by step and simulation results are illustrated. Finally, more complicated design, which is a balanced two-stage MMIC PA topology, is applied using high power GaAs pHEMT PPH25X design kit of UMS foundry. K-band design considerations of this design are introduced in detail. The MMIC chip is fabricated by UMS. The fabricated chip is measured on prepared DC board. Wire bonds are used for electrical connections between the chip and the DC board. The design is validated by comparison of S-parameter and CW output power measurement data with corresponding simulation results.

As a future work, after solving repeatability issues of our GaN HEMT fabrication process and improving transport properties of our transistors, our own design kit based on GaN HEMT technology can be developed by applying the temperature dependent large-signal nonlinear modeling approach that we mentioned in Chapter 4. Then, we will be able to transform our high frequency

and high power MMIC PA design capabilities to our promising high frequency and high power GaN technology.

Appendix-A

MOCVD Growth Steps of our GaN HEMT samples

Epitaxial Layers	B-1540	B-1545
GaN cap layer	Reactor temperature: 1100°C, Reactor pressure: 50 mbar Gases: 5 sccm TMGa, 500 sccm NH ₃ Thickness: 3 nm	Reactor temperature: 1075°C, Reactor pressure: 50 mbar Gases: 5 sccm TMGa, 200 sccm NH ₃ Thickness: 3 nm
Undoped AlGaN barrier Layer	Reactor temperature: 1100°C, Reactor pressure: 50 mbar Gases: 5 sccm TMGa, 10 sccm TMAI, 500 sccm NH ₃ Thickness: 30 nm	Reactor temperature: 1075°C, Reactor pressure: 50 mbar Gases: 5 sccm TMGa, 10 sccm TMAI, 200 sccm NH ₃ Thickness: 30 nm
AlN interlayer	Reactor temperature: 1100°C, Reactor pressure: 50 mbar Gases: 10 sccm TMAI, 200 sccm NH ₃ Thickness: 1-2 nm	Reactor temperature: 1075°C, Reactor pressure: 50 mbar Gases: 10 sccm TMAI, 200 sccm NH ₃ Thickness: 1-2 nm
Buffer layer	GaN Reactor temp.: 1030-1100°C Reactor pressure: 200 mbar Gases: 10-17 sccm TMGa, 1350-1800 sccm NH ₃ Thickness: 1700 nm (in total)	GaN Reactor temp.: 1000-1100°C, Reactor pressure: 200 mbar Gases: 10-17 sccm TMGa, 1350-1800 sccm NH ₃ Thickness: 1790 nm (in total) AlN Reactor temperature: 1130°C, Reactor pressure: 25 mbar Gases: 25 sccm TMAI, 50 sccm TMIn, NH ₃ ~ from 150 to 40 sccm in 1 min Thickness: 320 nm
Nucleation layer	LT-GaN Reactor temperature: 500°C Reactor pressure: 200 mbar Gases: 5 sccm TMGa, 1500 sccm NH ₃ Duration: 250 sec.	LT-AlN Reactor temperature: 750°C Reactor pressure: 50 mbar Gases: 15 sccm TMAI, 300 sccm NH ₃ Duration: 90 sec.

Appendix-B

Fabrication Process Summary of our GaN HEMTs

1. *MESA*

Lithography: AZ5214E

RIE dry etch: Freon-20sccm-200W-8μbar-3min.

2. *Ohmic Contacts:*

Lithography: TI35ES

Metalization: Ti/Al/Ni/Au (150Å/1500Å/400Å/700Å)

RTP annealing: 850C-30sec.

3. *Gate lithography - RIE O₂ descum etching - Metalization:*

Lithography: PMMA-A6-950K

RIE dry etch: O₂-40sccm-50W-33μbar-10sec.

Metalization: Ni/Au (500Å/3000Å)

4. *Gate Pad Metalization:*

Lithography: TI35ES

Metalization: Ti/Au (500Å/2500Å)

5. *SiN deposition - Etching:*

PECVD: 30min.

RIE dry etch: CHF₃-O₂-27sccm-8sccm-200W-33μbar-4min.

6. *Bridge post & Reflow:*

Lithography: Su1828

Reflow: 150C-10min.

7. *Seed layer:*

Metalization: Ti/Au (500Å/2500Å)

8. *Interconnect metalization:*

Lithography: TI35ES

Metalization: Electroplated Au (2um)

9. *Ti protect layer deposition:*

Metalization: Ti (500Å)

10. *Seed layers removing:*

Golden etchant - HF

11. *Bridge post removing:*

Ultrasonic Cleaner - Aceton

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