Physics-Based Analytical Model for Input, Output, and Reverse Capacitance of a GaN HEMT With the Field-Plate Structure

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Abstract—This paper presents an analytical model for input, output, and reverse capacitance of a normally ON AlGaN/GaN high-electron mobility transistor (HEMT) with a gate field-plate structure, when the device is in the subthreshold regime. Together with the existing model for the output I–V characteristics, the proposed capacitance model provides the complete set of analytical equations that relate the physical design parameters to the electrical characteristics of the device. The model was verified by the experimental characterization of a HEMT. In comparison to the physics-based models implemented in Finite Element Analysis tools, the obtained capacitance model has substantially lower level of complexity and, therefore, it is more suitable for implementation into iterative design optimization algorithms. In order to verify the proposed model for such usage, the prototype of a high-frequency buck converter was built, using previously modeled GaN HEMT as the main switch. The hybrid analytical-behavioral power loss model of a high-frequency buck converter was implemented into Simplorer simulation tool, using the proposed physics-based model as the device description for the capacitive part. The efficiency measurements showed good agreement with the simulation results, even at 20 MHz of switching frequency in the low range of the output power.

Index Terms—Field-plate structure, GaN-based high-electron mobility transistors (HEMTs), HEMT design optimization, OFF-state capacitance modeling, physics-based model.

I. INTRODUCTION

OVER the last few years, AlGaN/GaN high-electron mobility transistors (HEMTs) are considered to be the most promising candidates for high-frequency (HF) switching applications [1]. In comparison to commonly used Silicon MOSFETs, switching devices based on Gallium Nitride provide several times better figure of merit (defined as a product of on-resistance
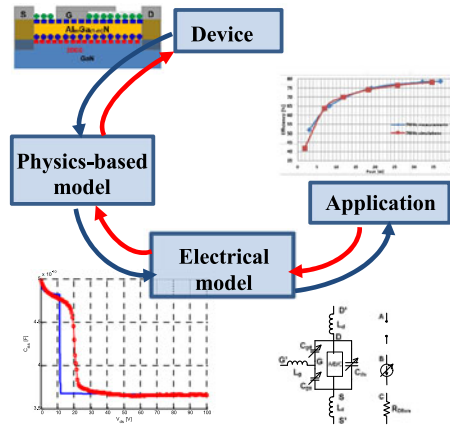
Fig. 1. Block scheme of a device design optimization.

and gate charge), because of their wider bandgap, higher critical electric field and saturation velocity [2]–[4]. Additional application of the field-plate structure provides even higher breakdown voltages [5]–[8] and reduces dynamic on-resistance which is one of the major concerns when AlGaN/GaN HEMTs are used as switching devices [9].

The target application for GaN device that will be analyzed and modeled in this work is a HF dc–dc converter called envelope amplifier, used as a dynamic power supply in envelope tracking and envelope elimination and restoration transmission techniques. The main challenge in envelope amplifier design is to increase the bandwidth of the signal transmission together with the overall efficiency of the converter [10]–[17].

In order to improve the design of the existing GaN devices for this particular application, it is required to obtain a reliable physics-based model that provides the connection between the device design parameters (geometry and spacing between the electrodes, type and geometry of the field plate, etc.) and electrical characteristics in terms of switching on-resistance and parasitic capacitances. In general, the physics-based model can be used to calculate the power losses in a certain topology where the device is applied, or to optimize the device design from the application point of view. This process is described by the block diagram in Fig. 1 where starting from the device itself and following the blocks in the counter clockwise direction, the overall efficiency of the chosen topology is being estimated. Alternatively, starting from a certain application and following

the same blocks in the clockwise direction, the device design is being optimized by power losses minimization. In both cases, the device description through analytical equations is needed. Therefore, a physics-based model is a necessary link between the device itself and its application.

Regarding the physics-based models of GaN HEMTs, charge-based and surface-potential-based models for currents and capacitances in the case of GaN HEMTs without the field-plate structure, have been widely investigated and presented [18]–[21]. A different modeling approach based on division by charge method also provided the compact physical I–V and C–V model [22], while [23] presented the improved capacitance model, taking into consideration parasitic capacitances and fringing between the electrodes. Analyzing these physics-based models, it can be said that GaN HEMT structure without the field plate has been completely modeled in terms of I–V and C–V characteristics. Since the field-plate influence on the I–V output characteristics and switching on-resistance is negligible, the I–V models from previous works can be applied in the case of GaN HEMTs that contain the field plate, without expectation of a significant error. However, the input, output, and reverse capacitance of the device are strongly affected by the type and the geometry of the field plate and previously referenced charge models cannot be used. Currently, most of the existing analytical models for GaN HEMTs that contain the field plate are focused on the calculation of the surface potential distribution and the channel electric field, with the aim of field-plate design optimization for a given breakdown voltage [24], [25]. However, the optimum electric field management is the only considered criterion in this optimization process, while the associated Miller's capacitance that is crucial for HF power performance is not taken into account.

Most of the previous works that relate the capacitances of the GaN HEMTs to the field-plate design were focused on the analysis of Miller's capacitance, $C_{\rm gd}$, in the case of GaN HEMTs designed for microwave application. For example, in [26] some qualitative explanations of Miller's capacitance origin were presented and a simple guideline on the field-plate design for the microwave application was provided. In [27], additionally, a simple model for $C_{\rm gd}$ that includes/excludes the capacitance under the field-plate electrode at lower/higher drain biases was given, using the maximum stable gain estimations based on s-parameters measurements. In [28], the characteristics of HEMTs with various field-plate and gate–drain dimensions were carried out only experimentally, while in [29], Miller's capacitance of a GaN HEMT with multiple field-plate structure was measured and different parts of this nonlinear dependence on the applied drain–source voltage were again qualitatively analyzed. Overall, the previous works provide the physical insight on the origin of Miller's capacitance in GaN HEMTs with the field-plate structure and provide some simple guideline on the device design for the microwave application, while the complete analytical model for capacitances of a HEMT designed for a switching application is still missing.

The common methods for design and analysis of GaN HEMTs with one or multiple field-plate structure are the Finite Element Analysis (FEA) simulations [5], [6], [30]. Although FEA simulations are quite useful for the field-plate design

$V_{\rm ds}$ [V]	I_d [A]	Measured $V_{\rm th}$ [V]	Substrate	Package
100	27	−2	SiC	TO-220

optimization for a given breakdown voltage, their drawback is the necessary fitting of the design equations to the simulated data curves, which makes the optimization valid only for the simulated structure. Therefore, FEA cannot be used for the complete design optimization of the device. On the other hand, the physical models implemented into FEA device simulation software are quite complex and time consuming. Therefore, these physics-based models are not suitable for incorporation into iterative optimization tool which is used for obtaining the optimum device design for a particular application.

This paper presents the complete physics-based analytical model for input, output, and reverse capacitance of the Al-GaN/GaN HEMT with the field-plate structure, when the device is in the OFF state.

The basic considerations of the capacitance modeling methodology presented in this paper have been addressed in [31], [32]. Since the capacitance modeling demands solving two-dimensional (2-D) Poisson's equation, the proposed methodology is based on the approximation of the charge depletion in two separated directions: perpendicularly (vertically) and laterally with respect to the channel. The vertical depletion of the two-dimensional electron gas (2DEG) leftover under the field-plate is modeled by applying Poisson's equations for AlGaN and GaN layers, together with Gauss law for charge conservation. The lateral extension of the depletion area around the drain-side gate edge and the field-plate edge is modeled by applying conformal mapping technique from [33], using the proposed modifications for the field-plate structure. This approach provides the complete model for Miller's capacitance of the device.

The origin of gate–source and drain–source capacitances $C_{\rm gs}$ and $C_{\rm ds}$ is found in the fringing between the corresponding electrodes inside the device as well as in the fringing between the pads that connect all fingers in the multifinger layout. Each of these fringing capacitances is modeled using the model from [34]. In this way, the complete model for $C_{\rm rss} = C_{\rm gd}$, $C_{\rm oss} = C_{\rm gd} + C_{\rm ds}$ and $C_{\rm iss} = C_{\rm gd} + C_{\rm gs}$ is obtained. Together with the existing model for I–V characteristics from [35], the proposed capacitance model provides the complete physics-based model for this type of switching devices. Having a quite low level of complexity, the proposed model is highly suitable for device design optimization for HF application.

II. GATE-TO-DRAIN (MILLER'S) CAPACITANCE MODELING

The GaN HEMT that will be analyzed and modeled in the following sections is a normally ON device with basic characteristics presented in Table I. The cross section of the device together with the charge distribution when the device is in the OFF state is shown in Fig. 2 while the values for the corresponding geometrical parameters are given in Table II. The physical
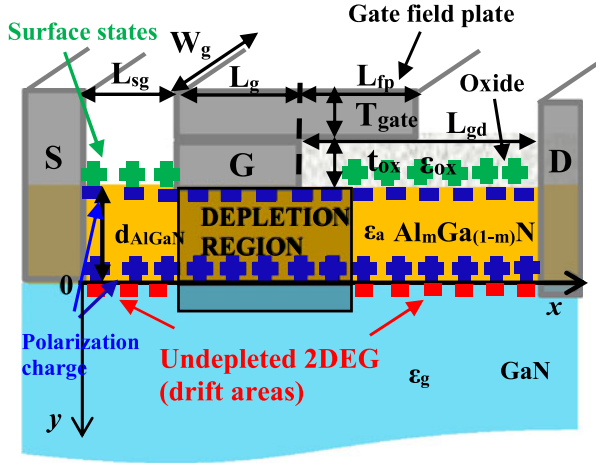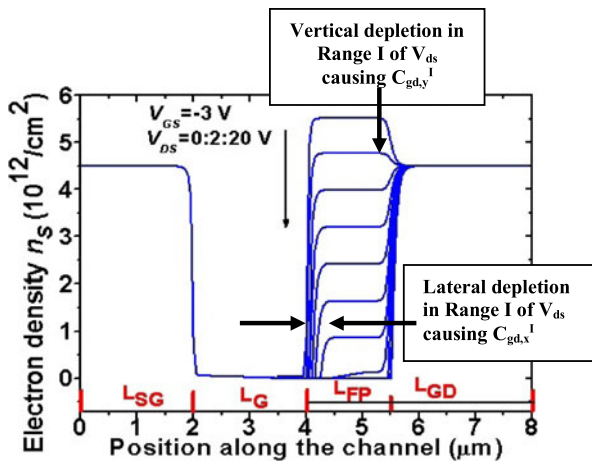
Fig. 2. Cross section of a GaN HEMT in the OFF state.

TABLE II
GEOMETRICAL PARAMETERS OF THE DEVICE

W_g [mm]	L_g [μm]	L_{sg} [μm]	L_{gd} [μm]	L_{fp} [μm]	t_{OX} [nm]	T_{gate} [nm]	d_{AlGaN} [nm]
120	2	2	4	1.5	80	100	24

TABLE III
PHYSICAL PROPERTIES OF THE HETEROSTRUCTURE

φ_{mi} [V]	m [%]	σ_{PZ} [C/m^2]	ε_a [C/(Vm)]	ε_g [C/(Vm)]	ε_{OX} [C/(Vm)]	ΔE_c [V]
2.2	24	0.01	$8.3\ 10^{-11}$	$8.6\ 10^{-11}$	$6.2\ 10^{-11}$	0.3

Fig. 3. Simulation of 2DEG depletion process under the field plate for V_{ds} up to 20 V.

parameters of the insulator/AlGaN/GaN heterojunctions are given in Table III.

The starting point for the analytical model of Miller's capacitance is the COMSOL simulation of the 2DEG distribution in the channel, in the conditions where gate–source voltage V_{gs} is kept below the threshold while drain–source voltage V_{ds} is being varied (see Figs. 3 and 4). Simulation results show that
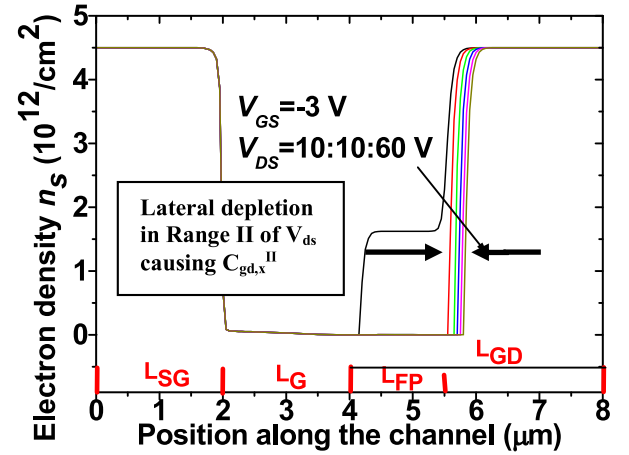
Fig. 4. Simulation of 2DEG depletion process under the field plate for V_{ds} up to 60 V.

significant amount of 2DEG leftover directly under the field plate is being depleted as V_{ds} increases up to approximately 14 V. On the other hand, Fig. 4 shows that for higher V_{ds}, only small lateral extension of the depletion area exists. In order to model these variations in the depletion area by avoiding FEA tools for solving 2-D Poisson's equation, two directions will be distinguished:

1) y-direction which is referred to the variation in the 2DEG density in one fixed point along the channel;
2) x-direction which is referred to the extension of the depletion laterally (see Fig. 2).

From the simulations results presented in Fig. 3 and 4, two ranges of V_{ds} can be distinguished: the Range I which covers the values up to approximately 14 V, where both vertical and lateral depletion of 2DEG exist and the Range II for V_{ds} higher than 14 V, where only lateral depletion exists.

A. Model for Vertical Depletion

In order to obtain the analytical model for 2DEG depletion process in y-direction, the following methodology is proposed. Since V_{gs} is kept constant at the value just below the threshold while V_{ds} is being varied, the depletion process can be analyzed as if the 2DEG under the field plate is being controlled by the gate-to-drain voltage, V_{gd}. The V_{gs} voltage that keeps the device in the OFF state is marked as V_{gs}^* and is equal to -3 V in this analysis.

The following analysis is based on the energy band-diagram of the metal–insulator–semiconductor HEMT (MISHEMT) structure (see Fig. 5). The reference point for the $v_a(y)$ potential is set to the bottom of the quantum well ($v_a(w_a^+) = 0$) as well as the position of the Fermi level voltage E_F for the complete range of V_{gd}. Basically, the value of Fermi level will depend on the applied V_{gd}, but comparing the values of E_F to the values of V_{gd}, this dependence can be ignored [36].

Since the AlGaN layer of the analyzed device is unintentionally doped, the doping density of charge in this layer will be neglected. Therefore, the Poisson's equation for the AlGaN
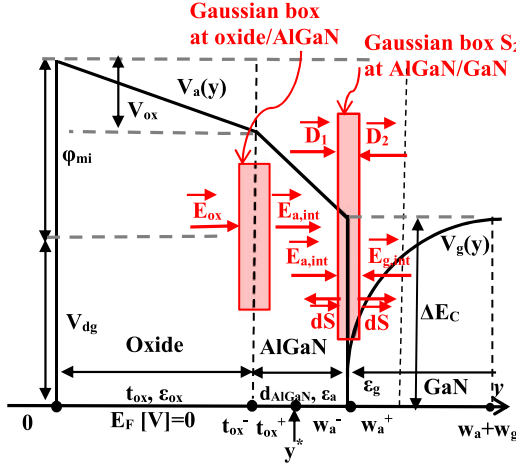
Fig. 5. Energy band-diagram of the MISHEMT structure.

layer is given by

$$\frac{d^2 v_a}{dy^2} = 0 \tag{1}$$

while the boundary conditions for the $v_a(y)$ are $v_a(0^+) = V_{dg} + \varphi_{mi}$ and $v_a(w_a^-) = \Delta E_C$. The electric field value at the AlGaN/GaN heterojunction is equal to

$$E_{a,\text{int}} = -\left.\frac{dv_a(y)}{dy}\right|_{y=w_a^-} \tag{2}$$

where $w_a = t_{ox} + d_{AlGaN}$. If (1) is being integrated from the point $y = y^*$ in the AlGaN layer to the point $y = w_a^-$ together with (2), it gives

$$E_{a,\text{int}} = -\left.\frac{dv_a(y)}{dy}\right|_{y=y^*}. \tag{3}$$

The previous equation shows that vertical component of the electric field inside AlGaN layer is constant, which is expected since the doping charge was neglected. Integration of (3) from $y = t_{ox}^+$ to $y = w_a^-$ gives

$$v_a\left(t_{ox}^+\right) - v_a\left(w_a^-\right) = E_{a,\text{int}}\left(w_a - t_{ox}\right). \tag{4}$$

Substituting the boundary condition for $v_a(t_{ox}^+)$ in (4) the electric field $E_{a,\text{int}}$ is obtained

$$E_{a,\text{int}} = \frac{v_a\left(t_{ox}^+\right) - \Delta E_c}{\left(w_a - t_{ox}\right)}. \tag{5}$$

From the band-diagram shown in Fig. 5, $v_a(t_{ox}^+)$ can be determined as

$$v_a\left(t_{ox}^+\right) = V_{dg} + \varphi_{mi} - E_{ox}t_{ox} \tag{6}$$

where E_{ox} is the value of the constant electric field inside the oxide of the field-plate, since the dielectric charge has been neglected.

In order to obtain the value of E_{ox}, Gauss law is applied to the surface at the oxide/AlGaN heterojunction (see Fig. 5). In order to simplify the analysis, the following assumptions will be made. Since the polarization field in AlGaN layer is strongly reduced by the field that originates from positive surface states

and negative 2DEG, it will be neglected. Furthermore, the density of the surface states charge will be treated as approximately equal to the density of surface polarization charge. Since the dielectric charge is neglected as well, the E_{ox} is obtained as

$$E_{ox} = \frac{E_{a,\text{int}}\varepsilon_a}{\varepsilon_{ox}}. \tag{7}$$

Combining (5), (6), and (7), the vertical component of the electric field inside the AlGaN layer is obtained

$$E_{a,\text{int}} = \frac{V_{dg} + \varphi_{mi} - \Delta E_c}{\left(w_a - t_{ox}\right)\left(1 + \frac{\varepsilon_a t_{ox}}{\varepsilon_{ox}(w_a - t_{ox})}\right)}. \tag{8}$$

In order to obtain the dependence of the 2DEG sheet density under the field plate on applied V_{gd}, it is necessary to solve Poisson's equation for GaN layer

$$\frac{dE_g}{dy} = \frac{qn_{\text{free},g}}{\varepsilon_g} \tag{9}$$

where $n_{\text{free},g}(y)$ and E_g are the concentration of free electrons and the electric field in GaN layer, respectively. Assuming that depletion area width in GaN layer is w_g, extending from $y = w_a^+$ at the interface to $y = w_a + w_g$, the electric field E_g satisfies the following boundary conditions: $E_g(y = w_a^+) = -E_{g,\text{int}}$ and $E_g(y = w_a + w_g) = 0$. Applying these boundary conditions and integrating (9) between the boundaries of the depletion region in GaN layer, the electric field at GaN/AlGaN heterointerface is obtained

$$E_{g,\text{int}} = \frac{q}{\varepsilon_g} n_{2DEG,FP} \tag{10}$$

where $n_{2DEG,FP}$ is the density of the 2DEG under the field plate.

Finally, in order to complete the obtainment of $n_{2DEG,FP}(V_{dg})$, it is necessary to apply Gauss law for charge conservation at AlGaN/GaN heterojunction in equilibrium. Observing the Gaussian surface S_2 from Fig. 5 and using $D_1 = \varepsilon_a E_{a,\text{int}}$ and $D_2 = \varepsilon_g E_{g,\text{int}}$ it is obtained

$$-\varepsilon_a E_{a,\text{int}} - \varepsilon_g E_{g,\text{int}} = -qn_{PZ}. \tag{11}$$

In (11), n_{PZ} is the sheet density of the 2DEG in equilibrium, equal to the polarization charge sheet density, σ_{PZ}/q. The polarization charge sheet density σ_{PZ} is calculated using [37] and the value for the analyzed structure with 24% of aluminum mole fraction is given in Table III.

Finally, by replacing (8) and (10) in (11), the expression for the vertical depletion of the 2DEG under the field plate is obtained

$$n_{2DEG,FP}(V_{dg}) = n_{PZ} - \frac{\varepsilon_a\left(V_{dg} + \phi_{mi} - \Delta E_C\right)}{q\left(d_{AlGaN} + \frac{\varepsilon_a}{\varepsilon_{ox}}t_{ox}\right)}. \tag{12}$$

Replacing $V_{dg} = -V_{gs}^* + V_{ds}$ in (12), the $n_{2DEG,FP}(V_{ds})$ dependence is obtained and shown in Fig. 6.

Since the vertical depletion of the 2DEG under the field plate is analytically modeled, the part of C_{gd} caused by this process can be calculated. The obtained analytical value for V_{ds} when vertical depletion ends will be marked as V_{ds}^I, since it determines the end of Range I of drain–source voltages. From the
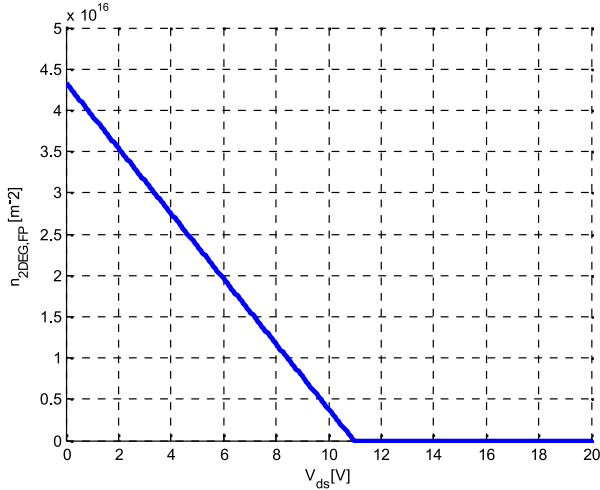
Fig. 6.　Analytical model for vertical depletion of the 2DEG under the field plate.

dependence shown in Fig. 6, it can be seen that $V_{\mathrm{ds}}{}^I = 11$ V. The corresponding part of C_{gd} will be marked as $C_{\mathrm{gd},y}^I$ and is equal to

$$C_{\mathrm{gd},y}^I(V_{\mathrm{ds}}) = qL_{\mathrm{fp}}W_g \frac{dn_{2\mathrm{DEG,FP}}}{dV_{\mathrm{ds}}}. \tag{13}$$

Substitution of (12) into (13) gives

$$C_{\mathrm{gd},y}^I(V_{\mathrm{ds}}) = L_{\mathrm{fp}}W_g \frac{\varepsilon_a}{\left(d_{\mathrm{AlGaN}} + \frac{\varepsilon_a}{\varepsilon_{\mathrm{ox}}}t_{\mathrm{ox}}\right)}. \tag{14}$$

For analyzed structure with parameters from Tables II and III, the obtained value for $C_{\mathrm{gd},y}^I$ is 113.9 pF.

B. Model for Lateral Extension Around the Gate Edge and the Field-Plate Edge

In order to complete the analytical model for $C_{\mathrm{gd}}(V_{\mathrm{ds}})$ in the subthreshold regime, it is necessary to model the dependence of the lateral extension of the depletion region on V_{ds}. In order to clarify where this extension takes place, the simulations of lateral component of the electric field in the channel were done using COMSOL simulation tool (see Fig. 7). Observing the different field distributions from Fig. 7, it can be seen that in the Range I of $V_{\mathrm{ds}}(V_{\mathrm{ds}} \le 11V)$, the lateral extension of the depletion area exists only around the drain-side gate edge while the depletion area around the field-plate edge remains unchanged. On the other hand, in the Range II of $V_{\mathrm{ds}}(V_{\mathrm{ds}} > 11V)$ only the extension around the field-plate edge exists, while the depletion area around the drain-side gate edge remains unchanged. The lateral extensions of the depletion area for the Ranges I and II of V_{ds} will be marked as $b^I(V_{\mathrm{ds}})$ and $b^{II}(V_{\mathrm{ds}})$, respectively. The corresponding parts of Miller's capacitance $C_{\mathrm{gd},x}^I$ and $C_{\mathrm{gd},x}^{II}$ can be calculated as

$$C_{\mathrm{gd},x}^{I/II} = qW_g n_{S0} \frac{db^{I/II}(V_{\mathrm{ds}})}{dV_{\mathrm{ds}}} \tag{15}$$
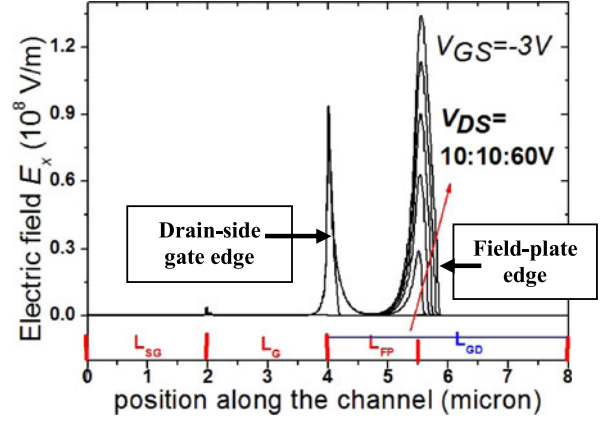

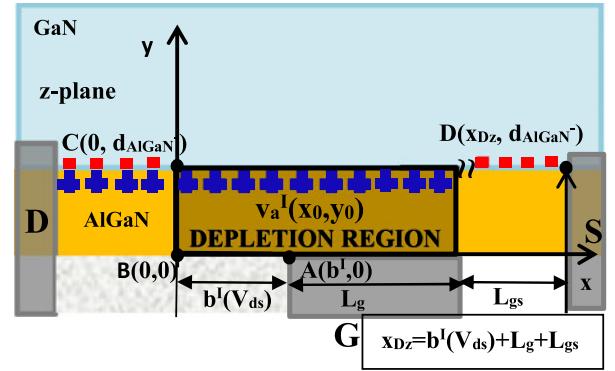Fig. 7.　Simulation of lateral electric field along the channel.

Fig. 8.　Applied physical model for extension of the depletion area around the drain-side gate edge.

where n_{S0} is previously obtained analytical value for 2DEG sheet density for $V_{\mathrm{ds}} = 0$. Observing the dependence from Fig. 6, it can be seen that $n_{S0} = 4.35 10^{16} 1/m^2$.

In order to obtain $b^{I/II}(V_{\mathrm{ds}})$, the methodology from [33] can be used, applying necessary modifications since this methodology was developed for the AlGaN/GaN HEMT without the field-plate structure.

The mathematical model for determination of $b^I(V_{\mathrm{ds}})$ is shown in Fig. 8. In order to obtain $b^I(V_{\mathrm{ds}})$, it is necessary to solve 2-D Poisson's equation in the depletion region of AlGaN layer (see Fig. 8)

$$\nabla^2 v_a^I = 0. \tag{16}$$

In order to solve (16), the following boundary conditions are used. The assumption that positive polarization charge density at the AlGaN/GaN interface is equal to the 2DEG density in the undepleted region, n_{S0}, gives the first boundary condition for $y = d_{\mathrm{AlGaN}}$, shown in Fig. 9. The second boundary condition for $y = 0$ and $x < b^I$ follows from the assumption about equality of positive surface states density and negative polarization charge density. Furthermore, the electric field outside the depletion region is negligible which gives the third boundary condition at the edge of the depletion area (see Fig. 9).
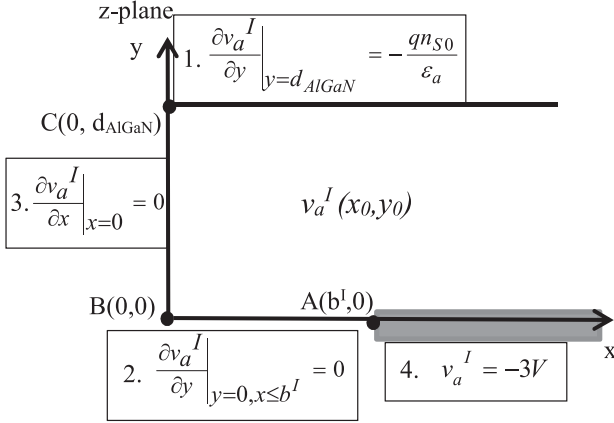
Fig. 9. Applied physical model with boundary conditions in the initial plane, before mapping transformations.
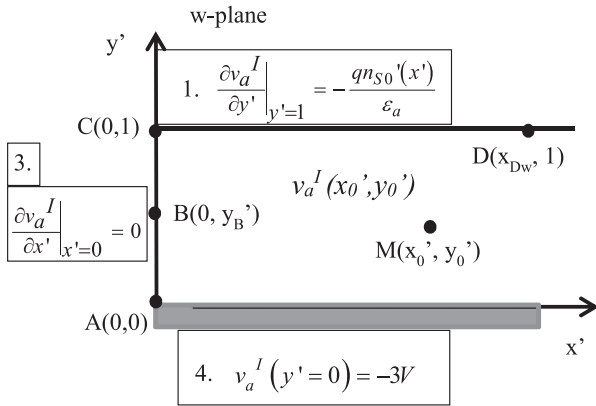

Fig. 10. Applied physical model with boundary conditions after conformal mapping transformations.

Finally, the gate is at the potential of $V_{gs}^* = -3$ V which presents the fourth boundary condition.

In order to avoid FEA tools for solving 2-D (16), the conformal mapping transformations from [33] are applied. In this way, the geometry from the initial z-plane shown in Fig. 9 is being transformed into the one in w-plane shown in Fig. 10. The transformed boundary conditions are also shown in Fig. 10. The transformed sheet density distribution $n_{s0}'(x')$ is obtained by transformation of the boundary conditions and is equal to

$$n_{S0}'(x') = \frac{n_{S0} d_{AlGaN}(c+1)\sinh(\pi x')}{\sqrt{(((c+1)\cosh(\pi x')) - (c-1))^2 - 4}}. \quad (17)$$

In (17), the parameter c is defined as $c = cosh(\pi b(V_{ds})/d_{AlGaN})$ while $b(V_{ds})$ is

$$b(V_{ds}) = \begin{cases} b^I(V_{ds}), V_{ds} \leq V_{ds}^I \\ b^{II}(V_{ds}), V_{ds} > V_{ds}^I \end{cases}. \quad (18)$$

The details about the conformal mapping transformations can be found in [33].

Since the transformed geometry from Fig. 10, contains the gate electrode as the conduction plane, the image charge method can be applied for obtaining the potential inside the depletion
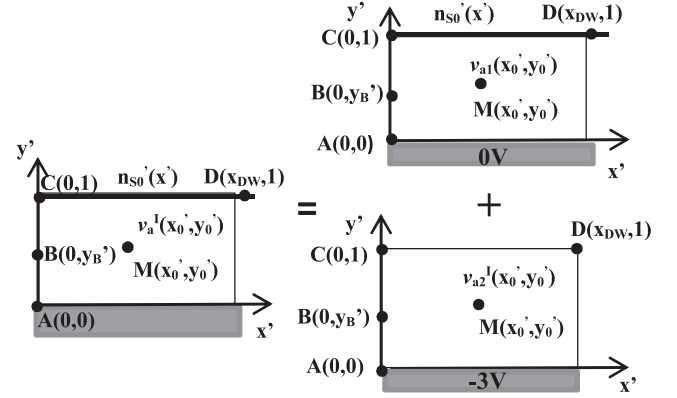

Fig. 11. Principle of superposition for determination of $v_a^I(x_0', y_0')$.

region for Range I of V_{ds}, $v_a^I(x_0', y_0')$. Comparing to the methodology from [33] that neglected the potential of the gate electrode, the following analysis will take it into account. In order to do that, the potential $v_a^I(x_0', y_0')$ will be calculated using the principle of superposition.

This potential will be obtained as

$$v_a^I(x_0', y_0') = v_{a1}(x_0', y_0') + v_{a2}^I(x_0', y_0') \quad (19)$$

where $v_{a_1}(x_0', y_0')$ is the potential that originates only from the sheet density $n_{s0}'(x')$, considering that the conduction plane is at zero volts, while $v_{a2}^I(x_0', y_0')$ is the potential that originates only from the conduction plane in the absence of $n_{s0}'(x')$. The superposition is shown in Fig 11. The dependence $v_{a_1}(x_0', y_0')$ was derived in [33] while $v_{a_2}(x_0', y_0')$ is obtained as the potential in the area near the conduction plane that has the potential of $V_{gs}^* = -3$ V referring to the source point $D(x_{DW}, 1)$ (see Fig. 11). Using the expression from [33] for $v_{a_1}(x_0', y_0')$, the potential $v_a^I(x_0', y_0')$ becomes

$$v_a^I(x_0', y_0') = \int_0^{+\infty} \frac{qn_{S0}'(x')}{2\pi\varepsilon_a} \ln\left(\frac{(x' - x_0')^2 + (1 + y_0')^2}{(x' - x_0')^2 + (1 - y_0')^2}\right) dx'$$
$$+ V_{gs}^*(1 - y_0'). \quad (20)$$

In order to obtain the relation $b^I(V_{ds})$, it is necessary to calculate (20) in the point $B(x_B', y_B')$ that corresponds to the mapped point of drain electrode. In w-plane, the point B has the coordinates: $x_B' = 0$ and $y_B' = a\cosh((3 - c^I)/(1 + c))/\pi$, where $c^I = \cosh(\pi b(V_{ds})/d_{AlGaN})$. Replacing x_B' and y_B' into (20), the parameter c^I and therefore b^I could be obtained as a function of V_{ds}. However, the parameter c^I is in the integral part of the (20) which makes it difficult for direct extraction. Therefore, the (20) was calculated for different values of c^I and this relation is shown in the lower part of the curve in Fig. 12. The wanted dependence $c^I(V_{ds})$ is finally obtained by reading the values of c^I for a particular value of V_{ds} (see Fig. 12).

In order to obtain the $b^{II}(V_{ds})$ which corresponds to the lateral extension of the depletion area around the field-plate edge, the physical model from Fig. 13 will be used. Comparing to the methodology used for obtaining $b^I(V_{ds})$, the main
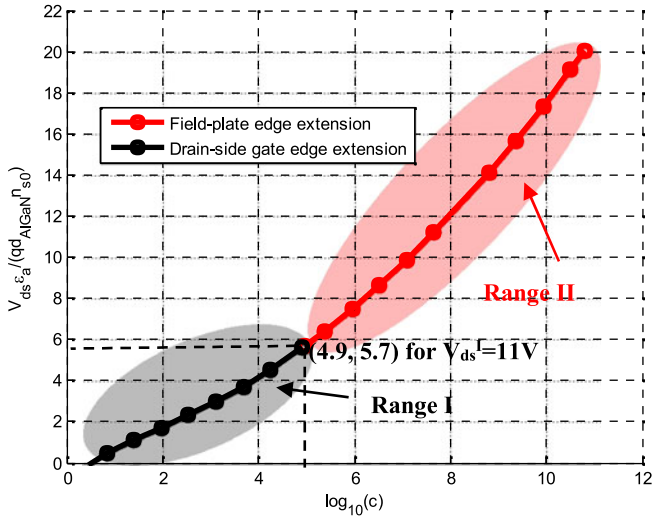
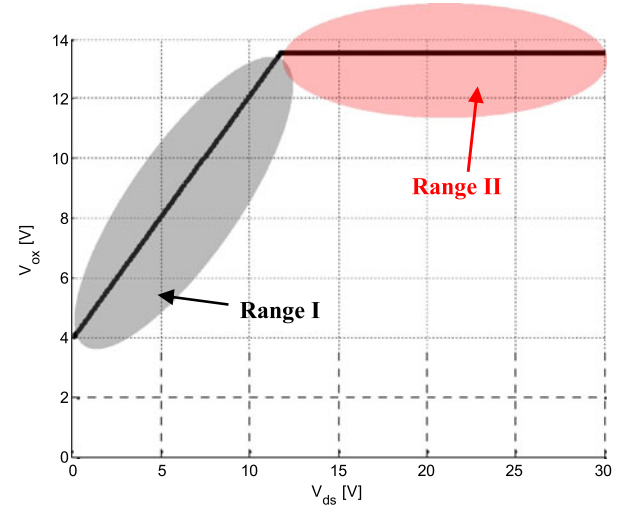Fig. 12. Obtained relation between the lateral extension around the gate edge/field plate edge and applied V_{ds}.

Fig. 13. Applied physical model for the extension of the depletion area around the field-plate edge.

Fig. 14. Oxide voltage drop dependence on the applied V_{ds}.

Fig. 15. Analytical model for the Miller's capacitance versus measurements.
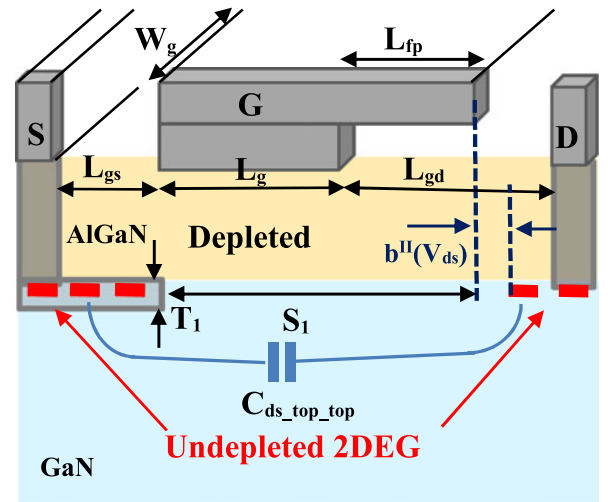
Fig. 16. Physical origin of C_{ds} capacitance.

difference is the presence of the oxide with the voltage drop V_{ox}. From the model for the vertical depletion under the field plate, the $V_{ox}(V_{ds})$ dependence is obtained (see Fig. 14). Observing this dependence, it can be seen that before vertical depletion is completed, the voltage drop inside the oxide will depend on the applied V_{ds} and the image charge method used for obtaining $b^{II}(V_{ds})$ would have different potentials of the conduction plane. But, since the lateral extension of the depletion area around the field-plate edge exists only for $V_{ds} > 11$ V, the V_{ox} used in the calculation of $b^{II}(V_{ds})$ will have a constant value of 13.5 V. Therefore, the potential $v_a^{II}(x_0', y_0')$ is equal to

$$v_a^{II}(x_0', y_0') = \int_0^{+\infty} \frac{q n_{S0}'(x')}{2\pi\varepsilon_a} \ln\left(\frac{(x'-x_0')^2 + (1+y_0')^2}{(x'-x_0')^2 + (1-y_0')^2}\right) dx'$$
$$+ \left(V_{gs}^* - V_{ox}\right)\left(1 - y_0'\right). \qquad (21)$$

Fig. 12 shows $b^I(V_{ds})$ and $b^{II}(V_{ds})$ in the complete range of drain-to-source voltages, calculated by previously presented methodology. Substituting the obtained $b^I(V_{ds})$ and $b^{II}(V_{ds})$ in (15), the $C_{gd,x}^{I/II}(V_{ds})$ is obtained.
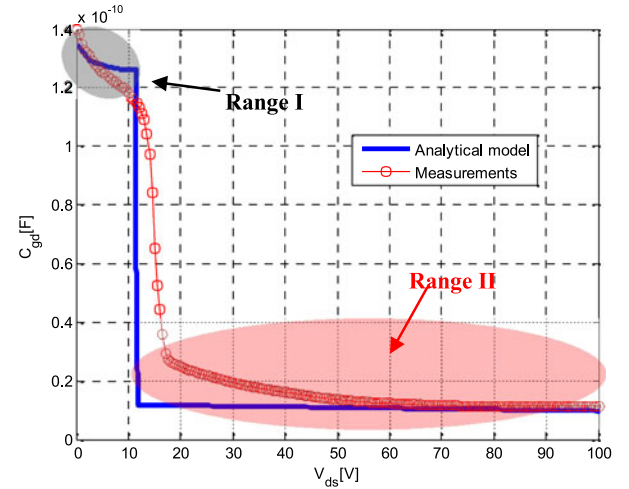
Fig. 17. Top view of the multifinger layout of the device.

Fig. 18. Analytical model for C_{oss} and C_{ds} together with the measured C_{oss}.

In order to complete the model for Miller's capacitance, it is necessary to model the fringing capacitance between the pads that connect all gate and drain fingers in the multifinger layout, $C_{\mathrm{gd\_pad}}$ (see Fig. 17). This capacitance can be obtained applying the model from [34] that calculates the fringing between top surfaces of two sufficiently long metal lines. Using the values of geometrical parameters obtained from the Nomarski microscope photo shown in Fig. 17, the obtained value for $C_{\mathrm{gd\_pad}}$ is 9 pF. Finally, the complete model for Miller's capacitance can be presented as

$$C_{\mathrm{gd}}(V_{\mathrm{ds}}) = \begin{cases} C_{\mathrm{gd},y}^{I} + C_{\mathrm{gd},x}^{I}(V_{\mathrm{ds}}) + C_{\mathrm{gd,pad}}, & V_{\mathrm{ds}} \leq V_{\mathrm{ds}}^{I} \\ C_{\mathrm{gd},x}^{II}(V_{\mathrm{ds}}) + C_{\mathrm{gd,pad}}, & V_{\mathrm{ds}} > V_{\mathrm{ds}}^{I} \end{cases} \tag{22}$$

and is shown in Fig. 15, together with experimentally obtained $C_{\mathrm{gd}}(V_{\mathrm{ds}})$ curve for $V_{\mathrm{gs}} = -3$ V.

In the case of $V_{\mathrm{ds}} = 40$ V switching application, the modeled and the measured value of gate-to-drain charge can be obtained as the area under each of the curves from Fig. 15 and are equal to 2.0185 and 2.3675 nC, respectively. This gives 14.7% of the deviation between the modeled and the measured value of gate-to-drain charge. As it will be shown in Section V, this discrepancy gives maximum deviation of 3% in the efficiency estimation of a HF buck converter at 7 MHz of switching frequency, which is acceptable from the application point of view.

III. DRAIN-TO-SOURCE CAPACITANCE MODELING

Since the output capacitance of the device C_{oss} is equal to the sum of Miller's C_{gd} and drain-to-source capacitance C_{ds}, this section will analytically model the capacitance between the drain and source electrodes.

Drain-to-source capacitance contains different fringing capacitances between drain and source electrodes, among which the biggest one is caused by fringing between the undepleted 2DEG in gate–source and gate–drain drift regions (see Fig. 16). These undepleted areas present the extensions of drain and source electrodes. The spacing between them is equal to the gate length for $V_{\mathrm{ds}} \leq V_{\mathrm{ds}}^{I}$ or to the sum of the gate length and the length of the field plate for $V_{\mathrm{ds}} > V_{\mathrm{ds}}^{I}$. As V_{ds} changes, the length of the drift area that contains the 2DEG will be decreased for $b^{I/II}(V_{\mathrm{ds}})$ as it was shown in the previous section. Using
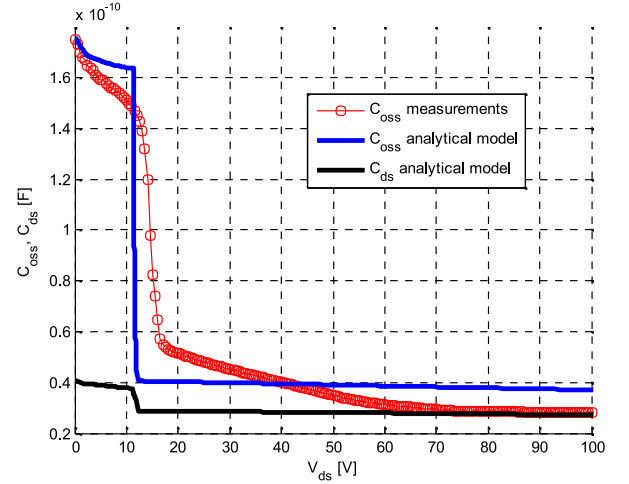
the analytical model from [34] for fringing capacitance between the top of the undepleted 2DEG in the gate–source region and the top of the undepleted 2DEG in the gate–drain region, it is obtained

$$C_{\mathrm{ds\_top\_top}}(V_{\mathrm{ds}}) = \varepsilon_g \frac{L_{\mathrm{gs}} \ln\left(1 + \frac{2L_{\mathrm{gs}}}{S_1}\right)}{\left(L_{\mathrm{gs}}\pi + (H_1 + T_1)\ln\left(1 + \frac{2L_{\mathrm{gs}}}{S_1}\right)\right)} \tag{23}$$

where $H_1 = 0$ (the height difference between the electrodes), $T_1 = 2$ nm (the approximation of the 2DEG height) while S_1 is equal to

$$S_1 = \begin{cases} L_g + b^{I}(V_{\mathrm{ds}}), & V_{\mathrm{ds}} \leq V_{\mathrm{ds}}^{I} \\ L_g + L_{\mathrm{fp}} + b^{II}(V_{\mathrm{ds}}), & V_{\mathrm{ds}} > V_{\mathrm{ds}}^{I} \end{cases}. \tag{24}$$

Similarly to the model for Miller's capacitance, the nonnegligible fringing capacitance exists between the pads that connect all drain and source fingers (see Fig. 17). This capacitance $C_{\mathrm{ds\_pad}}$ can be calculated using (23) with the values of the geometrical parameters determined from the microscope photo of the multifinger layout. For this multifinger layout, it is equal to 7.7 pF.

Finally, the $C_{\mathrm{ds}}(V_{\mathrm{ds}}) = C_{\mathrm{ds\_top\_top}}(V_{\mathrm{ds}}) + C_{\mathrm{ds\_pad}}$ is shown in Fig. 18. Using previously obtained model for $C_{\mathrm{gd}}(V_{\mathrm{ds}})$, the output capacitance of the device $C_{\mathrm{oss}}(V_{\mathrm{ds}})$ is obtained as $C_{\mathrm{oss}}(V_{\mathrm{ds}}) = C_{\mathrm{ds}}(V_{\mathrm{ds}}) + C_{\mathrm{gd}}(V_{\mathrm{ds}})$. The obtained model for $C_{\mathrm{oss}}(V_{\mathrm{ds}})$ versus measurements is also shown in Fig. 18.

IV. GATE-TO-SOURCE CAPACITANCE MODELING

Gate-to-source capacitance also needs to be analytically modeled in order to obtain the complete model for input capacitance of the device. This capacitance consists of different fringing capacitances which do not depend on V_{ds}, since the 2DEG concentration in the source drift area does not change with drain-to-source voltage (see Fig. 3 and 4). In order to distinguish different parts of C_{gs}, the cross section of the device shown in Fig. 19 will be observed.
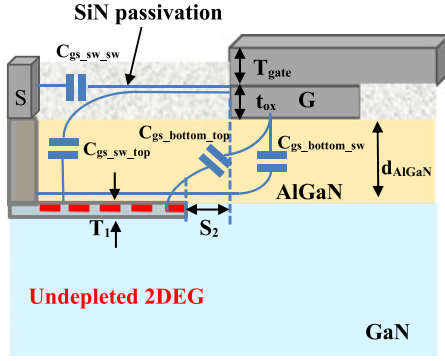
Fig. 19. Physical origin of C_{gs} capacitance.

Fig. 20. Fringing between gate and source finger-connecting pads.

The model that will be used for each of these capacitances is presented in [34]. As it can be seen in Fig. 19, the fringing capacitance between the bottom of the gate electrode and the top of the undepleted 2DEG in the source drift region is marked as $C_{\mathrm{gs\_bottom\_top}}$, and can be calculated as

$$C_{\mathrm{gs\_bottom\_top}} = \varepsilon_a L_g \frac{\ln\left(1 + \frac{2L_g}{S_2}\right)}{\left(L_g\pi + (d_{\mathrm{AlGaN}} + T_1)\ln\left(1 + \frac{2L_g}{S_2}\right)\right)}. \quad (25)$$

In (25), T_1 is the height of the 2DEG (estimated to 2 nm) while S_2 is the lateral distance between the 2DEG layer and the gate electrode. Theoretically, this distance is zero but in order to apply (25), the value of $S_2 = 2$ nm was used. Using the values from Table II, the value $C_{\mathrm{gs\_bottom\_top}} = 184.7$ pF is obtained.

The capacitance between the sidewall of the gate electrode and the top of the undepleted 2DEG is marked as $C_{\mathrm{gs\_sw\_top}}$ and also can be calculated applying the model from [34]. Since the gate electrode is passivated using SiN, the lines of the fringing field are contained in SiN and AlGaN layers. However, since the total height of the gate electrode is $T_{\mathrm{gate}} + t_{\mathrm{ox}} = 180$ nm while the thickness of AlGaN layer is only 24 nm, the $\varepsilon_{\mathrm{ox}}$ will be used in the model of this capacitance. Additionally, the dielectric constant of SiN is only 1.34 times higher than the constant of AlGaN so the expected error of not taking into consideration two materials in the fringing area is quite small. In this way, the analysis of this fringing capacitance is not additionally complicated and the model from [34] can be directly applied

$$C_{\mathrm{gs\_sw\_top}} = \frac{2}{\pi}\varepsilon_{\mathrm{ox}} \ln \left(\begin{array}{c} \frac{d_{\mathrm{AlGaN}} + T_{\mathrm{tot}}}{S_2 + d_{\mathrm{AlGaN}}} \\ + \frac{\sqrt{S_2^2 + T_{\mathrm{tot}}^2 + 2d_{\mathrm{AlGaN}}T_{\mathrm{tot}}}}{S_2 + d_{\mathrm{AlGaN}}} \end{array} \right) \quad (26)$$

where $T_{\mathrm{tot}} = T_{\mathrm{gate}} + t_{\mathrm{ox}}$. Calculation of (26) gives $C_{\mathrm{gs\_sw\_top}} = 107$ pF.

The third part of gate-to-source capacitance that presents the fringing through AlGaN layer between the bottom of the gate electrode and the sidewall of the source, $C_{\mathrm{gs\_bottom\_sw}}$ (see Fig. 19) can be calculated similarly to $C_{\mathrm{gs\_sw\_top}}$, using different
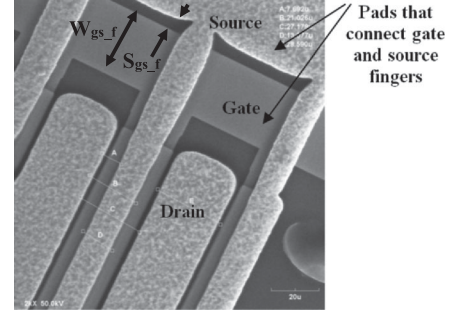
values that correspond to this geometry

$$C_{\mathrm{gs\_bottom\_sw}} = \frac{2}{\pi}\varepsilon_a \ln \left(\frac{d_{\mathrm{AlGaN}} + \sqrt{L_{\mathrm{gs}}^2 + d_{\mathrm{AlGaN}}^2}}{L_{\mathrm{gs}}} \right). \quad (27)$$

Calculating (27), it is obtained that this capacitance is quite small, $C_{\mathrm{gs\_bottom\_sw}} = 0.6$ pF.

The fourth part of C_{gs} is the plate capacitance between the sidewall of the source and the sidewall of the gate electrode, $C_{\mathrm{gs\_sw\_sw}}$, which can be calculated as $C_{\mathrm{gs\_sw\_sw}} = \varepsilon_{\mathrm{ox}}^* W_g^* (T_{\mathrm{gate}} + t_{\mathrm{ox}})/L_{\mathrm{gs}}$. The obtained value 0.7 pF is negligible. This capacitance exists between gate and drain electrodes as well, but has the order of 10^{-13} and was completely neglected.

Finally, as it was shown in the calculation of C_{ds}, the multi-finger layout of the device causes additional capacitance due to fringing between the areas that connect all the fingers. In this multifinger configuration, the areas that connect all gate and source fingers are placed quite close to each other, causing a significant portion of C_{gs} (see Fig. 20). Using the parameters marked on Fig. 20 this capacitance can be calculated as

$$C_{\mathrm{gs\_multifinger}} = \varepsilon_a W_{\mathrm{gs\_f}} \ln\left(1 + \frac{2W_{\mathrm{gs\_f}}}{S_{\mathrm{gs\_f}}}\right)$$
$$\bullet \frac{1}{W_{\mathrm{gs\_f}}\pi + (H_{\mathrm{gs\_f}} + T_{\mathrm{gs\_f}})\ln\left(1 + \frac{2W_{\mathrm{gs\_f}}}{S_{\mathrm{gs\_f}}}\right)} \quad (28)$$

where $T_{\mathrm{gs\_finger}}$ is the height of the pad that connects gate/source fingers and is approximated to the value of T_{gate} while $H_{\mathrm{gs\_finger}}$ is the height difference between these pads and is equal to zero. Using the values for W_{gs_f} and S_{gs_f} from Fig. 20, (28) gives $C_{\mathrm{gs\_multifinger}} = 69.2$ pF.

The sum of previously obtained capacitances gives the total gate–source capacitance equal to 362.2 pF. The complete analytical model for $C_{\mathrm{iss}}(V_{\mathrm{ds}}) = C_{\mathrm{gd}}(V_{\mathrm{ds}}) + C_{\mathrm{gs}}$ versus measurements is shown in Fig. 21.

V. EXPERIMENTAL VERIFICATION OF THE PROPOSED CAPACITANCE MODEL

The main advantage of the proposed modeling technique over physics-based models implemented in FEA tools is that it can be effectively utilized in algorithms that optimize the device design for a particular application (see Fig. 1). In order to verify
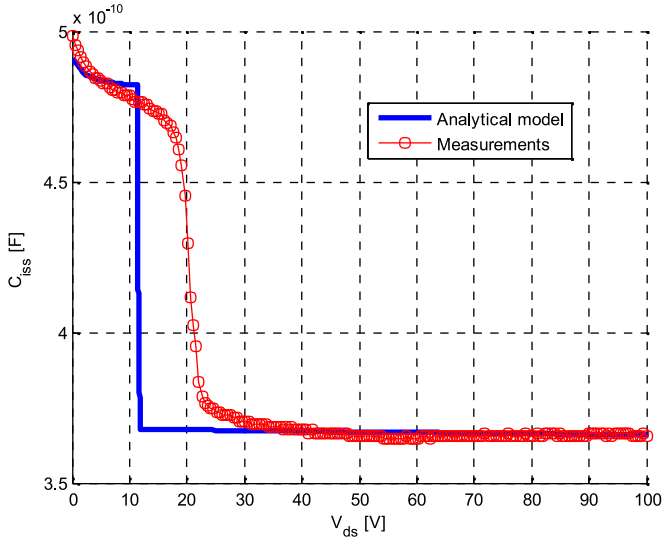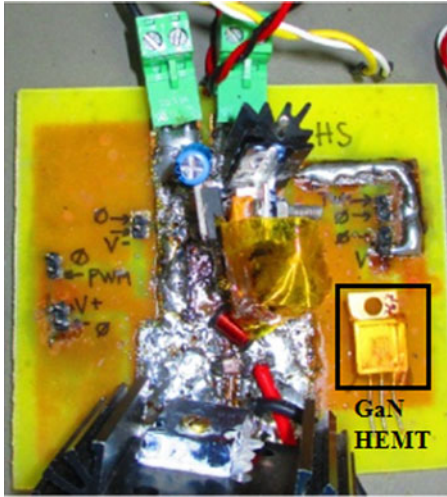
Fig. 21. Analytical model versus measurements for C_{iss}.

Fig. 23. Measured and simulated waveform at the input of the filter at switching frequency of 22 MHz.

Fig. 22. Implemented prototype of a high-frequency buck converter.

Fig. 24. Measured and simulated efficiency curves.

The converter operates in open loop. The specifications of the converter are the following:

1) input voltage: 24 V;
2) the load resistance: 6 Ω;
3) switching frequency is set to 7, 15, and 20 MHz.
   The implemented prototype is shown in Fig. 22 [17].

The measurements of the overall efficiency of the converter (including the driving losses), were done at 7, 15, and 20 MHz of switching frequency, keeping the same load resistance and changing the duty cycle in order to provide different output power levels (see Fig. 24). The measurements were performed in this manner since the envelope amplifier tracks the RF reference by the modulation of the duty cycle, while the load resistance is being constant.

In order to simulate the overall efficiency of a HF buck converter and compare it to the experimentally obtained curves, the hybrid analytical-behavioral power loss model from [39] was implemented into Simplorer simulation tool. This power loss model used previously obtained analytical curves for C_{iss}, C_{oss}, and C_{gd} dependence on V_{ds} as the description of the capacitive part of the device, while the model from [35] was used

the proposed methodology for such usage, HF buck converter is built and the overall efficiency of the converter is experimentally measured and simulated. The efficiency simulations incorporated the proposed capacitance model into the power loss model of the converter.

The implemented prototype of a HF buck converter uses the modeled GaN HEMT as the main switch while STPS20L25CT diode from ST microelectronics is used as the freewheeling diode. The RF inductor 144-02J12L from Coilcraft is used as the output inductor. The driving circuit consists of EL7155 commercially available driver from Intersil together with ISO721 isolation chip. The isolation chip receives the signal generated in Spartan 3 FPGA board. Since the analyzed switch has the threshold voltage of -2 V, the gate signal levels are set to -5 V for the OFF state and 0 V for the ON state of the device.
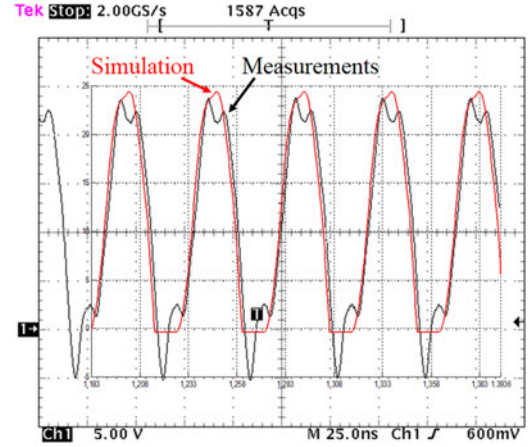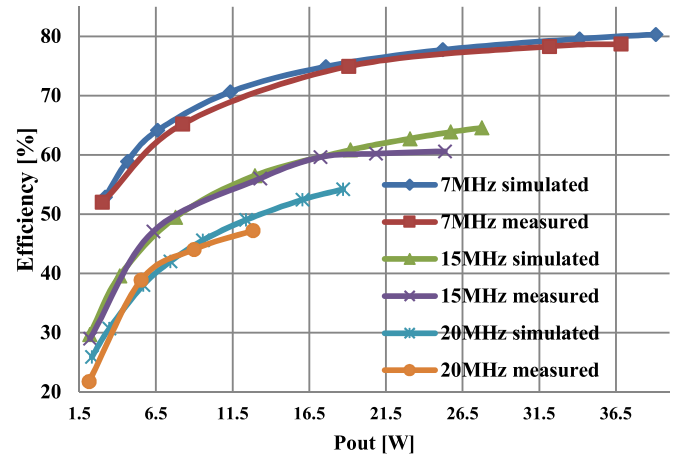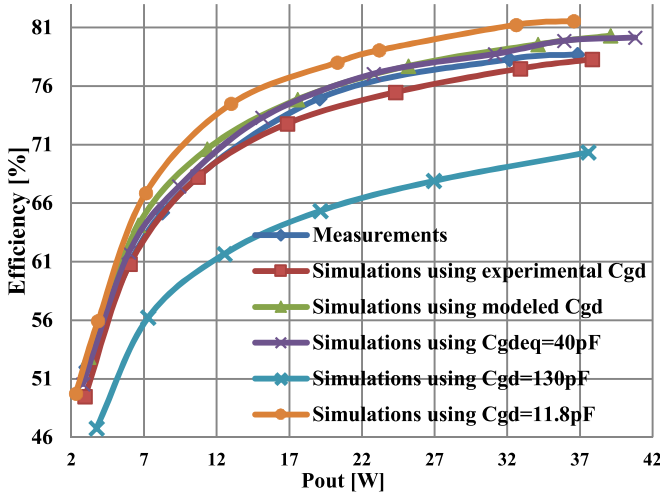
Fig. 25. Measured and simulated efficiency curves at 7 MHz of switching frequency.

for the description of forward transconductance dependence on gate–source voltage. The estimated values for drain, gate, and source parasitic inductances of TO-220 package are 1, 1, and 6 nH [38] while the additional parasitic inductance of the HF loop due to printed circuit board (PCB) layout is estimated to 5 nH. These values of parasitic inductances were implemented into the power loss model from [39].

Observing the comparison between the measured and simulated waveform of the input voltage of the filter (see Fig. 23), it can be seen that good agreement exists even at 22 MHz of switching frequency. The comparison between the simulated and measured efficiency curves showed good agreement at each switching frequency. Good agreement is obtained even at 20 MHz in the low range of the output power, verifying the power loss model together with the proposed physics-based model.

In order to examine the precision of the proposed physics-based model for Miller's capacitance, the additional simulations were made. These simulations employed the same power loss model, incorporating analytically and experimentally obtained $C_{gd}(V_{ds})$ from Fig 15. Furthermore, these results are compared to the simulated efficiencies obtained when a constant value for C_{gd} is used. The values that are used for this purpose are $C_{gd} = 130$ pF (which corresponds to the C_{gd} value in the Range I of V_{ds}), $C_{gd} = 11.8$ pF (which corresponds to the C_{gd} value in the Range II of V_{ds}), and finally $C_{gd} = C_{gd,eq} = 40$ pF which is the value obtained from the approximate calculation of the energy in the capacitor

$$E_{Cgd} = \frac{1}{2} C_{gd,eq} V_{max}^2. \tag{29}$$

In (29), $V_{max} = 24$ V, while E_{Cgd} was obtained as

$$E_{Cgd} = \int_0^{V_{max}} C_{gd}(V_{ds}) V_{ds} dV_{ds} \tag{30}$$

using the modeled characteristic for $C_{gd}(V_{ds})$. The comparison between the obtained efficiency curves for switching frequency

of 7 MHz is shown in Fig. 25. It can be seen that very good agreement exists between the curves that were obtained using modeled and experimental $C_{gd}(V_{ds})$ with the highest discrepancy of 3% for the output power lower than 7 W. Additionally, these curves show very good agreement with the simulations that used $C_{gd,eq}$ as well as with the measured efficiency curves. On the other hand, simulations that used constant C_{gd} equal to the value in the Range I or II of V_{ds}, showed significantly higher discrepancies: 10% in the case of $C_{gd} = 130$ pF and 5% in the case of $C_{gd} = 11.8$ pF. Therefore, the proposed nonlinear model for $C_{gd}(V_{ds})$ is necessary for precise losses estimation in a HF buck converter.

VI. CONCLUSION

Fully analytical physics-based model for the OFF state capacitances of a GaN HEMT with the field-plate structure is proposed in this paper, showing the physical origin of nonlinearity in each of these capacitances.

In order to avoid FEA tools for solving 2-D Poisson's equation, the proposed methodology analytically modeled Miller's capacitance using the approximation of the charge depletion in two separated directions: vertically and laterally with respect to the channel. Vertical depletion is modeled by determination of the 2DEG density control by gate-to-drain voltage for the metal—insulator–semiconductor AlGaN/GaN structure. The lateral extension of the depletion area in the channel is modeled using conformal mapping technique, applying the necessary modifications for the extension around the field-plate edge. Comparing to the measured value, the analytical model showed deviation of 14.7% in the value of gate-to-drain charge. The simulations of a HF buck converter that employed modeled GaN HEMT as the main switch showed that this deviation causes maximum discrepancy of 3% in the overall efficiency estimation at 7 MHz of switching frequency, which is acceptable from the application point of view. This discrepancy is significantly lower than the one obtained when constant values for C_{gd} are used, emphasizing the importance of nonlinear $C_{gd}(V_{ds})$ model for the precise loss estimation.

Furthermore, the drain–source and gate–source capacitances were modeled in order to complete the model for input and output capacitance of the device. These capacitances are dominantly caused by fringing between the corresponding electrodes and their extensions through the source and drain drift areas. Additionally, it was shown that fringing between the finger-connecting pads in the multifinger layout causes a considerable portion of these capacitances, especially in the case of gate–source capacitance. While drain–source capacitance slightly depends on the applied drain–source voltage (because of the extension of the drain electrode through the area under the field plate where vertical depletion takes place), the gate–source capacitance is constant in the whole range of V_{ds}. Therefore, the presented analysis showed that the field-plate design dominantly influences Miller's capacitance. Since the design of the field plate determines the breakdown voltage of the device, the obtained analytical model for C_{gd} can be used for obtaining the

device design with minimum gate-to-drain charge for a given breakdown voltage.

Finally, the proposed capacitance model was implemented into the power loss model of a HF buck converter using Simplorer as a simulation tool. The simulated efficiency curves at 7, 15, and 20 MHz of switching frequency showed very good agreement with the measurements on the implemented prototype, verifying the power loss model together with the accuracy of the proposed physics-based model. Since the complexity level of the proposed capacitance model is quite low, it can be effectively incorporated into algorithms that optimize the design of this type of switching devices for a particular HF application.

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