Matlab/simulink modeling of SIC power mosfets

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Matlab/Simulink Modeling of SiC Power MOSFETs

Paolo Giammatteo, Concettina Buccella, Carlo Cecati

Abstract – *Simulation and rapid prototyping of power converters requires accurate models of all passive and active elements, which take into account most important physical parameters and not only electrical quantities. Their availability is fundamental to verify the expected behaviour of the complete system including its control algorithm without building any prototype. For this reason, due to the wide use of Simulink® in simulation of complex systems, this paper attempts to study the main characteristics of a typical Silicon Carbide (SiC) power MOSFETs and proposes its Simulink® model. The static and dynamic characteristics of the device are described by voltage and current sources which behaviour depend on temperature values. Switching power losses are considered by introducing parasitic capacitances in its equivalent circuit, thus obtaining a dynamic characteristic of the device. The proposed model has been validated using a typical 4H-SiC MOSFET (1200V, 20A) in an illustrative example consisting of a 5-level cascaded inverter.*

Keywords: *Silicon Carbide, Device Characterization, Device Modeling, Device Simulation, MOSFET, Loss, Power Converter*

Nomenclature

α	The slope of the temperature variation of the gate threshold voltage [V°/C]
χ_{SiC}	Electron affinity of the SiC [J/mol]
λ	Channel modulation [V^{-1}]
μ	Electron mobility of SiC [m^2V/s]
μ_{it}	Interface traps mobility [m^2V/s]
μ_{ph}	Phonon scattering mobility [m^2V/s]
C_b	Bulk majority carrier concentration[m^{-3}]
C_{dq}	Parasitic gate to drain capacitance [F]
C_{gs}	Parasitic gate to source capacitance [F]
C_{iss}	Parasitic input capacitance [F]
C_{ox}	Oxide capacitance [F]
C_{rss}	Reverse Transfer Capacitance [F]
E_{eff}	The average transverse electric field in the MOSFET channel [V/m]
E_q	Band gap [J/C]
I_{dstd}	Drain current at standard temperature[A]
I_d	Drain current [A]
I_{load}	Full load darin-source current [A]
K	Transistor gain [A/V^2]
K_B	Boltzman constant [J/°C]
L	Channel length [m]
n_i	Intrinsic carrier concentrations [m^{-3}]
q	Carrier charge [C]
Q_b	Bulk charge [C]
Q_f	Fixed oxide charge [C]
Q_{it}	Interface traps charge [C]
R_q	Gate resistance [Ω]
T	Device Temperature [°C]
t	Time [s]
t_0	Time at which the gate signal rises up[s]
t_d	Time at which the gate signal drops down [s]
T_{std}	Device standard temperature [°C]
$V_{ds,load}$	Full load drain-source voltage [V]
$V_{ds,off}$	Device off drain-source voltage [V]
V_{ds}	Drain-source voltage [V]
V_{gs}	Gate-source voltage [V]
V_{pm}	Miller plateau voltage [V]
V_{th}	Threshold voltage [V]
W	Channel width [m]

I. Introduction

High power converters are widely used many fields including industry, transportation, oil&gas, lighting, home appliances, moreover, they are fundamental in full exploitation of distributed energy resources (DERs) and in their integration with the grid; they are also very important in ensuring high power factor and fulfilling power quality grid stability demands [1], [2], [3].

Modern systems have to be capable of handling active and reactive power demands, often to operate at high frequency and always to maintain both switching and conduction losses at lowest possible values. Fulfillment of previous requirements impose improvements in all parts including output power devices.

The emerging Silicon Carbide (SiC) and Gallium Nitrite (GaN) technologies [4], are attracting wide attention due to their new level of performance, in particular their ability to operate at high temperature, frequency and voltage [5], [6].

A synopsis of recent complementary technological developments in passives, integrated driver and protection circuitry and electronic packaging are described in [7]. Paper [8] presents the development and

experimental performance of a three-phase ac–dc–ac converter composed by SiC MOSFET, working at 250 °C junction temperature.The electromagnetic interference filter, thermal system, high temperature package, and gate drive design are discussed in detail.

Currently, SiC devices are considered excellent for power electronic applications in virtue of their extremely robust and stable behavior even at high frequency operations (above 20kHz), high voltage ratings (> 10kV) and high operating temperatures (> 100°C) [9], but until now their diffusion is quite limited, due to their high cost and the more complex driving circuit.

In particular they appear very promising in those applications where traditional silicon semiconductors are affected by severe limitations such as hybrid and full electric vehicles, energy storage devices, inverters for renewable energy and for industrial drives, power supplies, oil&gas industry and all those high power applications operating at high temperature or requiring high switching operations. As a consequence of better electrical/thermal performance, their use lead to significant reduction of electronic parts and of the heat-sink.

This characteristic represents a significant advantage in those applications where converter size is a critical issue, for instance in avionics or in automotive [10] too. Currently, a significant drawback is their cost, typically 5-10 times higher than a Si devices with similar v/i characteristics, but it is expected that it will be quickly reduced as technology will be improved and applications will grow [11].

There are many papers dealing with SiC devices: paper [5] presents an overview of the main available SiC devices introducing some guidelines for development of driver circuits suitable for some among the available SiC devices, [12] presents a 10kW high-power-density three-phase ac-dc-ac converter, employing SiC JFET and SiC Schottky diodes to reduce the switching losses and achieve a high operating junction temperature; paper [11] demonstrates that the application of a SiC converter in the wind generation system improves overall efficiency, provide more output power, and reduce size and cost due to the low-loss, high-frequency, and high-temperature properties of SiC devices.

Paper [13] proposes a physics-based model of a silicon carbide bipolar junction transistor, realized using MATLAB® and Simulink®, and presents verification of its validity through experimental testing. In paper [14] CREE CMF20120D SiC MOSFETs were considered and the results shown that both the two proposed gate assist circuits improve the switching performance under different operating conditions in comparison to the conventional gate drive. In paper [15] a MOSFET-based gate buffer implemented in a 2µm 4HSiC process has been presented. The paper demonstrates the potential for fully integrated SiC gate drivers and identifies and addresses some of the limiting factors presented to the SiC-integrated circuit designer.

From previous analysis follows that SiC MOSFET are becoming more and more diffused, and, due to their characteristics which are quite different from traditional silicon devices, researchers are addressing their attention to practical design issues.

On the other side, simulation of power converters is a common practice for avoiding problems in the realization of applications like the ones mentioned above, therefore, the aim of this paper is to present development, simulation, and validation of a complete Matlab/Simulink® model of a typical 4HSiC MOSFETs. In the following, the physical characteristics of the component are fully investigated and a complete Simulink® model is developed. In order to give practical meaning and validation to the obtained results, a commercially available device has been considered as tested, i.e. the 1200V – 20A SiC MOSFET, Cree CMF20120D [16].

This component is often used in converter designs based on SiC technology. In the best of authors' knowledge, while some papers report modeling of SiC devices using circuit simulation software, e.g. Spice [17], until now, no one has proposed accurate SiC models developed using Matlab/Simulink®. The relevance of the proposed model is that Simulink® is widely diffused in industry and academia to implement system-level simulations with full integration of complex converter topologies (e.g. multilevel or modular converters) employing numerous devices including SiC devices, control and modulation algorithms with circuital analysis.

Other available software tools are not so easy and powerful as Simulink®. While preserving previous characteristics the proposed Simulink® block is more accurate than other models such as [18]; in fact some parameters are extracted by a fitting procedure applied to the data sheet quantities. A validation of the model is done by comparing the I-V characteristic curves obtained by simulations with those provided by the manufacturer [16]. A very good agreement is observed in the used range of drain-source voltage values. It is worth notice that the same model can be adopted with other SiC MOSFETs. A 5-level cascaded inverter simulation using the proposed model is also considered as example of practical application of the proposed model and the simulated results are shown.

II. SiC vs. Si Properties

Silicon carbide has higher thermal conductivity, higher breakdown voltage, wider band-gap and an higher saturation velocity than the sole silicon [9], [19].

As discussed in previously cited papers, compared to Si components and for a given voltage, SiC devices with minority carriers show an increase by factor 100 in switching speed; those with majority carriers perform an improvement of 100 in strength.

For such a reason, many analysts expect that with the lowering of costs, SiC technology will spread in power electronics market. Table I summarizes and highlights the main electrical and physical properties of Si and SiC materials.

TABLE I
ELECTRICAL AND PHYSICAL PROPERTIES OF SI AND SIC

Property	Si	4H-SiC	6H-SiC	3C-SiC
Energy bandgap $E_g\ (eV)$	1,1	3,3	3	2,7
Critical field $E_c\left(\frac{MV}{cm}\right)$	0,3	3,5	2,5	1,5
Saturation velocity $v_{sat}\left(\frac{cm}{s}\right)$	1,00E+07	2,00E+07	2,00E+07	2,50E+07
Thermal conductivity $k\left(\frac{W}{cmK}\right)$	1,3	3,7	3,7	3,6

III. Mathematical Model

III.1. DC Static Characteristics

The N-channel SiC MOSFET modeling is complex due to the non-linear behavior of its drain current vs. drain-source voltage (I_d - V_{ds}) characteristic and the dependence on temperature of many electrical quantities.

The two most significant parameters, both strongly depending on temperature, are: the threshold voltage V_{th} and the electron mobility μ [20], respectively. The threshold voltage V_{th} can be expressed as follows [21]:

$$V_{th} = V_{fb} + V_{it} + \Psi_{Sinv} - \frac{Q_b}{C_{ox}} \tag{1}$$

where:

$$V_{fb} = \phi_m - \phi_{SiC} - \frac{Q_f + Q_{it}}{C_{ox}}$$

is the flat band voltage, V_{it} is the SiC/SiO_2 interface-trap voltage, $\Psi_{Sinv} = 2|\phi_B| + 6\phi_T$ is the inversion surface potential. The terms φ_m, $\phi_{SiC} = \chi_{SiC} + \frac{E_g}{2} + \frac{K_B T}{q} ln\left(\frac{C_B}{n_i}\right)$, φ_B and $\phi_T = \frac{K_B T}{q}$ represent the work function of the metal contact before the gate-oxide, the work function of the SiC, the Fermi potential in the bulk and the thermal voltage, respectively. It is worth notice that equation (1) contains a linear temperature dependence. In fact, both the terms Ψ_{Sinv} and φ_{SiC}, linearly depend on temperature.

For electron mobility, surface roughness and the high interface state density play important roles in the inversion layer.

Experimental values of mobility in the inversion layer reported in [22] show that for each operating regions of the device (subthreshold, linear and saturation) carrier mobility increases in the working temperature range [300–500] °K [23]. This behavior is due to the decrease of the occupied trap charges density with the rising temperature. The consequence is that, more electrons in the channel are available at a given gate voltage, hence, when the temperature increases, a movement of *Fermi level* toward the band gap can be observed. At temperatures higher than 500 °K, the mobility decreases since lattice scattering dominates and begins to release the interface trap charges. A detailed study about the dependence of 4H-SiC MOSFET mobility on the temperature is reported in [23].

According to previous considerations, the main mechanisms affecting carrier mobility of SiC MOSFET inversion layer are the phonon and interface traps scattering. The mobility can be expressed through the Mathiessen's rule [24]:

$$\mu(T, E_{eff}) \propto \left(\frac{1}{\mu_{ph}(T, E_{eff})} + \frac{1}{\mu_{it}(T, E_{eff})}\right)^{-1} \tag{2}$$

The phonon scattering mobility μ_{ph} depends on the temperature through the following expression:

$$\mu_{ph} \propto T^{-1.5} \tag{3}$$

For the interface traps, it is possible to consider a quite similar behavior, i.e.:

$$\mu_{it} \propto T^{\beta} \tag{4}$$

where β is a fitting coefficient induced by interface traps in SiC power MOSFET, carried out by the experimental data [25]. The SiC core MOSFET drain current vs. drain-source voltage (I_d - V_{ds}) characteristics are described by the following equations [18]:

$$I_d = 0 \quad \text{if } V_{gs} < V_{th} \tag{5}$$

$$I_d = K\left[(V_{gs} - V_{th})V_{ds} - \frac{(1+a)V_{ds}^2}{2}\right](1 + \lambda V_{ds}) \quad \text{if } 0 < V_{ds} < \frac{(V_{gs} - V_{th})}{(1+a)} \tag{6}$$

$$I_d = \frac{K}{2(1+a)}(1 + \lambda V_{ds})(V_{gs} - V_{th})^2 \quad \text{if } 0 < \frac{(V_{gs} - V_{th})}{(1+a)} < V_{ds} \tag{7}$$

In order to develop a more accurate model, the parameter a in the SiC MOSFET model is introduced, which takes into account the growth of the depletion layer and depends on the intrinsic structure of the SiC material and its properties. The linear temperature dependence of the threshold voltage V_{th} is expressed by the ideal voltage generator Etemp:

$$ETemp = [(T - T_{std})\alpha] \tag{8}$$

where T_{std} is the standard temperature of the device, which is 25°C. The parameter α can be obtained from the manufacturer datasheet values as [16]:

$$\alpha = \left(\frac{V_{th2} - V_{th1}}{T_2 - T_1}\right) = \left(\frac{1.8V - 2.5V}{125°C - 25°C}\right) = -0.007\frac{V}{°C} \tag{9}$$

where V_{th2} and V_{th1} are the threshold voltages evaluated at T_2 and T_1, respectively. The coefficient α represents the slope of the temperature variation of the threshold vol-

tage. The transistor gain K is related to the electron mobility μ through the following equation [20]:

$$K = \mu C_{ox} \frac{W}{2L} \tag{10}$$

The mobility is directly proportional to the drain current I_d and to the transconductance $g_m = \frac{\partial I_d}{\partial V_{gs}}$ as shown in Eqs. (6) and (7). According to Eqs (2), (3) and (4), an ideal current generator FTemp can be introduced and its value can be expressed as:

$$FTemp = I_{dstd}\left[\left(\frac{T}{T_{std}}\right)^{\beta} - \left(\frac{T}{T_{std}}\right)^{-1.5}\right] \tag{11}$$

In the previous equation, the first term represents the interface traps scattering, while the second one is the phonon scattering. The parameters in all previous equations model parameters are deduced from the manufacturer datasheet values, except the two parameters a (equations (5), (6) and (7)) and β (equation (11)), which are determined with a least square fit procedure, making a regression using the device curves given by the manufacturer. The mathematical model of the N-channel SiC MOSFET, just described, suggests the equivalent circuit model represented in Fig. 1 [18]. Infact, both the voltage (8) and current (11) generators add their contribution in opposition to the gate voltage, for the first one, and in the same direction to the drain-source current, for the second one, respectively.

III.2. Dynamic Characteristics

In order to evaluate the SiC MOSFET energy loss during the switching transient, the dynamic SiC MOSFET circuit model shown in Fig. 2 is considered, by introducing the parasitic capacitances [25]:

$$C_{gs}(V_{ds}) = C_{iss}(V_{ds}) - C_{dg}(V_{ds}) \text{ and}$$
$$C_{dg}(V_{ds}) = C_{rss}(V_{ds})$$

As it can be deduced from device datasheet, both capacitances present non-linear behavior in respect of the voltage V_{ds} [16].

The capacitance C_{iss} is assumed to be constant according to [16]. On the other hand, for the capacitance C_{dg}, and so for C_{rss}, an average value $C_{dg,ave}$ is considered as reported in [26], because of its strong dependence by V_{ds} [16]. The turn-on transient is developed through three time intervals [27]. The first interval is called subthreshold interval has duration t_1 - t_0, where t_0 is the gate signal rise time:

$$t_1 = R_g[C_{gs} + C_{dg}(V_{ds,off})]log\left(\frac{V_{gs}}{V_{gs} - V_{th}}\right) + t_0$$
$$V_{ds} = V_{ds,off} \tag{12}$$
$$I_d = 0$$

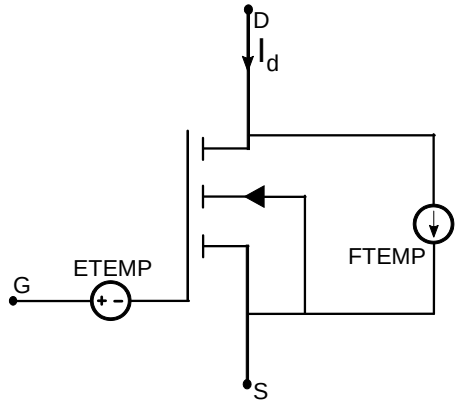


Fig. 1. SiC MOSFET equivalent circuit static models

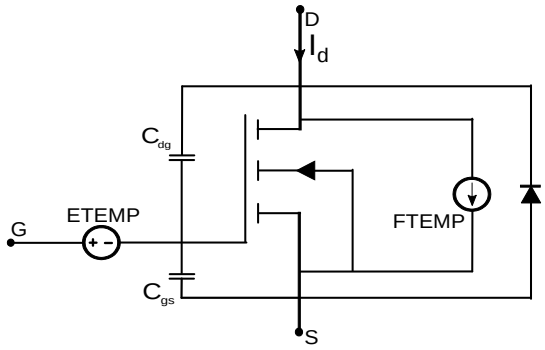


Fig. 2. SiC MOSFET equivalent circuit dynamic model

In this zone, the gate voltage is lower than the gate threshold voltage, hence the device remains off.

The second interval has duration t_2 - t_1. In this interval, the current begins to grow till it, at time t_2, reaches its full-load value (eq. (13)):

$$t_2 = R_g[C_{gs} + C_{dg}(V_{ds,off})]log\left(1 - \frac{V_{pm}}{V_{gs}}\right) + t_0$$
$$V_{ds} = V_{ds,off}$$
$$I_d = K\{V_{gs}\left[1 - exp\left(\frac{-(t - t_1)}{R_g\left(\frac{C_{gs} +}{+C_{dg}(V_{ds,off})}\right)}\right)\right] - V_{th}\}^2$$

The third interval of duration t_3 - t_2, is called Miller Plateau.

The drain-source voltage begins to fall down to its full load value reached at time t_3; in this interval the gate voltage assumes the constant value V_{pm}:

$$t_3 = R_g C_{dg,ave}\left(\frac{V_{ds,off} - V_{ds,load}}{V_{gs} - V_{pm}}\right) + t_2$$
$$V_{ds} = V_{ds,off} - t\frac{(V_{gs} - V_{pm})}{R_g C_{dg,ave}} \tag{14}$$
$$I_d = I_{load}.$$

After the time $t = t_3$, the device starts to conduct.

Also the turn-off transient is characterized by three time intervals. The first interval has duration t_4 - t_d, where t_d is the initial time, when the gate voltage signal drop down [27]. The gate voltage reaches the Miller Plateau value V_{pm} at the time t_4:

$$\begin{gathered} t_4 = R_g\left[C_{gs} + C_{dg}\left(V_{ds,load}\right)\right] log\left(\frac{V_{gs}}{V_{pm}}\right) + t_d \\ V_{ds} = V_{ds,load} \\ I_d = I_{load} \end{gathered} \tag{15}$$

The second interval has duration t_5 - t_4 and is called Miller Plateau. The drain-source voltage begins to rise up till its off value reached at time t_5:

$$\begin{gathered} t_5 = R_g C_{dg,ave}\left(\frac{V_{ds,off} - V_{ds,load}}{V_{pm}}\right) + t_4 \\ V_{ds} = V_{ds,load} - t\frac{V_{pm}}{R_g C_{dg,ave}} \\ I_d = I_{load} \end{gathered} \tag{16}$$

The third interval has duration t_6 - t_5. The drain current begins to drop down exponentially, until it reaches the zero value at the time t_6:

$$\begin{gathered} t_6 = R_g\left[C_{gs} + C_{dg}\left(V_{ds,off}\right)\right] \log\left(\frac{V_{pm}}{V_{th}}\right) + t_5 \\ V_{ds} = V_{ds,off} \\ I_d = K\left[V_{pm}\exp\left(\frac{-(t - t_5)}{R_g\left(\begin{matrix} C_{gs} + \\ +C_{dg}\left(V_{ds,off}\right) \end{matrix}\right)}\right) - V_{th}\right]^2 \end{gathered} \tag{17}$$

In this situation, the device is open and the conduction is stopped.

Through the Eqs. (12) - (17), it is possible to calculate the energy losses, according to the well-know relations [27]:

$$E_{turn-on} = \int_{t_0}^{t_3} V_{ds} I_d dt \tag{18}$$

$$E_{turn-off} = \int_{t_4}^{t_6} V_{ds} I_d dt \tag{19}$$

III.3. Simulink Model

Starting from previous analysis, this manuscript proposes a Matlab/Simulink® model of the CREE SiC MOSFET. It is worth notice that such a model can be easily adapted for describing a different family of SiC devices, just manipulating the parameters of the model equations. The model can be easily changed and so used to model different SiC MOSFET devices, giving the advantage to simulate a complex power system with different SiC MOSFET.

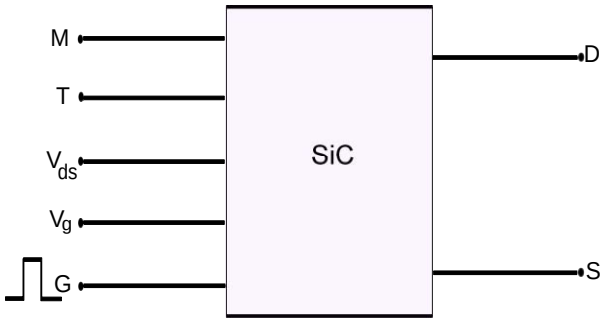


Fig. 3. SiC MOSFET Simulink block

As typical of Simulink®, the model is represented by a building block and is shown in Fig. 3. There are seven pins: Drain D, Source S, Gate G, Temperature *T* (i.e. the temperature value at which the device is working during the simulation), Drain-Source voltage V_{ds} (which is the voltage applied to the device), Gate voltage V_g (which is the gate input signal given to the device) and Mode M imposing the gate signal type (static or pulsed). As shown in Fig. 4, it is possible to identify three distinct parts:

- N-channel MOSFET, describing the core MOSFET with its body diode;
- ETemp block;
- FTemp block.

Each block implements the equations of the device described in Section III, inside the three Matlab® functions shown in corresponding figure.

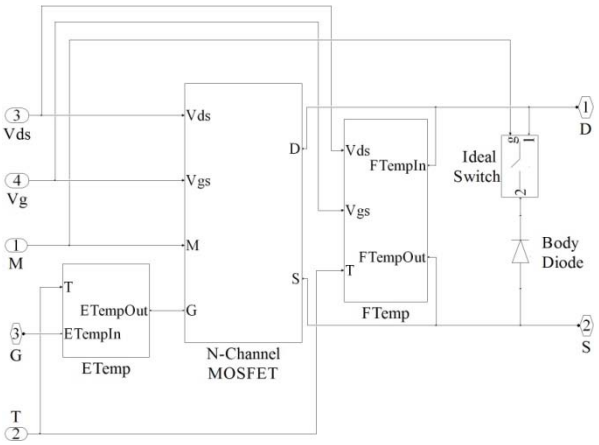


Fig. 4. Content inside SiC MOSFET Simulink block

These blocks exactly represent the static and dynamic SiC model in one solution, as in Figs. 1 and 2. According to the value assumed by M, it is possible to select which configuration has to be in use (static or pulsed) and decide which circuital elements have to be taken into account to execute the simulation. The development of these three sub-blocks are shown in Figs. 5, 6 and 7, respectively.

The Fig. 5 represents the ideal MOSFET core, without any temperature dependence, which is in charge of the main MOSFET behavior.

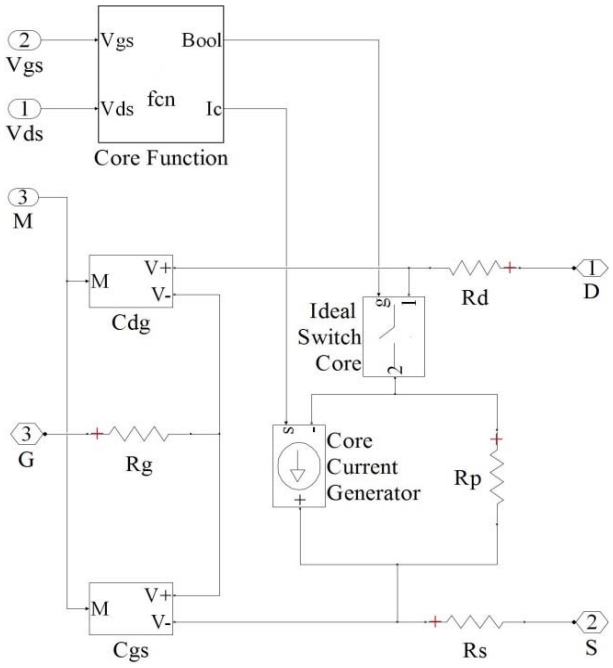


Fig. 5. The core block

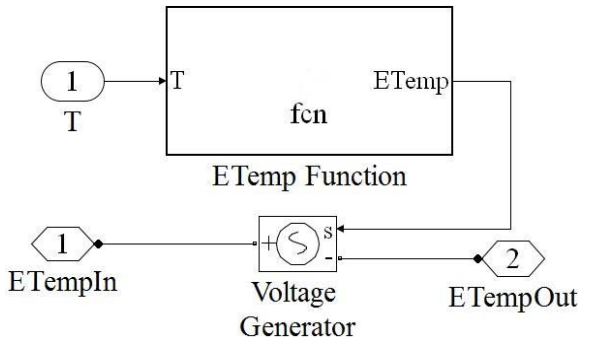


Fig. 6. The voltage generator Etemp

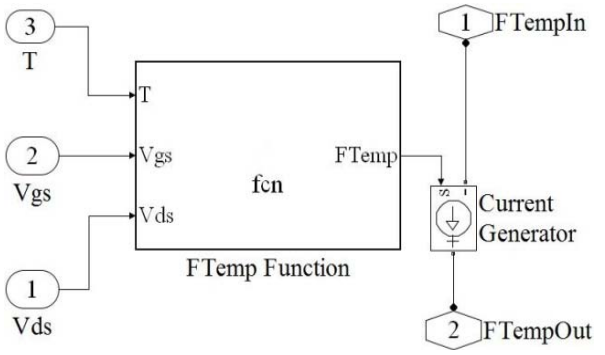


Fig. 7. The current generator Ftemp

The circuital design is developed in order to take into account all the aspect of the device, static and dynamic, and it is inspired to the MOSFET circuit shown in [18], with some little modification. Inside the Matlab Function there is the development of the equations which describe the MOSFET.

On the other hand, the Figs. 6 and 7 represent respectively the voltage and current generators. Each block consists of a generator which, according to the input values, impose respectively the correct output voltage and current to the generators, through the Eqs. (8) and (11) written inside the Matlab Function box.

III.4. Validation of the Proposed Model

The proposed Simulink/Matlab® model of the 4H-SiC MOSFET was validated comparing the I_d-V_{ds} characteristic curves obtained by simulations with those given by the manufacturer [16].

The validity intervals of the model for V_{gs} and T are [10] – [20] V and [25] – [125] °C, respectively. Figs. 8, 9 and 10 show the I_d - V_{ds} characteristic curves parametrized for applied voltage gate V_g = 10 V , V_g = 14 V and V_g = 18 V , evaluated at T = 25 °C; T = 75 °C and T = 125 °C, respectively. In order to point out the difference between simulated and experimental curves obtained at low values of drain-source voltage, the drain current relative percentage errors er are evaluated and shown in Figs. 11, 12 and 13. It is possible to denote that the errors, in the linear region, decrease when the temperature increases.

Fig. 14 shows the same characteristic curves evaluated for V_g = 14 V, parameterized for T = 25 °C, T = 50 °C ,T = 75 °C, T =100 °C and T = 125 °C. The high values of percentage error in the linear region are explainable observing that in the SiC MOSFET the epitaxial layer resistance is small and the channel resistance is high, compared to the model, thus making the MOSFET channel a more significant contributor to the on-state voltage.

This is due to the low channel surface mobility of SiC. This results in the gradual transition from the linear region to the saturation region of the SiC curves.

IV. Losses Calculations

The energy switching losses of the SiC device during the turn-on and the turn-off transients are computed, according to Eqs. (18) and (19). The model was simulated under the conditions $V_{ds,off}$ = 800 V, V_g = 20 V, I_{load} = 20A and R_g = 6,8 Ω. The transient curves are shown in Figs. 15.

Through them, it is possible to obtain both the rise time t_{rise} and the fall time t_{fall} of the device. The values obtained by simulation using the proposed model present a good agreement with the manufacturer values, as shown in Table II.

TABLE II
SIC MOSFET RISE AND FALL TIMES

Data source	t_{rise}(ns)	t_{fall}(ns)
Simulation	12,3	35,4
Manufacturer	13,6	35,6

The energy switching losses are evaluated for T inside [25], [125] °C and are shown in Fig. 16. A good agreement between computed and manufacturer data can be observed.

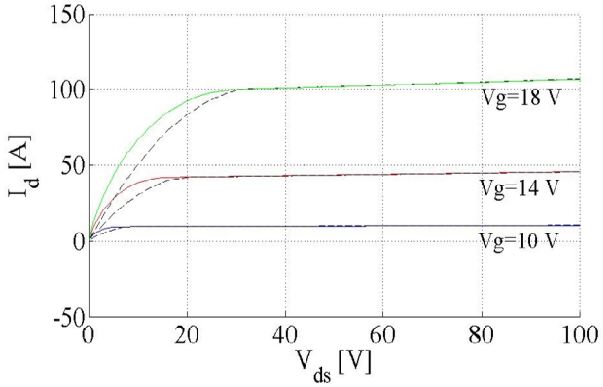


Fig. 8. I_d-V_{ds} characteristic curves evaluated at T = 25 °C

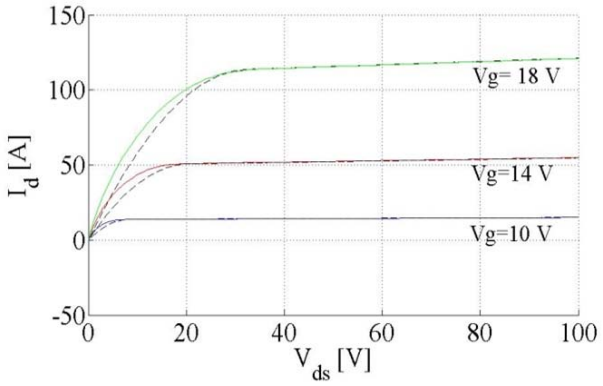


Fig. 9. I_d-V_{ds} characteristic curves evaluated at T = 75 °C

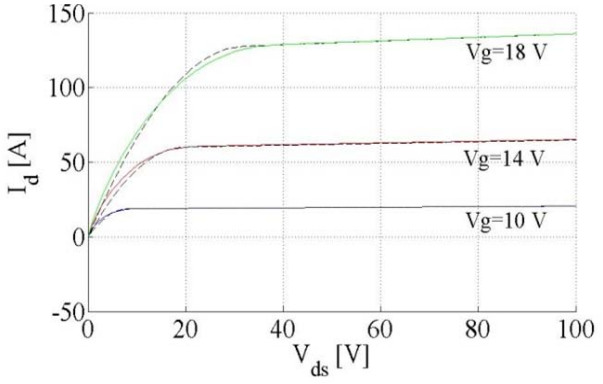


Fig. 10. I_d-V_{ds} characteristic curves evaluated at T = 125 °C

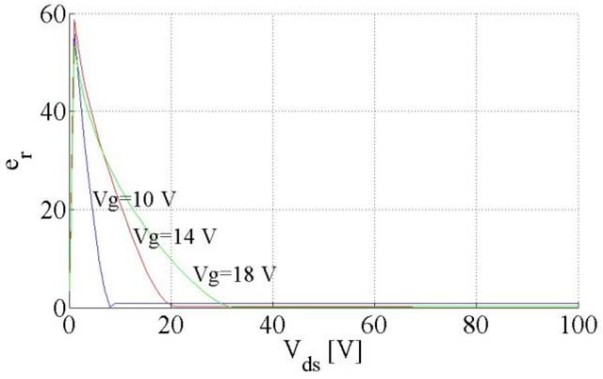


Fig. 11. Relative percentage error between the simulated and experimental curves shown in Fig. 8

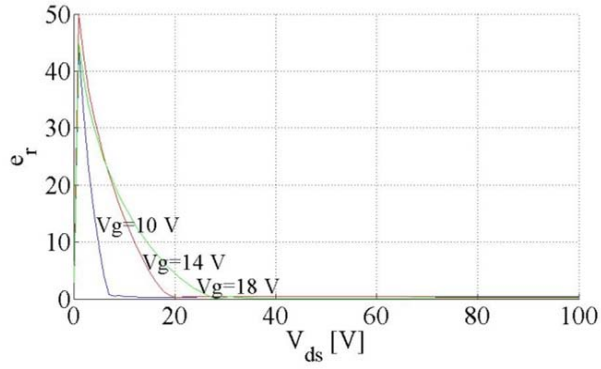


Fig. 12. Relative percentage error between the simulated and experimental curves shown in Fig. 9

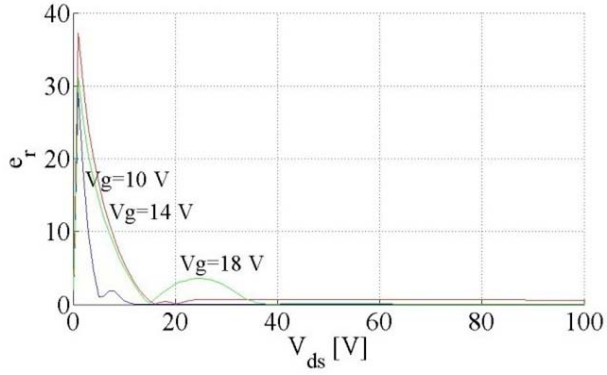


Fig. 13. Relative percentage error between the simulated and experimental curves shown in Fig. 10

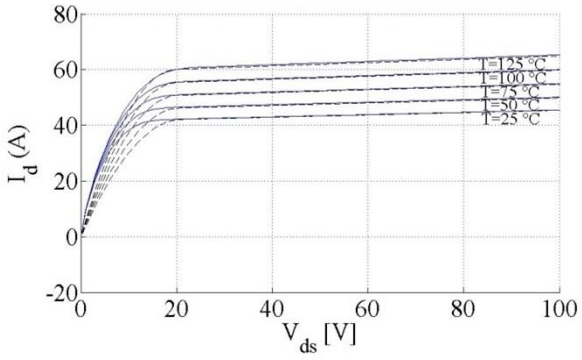
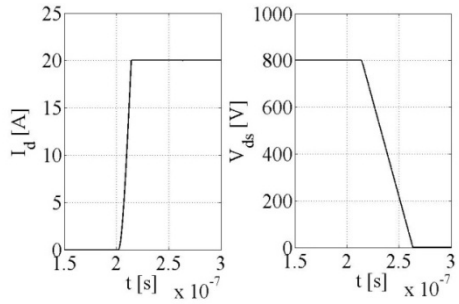


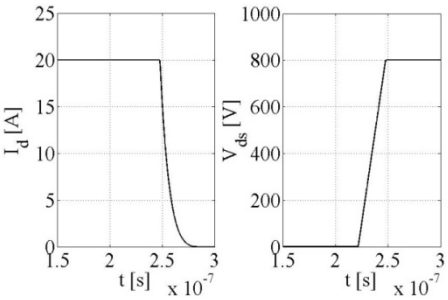
Fig. 14. I_d-V_{ds} characteristic curves evaluated for V_g =14 V

V. Application Example

In order to show the versatility of the Matlab/Simulink® SiC MOSFET model to compose more complex devices, the five level cascaded inverter shown in Fig. 17 has been considered. For this device the simulation results are obtained at two different temperature: T_1 = 50°C and T_2 = 100°C, for rated power equal to 12 kV A, V_{dc} = 600 V and a R-L load having R = 102Ω and L = 0.2 H. The pulse pattern, obtained by using the harmonic elimination algorithm, for modulation index m_1 = 0.8, is shown in Fig. 18 [28]. Output voltage and current on load, evaluated at T = 50°C, are shown in Figs. 19 and 20, respectively.



(a) Turn-on curves



(b) Turn-off curves.

Figs. 15. SiC MOSFET transient curves

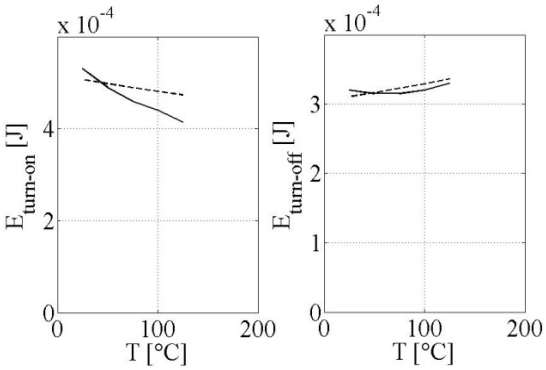


Fig. 16. SiC MOSFET switching losses: computed data (dashed line) and manufacturer data (continuous line)

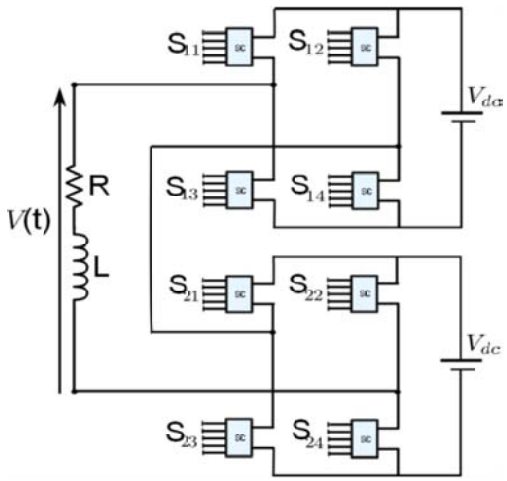


Fig. 17. Five level cascaded inverter

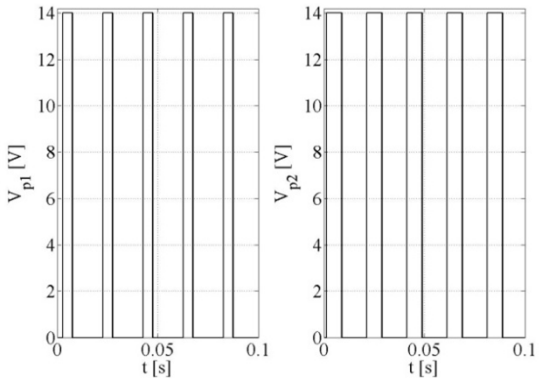


Fig. 18. Pulse pattern

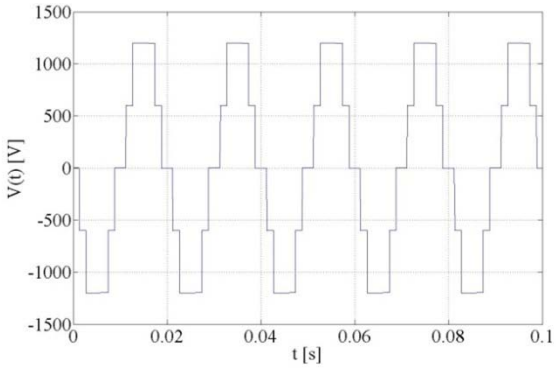


Fig. 19. Inverter output voltage

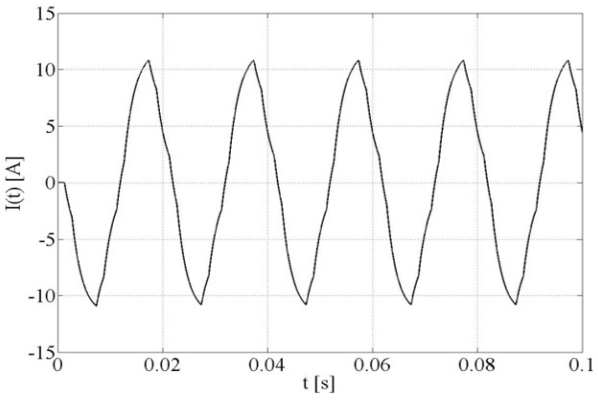


Fig. 20. Load current

It is worth noting, in the authors' knowledge, the proposed model is the only available for simulation of complex control algorithms on sophisticated power converter topologies. The same system, together with the control algorithm, cannot be practically simulated using circuital simulators like Spice.

VI. Conclusion

A detailed Matlab/Simulink® model of 4H-SiC MOSFET incorporating the equations (5) to (15b), has been proposed and fully implemented in a Simulink® library block with five input pins and two output pins. The proposed model is capable to estimate the switching losses.

It has been validated by comparing the obtained I_d-V_{ds}

characteristics with those given by the manufacturer for a widely diffused device (Cree CMF20120D).

The linear region is still underestimated, while the saturation region is successfully simulated. The block is very useful to verify complex converters topologies behavior. At this end, a 5-level cascaded inverter model has been selected and some significant simulation results have been shown. An important limit of this approach is the computational speed of the simulation, which could be very high for big systems (up to ten SiC devices).

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