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An Improved Compact Model for a Silicon-Carbide MOSFET, and its Application to Accurate Circuit Simulation

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***Abstract* — This paper presents an improved compact model for a discrete silicon-carbide MOSFET. This compact model based on the previous model features a new behavioral model of output characteristics and new non-linear models of internal capacitors. Simulation with the improved compact model is in better agreement with measurement than that with the previous compact model, as well as transient behavior of the drain-source voltage, the drain current and the leakage current out of a heatsink. Further, the improved model is useful for constructing the accurate compact model that can reproduce the high frequency characteristics of the transient waveforms of SiC-MOSFETs. This successful validation indicates that the improved compact model would be a promising tool for a full-simulation-based design system of the power converters using SiC-MOSFETs.**

***Index Terms*— MOSFETs, Semiconductor device modeling, Switching transients**

I. Introduction

SILICON-CARBIDE (SiC) power MOSFETs have been attracted as superior alternative power switching devices to conventional Si-based power switching devices. It has several preferable electrical and physical characteristics as power switching devices, such as low on-resistance, high-temperature operation, and high-frequency operation due to high-speed switching performance. Recently, SiC-MOSFETs molded in discrete packages or power modules have been putted on the market, which offers more opportunity to develop power converters using SiC-MOSFETs [1].

Most of the research and development activities of power converters using SiC-MOSFETs have been focusing on creating high-power-density power converters that realize both high conversion efficiency and miniaturization simultaneously [2] - [4]. As mentioned, electrical and physical properties of SiC-MOSFETs are suitable to meet these demands. For example, the property of low-loss-characteristics brings less heat generation of SiC-MOSFETs, thus resulting in downsizing or simplification of cooling equipment that is heavy and bulky in a power converter [5]. High-frequency operation of the power converter enables to downsize magnetic components such as a filter reactor that is another heavy and bulky component. From an economical point of view, a high power density brings a total cost reduction to the power converter, which results in mitigating an increased cost of SiC-MOSFETs.

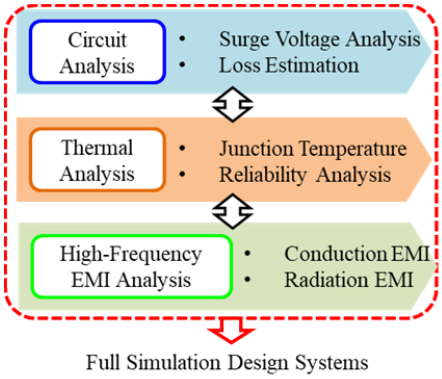

Fig. 1. Schematic illustration of a full-simulation-based design system using a compact model for a discrete SiC-MOSFET.

In order to design high-power-density power converters using SiC-MOSFETs, a simulation technique has been considered to be a promising design tool. Fig. 1 shows a schematic illustration of a full-simulation-based design system using a compact model for a discrete SiC-MOSFET. It gives several examples of required electrical, thermal, and electromagnetic interference (EMI) analyses. As noticed, these individual analyses are dependent each other. This dependency becomes stronger as the power density of a power converter gets higher [6]. Therefore, a comprehensive analysis is prerequisite to develop a high-power-density power converter using SiC-MOSFETs, and

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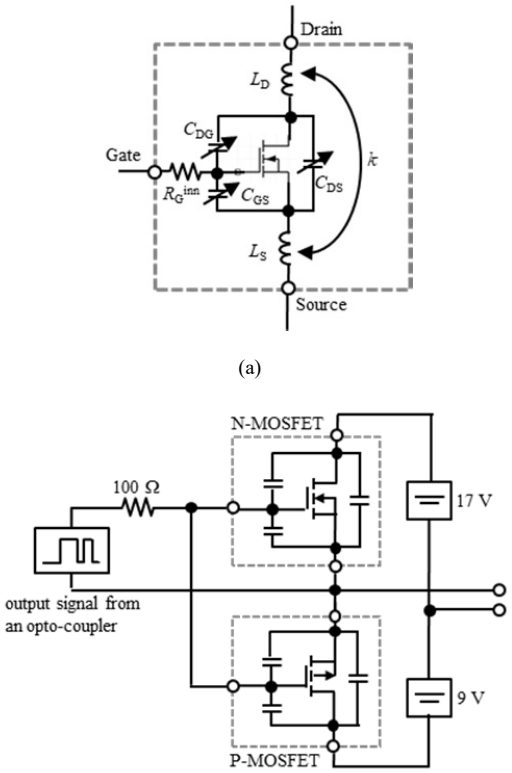

Fig. 2. The schematic circuit diagrams. (a) The compact model of the 1.2-kV 36-A discrete SiC-MOSFET molded in a standard TO-247 package. (b) The equivalent circuit model of the commercial gate drive circuit.

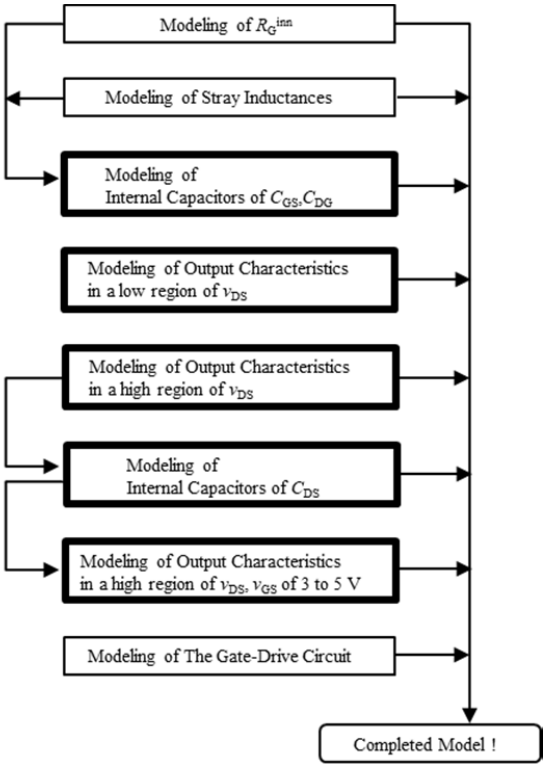

Fig. 3. The new modeling procedure for the improved compact model.

the compact model is indispensable to it.

Although several simulation analyses with various compact models for SiC-MOSFETs have been reported so far [7]-[9], the analysis of EMI is one of the advanced and undeveloped research fields. The primary reason for this undeveloped situation is a lack of an appropriate compact models for SiC-MOSFETs, which is able to reproduce transient waveforms of its high-speed switching behavior, dv_{DS}/dt and/or di_D/dt, accurately. Therefore, a circuit-based simulation method for EMI analysis of SiC-based power converters often uses a simplified trapezoidal waveform as a transient voltage waveform of SiC-MOSFET [10]. Although this method is practical and effective, it has a fundamental problem in preparing a suitable trapezoidal waveform for switching behavior. Normally, experimental results of switching waveforms are used to confirm a validation of the employed trapezoidal waveforms. The necessity of supportive experimental data is a critical limitation for developing a full-simulation-based design system.

This paper puts emphasis on an improved compact model for a commercially-available discrete SiC-MOSFET. The leakage current flowing out of a heat sink, i_{leak} occurs at the instant of switching in an inductive-load double-pulse switching system. Since it is one of the simplest EMI examples in a power converter, this paper pays attention to it [11]. A leakage-current path is considered as simple as possible between the grounded heat sink and the SiC-MOSFET. Thus, the waveforms of i_{leak} would be expected to directly reflect the characteristics of high-speed transient waveforms of the SiC-MOSFET. The details of the improved compact model are explained in the following Section II. Comparison between measurement and simulation in the transient waveforms of v_{DS} and its resulting i_{leak} evaluates feasibility of the improved compact model.

II. Model Improvement

Fig. 2 shows the schematic circuit diagrams used in this paper. Fig. 2(a) shows the compact model for a 1.2-kV 36-A discrete SiC-MOSFET molded in the standard TO-247 package (C2M0080120D, CREE) [12]. The compact model surrounded by a dashed square consists of three external electrodes; the gate, the drain and the source, output characteristics indicated by an electrical symbol of a general MOSFET, three internal capacitances between each pair of the electrodes; the drain-gate capacitance (C_{DG}), the gate-source capacitance (C_{GS}), and the drain-source capacitance (C_{DS}), the inner gate resistor (R_G^{inn}), and the stray inductances between the drain terminal and the source terminal; the drain-side inductance (L_D), the source-side inductance (L_S) and the coupling coefficient (k) between the two. Fig. 2(b) shows the equivalent circuit model of the commercially-available gate drive circuit (GDU40-2; Nihon Pulse Industry). The gate drive circuit is modeled with the simplified device models for N-channel and P-channel MOSFETs, two ideal positive and negative gate bias voltage sources, and an ideal voltage source that corresponding to an output signal from an opto-coupler. Since this gate drive circuit is used as a sup-

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portive tool for developing the compact model for the SiC-MOSFET, its easy availability is more emphasized than its optimization in this paper. The optimization of a gate drive circuit is beyond the scope of this paper, and left for future work.

A. *What is New in the Improved Model*

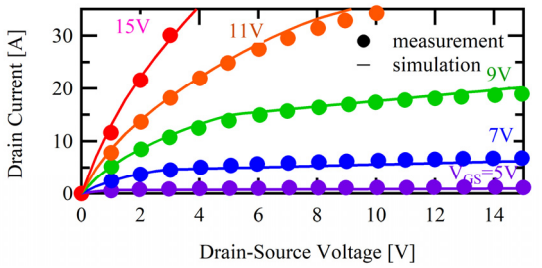
The improved compact model resulting from the previous model [13] features a new behavioral model of output characteristics, and new non-linear models of internal capacitors. The new modeling procedure shown in Fig. 3 is also developed, where the new models are marked with the bold squares. The brief overviews of the new models are itemized below.

(1) The output characteristics in a low region of v_{DS} of the previous model are measured by a commercial curve tracer with varying v_{GS} and v_{DS}, and then, are modeled on the basis of the cross-sectional structure and physical mechanism of MOSFETs operation [13]. The modeling procedure in [13] has been useful to conduct a self-consistent and time-efficient modeling. However, the biggest problem of this modeling is availability of the information of cross-sectional structure of MOSFETs. Usually, this sort of information is treated as a manufacture secret and covered to most of engineers or researchers who use it. Thus, this paper proposed a new behavioral model on the basis of the previous output characteristic equation. The new modeling procedure of this behavioral model is also considered.

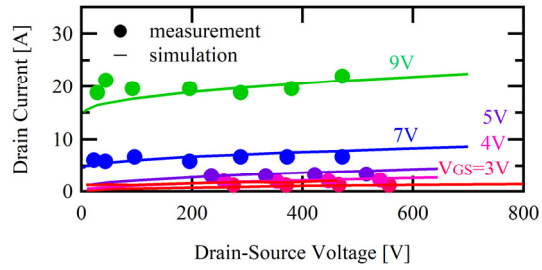
(2) The output characteristics in a high-voltage region of v_{DS} of the previous model are evaluated by analyzing turn-off transient waveforms [14]. This evaluation contains an inevitable error for correction of the values of i_D due to the current charged to C_{DS}. Therefore, the output characteristics of the improved model are re-evaluated from the load-short-circuit waveforms.

(3) The model of an internal drain-gate capacitor is appropriately modified by adding new data. The internal drain-gate capacitor was evaluated by analyzing gate currents during Miller periods, and modeled as a function of v_{GS} in [13]. Subsequently, it was re-evaluated and modeled as functions of v_{GS} and v_{DS} in [14]. The reproducibility of the dynamic behavior of the SiC-MOSFET in [14] was much accurate than that in [13]. This paper adds the new capacitance data that depend on higher voltage values of v_{GS}, representing the overall features related to the dependency of v_{GS} on C_{DG}.

(4) The model of internal drain-source capacitor is newly-developed. The previous compact model uses a conventional model of C_{DS} that is measured by a *LCR* meter for v_{GS} of 0 V, and modeled as a non-linear function of v_{DS}. Recently, Chen *et al.* proposed a new model of C_{DS} that takes the smaller capacitance values when a MOSFET is in the on-state than the off-state [15]. However, the physical description of this small capacitance phenomenon is too simple that the conduction path forming beneath the oxide layer reduces the effective area of



(a)



(b)

Fig. 4. Comparison in output characteristics between measurement and simulation at room temperature. (a) Comparison in output characteristics in the low region of v_{DS}. (b) Comparison in output characteristics in the high region of v_{DS}.

TABLE I
PARAMETER EXPRESSIONS OF THE NEW BEHAVIORAL MODEL

Symbol	Expression
K_1	$0.017\times(v_{GS}\text{-}v_{th})^2$
K_2	$0.138\times(v_{GS}\text{-}v_{th})$
v_{DS}^{sat}	$1.74\times(v_{GS}\text{-}v_{th})$
b	0.53
C_o	2

C_{DS}. The experimental verification of the above-mentioned characteristics of C_{DS} is neither described. Receiving this report, the characteristics of C_{DS} when the MOSFET is in the on-state are evaluated by analyzing the turn-off switching waveforms. The evaluation shows the new dependency of v_{GS} that is not used in the conventional models, and also quite different from the recent model in [15].

These improvements are justified to be effective in enhancing reproducibility of the transient switching waveforms of the SiC-MOSFET. The following subsections B and C make the detailed descriptions of new modeling of the output characteristics and two internal capacitors, respectively.

B. *Modeling of Output Characteristics*

Equation (1) is a new fitting equation for the output characteristics in the low region of v_{DS}, where K_1 and K_2 denote the proportional coefficient, C_o (>1) denotes the power factor, and

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b denotes the proportional coefficient of v_{DS}. Compared to the previous physics-based model [14], the first term in (1) that includes K_1, K_2, and C_o represents the cross-sectional information and the channel mobility. In order to identify the parameters of K_1, K_2, and b, the three independent formulas are used as described below.

$$i_D = \left\{\frac{K_1}{(1+(bv_{DS})^{C_o}} + K_2\right\} \times \left\{(v_{GS}-v_{th})(bv_{DS}) - \frac{1}{2}(bv_{DS})^2\right\} \cdots (1)$$

Formula (2) is obtained at the beginning of the saturation region for v_{GS} of 5 to 9 V. In (2), the first term in (1) is approximated as K_2 on the assumption that $(bv_{DS})^{Co}$ would be sufficiently large, and enable to cancel the effect of K_1. Formula (3) is also obtained at the same point of (2) by comparing the differential values. Solving the two formulas of (2) and (3), the two parameters of K_2 and b are identified. Formula (4) is obtained by comparing the differential values for v_{DS} of 0 V. Since the two parameters of K_2 and b are already obtained, the parameter of K_1 is given by (4).

$$i_D^{sat} = K_2 \times \left\{(v_{GS}-v_{th})(bv_{DS}^{sat}) - \frac{1}{2}(bv_{DS}^{sat})^2\right\} \cdots (2)$$

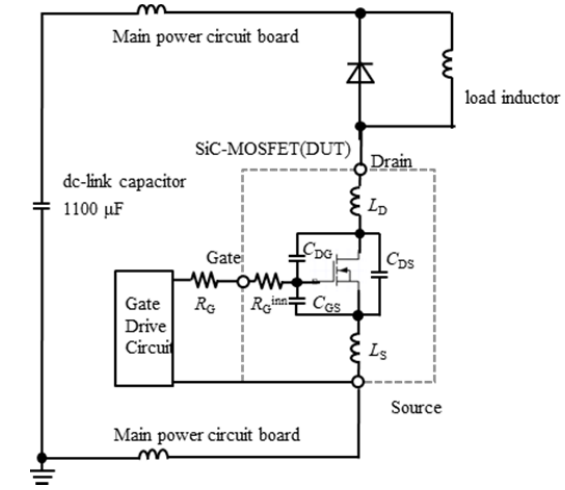
$$\frac{di_D}{dv_{DS}}(i_D = i_D^{sat}) = K_2 \times \{(v_{GS}-v_{th})(b) - b^2(bv_{DS}^{sat})\} \cdots (3)$$

$$\frac{di_D}{dv_{DS}}(i_D = 0) = (K_1+K_2) \times (b) \times (v_{GS}-v_{th}) \cdots (4)$$

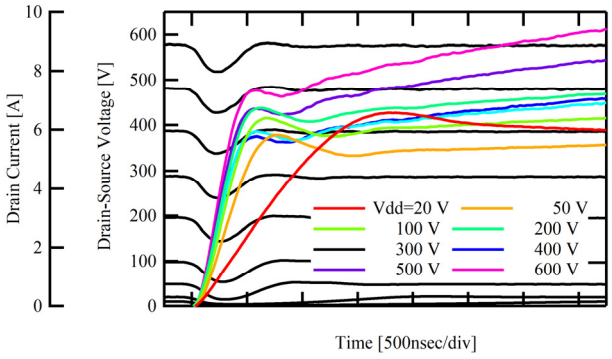
The last parameter of C_o is decided as the i-v curves show good agreement with the experimental data. These parameters mentioned above are expressed as a function of v_{GS}, or constant value for simplicity. The detailed expressions of these parameters are summarized in Table I. Fig. 4(a) shows the output characteristics model for the low region of v_{DS}, where the dots indicate the experimentally-extracted data, and the solid lines indicate the actually-used data with approximation.

The experimental evaluation of the output characteristics of the high region of v_{DS} is subdivided into two groups, depending on a region of v_{GS}.

The output characteristics in the high region of v_{GS} are evaluated by analyzing the load-short-circuit waveforms when the dc-link voltage is varied from 10 to 600 V. Fig. 5(a) shows the schematic circuit diagram of the load-short-circuit-switching test. The low-side SiC-MOSFET that is surrounded by the dashed square is the so-called "device under test (DUT)." The load inductor is a wire of 50 cm between the drain terminal of DUT and the drain terminal of the high-side diode. Fig. 5(b) shows the experimental waveforms of v_{DS} and i_D for v_{GS} of 7 V when the dc-link voltage is varied from 20 to 600 V, where the black lines indicate the waveforms of v_{DS}, and the colored lines indicate these of i_D. The i_D-v_{DS} characteristics are depicted when the waveforms of v_{DS} recover to the dc-link voltages, and are in stable in order to avoid the undesirable effects of the charged current to C_{DS}.



(a)



(b)

Fig. 5. A load-short-circuit-switching test. (a) Schematic circuit diagram of a load-short-circuit-switching test. (b) The experimental waveforms of v_{DS} and i_D for v_{GS} of 7 V.

The output characteristics for v_{GS} of 3 to 5 V are evaluated by analyzing turn-on waveforms at nominal zero drain current with varying the dc-link voltage from 200 to 650 V. In this evaluation, the values of v_{GS} are corrected by compensating for a voltage drop across the inner gate resistor. A voltage drop across the source-side stray inductor is neglected due to the nominal zero-drain-current-switching conditions. The channel current is calculated by adding the current discharged from C_{DS} to the drain current measured at the drain terminal of the package. The discharged current is calculated by multiplying the new capacitance value of C_{DS} and the value of dv_{DS}/dt, where the capacitance value of C_{DS} is represented as functions of v_{GS} and v_{DS} as explained in the following subsection C.

Fig. 4(b) shows a comparison in output characteristics of the high region of v_{DS} between measurement and simulation for v_{GS} of 3 to 9 V at room temperature. Each curves of i_D shows gradually-increasing behavior according to v_{DS}. Therefore, these i-v curves are approximated by the fitting equations given by (5), where K_3 denotes the proportional coefficient, v_{DS}^{sat} denotes the saturation voltage, and i_D^{sat} denotes the saturation current. The equations of (1) and (5) are described in VHDL-AMS language, and programed in the Simplorer software.

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$$i_{\mathrm{D}} = K \times (v_{\mathrm{DS}} - v_{\mathrm{DS}}^{sat})^{0.5} + i_{\mathrm{D}}^{sat} \cdots (5)$$

C. *Modeling of Internal Capacitors*

Among the three internal capacitors of C_{GS}, C_{DS}, and C_{DG} as shown in Fig. 2(a), the model of C_{DG} is appropriately-modified, and that of C_{DS} is newly-developed on the basis of the experimental results.

C_{DG} is known as the most critical capacitor that decides the transient waveforms of the SiC-MOSFET. Each capacitance values of C_{DG} are calculated by analyzing the gate current during a Miller period of turn-on switching at a nominal zero drain current. Fig. 6 shows the experimental waveforms of v_{GS}, v_{DS}, and i_{G} for a gate bias voltage of 15 V. As seen in Fig. 6, the waveform of v_{GS} shows the plateau voltage during the Miller period. During this period, most of the gate current is supposed to flow into C_{DG}. Therefore, the capacitance value of C_{DG} is obtained by differentiating the amount of charge to C_{DG} with respect to v_{DG}. This analysis gives the dependency of v_{DS} on C_{DG} at a certain value of v_{GS} that is called as a Miller voltage. In order to examine the dependency of v_{GS} on C_{DG}, the gate bias voltage is also varied, which prepares several Miller periods with the different Miller voltages. Based on the above-mentioned experiments, C_{DG} is modeled as a pair of parallel-connected capacitors; one is a function of v_{GS} and the other is that of v_{DS}.

Fig. 7(a) shows the dependency of v_{GS} on C_{DG}, where the dots indicate the experimental results that were obtained with the above-mentioned method in the previous work [14], the open-dot indicates data from the datasheet, the open-squires indicate the newly-added experimental results, and the dashed line indicates the approximated data used in this paper. The new data are obtained by the same method with a small outer gate resistor. The small outer gate resistor offers higher switching operation, accompanied by an increased channel current during the Miller periods. The channel current that consists of the gate current and the current discharged from C_{DS} gives the Miller periods with the higher plateau voltages, which expands the research area of the dependency of v_{GS} on C_{DG}. The new data compensate for the dependency of the higher region of v_{GS} on C_{DG}. The new data show the saturation behavior above v_{GS} of 8.0 V that is a similar value to the flat band voltage of the SiC-MOSFET used in this research [16]. Fig. 7(b) shows the dependency of v_{DS} on C_{DG}, where the dots indicate the experiments and the dashed line indicates the approximated data. The exponential function prepared in the Simplorer software is used to approximate the experimental data as shown in (6) that is described in VHDL-AMS language.

$$\begin{aligned} C_{\mathrm{DG}} &= C_{\mathrm{DG}}(v_{\mathrm{GS}}) + C_{\mathrm{DG}}(v_{\mathrm{DS}}) \\ &= \{(7.0 \times 10^{-12}) e^{0.19 \times v_{\mathrm{GS}}}\} \\ &\quad + (2.07 \times 10^{-11}) e^{-0.026 \times v_{\mathrm{DS}}} \quad \cdots (6) \end{aligned}$$

The accuracy of the model of C_{DS} in collaboration with that

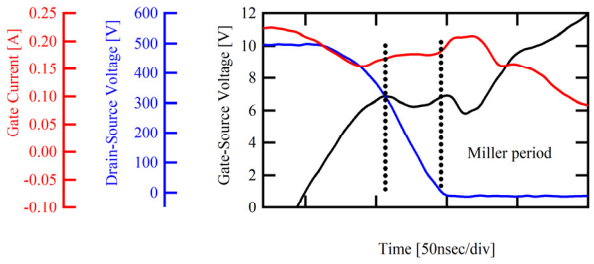

Fig. 6. The experimental waveforms of v_{GS}, v_{DS}, and i_{G} of turn-on switching at a nominal zero drain current.

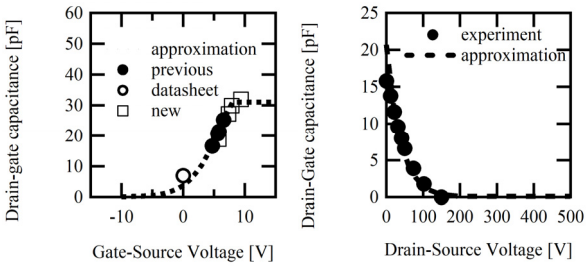

Fig. 7. The drain-gate capacitance as functions of v_{GS} and v_{DS}. (a) The v_{GS} dependency of the drain-gate capacitance. (b) The v_{DS} dependency of the drain-gate capacitance.

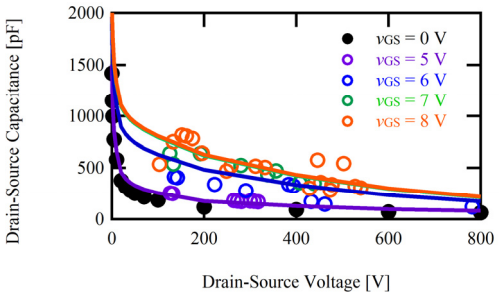

Fig. 8. The drain-source capacitance as functions of v_{GS} and v_{DS}.

of output characteristics decides the waveforms of i_{D}, since i_{D} flows separately into a channel and C_{DS} in the MOSFET device. As mentioned, Chen *et al.* has suggested that the capacitance values of C_{DS} when the MOSFET is in the on-state are different from these in the off-state. Thus, in this paper, the capacitance values of C_{DS} when the MOSFET is in the on-state are experimentally examined by analyzing the turn-off waveforms. The capacitance values of C_{DS} are obtained by dividing the current charged to C_{DS} by the rate of the drain-source voltage change (dv_{DS}/dt). The charged current of C_{DS} is obtained by subtracting the channel current from i_{D}. The channel current is accurately calculated using (5) as described in subsection B.

Fig. 8 shows the evaluation results of C_{DS}, where the dots indicate experimental data for v_{GS} of 0 V measured by a *LCR* meter, the open-dots indicate the experimentally-evaluated data for v_{GS} of 5 to 8 V by the above-mentioned analysis, and the solid lines are the approximation ones used in the new model of

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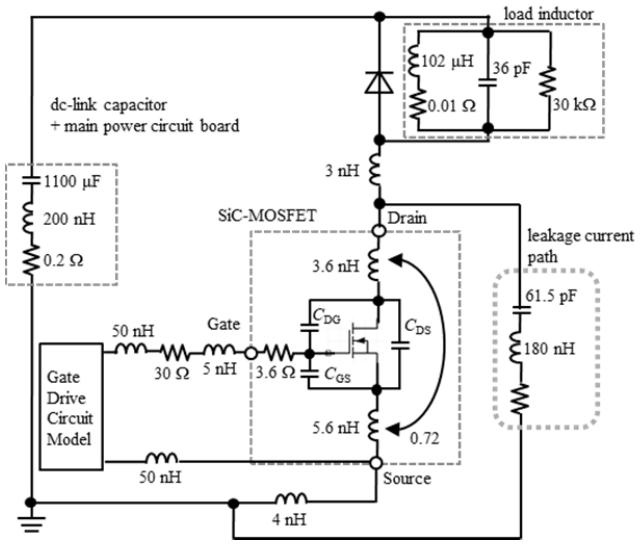

Fig. 9. Schematic circuit diagram of an inductive-load double-pulse-switching test bench with a leakage current path.

C_{DS}. Remarkably, the capacitance values for v_{GS} of 5 to 8 V, when the MOSFET is in the on-state, show the larger capacitance values than these for v_{GS} of 0 V. This v_{GS} dependency on the capacitance values is not used in the previous model [14], and is opposite to that of the recent model in [15]. Note that the characteristics of C_{DS} can be represented by two independent voltages among v_{GS}, v_{DS}, and v_{DG}. This paper represents the model of C_{DS} as functions of v_{GS} and v_{DS}. A pair of v_{DS} and v_{GS} is familiar and convenient for most circuit designers because the values of v_{DS} and v_{GS} are two of the main design parameters of power conversion circuits. Therefore, this model of C_{DS} is suitable for a design system based on full circuit simulation as mentioned in Introduction.

One of the possible explanations of this result is capacitance formation between the channel and the JFET region. The depletion width between the channel and the JFET region decreases with respect to v_{GS}. This is because the top of the valence band of p-layer bends downward and is close to the Fermi level, which results in decreasing the potential difference between the valence band of p-layer of the channel and that of n-layer of the JFET. This brings the shorter depletion width, and results in the increase of the capacitance value of C_{DS}.

The characteristics of C_{DS} shown in Fig. 8 are approximated with the fitting equation given by (7), where C_{DS}^{1} is the previous model that is measured at v_{GS} of 0 V, and the second term represents the increased capacitance values when the MOSFET is in the on-state. With the modeling of C_{DS}^{1}, a 2-D data table in the capacitor model of the Simplorer software is prepared and used. In the second term, the fraction expression of v_{GS} is a quasi-step function which represents the transition from the on-state to the off-state. The following exponential function of v_{DS} represents the increased capacitance values. Equation (8) shows the approximated differential equation of the second term of (7) that is used to simulate the charged and discharged currents of C_{DS}. Equation (7) and (8) are described in VHAL-AMS language, along with the Simplorer software.

$$C_{\mathrm{DS}} = C_{DS}^{1} + \frac{1}{1+e^{-3(v_{\mathrm{GS}}-5.7)}} \times (7.6\times10^{10})e^{(-2\times10^{-3})v_{\mathrm{DS}}} \cdots (7)$$

$$\left\{\frac{(7.6\times10^{10})\times(-2\times10^{-3})}{1+e^{-3(v_{\mathrm{GS}}-5.7)}} \times e^{(-2\times10^{-3})v_{\mathrm{DS}}}\right\}\frac{dv_{\mathrm{DS}}}{dt} \cdots (8)$$

III. Model Validation

The dynamic performance of the improved model is verified by an inductive-load double-pulse switching test at a drain current of 15 A. The feasibility of the improved compact model for analyzing electromagnetic interference is also verified by comparison in the time-domain waveforms of i_{leak}.

Fig. 9 shows the schematic circuit diagram of an inductive-load double-pulse switching test with a leakage current path. The low-side SiC-MOSFET that is surrounded by the dashed square is DUT, where the improved compact model explained in Section II is assigned. The two outer stray inductances of the standard TO-247 package are 3 nH and 4 nH. The body diode of the high-side MOSFET is used as a free-wheeling diode, and modeled with its static *i-v* characteristics from the datasheet. No reverse recovery effect is considered in this model. The equivalent circuit models of the dc-link capacitor and the inductive load are constructed on the basis of their measured impedance data. The leakage current path marked by the dashed rectangular, is represented as a series connection of *LCR*. The stray capacitor of 61.5 pF is putted between the drain terminal located at the backside of the package and the heatsink on which the low-side SiC-MOSFET is mounted. The capacitance value of this stray capacitor is measured by a commercial *LCR* meter (4285A, Keysight) at a frequency of 1 MHz.

Then, it is modeled as a lumped capacitor component. The inductor of 180 nH comes from the ground wire between the heatsink and the N-terminal of the dc-link capacitor. The value of this inductance is calculated on the basis of the length of the wire. The leakage current is measured by a toroidal current monitor inserted in the ground wire.

Fig. 10 shows the transient waveforms of v_{DS}, i_D, and i_{leak} of measurement, simulation with the previous model, and that with the improved model at a drain current of 15 A.

Fig. 10(a) shows comparisons in turn-on switching waveforms. The comparison in v_{DS} shows slight improvement in the waveform of the improved model. The waveforms of v_{DS} have two major slopes. The improved model shows better agreement with the measurements in the slope of v_{DS}. The values of dv_{DS}/dt at the first slope are evaluated as 7.0 kV/μsec for measurement, 8.8 kV/μsec for simulation with the previous model, and 7.7 kV/μsec for that with the improved model. The values of dv_{DS}/dt at the second slope are evaluated as 12.5 kV/μsec for measurement, 11.0 kV/μsec for simulation with the previous model, and 11.5 kV/μsec for that with the improved model. The comparison in i_D also shows good agreement between measurements and simulations in the slope of i_D. The waveforms of the both simulation show the less peak values of i_D than that of measurement. This deviation is attributed to the models of the

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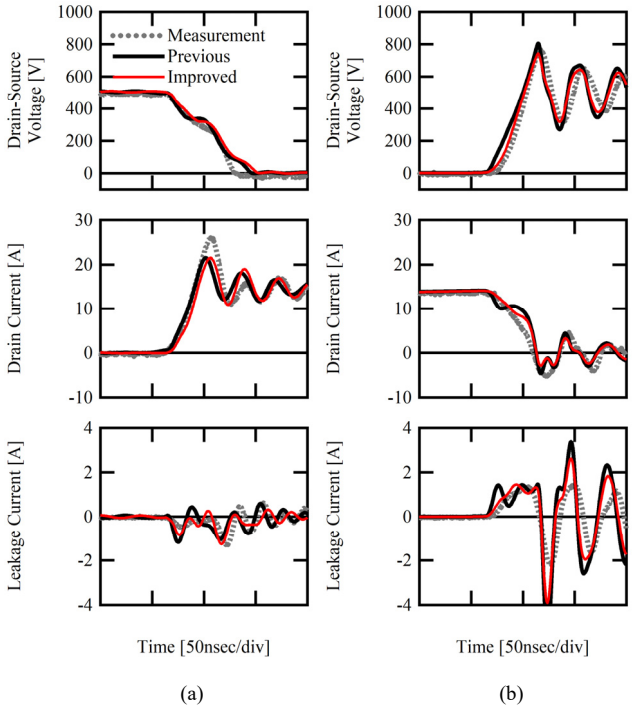

Fig. 10. Comparisons in transient waveforms of the drain-source voltage, the drain current, and the leakage current at a drain current of 15 A between measurement, simulation with the previous model, and that with the improved model. (a) Turn-on switching. (b) Turn-off switching.

main power circuit, which is beyond the scope of this research. The waveform of i_{leak}, obtained from the improved model, shows much better agreement with that of the measurement than that from the previous model. The improved model shows similar waveform with the measurement in terms of the two major valley shapes and the minor valley shape between them. At the first valley moment denoted by a solid arrow, the peak values of i_{leak} are evaluated as -0.45 A for measurement, -1.17 A for simulation with the previous model, and -0.83 A for that with the improved model. This improvement is a result of the accuracy of the model of output characteristics in the high region of v_{DS}. The channel of the low-side SiC-MOSFET is still in the high resistance condition, and holds most of the dc voltage of the dc-link capacitor. In other words, it acts as a dominant resistor of the series-connected *LCR* loop path of i_{leak}, and has a strong influence on the waveform of i_{leak}. At the second valley moment of i_{leak} denoted by the dashed arrow, the peak values of i_{leak} are evaluated as -1.31 A for experiment, -1.02 A for simulation with the previous model, and -1.26 A for that with the improved model.

Fig. 10(b) shows comparisons in turn-off switching waveforms in the same manner as the turn-on switching waveforms as shown in Fig. 10(a). The comparison in v_{DS} shows the noticeable improvement in the waveform from the improved model. In the beginning of the voltage increasing, the slope of v_{DS} of the improved model shows the similar gentle gradient to that of the measurement. On the other hand, the waveform from the previous model shows straightforward increasing. After a while, the waveforms of both simulations look similar each other, and show good agreement with that of the measurement.

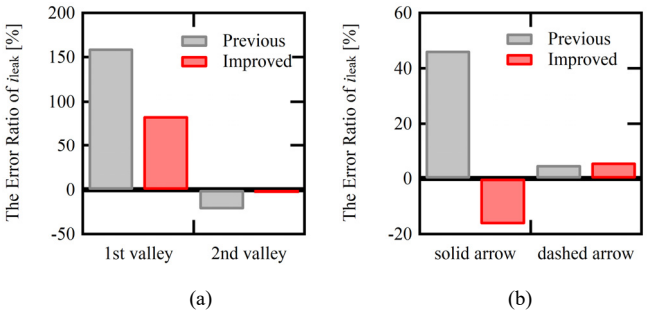

Fig. 11. Comparison in the error ratios of i_{leak} between the previous and the improved model. (a) Turn-on switching. (b) Turn-off switching.

TABLE II
THE EFFECTS OF THE IMPROVED MODEL

Components	Improvements in v_{DS}	Improvements in i_D	Improvements in i_{leak}
(1) The new behavioral model	Enhance the adaptability of this compact model for SiC-MOSFETs		
(2) The output characteristics in the high region of v_{DS}	dv_{DS}/dt in the high region of v_{DS} at turn-on switching.		The corresponding waveform of i_{leak}
(3) The model of C_{DG}	dv_{DS}/dt at turn-on switching for i_D of 15 A		The corresponding waveform of i_{leak}
(3) The model of C_{DS}	dv_{DS}/dt at turn-off switching for i_D	The waveform of i_D at turn-off switching	The corresponding waveform of i_{leak}

The comparison in i_D also shows significant improvement in the waveform from the improved model. In the beginning of the current decreasing, the waveform from the improved model is similar to that from the measurement. The waveform from the previous model is the heavily curved line, and shows significant deviation. This improvement is due to the accuracy of the model of C_{DS}. As mentioned in Section II, the improved model of C_{DS} has the larger capacitance values than the previous model when the MOSFET is in the on-state. This increased capacitance creates new current sharing behavior between the channel and C_{DS} in the MOSFET device, and results in the improved waveform of i_D. The waveform of i_{leak} obtained from the improved model shows the clear improvement of gentle gradient due to the gentle increase of v_{DS} from the improved model. On the other hand, the waveform of i_{leak} from the previous model shows the peaky shape due to the straightforward increase of v_{DS} from the previous model.

Fig. 11 summarizes the error ratios of the values of i_{leak} at the moments denoted by the arrows in Fig. 10. Fig. 11(a) shows comparison in the error ratios of the current amplitude of i_{leak} of turn-on switching. The error ratio at the first valley moment of the improved model shows the significant reduction compared

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to that of the previous model. Again, this improvement is attributed to the accuracy of the model of output characteristics in the high region of v_{DS}. The error ratio of the improved model at the second valley moment also shows the significant reduction. This is attributed to the modified model of C_{DG}, which affects the value of dv_{DS}/dt. Fig. 11(b) shows the error ratios of the current amplitude of i_{leak} of turn-off switching. The improved model also shows the smaller error ratio than the previous model. This improvement is mainly due to the new model of C_{DS}.

Table II summarizes the effects of the improved compact model on the transient waveforms of v_{DS}, i_D, and i_{leak}. The new behavioral model enables to prepare compact models of SiC-MOSFETs without their cross-sectional information, thus expanding the adaptability of this model. The modified model of C_{DG} brings better reproducibility of the turn-on switching waveform of v_{DS} and i_{leak}. The new model of C_{DS} makes a significant contribution to improving the turn-off switching waveforms of v_{DS}, i_D, and i_{leak}. This table offers useful information for constructing an accurate compact model to simulate high frequency characteristics of switching of SiC-MOSFETs.

IV. Conclusion

This paper has presented an improved compact model for a discrete SiC-MOSFET. The improved model features a new behavioral model of the output characteristics, and new non-linear models of two internal capacitors. The improved model shows better reproducibility of the transient waveforms of v_{DS}, i_D and i_{leak} than the previous model. In addition, a comparison in transient waveform between the previous and improved models gives the useful information for constructing the accurate compact model that can reproduce the high frequency characteristics of the transient waveforms of SiC-MOSFETs. The model is also expected to result in a promising circuit simulation tool for evaluating electromagnetic interference phenomena.

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An Improved Compact Model for a Silicon-Carbide MOSFET, and its Application to Accurate Circuit Simulation

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Bizim için fikir verebilecek, doğrudan bizim çalışmalarımız ile örtüşen bir makale

Kapasitans modellenmesi ile ilgili kısım özellikle faydalı olabilir