Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors

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Keywords

«Gallium Nitride (GaN)», «Wide bandgap devices», «Device characterisation», «Device modeling», «Device simulation»

Abstract

In this paper, turn-on and turn-off switching behavior of 650V enhancement-mode GaN power FETs are investigated. An analytical model is developed to analyze the current-voltage characteristics of the device during switching transients both with and without the effects of parasitic components. In addition, the effect of the temperature and circuit parameters on the switching characteristics are investigated.

Introduction

Wide band-gap power semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming more widespread, thanks to their superior efficiency and power density performance over Silicon (Si) based power semiconductor devices. Although current GaN devices are available at lower voltage (< 650V) and lower current (< 50A) ratings, they already became an attractive solution in several power converter applications. Several enhancement-mode (e-mode) GaN transistors are now commercially available up to 650 V ratings, which have better performance than cascode devices in terms of the switching speed, $R_{ds\text{-}on}$ and reverse conduction. E-mode GaN FETs have low specific $R_{ds\text{-}on}$ due to their high breakdown field as well as high electron mobility. They can be manufactured with smaller size so that the parasitic components due to packaging are lower resulting in faster switching [1]. Switching losses of these devices are much lower compared to their Si counterparts, which allows them to be used in high frequency applications; the size of passive components can be reduced.

Investigation of switching behavior of GaN power FETs is important for several reasons. First, high switching speed of GaNs make them more vulnerable to di/dt and dv/dt effects and parasitic components. Secondly, e-mode GaNs have reverse conduction capability without an intrinsic or external diode [2]. They act as a resistor just like MOSFETs in forward conduction; however, their behavior in reverse conduction is different from the forward conduction, varying with the applied gate-source (V_{gs}) voltage. Therefore, turn-on and turn-off characteristics are dependent on applied gate-source voltage. Usually in

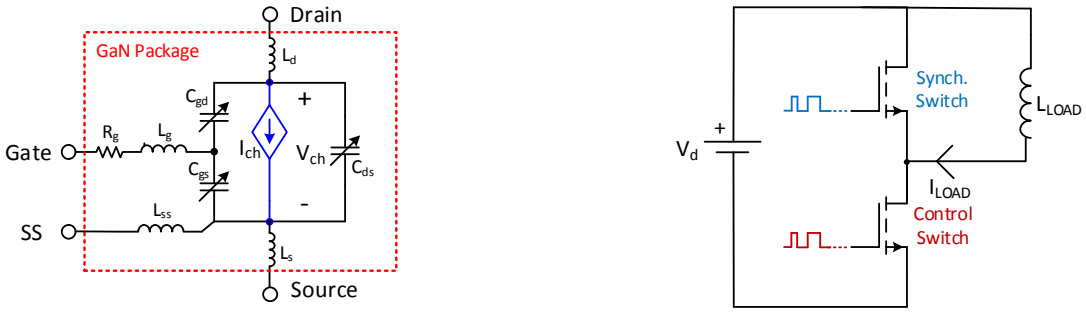
half bridge configurations, a negative gate voltage is required to avoid false turn-on, which results in a much higher on-state voltage when the device is not actively turn-on during dead-time [3]. Another reason for studying switching behavior of GaN is that their switching loss and reverse conduction loss model is not the same as Si MOSFETs. Although dead-time period and its effects on power loss calculations are usually ignored in other applications, it may affect the converter efficiency significantly in e-mode GaN applications [3].

Several recent studies have been published regarding e-mode GaN FET modeling. In [4], the I_{ds}-V_{ds}, I_{ds}-V_{gs} characteristics and dynamic $R_{ds\text{-}on}$ behavior of e-mode GaNs are obtained using curve fitting from experimental data. An analytical model is applied with steady-state behavior with temperature dependency and dynamic response with varying input and output capacitances in [5]. A mode-by-mode analysis is investigated in [6] for estimating the switching losses under various parasitic effects using small-signal models. The false turn-on phenomenon and its relationship with the applied V_{gs} voltage are investigated in [3]. Several methods have been proposed for the minimization of the reverse conduction losses such as using a schottky diode in parallel with the synchronous GaN transistor [3]. In this paper, a hybrid model is proposed for the investigation of steady-state behavior and the switching transients of e-mode GaN power FETs. The state trajectories of the device during the turn-on and turn-off periods are obtained. The active turn-on and passive turn-on characteristics of the device are investigated on a double pulse test circuit. The effect of varying device capacitances and parasitic inductances on these trajectories and their possible outcomes are studied. In addition, the effect of the temperature and circuit parameters on the turn-on and turn-off characteristics are investigated.

GaN Modeling

In this study, a hybrid model is proposed as shown in Fig. 1(a). In this model, the drain-source characteristics is modeled by a dependent current source, which varies with gate-source voltage, drain-source voltage and temperature. The blue branch in Fig. 1(a) indicates device channel and its current and voltage equals to $I_{ds} - V_{ds}$ in steady state. The analysis during the switching transients will be located onto these steady state characteristics to show the regions that device operates during these transient periods. Moreover, the Kelvin source pin (SS) is included in the model to analyze the switching behavior clearly. Since the I_{ds} current flows through the source pin and since GaN FETs are able to switching fast, which results in high di/dt ratio, the gate-source voltage is distorted because of the source parasitic inductance. Thus, using the Kelvin source pin increases the stability as discussed in more detail in the following sections.

The equations used for steady-state models are shown in (1) and (2) for forward conduction and reverse conduction, respectively. These equations correspond to the I_{ds}-V_{ds} curves of the device and the dynamic $R_{ds\text{-}on}$, derived from the manufacturer's models. The logarithmic multiplier of the equations represents the trans-conductance of the device where V_{th} is the threshold voltage. The fractional multiplier represents the region in which the device is operating; i.e., active region or ohmic region. Using this model, both steady state and transient behavior of the conduction paths are obtained. The model is used in MATLAB/Simulink with a Double Pulse Test (DPT) circuit to investigate the switching behavior as shown in Fig. 1(b). The nominal values of this test circuit used for the simulations are listed in Table 1.



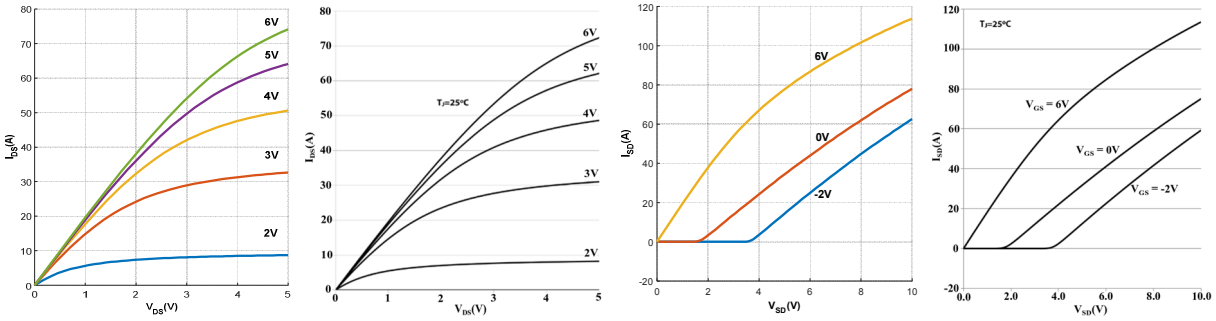
(a) Model (b) DPT Circuit

Fig. 1: Proposed hybrid model of e-mode GaN power FET (a) & the DPT circuit used for the analysis (b)

$$I_{ds} = K_1(T) * \ln\left[1 + e^{\left(\frac{V_{gs}-V_{th}}{K_2}\right)}\right] * \frac{V_{ds}}{1 + \max\left(K_4 + K_5 * (V_{gs} + K_6), K_7\right) * V_{ds}}, K_i \text{ are constant} \quad (1)$$

$$I_{ds} = -K_1(T) * \ln\left[1 + e^{\left(\frac{V_{gd}-V_{th}}{K_8}\right)}\right] * \frac{V_{sd}}{1 + \max\left(K_4 + K_5 * (V_{gd} + K_9), K_7\right) * V_{sd}}, K_i \text{ are constant} \quad (2)$$

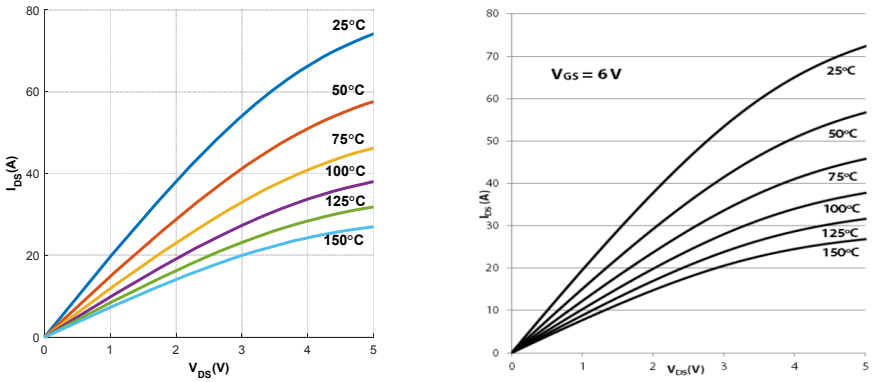
To show the accuracy of the steady state models, I_{ds}-V_{ds} characteristics of the selected device (GS66508B from GaN Systems) with varying V_{gs} is obtained in both forward and reverse conduction regions at 25 ^{0}C, and plotted side-by-side with the actual characteristics given in the datasheet of the selected device in Fig. 2 [7]. As shown, the reverse conduction behavior is highly dependent on the applied gate voltage, and shows a different behavior at negative gate voltage. In freewheeling modes, this should make no difference since the applied gate voltage is positive. However, during dead-time periods, a negative gate voltage is applied increasing the reverse conduction loss, which makes the optimization of the negative gate voltage and dead-time duration very critical.



(a) Model (b) Datasheet (c) Model (d) Datasheet

Fig. 2: Steady-state characteristics of GS66508B obtained by the proposed model and the actual characteristics [7] for forward conduction (a & b) and reverse conduction (c & d)

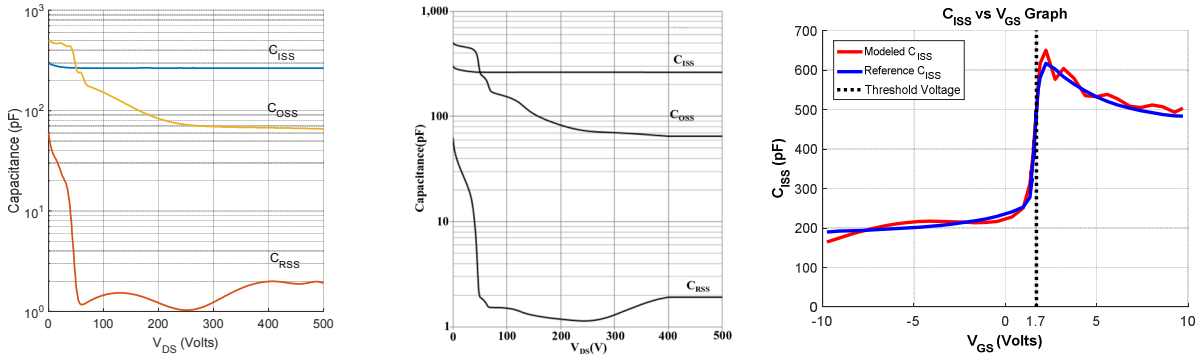
Secondly, the steady-state behavior of the GaN FETs is dependent greatly on the temperature, so its performance is affected by the temperature significantly as given in Fig.3. The trans-conductance of the GaN transistor is nearly halved for every 75^{0}C increase in junction temperature. Therefore, the thermal analysis is required to investigate the switching behavior more precisely.



(a) Model (b) Datasheet

Fig. 3: Thermal characteristics of GS66508B obtained by the proposed model and the actual characteristics [7] for forward conduction at 6V gate-source voltage

Thirdly, the voltage-dependent parasitic capacitances are modeled using curve fitting obtained from datasheet [7] and [3]. The resultant curves are given in Fig. 4. The manufacturer provides the curve for parasitic capacitances with respect to the drain-source voltage and it is seen that C_{ISS} is constant. However, the C_{ISS} changes significantly with varying gate-source voltage and the model should be constructed by identifying the gate charge. Therefore, in this paper, in order to model the dynamic behavior accurately, C_{ISS}-V_{GS} curve is obtained from the reference graph given in [3].



(a) Model (b) Datasheet (c) C_{ISS} vs V_{GS} [3]

Fig. 4: Modeling of the capacitances using curve fitting

Switching Behavior of GaN

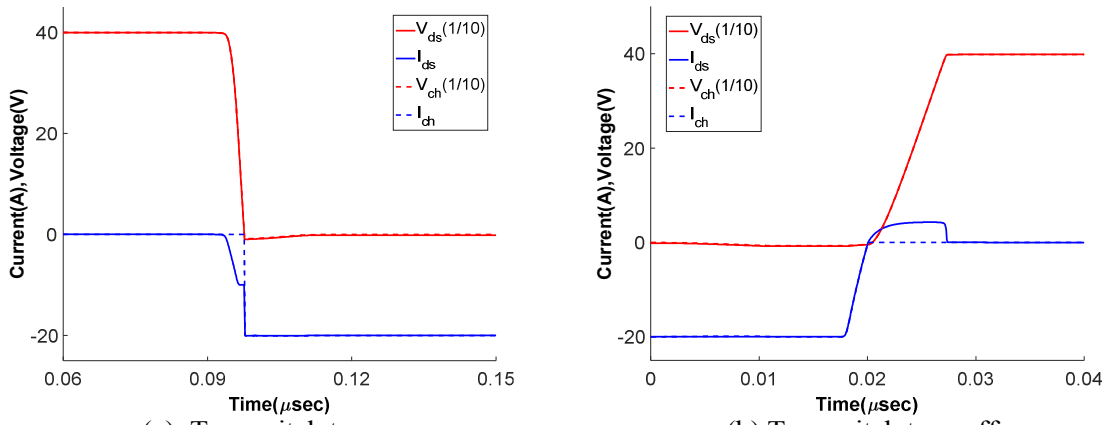
For better understanding of the switching behavior of e-mode GaNs, the turn-on and turn-off behavior of the selected device is investigated with a DPT circuit step-by-step using three models: the simplest model with constant capacitances and without parasitic inductances, the model with variable capacitances but without parasitic inductances, the most comprehensive model with variable capacitances and with parasitic inductances.

Table 1. The parameters used for the test circuit in MATLAB/Simulink [3, 7]

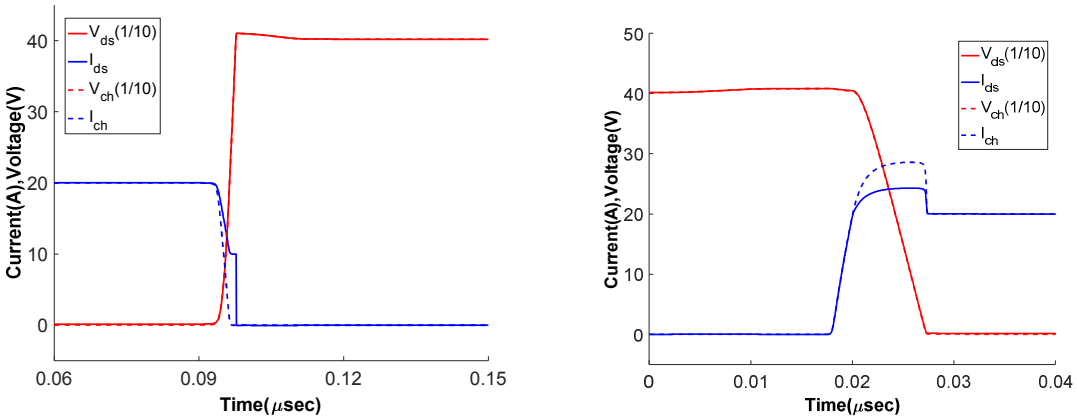
Input voltage (V_d)	400 V	Internal gate resistance (R_g)	1.5 Ω	Gate parasitic inductance (L_g)	3.0 nH
Output Current (I_{LOAD})	20 A	Drain/source inductances (/L_s)	0.9 nH	Power loop inductance (L_p)	7.0 nH
Load inductance (L_{LOAD})	35 mH	Turn-on gate resistance ($R_{G\text{-}ON}$)	10 Ω	Junction Temperature (T_J)	125 ^{0}C
Applied gate voltage (V_{gs})	-3V/+6V	Turn-off gate resistance ($R_{G\text{-}OFF}$)	1 Ω	Dead-time (t_{dead})	20 ns

a) Model 1: The simplest model with constant capacitances and without parasitic inductances

For simplicity, the control switch is going to be labeled as “Bottom Switch” and the synchronous switch is going to be labeled as “Top Switch” from now on, in the DPT circuit. For Model 1 described above, turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. 5.



(a) Top switch turn-on (b) Top switch turn-off



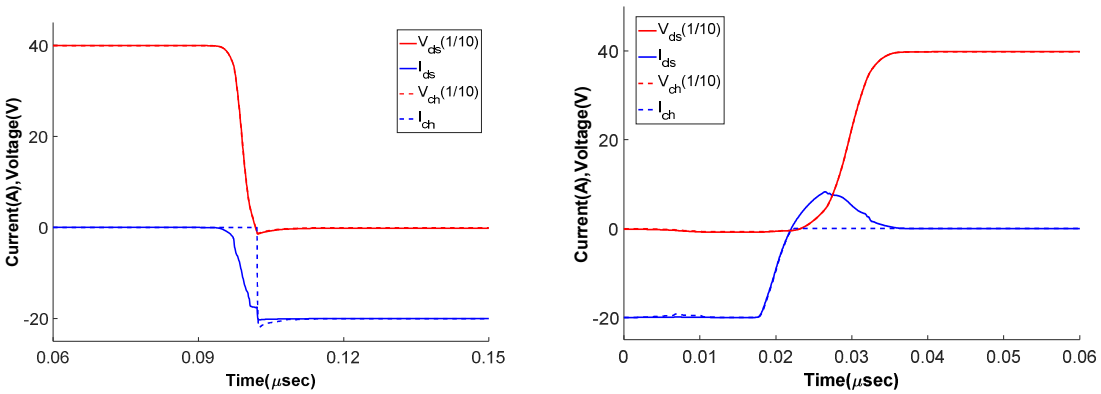
(c) Bottom switch turn-off (d) Bottom switch turn-on

Fig. 5: Switching characteristics in time domain obtained using Model 1

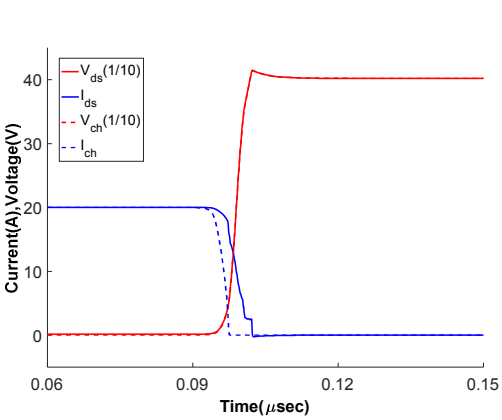
The drain-source current and the channel current is plotted together to clearly show the device characteristics. Since the inductances are not included in this model, the channel voltage is equal to the drain-source voltage. However, due to capacitors charging & discharging in transient periods, the channel current is different from the drain-source current and drain-source current does not reflect the channel characteristics completely. As shown in Model 1, Figure 5(d), when the bottom switch is being turned on, the drain-source current and channel current make an overshoot with different amplitudes. Since the top switch stops conducting, C_{OSS} (=Cgd +Cds) of the top switch requires to be charged which results in a positive current flow through the top switch. When the drain-source voltage of the top switch increases, the drain-source voltage of the bottom switch decreases, so the C_{OSS} of the bottom switch discharges, which results in an extra overshoot in the channel of the bottom switch. Thus, even though the channel of the bottom switch is active to discharge the C_{OSS} of the bottom switch, only the top switch effect on the drain-source current is observed. One should note that the main characteristics observed in Model 1 are important to understand GaN behavior because even though these characteristics exist in complicated models, it might be hard to catch them with the presence of oscillations due to parasitic inductances and varying capacitances.

b) Model 2: The model with variable capacitances but without parasitic inductances

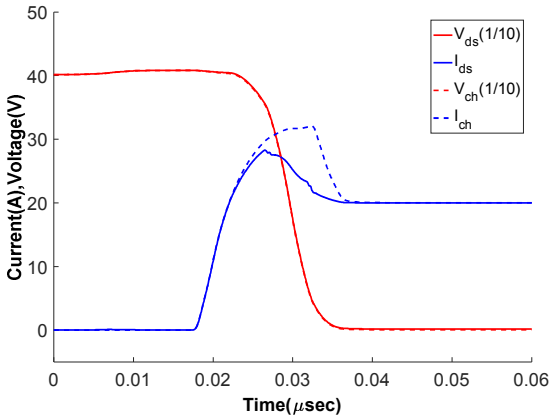
In this step, the capacitance values, which were kept constant previously, are treated as variable capacitances using the capacitance models presented in modeling section. As shown in Figure 3, the capacitances change with respect to the applied drain-source voltage and gate-source voltage. The turn-on and turn-off characteristics of the top and the bottom switches are obtained against time and can be seen in Fig. 6.



(a) Top switch turn-on (b) Top switch turn-off



(c) Bottom switch turn-off

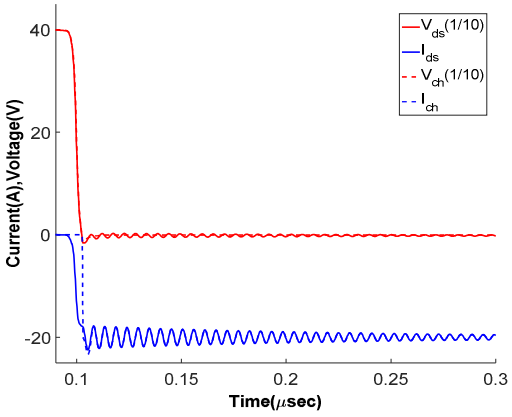


(d) Bottom switch turn-on

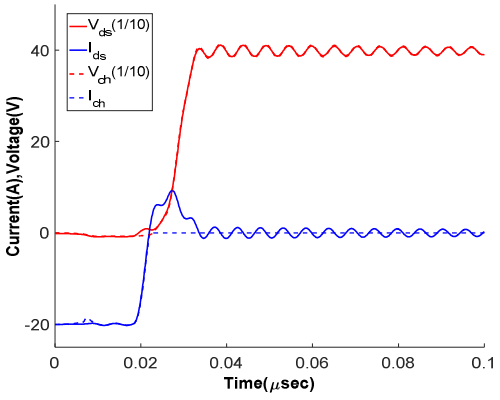
Fig. 6: Switching characteristics in time domain obtained using Model 2

In Model 2, again the drain-source voltage is directly equal to the channel voltage as expected. However, in this case, it is observed that the peak of the overshoot in the channel current and drain-source current of bottom switch increased because C_{OSS} is greater for lower drain-source voltages, which results in higher current flow under similar voltage change in time. Therefore, in order to estimate the overshoot amplitude correctly, the parasitic capacitances should be modeled properly. Moreover, for all transient periods given in Figure 6, it is observed that the voltage changes are smoother, which makes the model more realistic.

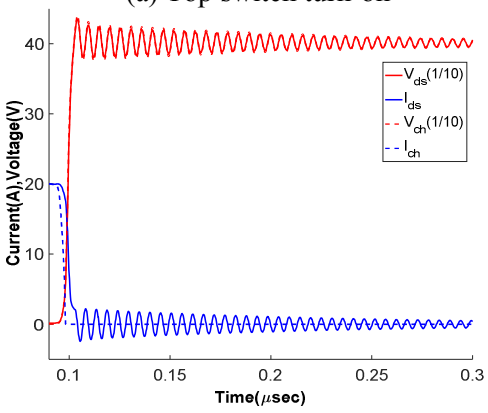
c) Model 3: The most comprehensive model with variable capacitances and with parasitic inductances



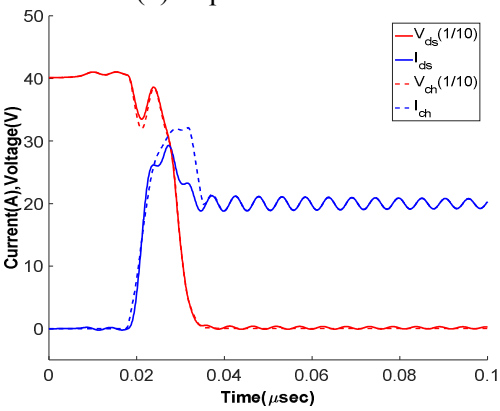
(a) Top switch turn-on



(b) Top switch turn-off



(c) Bottom switch turn-off



(d) Bottom switch turn-on

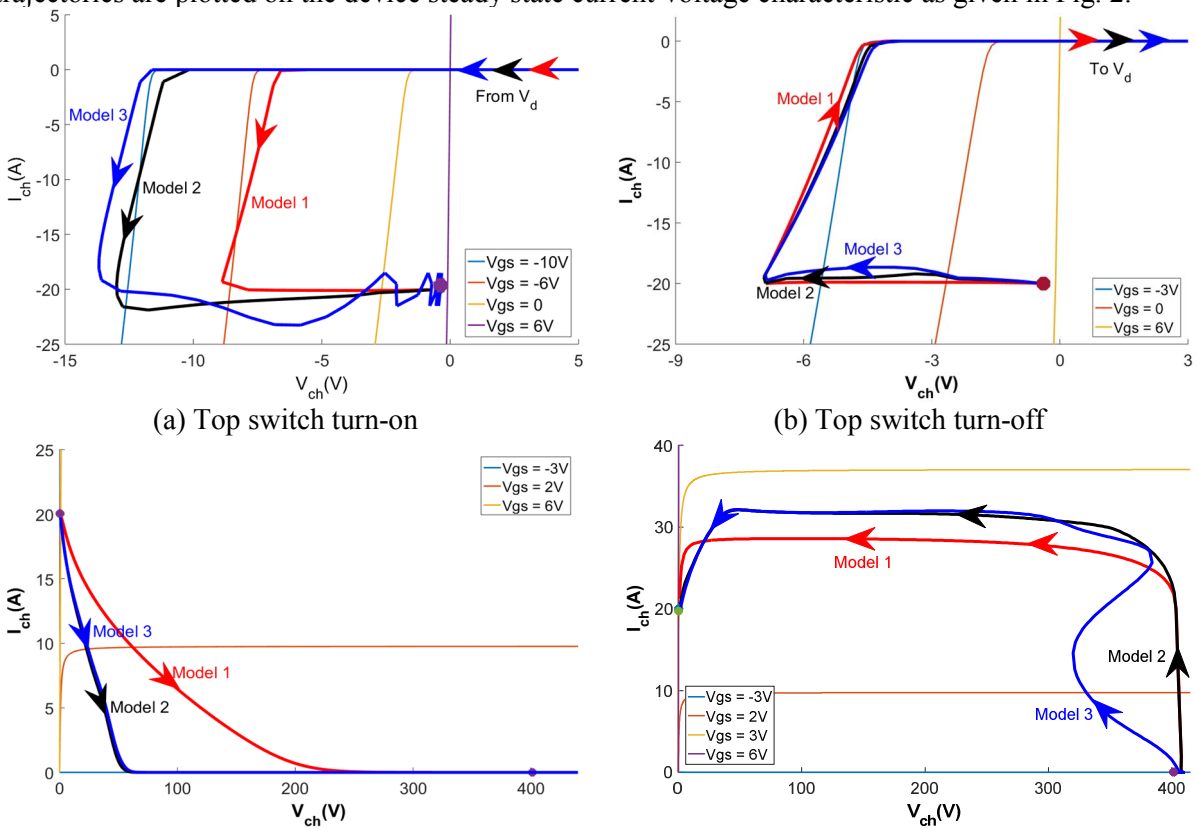
Fig. 7: Switching characteristics in time domain obtained using Model 3

Finally, to see the effect of the oscillations created by the LC resonance paths, the parasitic inductances are added to the model, which are caused by packaging, busbar, conducting parts on the DC side and Capacitor ESLs. In Model 3, in which all the parasitic effects are included, as shown in Fig. 7, the

oscillations started to emerge due to energy transfer between parasitic capacitances and inductors. In addition, a large dip is observed during the turn-on transient of bottom switch because since the current, which flows through the power loop, increases in time, a voltage is created on the loop inductance. Even though loop inductance is not related with the transistor type, due to fast switching capability of GaN FETs, the voltage drop increases relatively. Moreover, in Fig. 7, it is observed the oscillation damps in time. The damping duration of the oscillation is studied in [8] and it is shown that the damping duration is dependent on the C_{OSS}, loop inductance and drain/source parasitic inductances and trans-conductance. Since the increasing temperature reduces the trans-conductance, the oscillation damps faster as junction temperature gets higher as stated in [8].

d) State Trajectories

In order to show these transients better, the I_{ch}, V_{ch} paths, which the top and the bottom switches follow during turn-on and turn-off periods, are also obtained as state trajectories and given in Fig. 8. These trajectories are plotted on the device steady state current-voltage characteristic as given in Fig. 2.



(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off

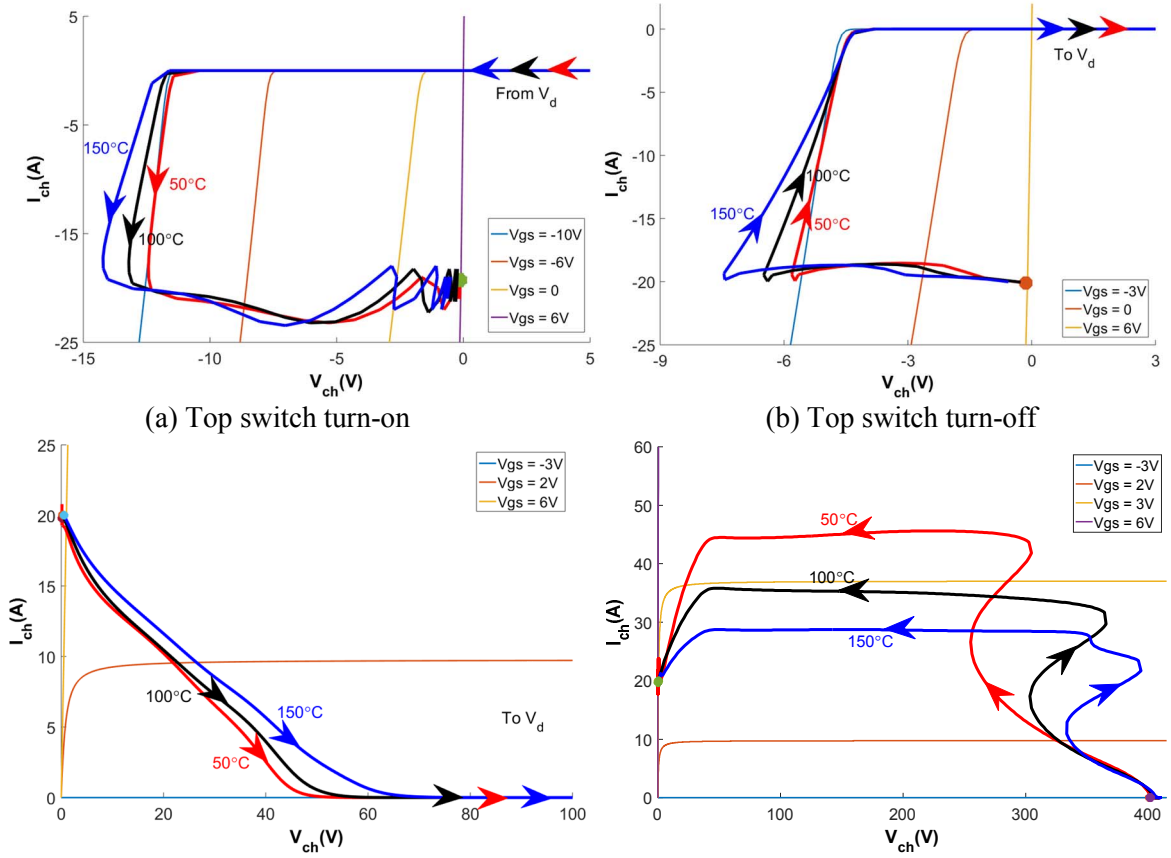
(d) Bottom switch turn-on

Fig. 8: Switching characteristics as state trajectories (obtained using all the models)

When we look at the trajectory for the turn-on period of the Bottom Switch, Fig. 8(d), it is easy to see the Miller Plateau where the voltage drops and current stays constant ideally. The importance of the using the Kelvin source pin can be deduced here. When the current changes, a voltage is created on the source parasitic inductance as described earlier. Therefore, if the Kelvin Source pin is not used, huge vertical oscillations would be observed on the state-trajectories due to the oscillations on gate-source voltage. However, now the channel seems very stable though the high di/dt ratio of the channel. Moreover, it is observed that the main channel behavior is in two directions; that is, in general, the channel state moves either horizontally or vertically. Horizontal movement of the channel state for the first quadrant, i.e. forward conduction, means the channel voltage changes while the gate-source voltage and channel current stays constant. However, vertical movement of the channel state in the first quadrant means the channel current and gate-source voltage varies while channel voltage stays constant. On the other hand, for the third quadrant, i.e. reverse conduction, when the channel state moves horizontally, the channel voltage and gate-source voltage change while the channel current do not vary. Conversely, vertical movement of the channel state means the channel current varies while the channel voltage and

gate-source voltage stay constant. The third quadrant behavior of the GaN FETs are unique because the channel is able to conduct in reverse direction with any gate-source voltage.

Furthermore, focusing on the trajectories given in Fig. 8(a), the channel state moves first vertically and then horizontally after conduction starts in channel. The conduction starts because the Bottom Switch is being turned off and dead time begins. Therefore, the channel is activated even though the gate-source voltage of the Top Switch is not changed yet. Then, changing the gate-source voltage from -3V to 6V do not affect the channel current but it only decreases the reverse conduction losses. In order to simplify the concept, the rise of the channel current can be called as **active turn-on** and increasing the gate-source voltage can be called as **passive turn-on** because it changes nothing for channel current but only decreases the losses. Similarly, in Fig. 8(b), the channel state first moves in horizontal direction and then it moves vertically before the current falls to zero. Due to the safety considerations, before firing the bottom switch, the top switch gate-source voltage should be decreased; however, the channel current of the top switch is not affected by the change in gate-source voltage. The channel current falls to zero when the bottom switch is fired and it starts conducting. Therefore, reducing the gate-source voltage can be called as **passive turn-off** and the fall in the current can be called as **active turn-off**. Even though this unique behavior of the GaN FETs is discussed in the literature, having these definitions make the concept more understandable. In IGBTs or MOSFETs, current flows through anti-parallel diode or body diode, respectively, during the reverse conduction. Therefore, the channel is not turned on or off. However, in GAN FETs, since body diode or anti-parallel diode does not exist, the reverse current flows through the device channel.



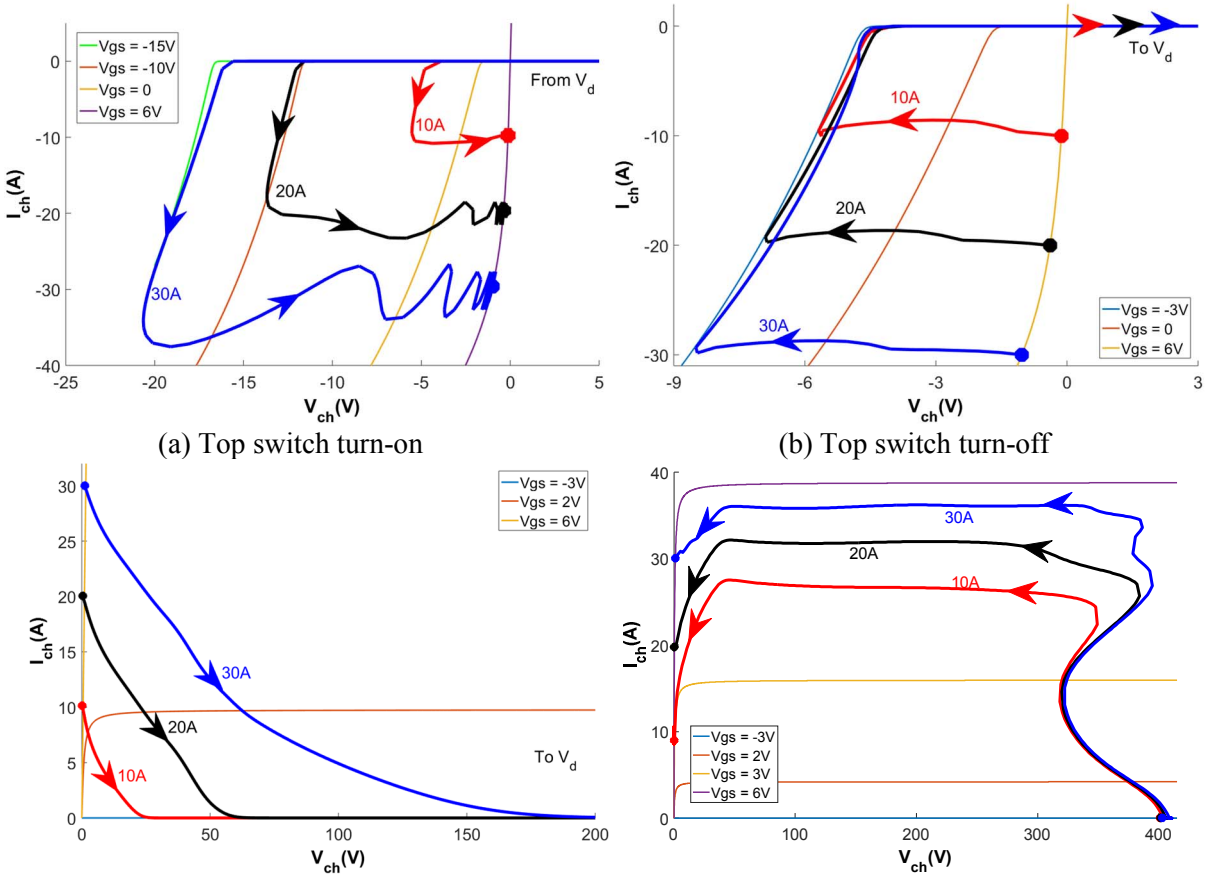
(a) Top switch turn-on (b) Top switch turn-off

(c) Bottom switch turn-off (d) Bottom switch turn-on

Fig. 9: Switching characteristics as state trajectories for different temperatures (Model 3)

In Fig. 9, the channel state trajectories are given for Model 3 at different junction temperatures. It is observed in (a), (b) and (c), the channel voltage and gate-source voltage are high in amplitude during transition at high junction temperatures due to the low trans-conductance. In Fig. 9(d), it is seen that the temperature increases the stability and reduces the current rise and voltage fall speed. A horizontal dip is observed due to the voltage created on the loop inductance when the current rises immediately. However, for the higher junction temperatures, the decrease in the voltage is small because of the

reduced switching speed of the GaN FET. Similarly, for the rest of transition, the channel current makes the maximum overshoot for the lowest junction temperature as expected for the same reason.

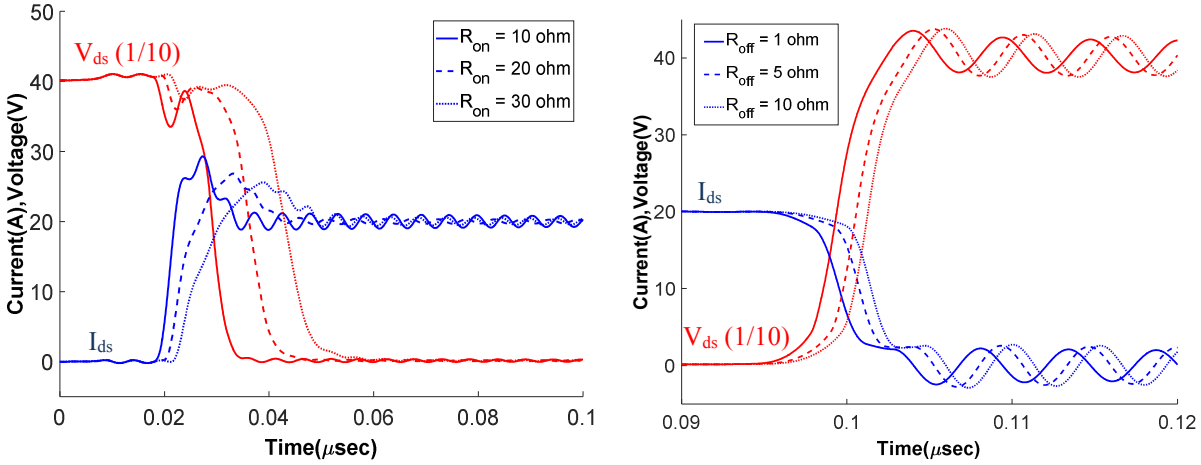


(a) Top switch turn-on (b) Top switch turn-off

(c) Bottom switch turn-off (d) Bottom switch turn-on

Fig. 10: Switching characteristics as state trajectories for different load currents (Model 3)

In Fig. 10, it is observed that the gate-source voltage is significantly affected by the channel current during the transition. In (a), it is seen that the gate-source voltage decreases dramatically in transient period for high channel current because when the load current commutes from bottom switch to top switch the load current discharges the gate-source capacitance instantaneously so as to reach the right conduction state before the gate-source voltage is set to high. In addition, as shown in (d), the channel voltage drops equally for all current ratings as expected because the load current does not change the GaN FETs transition speed.



(a) Turn-on (b) Turn-off

Fig. 11: Switching characteristics for different turn-on and turn-off resistances (Model 3)

Lastly, the effect of the turn-on and turn-off resistances are investigated as given in Fig. 11. The turn-on and turn-off speed of the GaN FET is related with how fast the gate-source capacitance is being charged or discharged. With low gate driver resistances, the gate-source voltage changes rapidly. Therefore, as resistances get higher, the switching speed decreases, so the transition takes longer. In addition, due to the reduced switching speed, the voltage drop caused by the loop inductance decreases for high gate driver resistances but the switching losses are increased as well.

Conclusions

In this paper, turn-on and turn-off characteristics of GaN devices are investigated gradually including different parasitic effects. Understanding the effect of the parasitics on turn-on and turn-off characteristics of GaN is important to understand GaN behavior and operating safely. For this purpose, a GaN device is modeled and the model is verified by comparing simulation results with datasheet results. Then, the channel current and channel voltage, which represent device characteristics better, are investigated on a double pulse test circuit using accurately modeled GaN device. The simulation results belonging to channel current and voltage waveforms are presented as state-trajectories on the steady state $I_{ds} - V_{ds}$ graph to discuss characteristics better. Moreover, in order to emphasize and express the unique conduction characteristics of GaN better, important definitions, active/passive turn-on/off, are explained.

Furthermore, the effects of the temperature on the channel trans-conductance and oscillations are studied on state-trajectory plots. It is shown that increasing operation temperature reduces trans-conductance significantly, so the overshoots and damping time of oscillation are decreased for high junction temperature of the device. Additionally, the state-trajectories are shared for different load ratings and it is shown that the transient gate-source voltage is affected by the current whereas the switching speed is not changed as expected. Lastly, the channel voltage and channel current transition are given on time axis for different turn-on and turn-off resistances. High gate-driver resistances make the switching period longer, so since the current changes slowly, the overshoots in current and voltage drops decrease.

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