Modeling of SiC MOSFET in Matlab/Simulink

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***Abstract*- New power semiconductor devices, such as SiC MOSFET, have widely fascinated people in recent years. They are playing more and more important roles in modern power electronic converters. Most of current SiC MOSFET models are implemented in simple simulator, such as PSPICE, and have problems in some applications, for example, the accuracy of these models can not satisfy the demand with the increasing of main circuit complexity. A novel model of SiC MOSFET implemented in Matlab/Simulink is proposed in this paper, where its physical mechanism of the device is considered. Firstly the model is established based on its static and transient characteristics. Then the parameters in the model are extracted. And finally simulation and experiment results are compared to validate the model.**

Keywords: **SiC devices, modeling, Matlab/Simulink.**

I. INTRODUCTION

Silicon power[1][1] semiconductor devices have been widely used in power electronic converters. The performances of silicon-based devices has been improving over the last century. However, as the current technology is reaching the theoretical limits of silicon, new semiconductor devices such as silicon carbide (SiC) are being increasingly fascinating to researchers. One of those devices that has been used in industry is SiC MOSFET. More and more studies have been conducted on SiC MOSFET models A classical SiC MOSFET model was raised in [1], as is shown in fig.1. This model is a scripture in simulation of SiC MOSFET and is widely used. Some effective improvements are proposed in [2]. However, the existing models are mostly implemented in PSPICE and have usability problems in some cases, as mentioned in [3]. Those problems can be well solved in Matlab/Simulink. So a novel MOSFET model in Matlab/Simulink should be researched. This paper proposes a model for the commercial SiC MOSFET CMF20120D(1200 V/33 A) from CREE and simulation results are achieved via Matlab/Simulink. Firstly the model is established based on its static and transient characteristics. Then the parameters in the model are extracted. Finally both the simulation and the experiment results are compared to validate the model.

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II. MODEL STRUCTURE

A picture of CMF20120D CREE MOSFET and its internal structure are given in Fig 2. The device has three terminals, gate, drain and source. There's a highly doped *N*+ region between the drain and the source so that more carriers can be provided. Also the vertical structure is used so that a higher current can be achieved in on-state, as mentioned in [4, 5].

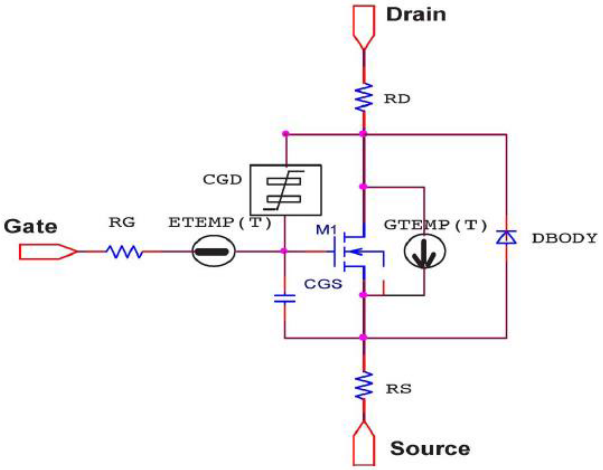


Fig. 1. A classical SiC MOSFET model

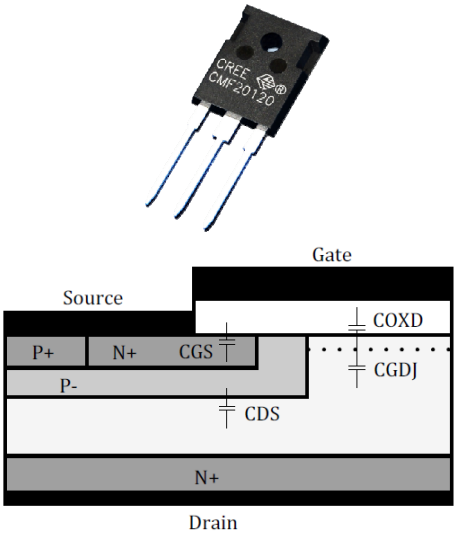


Fig. 2. Commercial SiC MOSFET and its internal structure

References [6, 7] demonstrate the turn-on principle of a MOSFET. When V_{ds} is positive and V_{gs} goes up gradually, the MOSFET experiences 3 stages before it is on.

Stage (1): when V_{gs} just begins to rise, holes below the silicon dioxide layer are pushed off by the electric field generated by V_{gs} and result in a depletion layer.

Stage (2): V_{gs} keep rising, the depletion layer turns to inversion layer, which means the carriers in this region are electronics but not holes in the previous. But there are too few of them to form a circuit.

State (3): V_{gs} rises to a voltage that is higher than the turn-on voltage(V_T) and the number of electronics in the inversion layer is big enough to form a circuit from drain to source, or I_d. Channel emerges in the P semiconductor below the insulation layer. The higher V_{gs} is, the wider the channel is and the better its conductivity is.

In a SiC MOSFET, the PN junction is charged under a reverse voltage and can be equivalent to a capacitance. The barrier capacitance effect is the charging effect caused by the change of width of space-charge region when the voltage over PN junction changes. The change of voltage over PN junction causes movement of majority carrier in both N region and P region, which is equivalent to a charging process to a capacitance at the PN junction. The barrier capacitance parameters are related to the frequency and amplitude of the external voltage; The diffusion capacitance effect is caused by the time delay of electronic mobility. When PN junction is offset positively, electronics enter N region from P region to combine with the holes. But the combinations couldn't complete immediately, for the electronics need to diffuse in P region, which causes accumulation of electronics in the diffusion region. Obviously the accumulation is related with the circuit through the junction. The larger the circuit is, the more electronics are accumulated. This process is also like a charging process in a capacitance, so it is defined as diffusion capacitance. These parasitics capacitances have obvious impact on transient performance. References [8-10] state the impact specifically.

Based on the principles above, static and transient models are established.

The static model describes the U-I characteristics in on-state. On-state current is determined by Vgs as well as Vds . The model is built up via Matlab/Simulink by solving on-state function in a S-function. V_{gs} and V_{ds} are the inputs of the function. Then the calculation result is delivered to a VCCS, where a current signal is produced. This process is shown in Fig 3.

Then gate driver, stray inductance, base resistance and parasitics capacitances are added to the external circuit of the static model to establish a transient model, as depicted in Fig 4.

In this model, C_{gd}, C_{gs} and C_{ds} are respectively gate-to-drain, gate-to-source and drain-to-source capacitances respectively. L_d is the stray inductance inside the device, while R_{ds} is the stray resistance of the base.

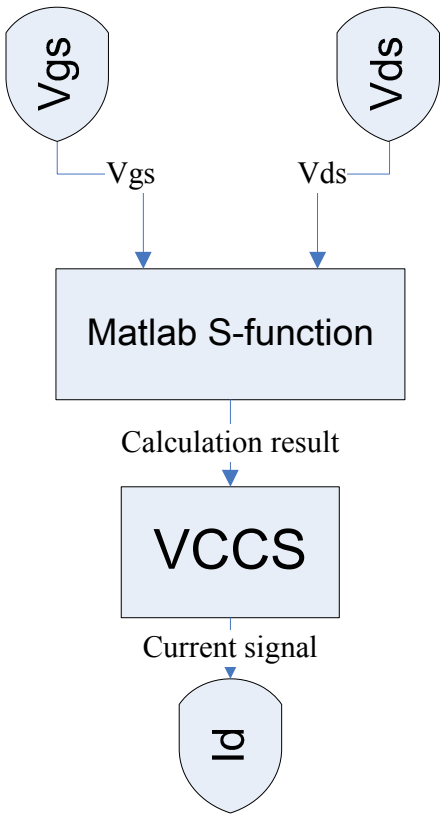


Fig. 3. Static model process

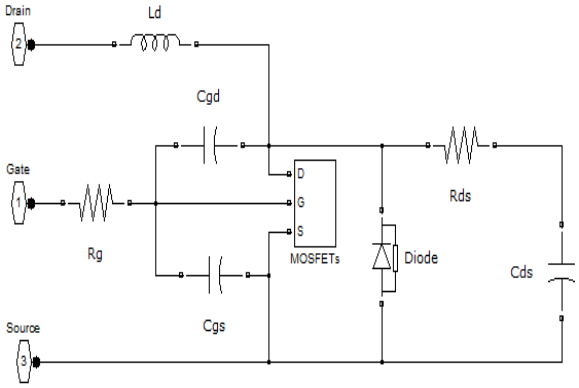


Fig. 4. Transient model of SiC MOSFET

III. PARAMETER EXTRACTION

In the formal section, the SiC MOSFET model based on Matlab/Simulink has been attained. In this section, the parameters in the model are extracted.

In the static model, output current I_d is described as the formula below, mentioned in [11].

$$I_D = \begin{cases} 0, U_{GS} < U_T \\ K_p(U_{GS} - U_T - U_{DS}/2)U_{DS}, U_{GS} \geq U_T, U_{DS} < U_{GS} - U_T \\ K_p(U_{GS} - U_T)^2/2, U_{GS} \geq U_T, U_{DS} \geq U_{GS} - U_T \end{cases}$$

The static model describes the U-I characteristics when MOSFET is in static state. The output I is determined by V_{gs} as well as V_P, as described in the formul. U_T and K_P are given parameters in the model. Using the least square method to extract them.

In this model, U_T=2.122V, K_P =0.745.

The parameters in the transient model are also extracted, listed in Table1.

Table. 1. Parameters in the transient model

Parameter	Symbol	Unit	Value
External stray inductance	L_s	nH	90
External stray resistance	R_s	Ω	3
Resistance of diode	R_{diode}	Ω	0.2
Parasitic capacitance of diode	C_{diode}	pF	70
Gate-to-source capacitance	C_{gs}	pF	1902
Drain-to-source capacitance	C_{ds}	pF	40
Gate-to-drain capacitance	C_{gd}	pF	70
Internal inductance of the device	L_d	nH	20

It is crucial for the validity of the model that the parameters in the circuit are reasonably decided. In this paper, those parameters are decided by the following principles:

i. External stray inductance L_s :

For an inductance, it is known that its voltage and current can be described by

$$\Delta V = L_s \frac{di}{dt}$$

According to this law, the experimental di⁄dt is firstly abstracted, secondly the experimental ΔV is obtained. Finally L_s is estimated with the two parameters. In this paper, L_s =70mH.

ii. Oscillation resistance R_s and on-resistance of diode R_{diode}

These two parameters can be estimated by the number the waveform oscillate in a single switch and the oscillation time. In this paper, R_s =3Ω, R_{diode} =0.2Ω.

iii. Capacitance inside diode, C_{diode}

According to [12], the frequency of oscillation in a single switch is determined by

$$2\pi f = \frac{1}{\sqrt{LC}}$$

Therefore C_{diode} can be estimated using the experimental oscillation frequency and the estimated L_s. In this paper C_{diode} =70pF .

iv. C_{ds}, C_{gs} and C_{gd}

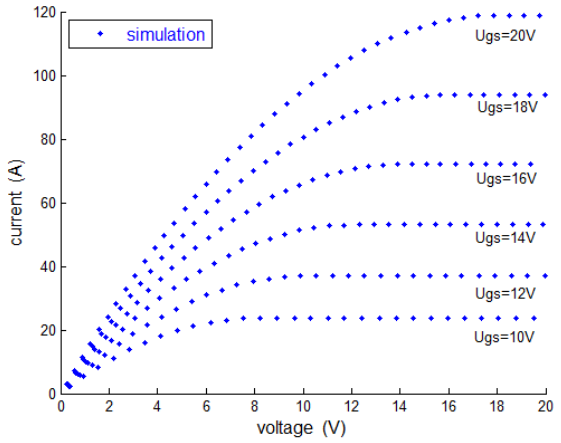
Those capacitance parameters inside the SiC MOSFET could be obtained from the datasheet. In this paper, C_{ds} =40pF, C_{gs} =1902pF , C_{gd} =70pF .

v. Internal inductance L_s

This parameter can be estimated from the overshoot of the voltage waveforms in the progress of switching on and off. In this paper, L_s =20mH.

IV. SIMULATION AND EXPERIMENT RESULTS

Firstly the on-state characteristics of the SiC MOSFET are tested using a SONY 371A instrument. The U-I curves are drawn and compared with the simulation results. Fig 5 a) shows the test curves of the commercial SiC MOSFET CMF20120D（1200 V/33 A）from CREE. It can be seen that the function in the formula mentioned above fits the experiment static characteristics well.



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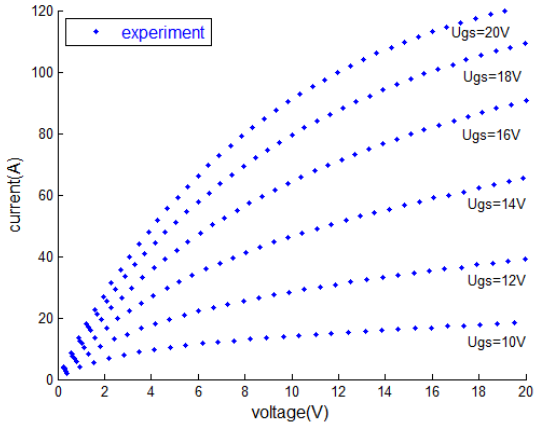
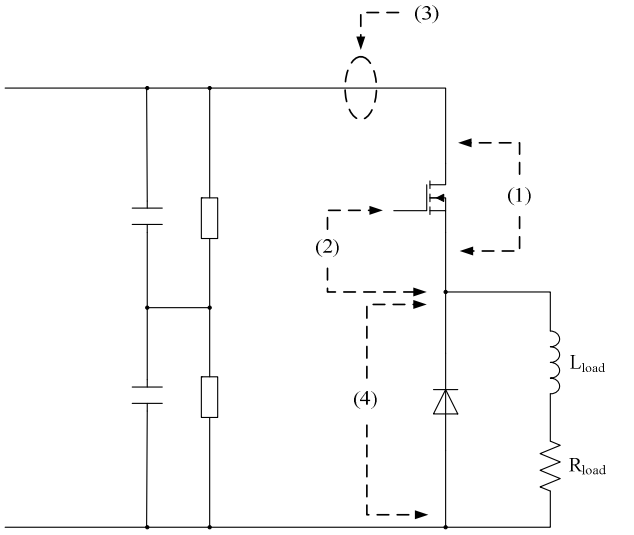


b)

Fig. 5. Comparison of simulation and experiment results of V-A characteristic

Then a test circuit is designed to validate the established model, as shown in Fig 6. Four waveforms are observed as indicated by the numbers in the circuit, namely V_{ds} , V_{gs} , I_d and V_{load} .



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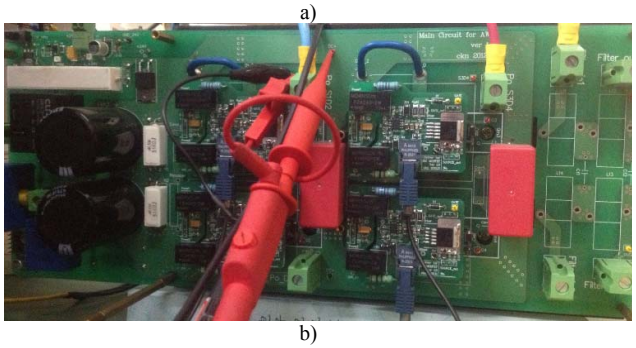


b)

Fig. 6. Test circuit of the established model (a: equivalent circuit b: PCB)

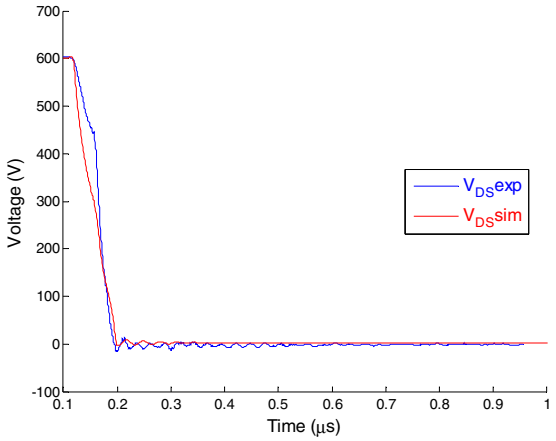
The parameters in the test circuit are given in table2.

Table. 2. Parameters in the test circuit

Name of the parameters	**Numerical value or detailed information**
SiC MOSFET	CMF20120D
SiC SBD	C4D30120D
L_{load}	1.296mH
R_{load}	1Ω，100W
Internal resistance of L_{load}	0.93Ω

Also, simulation results are obtained at a bus voltage of 600V and a load current of 20A. The simulation and the experiment are compared in Fig. 7 and Fig. 8.

It can be seen that the simulation waveforms are very similar to the experimental waveforms, in peak voltage, peak current, rise/fall time and the oscillation. It concludes that the established model has a good performance.



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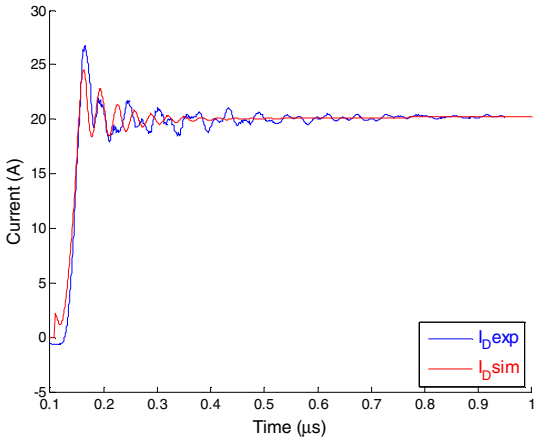

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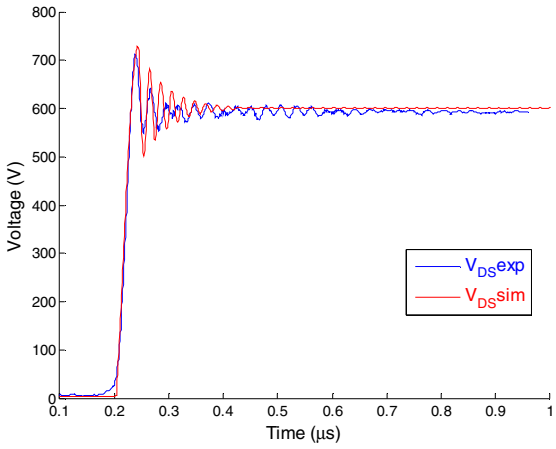
Fig. 7. Turn-on waveforms (a: voltage waveform b: current waveform)



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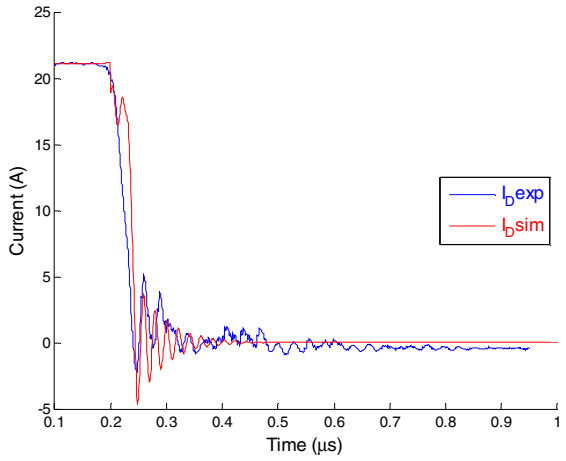

b)

Fig. 8. Turn-off waveforms (a: voltage waveform b: current waveform)

V. CONCLUSIONS

As the existing models for SiC MOSFET are mostly in PSPICE and have problems in some applications, this paper presents a model for the high-voltage SiC MOSFET in Matlab/Simulink. To validate the model, a buck circuit is designed and the transient experiment results of the SiC MOSFET are obtained. The comparison results show that the established model can well describe the performance of the SiC MOSFET in its dynamic transient.

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