An Analytical Model for False Turn-On Evaluation of High-Voltage Enhancement-Mode GaN Transistor in Bridge-Leg Configuration

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***Abstract*—Compared with the state-of-the-art Si-based power devices, enhancement-mode Gallium Nitride (E-mode GaN) transistors have better figures of merit and exhibit great potential in enabling higher switching frequency, higher efficiency, and higher power density for power converters. The bridge-leg configuration circuit, consisting of a controlling switch and a synchronous switch, is a critical component in many power converters. However, owing to the low threshold voltage and fast switching speed, E-mode GaN devices are more prone to false turn-on phenomenon in bridge-leg configuration, leading to undesirable results, such as higher switching loss, circuit oscillation, and shoot through. In order to expand gate terminal's safe operating margin without increasing reverse conduction loss during deadtime, negative gate voltage bias for turn-off and antiparallel diode could be applied to E-mode GaN device. In this paper, with consideration of strong nonlinearities in *C–V* and *I–V* characteristics of high-voltage (650 V) E-mode GaN transistors, analytical device models are first developed. Then, we develop an analytical circuit model that combines the circuit parameters with intrinsic characteristics of the high-voltage GaN transistor and antiparallel diode. Thus, key transient waveforms with regard to the false turn-on problem can be acquired, including displacement current and false triggering voltage pulse on gate terminal. The simulated waveforms are then verified on a testing board with GaN-based bridge-leg circuit. In contrast to piecewise switching process models and PSpice simulation, the proposed model exhibits outstanding performances. To provide design guidelines for mitigating false turn-on of GaN transistor, the impacts of different circuit parameters, along with the optimum negative gate voltage bias, are investigated based on the proposed model.**

***Index Terms*—Bridge-leg configuration, false turn-on, gate drive design consideration, high-voltage enhancement-mode Gallium Nitride (E-mode GaN) transistor.**

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I. Introduction

NEXT-generation power electronic converters are expected to deliver high power density and high conversion efficiency, and heavily rely on the advancement of power semiconductor device technology [1]. After several decades of intensive development, the mainstream Si power devices are close to their fundamental material limits. Further performance enhancement in power converters requires adoption of wide bandgap semiconductors (SiC, GaN, diamond, etc.) with superior material properties. Among the wide bandgap power devices, the GaN-on-Si lateral heterojunction power devices are emerging as a competitive candidate since they can be manufactured on low-cost and large-size Si substrates using existing Si process lines [2]–[6]. In particular, high-performance enhancement-mode Gallium Nitride (E-mode GaN) transistors are commercially available for single-chip solution [7]–[9].

GaN power devices can be adopted in bridge-leg or phase-leg configuration [formed by a controlling switch (CtrlSW) and a synchronous switch (SyncSW)] that is commonly used in various power converters, including synchronous buck converter, synchronous boost converter, single-phase inverter, etc., [10]. However, during the turn-on process of CtrlSW under high-speed switching, the bridge-leg circuit suffers from false triggering pulses at the gate of SyncSW. When the false triggering voltage exceeds the threshold voltage $V_{\rm th}$ of SyncSW, a false turn-on of SyncSW will takes place [11]. The false turn-on problem in Si-based bridge-leg configuration has been analyzed in details [12]–[22]. During the deadtime, both CtrlSW and SyncSW are in OFF state, and the antiparallel diode or the body diode of SyncSW conducts the load current. With CtrlSW being turned ON, the load current will be gradually transferred from the freewheeling diode to CtrlSW. After CtrlSW takes all the load current and the freewheeling diode is turned OFF, the consequent rise in drain-to-source voltage of SyncSW will induce a displacement current that charges up the gate–drain capacitance of SyncSW, resulting in a false triggering pulse at the gate terminal. The impact of gate resistance on false triggering pulse is studied in [12]. As described in [13] and [14], the common source inductance shared by the power loop and the gate drive loop can worsen the false turn-on problem because of the voltage drop on this inductance, which is induced by the fast-changing displacement current in the power loop. In [18],

the reverse recovery current of the body diode is regarded as another factor that enlarges false triggering voltage pulse.

Compared with Si-based power devices, E-mode GaN transistors feature significantly smaller input capacitance $C_{\rm iss}$ [23], [24]. As a result, in a GaN-based bridge-leg, the fast switching speed of the CtrlSW along with the small gate-to-source capacitance $C_{\rm gs}$ of the SyncSW could possibly cause a higher false triggering voltage. On the other hand, the small $C_{\rm iss}$ of the SyncSW could lead the gate-loop's resonance frequency to a value near the ringing frequency of the displacement current, inducing resonance oscillation. Thus, the impacts of circuit parameters on false turn-on of the GaN transistor could be more complicated. Besides, the strong nonlinearities in capacitance–voltage (*C–V*) and current–voltage (*I–V*) characteristics of the high-voltage GaN device could also lead to different switching transient waveforms from those of Si devices. As the commercially available E-mode GaN transistors feature lower threshold voltage (0.7–1.6 V) [23], [25], the GaN transistor is more sensitive to the circuit parameters and more prone to the false turn-on problem. In addition, since GaN power transistors exhibit inherent reverse conduction capability without body diode in its structure, the reverse recovery charge is of less concern.

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Although there exist noticeable differences between the false turn-on problems in Si-based and GaN-based bridge-leg configurations, limited discussions can be found in the literature. For the purpose of false turn-on evaluation and design optimization, an analytical model that takes into account the nonlinear behaviors of high-voltage GaN device as well as the circuit elements is highly desirable. In previous works, piecewise switching process model and PSpice simulation are the most commonly used approaches for switching behavior or false turn-on analysis [18], [26], [27]. With regard to piecewise analysis, the oversimplification of device characteristics along with the discontinuities among different intervals could lead to less accurate transient waveforms. Although the PSpice simulation makes improvement in device modeling and employs continuous circuit simulation, the accuracies of *I–V* characteristics under various temperatures and $C-V_{\rm ds}$ (drain-to-source voltage) curves are unsatisfactory. As the internal gate inductance and resistance inside device package could intensify the false triggering voltage [18], it is difficult to monitor the actual false triggering voltage inside device package by PSpice simulation.

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Moreover, the relationship between GaN transistor's input capacitance $C_{\rm iss}$ and gate-to-source voltage $V_{\rm gs}$ could significantly affect the $V_{\rm gs}$ waveform of CtrlSW [18], and consequently influences SyncSW's displacement current and false triggering voltage. However, neither the piecewise process model nor the PSpice simulation has fully taken this factor into account. As a consequence, there always exist remarkable distinctions between the simulation and experimental results. Since the false turn-on of GaN transistor could be affected by the resonance between SyncSW's gate loop and displacement current, it is difficult for the models with less accurate displacement current to achieve good performances in evaluating false turn-on and providing guidelines for circuit optimization.

In this paper, an analytical model is proposed that can accurately simulate the switching transient waveforms with regard to the false turn-on problem. In Section II, hyperbolic-tangent-function-based analytical device models are first established that are robust and perform well in representing GaN transistor's nonlinear *I–V* and *C–V* characteristics. Then, a continuous circuit-level model is built to simulate the displacement current and the false triggering voltage of SyncSW. In Section III, simulation results obtained from the proposed device/circuit model are verified with measurement from circuit implementation and compared with other models' results. Good agreement between measured and simulated waveforms validates the analytical model. In Section IV, the impacts of various circuit elements and their mechanisms, along with the optimization of the negative gate bias for turn-off, are investigated to provide design guidelines for false turn-on mitigation. Section V concludes the paper.

II. Modeling for the False Turn-On Voltage

In this paper, a negative gate–source voltage bias is applied on the GaN transistor for turn-off, the purposes of which are as follows. First, unlike the method that suppresses the false turn-on problem by compromising the device switching speed and increasing switching loss, adding negative gate voltage bias can expand gate terminal's safe operating margin and consequently retains high switching speed of the GaN transistor. Larger safe operating margin of gate–source voltage could also prevent the device from being damaged. Second, the usage of negative gate voltage bias can widen the selection ranges of circuit parameters. Thus, more information could be obtained about the impacts of various circuit elements on the false turn-on problem. Third, as there exists a negative gate voltage limit in the high-voltage E-mode GaN transistor (around –10 V), it is essential to investigate the optimum value of the negative gate voltage bias.

According to the reverse conduction characteristics of the E-mode GaN transistor, the reverse conduction voltage would be increased by a negative gate voltage bias [29], leading to higher conduction loss during deadtime. Such a problem can be solved by shorting out the reverse conducting GaN transistor with an antiparallel Schottky barrier diode (SBD). Although the common source inductance shared by the gate loop and power loop could cause severe false turn-on problem to Si device, it can be intentionally decoupled or eliminated in the GaN transistor. For instance, laying a packaged (e.g., TO-220) GaN transistor flat on printed circuit board (PCB) could largely decouple the gate drive loop from the power loop [10], [29], while using an optimized device package with kelvin connection can remove the common source inductance [30]. Besides, adding external gate–source capacitance is another efficient approach to damp fluctuation on gate–source voltage [31], [32]. Thus, the study object of this paper is a bridge-leg circuit, formed by high-voltage E-mode GaN transistors free of common source inductance and antiparallel SBDs, with negative gate voltage bias and intentionally added external gate–source capacitances. By investigating into this object, the impacts of various circuit elements on false turn-on can be evaluated, and the approaches for mitigating the problem can be developed.

The schematic diagram of the study object is illustrated in Fig. 1, where the high-side switch $\rm SW_1$ is CtrlSW and the low-side switch $\rm SW_2$ is SyncSW, both of which are assigned

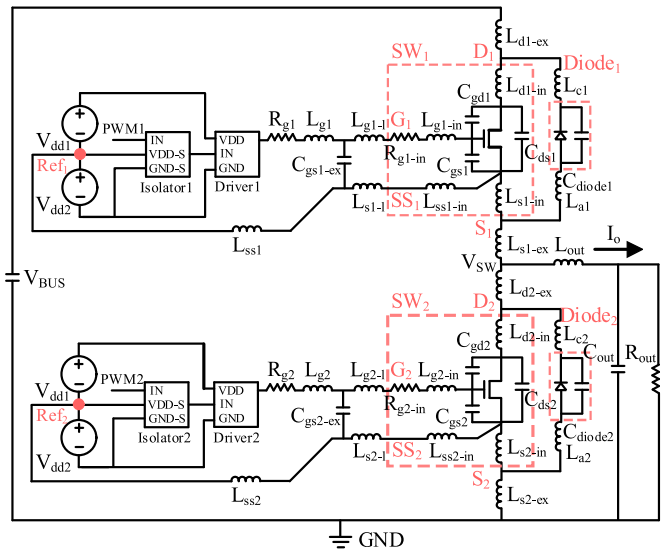

Fig. 1. Schematic diagram of GaN-based bridge-leg configuration.

TABLE I
DEFINITIONS OF CIRCUIT PARAMETERS IN GAN-BASED BRIDGE-LEG CONFIGURATION

Input voltage	V_{BUS}	Positive gate supply	V_{dd1}
Negative gate supply	V_{dd2}	Drain external	$L_{\mathrm{dk-ex}}$
Source external ind.	$L_{\mathrm{sk-ex}}$	Drain internal ind.	$L_{\mathrm{dk-in}}$
Source internal ind.	$L_{\mathrm{sk-in}}$	Gate resistance	R_{gk}
Gate driver resistance	R_{drk}	Gate internal resistance	$R_{\mathrm{gk-in}}$
SS internal ind.	$L_{\mathrm{ssk-in}}$	Gate internal ind.	$L_{\mathrm{gk-in}}$
Gate lead ind.	$L_{\mathrm{gk}-l}$	Source lead ind.	$L_{\mathrm{sk}-l}$
External gate–source cap.	$C_{\mathrm{gsk-ex}}$	Diode anode ind.	L_{ak}
Diode cathode ind.	L_{ck}	Gate ind.	L_{gk}
SS ind.	L_{ssk}	Diode cap.	$C_{\mathrm{diode}k}$
Intrinsic gate–source cap.	C_{gsk}	Intrinsic gate-drain cap.	C_{gdk}
Intrinsic drain–source cap.	C_{dsk}	Output Filter	L/C_{out}

Remarks: "ind." denotes inductance; "cap." denotes capacitance;"k" denotes different switches ($k = 1$ for CtrlSW and $k = 2$ for SyncSW).

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2 notes:

according to the direction of load current. The antiparallel diode of SW_2 conducts the load current during deadtime. The isolation between the gate drive circuit and the high-side switch is realized by transmitting the input signal through a digital isolator and employing an isolated power supply for the gate drive circuit. Ref_1 and Ref_2 in Fig. 1 represent the voltage reference points of the positive and negative isolated gate voltage supplies. The source-sense (SS) terminal is designed by the device manufacturer as a connector to the gate driver to achieve kelvin connection.

Definitions of circuit parameters are given in Table I, where subscript $k = 1$ or 2 identifies different transistors and diodes. Internal parameters indicate parameters inside device package, while external parameters represent circuit elements of PCB. Source-sense inductance L_{ss} includes the stray inductance between the driver chip and gate voltage supply, as well as the parasitic inductance between the *SS* terminal and *Ref* point. Lead inductance is the sum of the device lead inductance and the stray inductance between $C_{\mathrm{gs-ex}}$ and device.

In order to evaluate the false turn-on of the study object, the nonlinear *I–V* and *C–V* characteristics of high-voltage E-mode GaN transistor, along with the behavior of antiparallel SBD, are first modeled. Then, a circuit-level model is established, which combines device nonlinear behaviors with circuit parameters. By employing the iterative algorithm, the critical transient waveforms, such as displacement currents and false triggering voltage, can be accurately simulated.

A. Modeling for High-Voltage E-Mode GaN Transistor and Antiparallel SBD

With regard to the switching transient simulation, the device modeling should be mainly focused on the nonlinear *I–V* and *C–V* characteristics [27]. The device modeling methods of the PSpice simulation [33] and the latest piecewise switching process models (Mode A for Si MOSFET [18] and Model B for low-voltage GaN transistor [27]) are summarized in Table II. The *I–V* characteristics of piecewise switching process models are expressed by the product of a constant/variable transconductance g_m and the difference between gate–source voltage and threshold voltage ($V_{\mathrm{gs}} - V_{\mathrm{th}}$). Such a method, however, ignores the linear region current as well as the transition zone between the linear and saturation region, and performs poorly in representing GaN transistor's nonlinear behavior (i.e., the bias dependence) in saturation region. Although PSpice device model takes the linear region into account, the features of saturation region and transition zone cannot be accurately reflected. Besides, neither of the two models could fully consider the temperature dependence of the *I–V* curves.

Since the *I–V* characteristics of GaN transistor largely determine the channel current of CtrlSW, the displacement current and false triggering voltage of SyncSW could not be well simulated without accurate *I–V* model. In order to accurately represent the *I–V* characteristics of a GaN transistor, (1) is established. The underlying principle is to make corrections to the *I–V* equations of Si devi... The correction functions F_1 to F_4 are expressed in (2)–(5). The polynomial function F_1 and exponential function F_2 are designed to adjust the saturation region current in small and large scale, respectively. Due to the limited effects of F_1 and F_2 on linear region, a Gaussian distribution function F_3 that only works under small V_{ds} is introduced. To further enhance the precision in the transition zone, an inverse trigonometric function F_4 with small amplitude is employed

$$\begin{cases} \text{if} \quad V_{\mathrm{ds}} < (V_{\mathrm{gs}} - V_{\mathrm{th}}) \text{ and } V_{\mathrm{gs}} \geq V_{\mathrm{th}} \\ \quad I_{\mathrm{ch}} = \beta V_{\mathrm{ds}}[2(V_{\mathrm{gs}} - V_{\mathrm{th}}) - V_{\mathrm{ds}}](1 + \lambda V_{\mathrm{ds}}) F_1(V_{\mathrm{gs}}) \\ \quad F_2(V_{\mathrm{gs}}) F_3(V_{\mathrm{ds}}) F_4(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \\ \text{if} \quad V_{\mathrm{ds}} \geq (V_{\mathrm{gs}} - V_{\mathrm{th}}) \text{ and } V_{\mathrm{gs}} \geq V_{\mathrm{th}} \\ \quad I_{\mathrm{ch}} = \beta (V_{\mathrm{gs}} - V_{\mathrm{th}})^2 (1 + \lambda V_{\mathrm{ds}}) F_1(V_{\mathrm{gs}}) F_2(V_{\mathrm{gs}}) \\ \quad F_3(V_{\mathrm{ds}}) F_4(V_{\mathrm{gs}}, V_{\mathrm{ds}}) \\ \text{if} \quad V_{\mathrm{gs}} < V_{\mathrm{th}} \\ \quad I_{\mathrm{ch}} = 0 \end{cases} \tag{1}$$

$$F_1(V_{\mathrm{gs}}) = \frac{1 + M_1 V_{\mathrm{gs}} + M_2 {V_{\mathrm{gs}}}^2 + M_3 {V_{\mathrm{gs}}}^3 + M_4 {V_{\mathrm{gs}}}^4}{1 + M_5 V_{\mathrm{gs}} + M_6 {V_{\mathrm{gs}}}^2 + M_7 {V_{\mathrm{gs}}}^3 + M_8 {V_{\mathrm{gs}}}^4} \tag{2}$$

$$F_2(V_{\mathrm{gs}}) = M_9 \max\left[M_{10} - M_{11} \exp(-M_{12} V_{\mathrm{gs}}), 0\right] \tag{3}$$

TABLE II
COMPARISON AMONG DEVICE MODELING OF DIFFERENT MODELS

Models	*I-V* Characteristics				*C-V* Characteristics	
	Linear Region	Transition Zone	Saturation Region	Temperature Dependence	$C_{oss}/C_{iss}/C_{rss}$ versus V_{ds}	C_{iss} versus V_{gs}
Model A	/	/	Not Accurate	/	/	/
Model B	/	/	Not Accurate	/	Not Accurate	/
PSpice Model	Accurate	Not Accurate	Not Accurate	Not Accurate	Not Accurate	Not Accurate
Proposed Model	Accurate	Accurate	Accurate	Accurate	Accurate	Accurate

Remark: "/" denotes that the aspect is not taken into account in the model.

$$F_3(V_{ds}) = 1 - M_{13}\exp\left[-\frac{(V_{ds}-M_{14})^2}{2{M_{15}}^2}\right] \quad (4)$$

$$F_4(V_{gs},V_{ds}) = M_{16}\left[\frac{-\arctan(M_{17}(V_{gs}-V_{ds}))+\pi/2}{\pi}\right]+M_{18} \quad (5)$$

where β, λ, and M_1–M_{18} are constants.

The influences of temperature on *I–V* characteristics could be expressed by multiplying the *I–V* equations by a temperature coefficient α_T, which is denoted as

$$\alpha_T = \sum_n N_{1n}\exp\left[-N_{2n}(T-N_{3n})\right]+N_0 \quad (6)$$

where n, N_0, and N_{1n}–N_{3n} are constants.

The GaN transistor employed in this study is "GS66508P 650 V-30 A enhancement-mode GaN transistor" from GaN Systems. The ranges of parameters used in (1)–(6) are displayed in Tables A (I) and A (II) in Appendix A. Good agreements between the modeled and measured *I–V* curves are obtained, as shown in Fig. 2. In contrast to the PSpice device model, the proposed device model has the capability of accurately representing GaN transistor's *I–V* curves under various temperatures. Since the GaN transistor is constructed with numerous identical cells in parallel, with regard to the GaN transistors with different sizes, both the *I–V* and *C–V* characteristics are in proportional to their current rates.

The nonlinear characteristics of intrinsic capacitances of the high-voltage GaN transistor, including the effects of field plates [34], can also affect the switching performances of both CtrlSW and SyncSW. The displacement currents and false triggering voltage could be influenced as well. Modeling methods of the nonlinear relationship between intrinsic capacitances and drain-to-source voltage ($C-V_{ds}$) vary among different models. As described in Table II, piecewise process model A uses charge-related constant intrinsic capacitances. Both piecewise process model B and PSpice model improve the accuracy of $C-V_{ds}$ modeling, but there still exist noticeable distinctions between measured and modeled curves. In order to accurately represent the $C-V_{ds}$ characteristics, a method is employed that combines multiple logarithms (F_5) with multiple Gaussian distribution functions (F_6), as expressed in (7). The basic trend of the $C-V_{ds}$ is determined by F_5, while F_6 fills the gaps between the basic and target curves. The ranges of parameters of (7) are presented in Table A (III) in Appendix A. Compared with the $C-V_{ds}$ characteristics of PSpice device model, the modeled curves are in excellent agreement with the measured results, as illustrated in Fig. 3(a) where the input capacitance $C_{iss} = C_{gs} + C_{gd}$, the output capacitance $C_{oss} = C_{ds} + C_{gd}$, and the reverse transfer

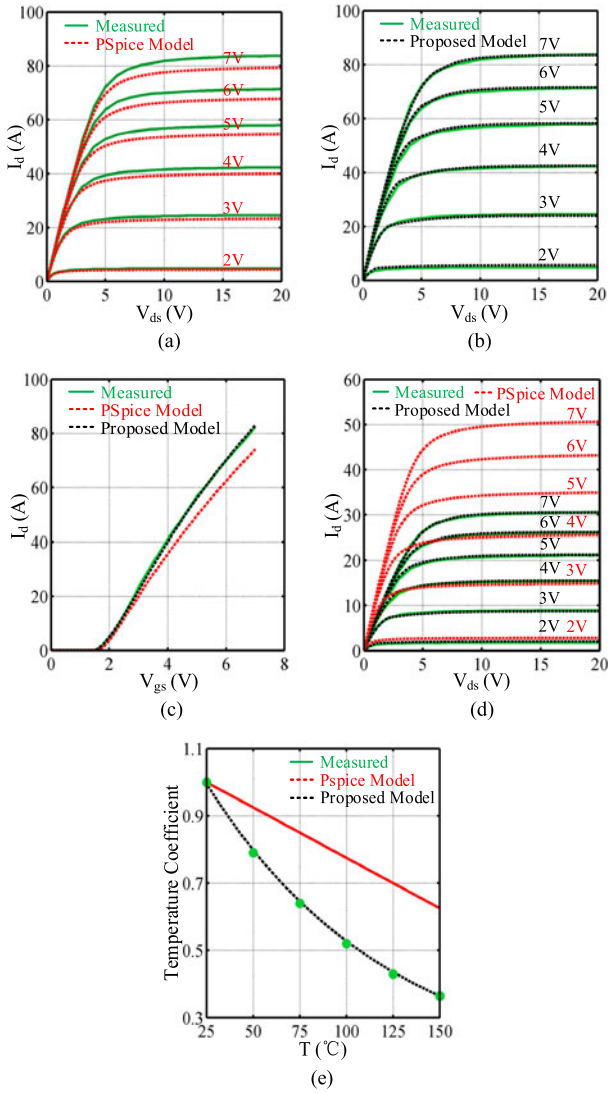

Fig. 2. (a) Measured and PSpice model's *I–V* characteristics at 25 °C. (b) Measured and modeled *I–V* characteristics at 25 °C. (c) Measured and modeled transfer characteristics at 25 °C. (d) Comparison between the *I–V* characteristics of the PSpice model and proposed model at 150 °C. (e) Comparison between the temperature coefficient of the PSpice model and proposed model.

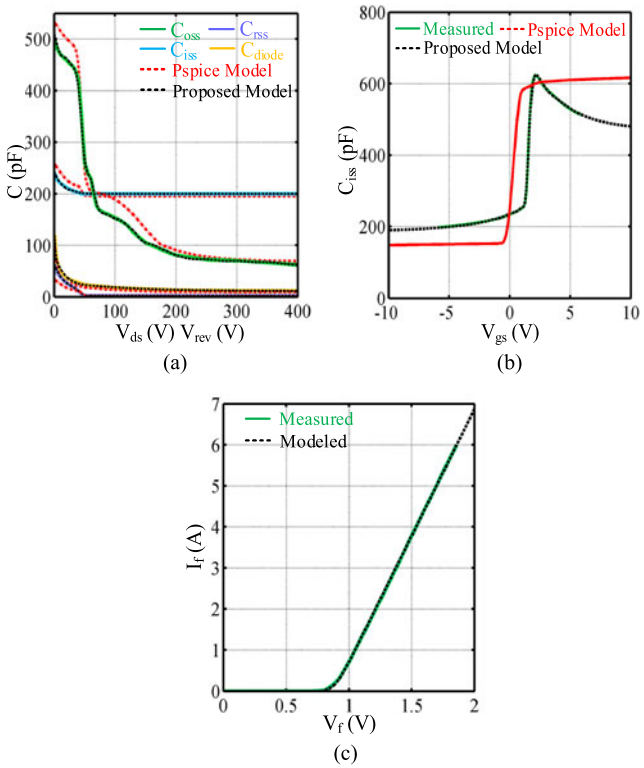

Fig. 3. (a) Comparison of the measured and modeled $C - V_{\rm ds}/V_{\rm rev}$ characteristics of GaN transistor and SiC SBD. (b) Comparison of measured and modeled $C_{\rm iss} - V_{\rm gs}$ characteristic of GaN transistor. (c) Comparison of measured and modeled forward characteristic of SiC SBD.

capacitance $C_{\rm rss} = C_{\rm gd}$

$$F_5 + F_6 + C_0 = \sum_n A_n \log(1 + \exp(-V_{\rm ds} + V_n)) + \sum_m B_m \exp((V_{\rm ds} - V_m)^2/2{\sigma_m}^2) + C_0 \quad (7)$$

where A_n, V_n, B_m, V_m, σ_m, and C_0 are constants.

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During the turn-on process of a transistor, its $C_{\rm iss}$ will significantly increase after the channel region is formed [28]. However, in the piecewise switching process models, the $C_{\rm iss} - V_{\rm gs}$ relationship has been ignored. As a consequence, inaccurate switching speed and displacement current could be caused during simulation. PSpice device model attempts to express this relationship, but the on-set of $C_{\rm iss}$'s rise is of less accuracy, as depicted in Fig. 3(b). Since the p-GaN gate technology is employed in most of the commercially available GaN transistors to achieve normally-off [7], [8], the Schottky contact capacitance between gate metal and p-GaN layer contributes a portion of $C_{\rm iss}$. With the positive $V_{\rm gs}$ increasing, the depletion region formed by gate-metal/p-GaN Schottky contact will be widened, making $C_{\rm iss}$ decline gradually [28]. This feature of the p-GaN device, however, has been neglected in PSpice.

To represent the $C_{\rm iss} - V_{\rm gs}$ relationship of the high-voltage E-mode GaN transistor, an inverse trigonometric function based modeling approach is employed, as expressed in (8). The arc tangent function F_7 determines the sharp rise near the $V_{\rm th}$, while the effective ranges of F_8 and F_9 are restricted by their exponents. Thus, F_8 and F_9 could affect the variation trend of F_7 before and after the sharp rise, respectively. Similar to the equation for $C - V_{\rm ds}$ curves, multiple Gaussian distribution functions (denoted as F_{10}) are brought in to enhance the precision. The ranges of parameters are presented in Table A (IV) in Appendix A, and the modeled $C_{\rm iss} - V_{\rm gs}$ characteristic is plotted in Fig. 3(b) in contrast to that of PSpice device model. In addition, the hyperbolic tangent functions employed in the *C–V* modeling could make the device model more robust

$$\begin{aligned} C_{\rm iss}(V_{\rm gs}) &= P_0 + F_7 + F_8 + F_9 + F_{10} \\ &= P_0 + P_1 \arctan[P_2(V_{\rm gs} - V_{\rm th})] \\ &\quad + P_3[\exp(P_4 V_{\rm gs} - P_5)]^{\arctan(P_6 V_{gs} + P_7)} \\ &\quad + P_8[\exp(P_9 V_{\rm gs} - P_{10})]^{\arctan(-P_6 V_{gs} - P_7)} \\ &\quad + \sum_k B_k \exp((V_{\rm gs} - V_k)^2/2{\sigma_k}^2) \end{aligned} \quad (8)$$

where P_0, $P_{1j} - P_{5j}$, B_k, V_k, and σ_k are constants.

From (7) and (8), $C_{\rm iss}$ of the GaN transistor is correlated with $V_{\rm gs}$ and $V_{\rm ds}$. However, it is difficult to acquire this correlation by device testing, owing to the extremely large drain current under high $V_{\rm ds}$ when the transistor is turned ON. In order to approximate the relationship, the $C_{\rm iss} - V_{\rm ds}$ curve could be multiplied by the normalized $C_{\rm iss} - V_{\rm gs}$ curve. As there exist small difference between the modeled Q_g (6.3 nC) and the Q_g (6.5 nC) given by device datasheet ($V_{\rm gs}$ varies from 0 to 7 V under 400 V $V_{\rm ds}$) [23], the approximation method is acceptable.

The antiparallel diode used in this paper is "C3D03060E 600 V-6 A SiC Schottky Diode" from CREE, forward characteristics of which can be expressed by (9), as displayed in Fig. 3(c). The ranges of parameters can be found in Table A (V) in Appendix A. The modeling method for $C - V_{\rm ds}$ relationships of GaN transistor could be applied to SBD as well, the result of which is depicted in Fig. 3(a)

$$I_f = Q_1 \log[1 + \exp((Q_2 V_{\rm rev} - Q_3)/Q_4)] \quad (9)$$

where Q_1–Q_4 are constants.

TABLE III
COMPARISON AMONG THE CIRCUIT-LEVEL MODELING OF DIFFERENT MODELS

Models	Parameters of Diode	Gate Driver's Resistance	Continuity of the Model	Observe Inside Package
Model A	Not Accurate	/	Discontinuous	Capable
Model B	/	/	Discontinuous	Capable
PSpice	Accurate	Accurate	Continuous	Incapable
Proposed	Accurate	Accurate	Continuous	Capable

Remark: "/" denotes that the aspect is not taken into account in the model.

B. Circuit-Level Modeling

On the basis of the device models, a circuit-level modeling can be carried out to obtain the switching transient waveforms related to false turn-on. As shown in Table III, with regard to piecewise switching process models, the discontinuities among the intervals, the less accurate diode parameters, and the negligence of gate driver's resistance could reduce the

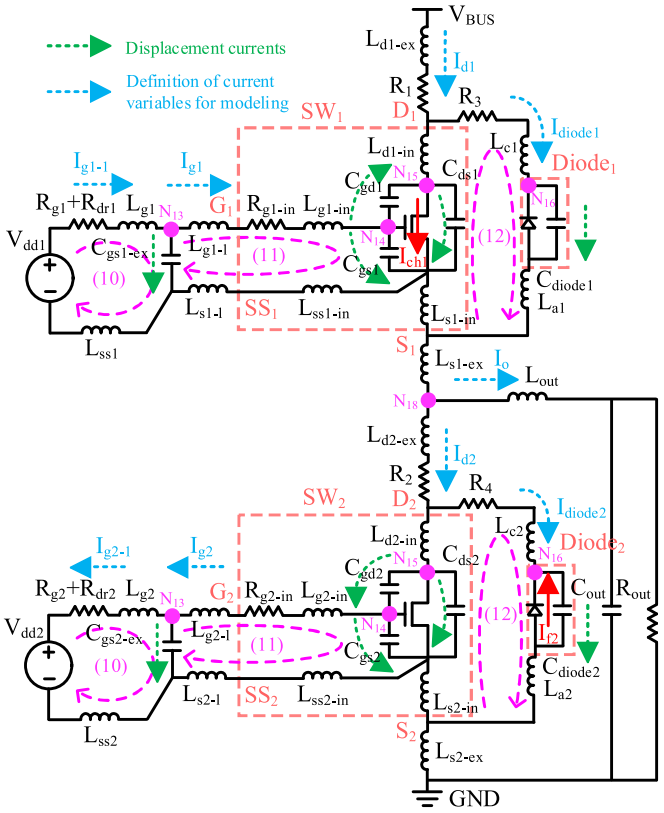

Fig. 4. Equivalent circuit of GaN-based bridge-leg configuration with loops and nodes.

accuracy of simulation. In spite of the continuity of PSpice circuit simulation, the actual false triggering voltage inside device package cannot be monitored. As all the circuit elements are taken into account and the waveforms inside device package can be observed, the proposed circuit-level model shows improved performance.

As illustrated in Fig. 4, the displacement currents flowing through externally added and intrinsic capacitances are marked, and the current variables for modeling are defined. Based on the equivalent circuit, the KVL and KCL equations can be derived for circuit modeling. Equations (10) and (11) represent the voltages in gate drive circuit of SW_k, where $k = 1$ or 2 denotes different transistors or diodes. Equation (12) describes the loop formed by SW_k and Diode_k. The current relationships with respect to the gate loop are expressed by KCL equations (13) and (14), while the currents flowing through Diode_k and SW_k are denoted by KCL equations (15) and (16), respectively. Equation (17) describes the voltage relationship among intrinsic capacitances of SW_k, and (18) represents the current relationship between SW_1 and SW_2. Voltages in the power loop can be expressed by (19).

Gate-loop KVL equations of SW_k ($k = 1$ or 2)

$$V_{\mathrm{dd}k} = I_{\mathrm{gk}-k}(R_{\mathrm{gk}} + R_{\mathrm{drk}}) + (L_{\mathrm{gk}} + L_{\mathrm{ssk}})\frac{dI_{\mathrm{gk}-k}}{dt} + (-1)^{(k+1)}V_{\mathrm{gsk}-\mathrm{ex}} \tag{10}$$

$$V_{\mathrm{gsk}} = (-1)^k(L_{\mathrm{gk}-l} + L_{\mathrm{gk}-\mathrm{in}} + L_{\mathrm{sk}-l} + L_{\mathrm{ssk}-\mathrm{in}})\frac{dI_{\mathrm{gk}}}{dt} + (-1)^k I_{\mathrm{gk}}R_{\mathrm{gk}-\mathrm{in}} + V_{\mathrm{gsk}-\mathrm{ex}}. \tag{11}$$

KVL equation of the loop formed by SW_k and Diode_k

$$V_{\mathrm{dsk}} + (L_{\mathrm{dk}-\mathrm{in}} + L_{\mathrm{sk}-\mathrm{in}})\frac{d(I_{\mathrm{dk}} - I_{\mathrm{diode}\vec{k}})}{dt} = (L_{\mathrm{ck}} + L_{\mathrm{ak}})\frac{dI_{\mathrm{diode}k}}{dt} + V_{\mathrm{diode}k} + R_{(k+1)}I_{\mathrm{diode}1}. \tag{12}$$

KCL equations of gate drive circuit of SW_k

$$I_{\mathrm{gk}} = (-1)^k C_{\mathrm{gsk}-\mathrm{ex}}\frac{dV_{\mathrm{gsk}-\mathrm{ex}}}{dt} + I_{\mathrm{gk}-1} \tag{13}$$

$$I_{\mathrm{gk}} = C_{\mathrm{gdk}}\frac{dV_{\mathrm{gdk}}}{dt} + C_{\mathrm{gsk}}\frac{dV_{\mathrm{gsk}}}{dt}. \tag{14}$$

KCL equations of currents flowing through SW_k and Diode_k:

$$I_{\mathrm{dk}} - I_{\mathrm{diode}k} = (-1)^k C_{\mathrm{gdk}}\frac{dV_{\mathrm{gdk}}}{dt} + \frac{[1 + (-1)^{(k+1)}]}{2}I_{\mathrm{ch1}} + C_{\mathrm{dsk}}\frac{dV_{\mathrm{dsk}}}{dt} \tag{15}$$

$$I_{\mathrm{diode}k} = C_{\mathrm{diode}k}\frac{dV_{\mathrm{diode}k}}{dt} + \frac{[1 + (-1)^k]}{2}I_f. \tag{16}$$

KVL equation denoting voltage relationship among intrinsic capacitances of $\mathrm{SW_k}$

$$V_{\mathrm{gsk}} = (-1)^{(k+1)}V_{\mathrm{gdk}} + V_{\mathrm{dsk}}. \tag{17}$$

KCL equation representing current relationship of SW_1 and SW_2

$$I_{d1} = I_{d2} + I_o. \tag{18}$$

Power-loop KVL equation

$$V_{\mathrm{BUS}} = V_{\mathrm{ds1}} + V_{\mathrm{ds2}} + I_{d1}R_1 + I_{d2}R_2 + (L_{d1-ex} + L_{s1-ex})\frac{dI_{d1}}{dt} + (L_{d2-\mathrm{ex}} + L_{s2-\mathrm{ex}})\frac{dI_{d2}}{dt} + (L_{d1-\mathrm{in}} + L_{s1-\mathrm{in}})\left(\frac{dI_{d1}}{dt} - \frac{dI_{\mathrm{diode1}}}{dt}\right) + (L_{d2-\mathrm{in}} + L_{s2-\mathrm{in}})\left(\frac{dI_{d2}}{dt} - \frac{dI_{\mathrm{diode2}}}{dt}\right). \tag{19}$$

The variables in equations above are defined as follows: voltages on gate–source, gate–drain, drain–source, and diode intrinsic capacitance, V_{gsk}, V_{gdk}, V_{dsk}, $V_{\mathrm{diode}k}$; voltage on external gate–source capacitance, $V_{\mathrm{gsk}-\mathrm{ex}}$; current flowing into SW_k and Diode_k, I_{dk}; charging currents in gate drive circuit, I_{gk} and $I_{\mathrm{gk}-1}$; diode current, $I_{\mathrm{diode}k}$; output current, I_o, and channel current of SW_1, I_{ch1}. Resistances R_1, R_2, R_3, and R_4 are the stray resistances in the power loop [35]. As the output current I_o can be regarded as a constant during the turn-on period, dI_{d2}/dt in (19) could be replaced by dI_{d1}/dt.

By combining circuit equations (10)–(19) with the characteristics of GaN transistors and SBDs [from (1)–(9)], the relevant

currents and voltages could be solved. However, due to the complexities of the *I–V* and *C–V* curves, it is hard to directly acquire explicit solutions without simplifying certain equations at the price of lower accuracy [18]. Such a problem can be dealt with by employing iteration. By sorting (10)–(19) into 16 first-order differential equations and transforming them into a 16 × 16 matrix, an iterative computation, expressed by (20) and (21), can be performed. Matrix *A* and vector *B* are given by (B.1) to (B.46) in Appendix B. During the computing process, before the $(N+1)$th iteration, devices' intrinsic capacitances and channel currents in *A* and *B* will be first calculated based on the results of Nth iteration *X(NΔT)*

$$dX/dt = AX + B \tag{20}$$

$$X((N+1)\Delta T) = X(N\Delta T) + [AX(N\Delta T) + B]\Delta T \tag{21}$$

where ΔT is the iteration step and the vector of variable

$$X = [I_{d1}\ \ I_{g1}\ \ I_{g1-1}\ \ V_{\mathrm{gs1}}\ \ V_{\mathrm{ds1}}\ \ V_{\mathrm{gs1-ex}}\ \ I_{\mathrm{diode1}}\ \ V_{\mathrm{diode1}}\ \ I_{d2}\ \ I_{g2}\ \ I_{g2-1}\ \ V_{gs2}\ \ V_{ds2}\ \ V_{\mathrm{gs2-ex}}\ \ I_{\mathrm{diode2}}\ \ V_{\mathrm{diode2}}]^T.$$

Similar to studies on false turn-on phenomenon of Si power devices, an assumption is made that SyncSW will remain in off-state even if the peak voltage of the false triggering voltage exceeds V_{th} [18]. We made this assumption to avoid dangerous shoot-through or self-oscillation that is complicated to study and also risky in real testing. Although the simulation results based on the proposed model might vary from reality when false triggering pulse exceeds V_{th}, the variation trend of false triggering voltage would be reasonably accurate and the safe operating areas (SOAs) of circuit parameters would be accurate, since SOA represents the situation when the false triggering voltage is lower than V_{th}.

C. Parameters Extraction and Model Calibration

Before verifying the proposed model on the testing board, the circuit parameters need to be extracted. Since the external-added resistance and capacitance could be measured by *LCR* Meter before being implemented on the board, the extraction of circuit elements should be mainly focused on the stray inductances in the circuit [36]. A detailed view of the power loop on the PCB is illustrated in Fig. 5(a). To freely adjust the power-loop inductance L_{power}, a piece of air-cored wire could be inserted between bus capacitors and SW_1, whose inductance is denoted as L_{wire}. Apart from the measurements under various L_{power}, a 1 nH L_{wire} is employed.

Through the finite-elements analysis simulation using "Ansoft Q3D Extractor," the stray inductances of the PCB could be extracted [36]. The simulated value of the total stray inductance L_{total} is 12.5 nH (including L_{wire}), which is composed of $L_{\mathrm{dk-ex}}$, $L_{\mathrm{sk-ex}}$, $L_{\mathrm{dk-in}}$, and $L_{\mathrm{sk-in}}$ as denoted in (22). Then, the simulations of $L_{\mathrm{dk-in}}$ and $L_{\mathrm{sk-in}}$ are conducted. Since the "Q3D Extractor" rules out the device package, the parasitic inductances of the package are added to simulation results afterward. With respect to external inductances $L_{\mathrm{dk-ex}}$ and $L_{\mathrm{sk-ex}}$, as long as their sum remains unchanged, their impacts are consistent [18]. Thus, an assumption could be made that the four

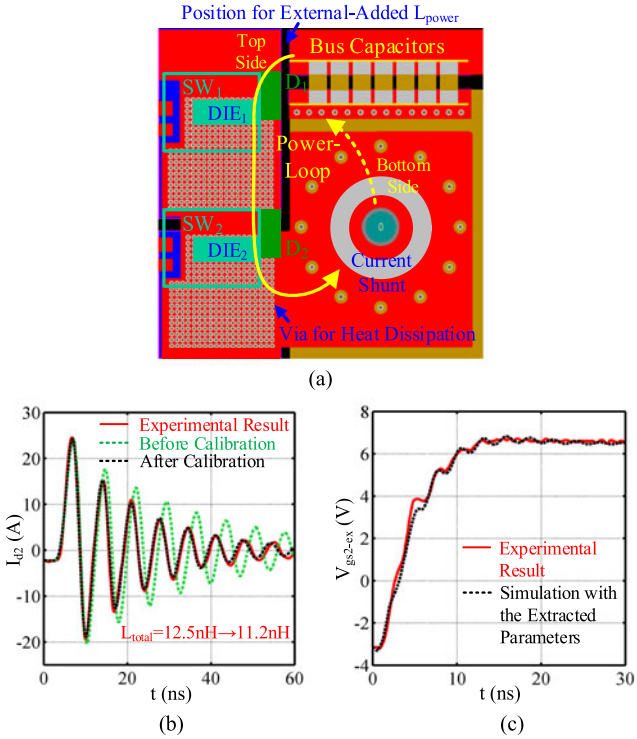

Fig. 5. (a) PCB board for extracting parasitic inductances in the power loop. (b) Comparison of displacement current I_{d2} before and after model calibration. (c) Voltage signal on $C_{\mathrm{gs2-ex}}$ ($V_{\mathrm{gs2-ex}}$).

pieces of external inductances are equal, whose values can be calculated by (23). Since the gate-loop's circuit design is simpler than that of power loop, the parasitic inductances in the gate drive circuit could be directly extracted

$$L_{\mathrm{total}} = L_{\mathrm{dk-ex}} + L_{\mathrm{sk-ex}} + L_{\mathrm{dk-in}} + L_{\mathrm{sk-in}} \tag{22}$$

$$L_{\mathrm{dk-in}} = L_{\mathrm{sk-in}} = (L_{\mathrm{total}} - L_{\mathrm{dk-in}} - L_{\mathrm{sk-in}})/4 \tag{23}$$

where $k = 1$ and 2.

Owing to the distinctions of each component's physical placement and current paths between the simulation and real implementation [36], the proposed model is required to be calibrated before further study. It is worth mentioning that the actual L_{power} is complicated due to the existence of antiparallel diode, but it could be calibrated by adjusting the extracted L_{total}. As expressed in (24) and (25), the total stray inductance (L_{total}) could be corrected based on the ringing frequency ω and damping ratio α of the displacement current I_{d2}. The displacement current under 200-V input voltage is employed for model calibration, as illustrated in Fig. 5(b) where L_{total} is reduced by 1.3 nH and the stray resistance R_{stray} could be adjusted accordingly

$$\omega \approx 1/\sqrt{C_{\mathrm{oss}} L_{\mathrm{total}}} \tag{24}$$

$$\alpha \approx R_{\mathrm{stray}}/2\omega L_{\mathrm{total}} \approx R_{\mathrm{stray}}\sqrt{C_{\mathrm{oss}}}/2\sqrt{L_{\mathrm{total}}}. \tag{25}$$

With regard to the inductances in gate drive circuit, the calibration could be made by measuring the voltage signal on the external-added gate-to-source capacitor of SW_2 ($C_{\mathrm{gs2-ex}}$), as plotted in Fig. 5(c). Through the comparison between measure-

TABLE IV
EXTRACTED CIRCUIT PARAMETERS IN GAN-BASED BRIDGE-LEG CONFIGURATION

Parameter	Symbol	Value
e gate voltage supply	$V_{\mathrm{dd}1}$	6.5 V
tive gate voltage supply	$V_{\mathrm{dd}2}$	−3.3 V
Drain external inductance	$L_{\mathrm{dk-ex}}$	2.1 nH
external inductance	$L_{\mathrm{sk-ex}}$	2.1 nH
nternal inductance	$L_{\mathrm{dk-in}}$	0.9 nH
internal inductance	$L_{\mathrm{sk-in}}$	0.9 nH
nternal resistance	$R_{\mathrm{gk-in}}$	1.5 Ω
Gate resistance	R_{gk}	4.7 Ω
Gate driver resistance of SW_1	$R_{\mathrm{dr}1}$	2.0 Ω
river resistance of SW_2	$R_{\mathrm{dr}2}$	0.2 Ω
rnal inductance	$L_{\mathrm{ssk-in}}$	1.0 nH
internal inductance	$L_{\mathrm{gk-in}}$	1.0 nH
Source lead inductance	$L_{\mathrm{sk}-l}$	2.3 nH
Gate lead inductance	$L_{\mathrm{gk}-l}$	2.3 nH
Diode cathode inductance	L_{ck}	2.0 nH
Diode anode inductance	L_{ak}	3.0 nH
Gate external inductance	L_{ssk}	2.0 nH
SS inductance	L_{ssk}	10.0 nH
l gate–source capacitance	$C_{\mathrm{gsk-ex}}$	47 pF
filter capacitance	C_{out}	330 nF
filter inductance	L_{out}	470 μH
resistance	R_{out}	30 Ω

Remarks: "$L_{\mathrm{dk-in}}$" denotes the internal inductance from the D terminal of device package to the die of GaN transistor; "$L_{\mathrm{sk-in}}$" denotes the internal inductance from the S terminal of device package to the die of GaN transistor; "L_{ck}" is the inductance inside diode's package, as the leads of diode are cut off;"L_{ak}" includes the inductances inside diode's package and the stray inductance from diode to S terminals of GaN transistor; "$R_{\mathrm{dr}1}$" and "$R_{\mathrm{dr}2}$" are acquired from the manufacturer of the gate driver (LM5114); "k" denotes different transistors or diodes ($k = 1$ for CtrlSW and $k = 2$ for SyncSW).

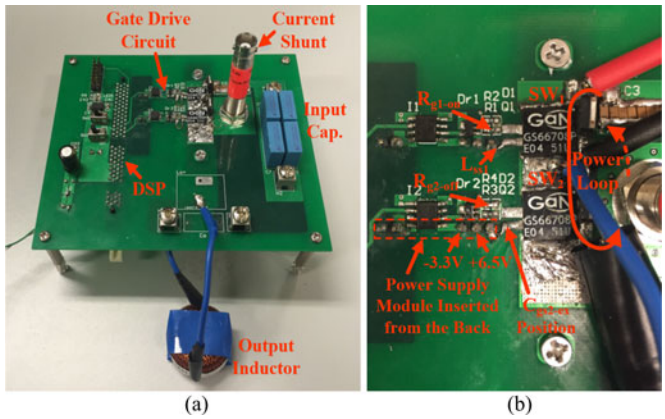

Fig. 6. (a) GaN-based testing board with bridge-leg configuration circuit operating in synchronous buck mode. (b) Detailed view of the power loop and gate drive circuit.

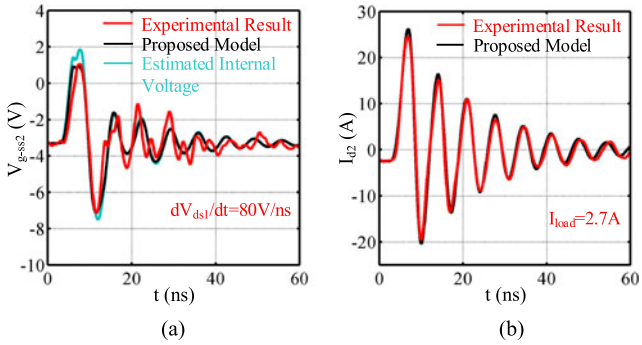

Fig. 7. Comparison of measured and simulated results with circuit parameters in Table IV: (a) Voltage between G and SS terminals of SW_2 $V_{g-\mathrm{ss}2}$; (b) displacement current I_{d2}.

ment and circuit simulation, the gate-loop's parameter extraction shows satisfactory accuracy. The calibrated circuit parameters are displayed in Table IV.

III. EXPERIMENTAL VERIFICATION AND DISCUSSION

The proposed analytical model is then verified on a 200-to-80 V bridge-leg circuit implemented with 650 V E-mode GaN transistors on PCB. The bridge-leg circuit is configured in synchronous buck mode such that the SyncSW is on the low-side and can be easily monitored. Although the proposed model is capable of evaluating the circuit under various temperatures, it is hard to obtain the exact junction temperature of the device during experiment. Therefore, the measurement is required to be carried out under the room temperature. To reduce losses and the consequent temperature rise, the testing circuit is designed to operate with a 100 kHz switching frequency and a 213 W output power. Furthermore, the testing process is required to be finished rapidly, and the forced convection is applied to improve heat dissipation. Fig. 6 illustrates the experimental setup along with a detailed view of the gate drive circuit, key parameters of which are extracted and displayed in Table IV. In order to freely adjust the SS inductance and regulate the negative gate voltage bias for turn-off, standalone power supply modules implemented with charge pump chips are inserted into the testing board from the back.

Since the displacement current I_{d2} is critical to the false turn-on problem, an "SSDN-10" coaxial current shunt from T&M Research Products is employed for current measurement. The current shunt presents a 0.1-Ω resistor connected in series into the power loop. However, the parasitic inductance of the current shunt could affect the measurement accuracy of the fast-changing displacement current [36]. The current shunt can be modeled as a resistor and an inductor in series [36], and the actual waveform of the displacement current can be acquired.

A. Experimental Results Under Various Circuit Conditions

Comparisons between the waveforms from measurement and simulation using the proposed device/circuit model are displayed in Figs. 7–11, under various circuit parameters. As there exist internal gate resistance and inductance inside the device package, only the voltage between G and SS terminals ($V_{g-\mathrm{ss}2}$) can be measured rather than the actual internal gate–source voltage $V_{\mathrm{gs}2}$ [18]. The simulated waveforms of the false triggering voltage pulse on $V_{g-\mathrm{ss}2}$ and the displacement current I_{d2} are in reasonable agreements with the experimental results. The differences between measurements and theoretical analysis mainly come from the electromagnetic interference on the testing board,

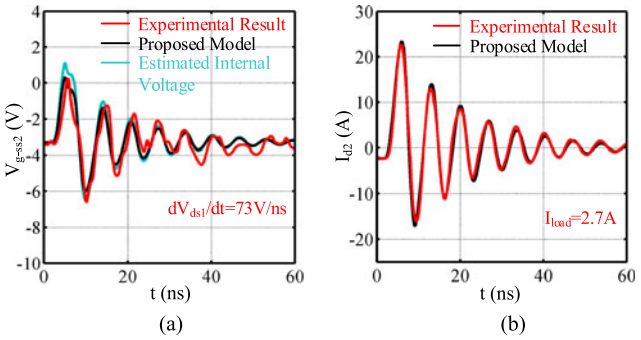

Fig. 8. Comparison of measured and simulated results when $L_{\mathrm{ss1}} = L_{\mathrm{ss2}} = 3$ nH: (a) Voltage between G and SS terminals of SW_2 $V_{g-\mathrm{ss2}}$; (b) displacement current I_{d2}.

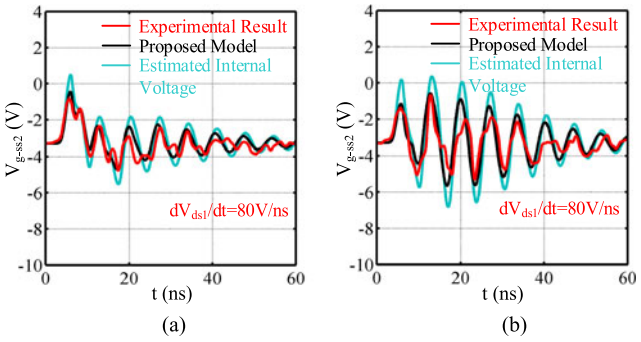

Fig. 9. Comparison of measured and simulated results when $C_{\mathrm{gs2-ex}}$ increases: (a) Voltage between G and SS terminals of SW_2 $V_{g-\mathrm{ss2}}$ when $C_{\mathrm{gs2-ex}} = 470$ pF; (b) voltage between G and SS terminals of SW_2 $V_{g-\mathrm{ss2}}$ when $C_{\mathrm{gs2-ex}} = 1.2$ nF.

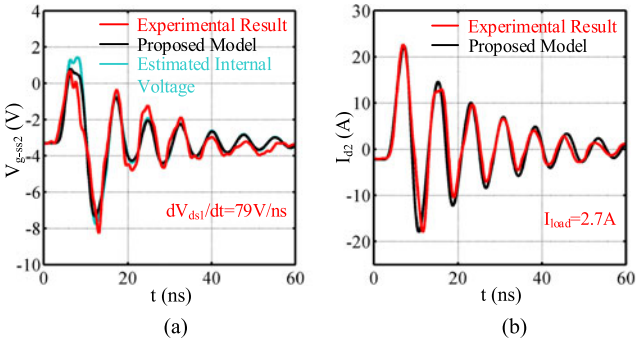

Fig. 10. Comparison of measured and simulated results when $L_{d1-\mathrm{ex}}$ increases by 3 nH: (a) Voltage between G and SS terminals of SW_2 $V_{g-\mathrm{ss2}}$; (b) Displacement current I_{d2}.

variations in transistor performance, and possible inaccuracies in parameter extractions.

The measured and simulated waveforms of $V_{g-\mathrm{ss2}}$ and I_{d2} are plotted in Figs. 7–11, along with the estimated internal gate–source voltage V_{gs2} [18]. As illustrated in Fig. 7(a), the measured and simulated peak values of $V_{g-\mathrm{ss2}}$ are about 1 V, while the estimated peak value of V_{gs2} approaches 2 V. Although the peak of V_{gs2} already exceeds V_{th} of the chosen GaN transistor (1.6 V), it has little impact on the displacement current since

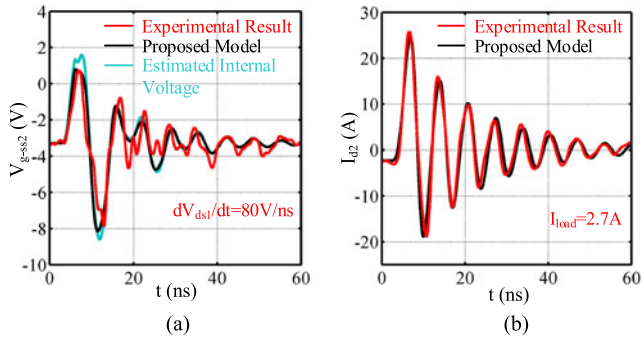

Fig. 11. Comparison of measured and simulated results when $R_{g2-\mathrm{off}} = 3.3\,\Omega$: (a) Voltage between G and SS terminals of SW_2 $V_{g-\mathrm{ss2}}$; (b) displacement current I_{d2}.

the duration of this voltage peak is short and SW_2 still exhibits large resistance in the subthreshold region.

As depicted in Fig. 8, the amplitude of I_{d2} can be reduced with a smaller source-sense inductance L_{ss}, leading to a reduced voltage slew rate of SW_1 (dV_{ds1}/dt). The false triggering voltage is suppressed as well. The impacts of the external gate–source capacitance of SW_2 $(C_{\mathrm{gs2-ex}})$ are presented in Fig. 9. As there is no obvious change in I_{d2} at a larger $C_{\mathrm{gs2-ex}}$, only the waveforms of false triggering voltage are presented. The voltage fluctuation is first damped when $C_{\mathrm{gs2-ex}}$ is at 470 pF, but becomes severer when $C_{\mathrm{gs2-ex}}$ increases to 1.2 nF. Such a phenomenon will be further discussed and explained in the next section. Fig. 10 indicates the case when a larger external drain inductance of SW_1 $L_{d1-\mathrm{ex}}$ is used, which yields a larger power-loop inductance. With the power-loop inductance increasing, the amplitude and frequency of I_{d2} are reduced. Thus, the first voltage peak of the false triggering pulse is damped, while the second voltage peak becomes much higher.

Fig. 11 plots the waveforms of $V_{g-\mathrm{ss2}}$ and I_{d2} when a smaller turn-off resistance $(R_{g2-\mathrm{off}})$ for SW_2 is applied. As described in [21] and [22], the false triggering voltage can be mitigated by designing a low-impedance path to sink the current of SW_2 (e.g., an independent current path for turn-off and smaller $R_{g2-\mathrm{off}}$). When $R_{g2-\mathrm{off}}$ is reduced from 4.7 to 3.3 Ω, the voltage peak of V_{gs2} is slightly decreased, while the minimum voltage, on the other hand, exhibits a remarkable drop and approaches the negative gate voltage limit of the GaN transistor (−10 V). Thus, investigations of mitigation methods for false turn-on should take gate undershoot into consideration as well.

The measurements under different input voltages V_{in} are also conducted to verify the proposed model. Since the risk of dangerous circuit conditions (e.g., shoot through) would significantly increase with V_{in} [17], it could be hard to handle the testing under high voltage. As GaN transistor's C_{oss} almost remains constant after V_{ds} surpasses 300 V, $V_{\mathrm{in}} = 300$ V could be selected as a representative condition for high-voltage testing. During the experiments, modest circuit parameters ($L_{\mathrm{ss1}} = L_{\mathrm{ss2}} = 3$ nH) are applied to decrease the risk of false triggering. Besides, the load current is reduced to 2.4 A under 300 V testing to restrict power loss. The waveforms under 100 and 300 V input voltages are depicted in Fig. 12, where the proposed model shows acceptable performances.

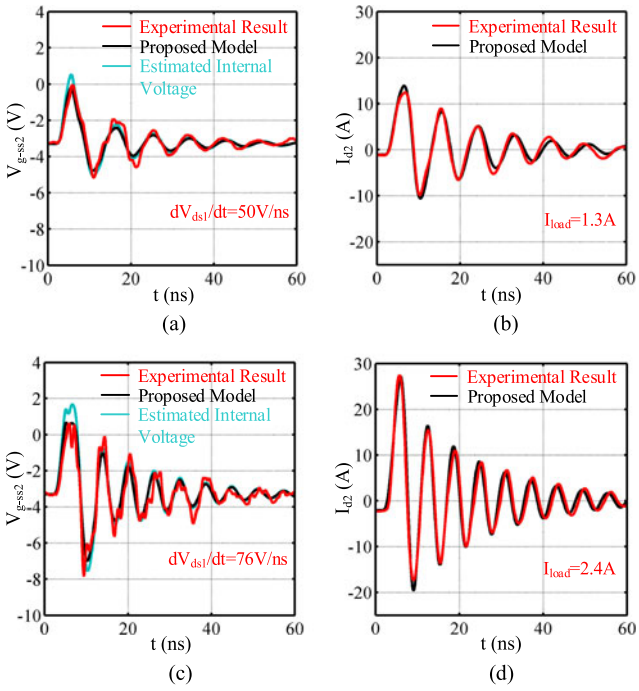

Fig. 12. Comparison of measured and simulated results with $L_{ss1} = L_{ss2} = 3$ nH under different V_{in}: (a) Voltage between G and SS terminals of SW_2 V_{g-ss2} when $V_{in} = 100$ V; (b) displacement current I_{d2} when $V_{in} = 100$ V; (c) voltage between G and SS terminals of SW_2 V_{g-ss2} when $V_{in} = 300$ V; (d) displacement current I_{d2} when $V_{in} = 300$ V.

Through the aforementioned measurements, the device/circuit models under ambient temperature are verified. To further validate the performances of device model under higher temperatures, a boost converter is built as depicted in Fig. 13(a). The GaN transistor is placed on a probe station with temperature control capability. In order to remove the interference of other parts in the setup, the other circuit components are required to keep a distance from the probe station and the gate driver is replaced by a pulse generator. For the purpose of protecting the pulse generator, a current-limiting resistance is inserted into the gate loop. As a result, the stray inductance in the power loop could be significantly enlarged. Key parameters of the setup are displayed in Table.V.

As plotted in Fig. 13(b), the drain-to-source voltage of GaN transistor (V_{ds3}) during turn-on period is measured at 25, 75, and 125 °C, respectively. Owing to large stray inductance and limited drive capability, the switching speed would be largely reduced, in contrast to the testing on PCB. Besides, the nonnegligible inductances between testing points and device terminals (L_{d3} and L_{s3}) could also influence the tested waveforms. Despite the restrictions of experimental conditions, it is noticeable that the turn-on process would be prolonged at a higher temperature. Based on the proposed device model, the waveforms of V_{ds3} can be obtained, which are in acceptable agreements with the measurements.

As the proposed device model is usable under higher temperatures, the transient waveforms relevant to false turn-on could be simulated under high-voltage/high-temperature conditions. Fig. 13(d)–(f) plots the simulation results of the drain-to-source

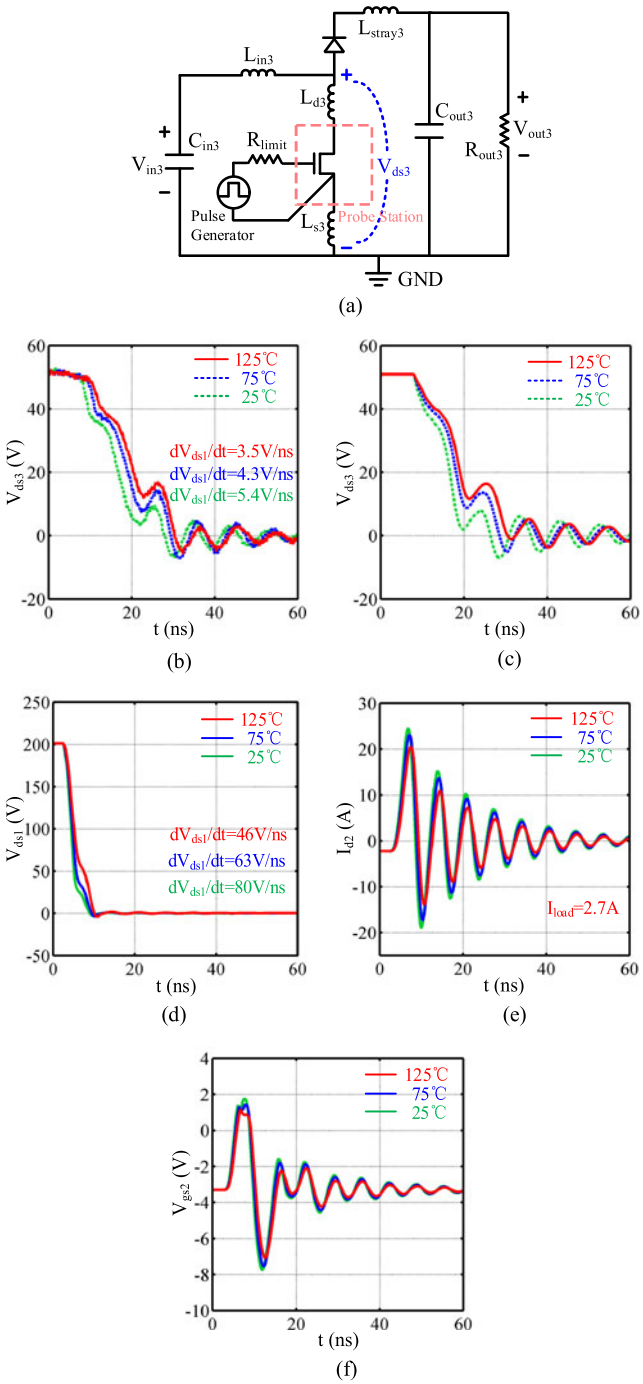

Fig. 13. (a) Schematic of the boost converter; (b) measured V_{ds3} waveforms of the boost converter under different temperatures; (c) simulated V_{ds3} waveforms of the boost converter under different temperatures; (d) simulated V_{ds1} waveforms of GaN-based bridge-leg under different temperatures; (e) simulated I_{d2} waveforms of GaN-based bridge-leg under different temperatures; (f) simulated V_{gs2} waveforms of GaN-based bridge-leg under different temperatures.

voltage of SW_1 (V_{ds1}), the displacement current (I_{d2}), and the actual false triggering voltage inside device package (V_{gs2}) under 200 V input voltage and various temperatures. Although GaN transistor's saturation region current declines by 63% when the temperature rises from 25 to 125 °C, the amplitude of I_{d2} only decreases by 17%. This phenomenon can be explained by (26), which is obtained from Appendix C. Due to the negative

TABLE V
CIRCUIT PARAMETERS IN GAN-BASED BOOST CONVERTER

Parameter	Symbol	Value
Input voltage	$V_{\text{in}3}$	25 V
Output voltage	$V_{\text{out}3}$	50 V
Switching frequency	f_s	100 kHz
Drain inductance	L_{d3}	12 nH
Source inductance	L_{s3}	12 nH
Stray inductance	$L_{\text{stray}3}$	60 nH
Current-limiting resistance	R_{limit}	50 Ω
Output filter inductance	L_{out}	150 μH
Output filter capacitance	C_{out}	360 nF
Output resistance	R_{out}	100 Ω

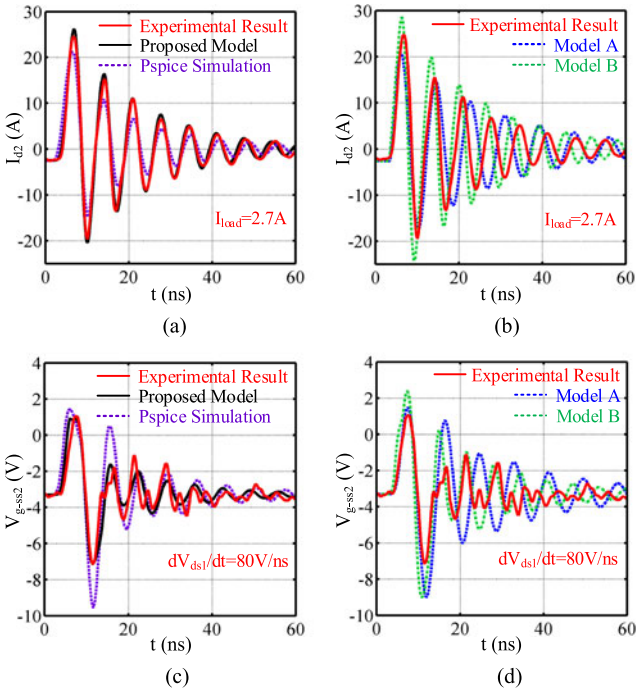

Fig. 14. Comparison of experimental and simulated results with circuit parameters in Table IV: (a) Displacement current I_{d2} of PSpice model and proposed model; (b) displacement current I_{d2} of Model A and Model B; (c) voltage between G and SS terminals of SW_2 $V_{g-\text{ss}2}$ of PSpice model and proposed model; (d) voltage between G and SS terminals of SW_2 $V_{g-\text{ss}2}$ of Model A and Model B.

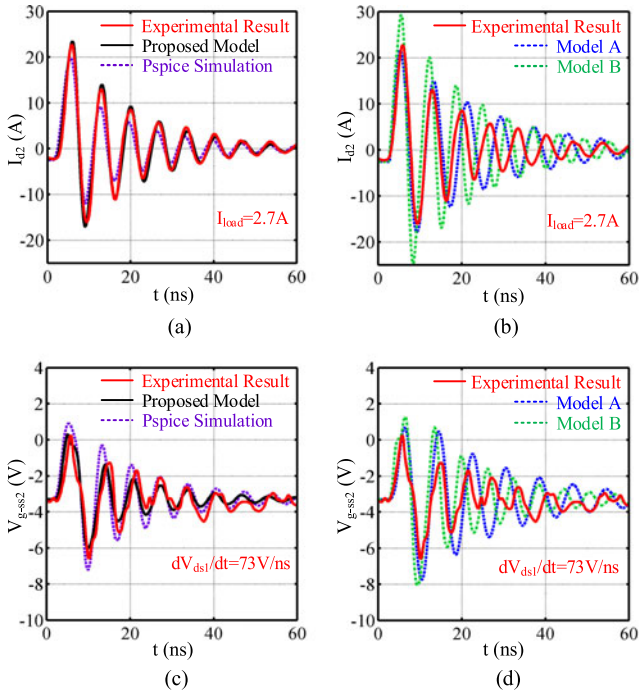

Fig. 15. Comparison of experimental and simulated results when $L_{\text{ss}1} = L_{\text{ss}2} = 3$ nH: (a) Displacement current I_{d2} of PSpice model and proposed model; (b) displacement current I_{d2} of Model A and Model B; (c) voltage between G and SS terminals of SW_2 $V_{g-\text{ss}2}$ of PSpice model and proposed model; (d) voltage between G and SS terminals of SW_2 $V_{g-\text{ss}2}$ of Model A and Model B.

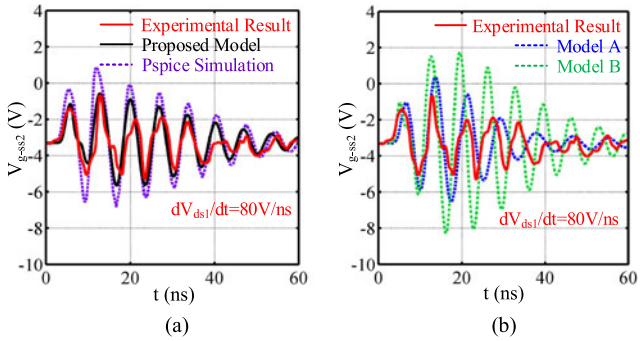

Fig. 16. Comparison of experimental and simulated results when $C_{\text{gs}2-\text{ex}} = 1.2$ nF: (a) Voltage between G and SS terminals of SW_2 $V_{g-\text{ss}2}$ of PSpice model and proposed model; (b) voltage between G and SS terminals of SW_2 $V_{g-\text{ss}2}$ of Model A and Model B.

feedback of SW_2's channel current ($I_{\text{ch}1}$) on its gate-to-source voltage (V_{gs1}), SW_1 would increase faster under high temperature, so that the decrease of *I–V* curves at high temperature could be partially compensated. With regard to false turn-on, with temperature rising, the false triggering voltage could be mitigated

$$\frac{dV_{\text{gs}1}}{dt} = \frac{C_{\text{gd}1}(I_{d1} - I_{\text{diode}1}) + C_{\text{oss}1}I_{g1} - C_{\text{iss}1}I_{\text{ch}1}}{C_{\text{gd}1}C_{\text{gs}1} + C_{\text{ds}1}C_{\text{iss}1}}. \quad (26)$$

B. Comparison With Other Models

For the purpose of comparison, the transient waveforms related to false turn-on are also simulated by piecewise switching process models and PSpice simulation. As illustrated in Figs. 14–16, besides the simulation under circuit parameters of Table IV, the waveforms under different source-sense inductance L_{ss} and external-added gate-to-source capacitance $C_{\text{gs}-\text{ex}}$ are obtained as well. As the result of the underestimated *I–V* characteristics and the less accurate $C_{\text{iss}}-V_{\text{gs}}$ curve, the displacement current I_{d2} of PSpice model is lower than tested. Due to the underrated C_{iss} when V_{gs} is negative, the false triggering voltage pulses, however, could be overestimated.

With regard to piecewise switching process models, owing to the shortcomings in device modeling (less accurate *I–V* and $C - V_{\text{ds}}$ curves along with negligence of $C_{\text{iss}} - V_{\text{gs}}$ relationship) and the discontinuities among intervals, both the amplitude and ringing frequency of I_{d2} are of less accuracy. Thus, the impacts

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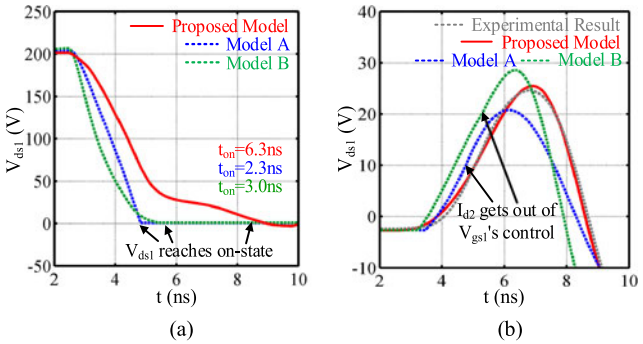

Fig. 17. Comparison between the simulated waveforms of piecewise process models and proposed model: (a) Detailed $V_{\rm ds1}$ waveforms; (b) detailed I_{d2} waveforms.

of circuit parameters could be falsely predicted. As plotted in Fig. 16, there exist significant distinctions between the measured and simulated false triggering voltages, when a large external capacitance $C_{\rm gs2-ex}$ is employed.

Furthermore, it is remarkable that the simulations of piecewise process models indicate an opposite impact of $L_{\rm ss1}$ from the experiments. By exploring the detailed $V_{\rm ds1}$ and I_{d2} waveforms depicted in Fig. 17, this phenomenon could be further explained. In piecewise process models, as the result of the constant $\rm C_{iss}$ when gate terminal's voltage changes, the total gate charge during the turn-on process would be much smaller than reality (1.9 nC versus 6.5 nC). Consequently, the displacement current I_{d2} would rise more rapidly. The fast-changing current along with the less accurate $C-V_{\rm ds}$ curves could enlarge the slew rate of $V_{\rm ds1}$ (over 100 V/ns), making the turn-on process terminate much earlier. Although $V_{\rm gs1}$ could be affected by gate-loop's elements, the amplitude of I_{d2} would get out of $V_{\rm gs1}$'s control once $V_{\rm ds1}$ reaches the on-state value, according to piecewise process models' criteria for intervals [18], [27].

In summary, in contrast to piecewise process and PSpice simulation, the proposed model exhibits outstanding performances in simulating the transient waveforms relevant to false turn-on. By taking advantages of the proposed model, the false turn-on of high-voltage GaN transistor in bridge-leg configuration could be better evaluated.

IV. Impacts of Circuit Parameters on False Turn-On and Design Optimization

A comprehensive study of false turn-on in Si-based bridge-leg is conducted in [18], the conclusions of which are summarized in Table VI. Compared with the GaN transistor, the Si MOSFET with comparable voltage/current rate has a significantly larger $C_{\rm iss}$ (over 2000 pF) [24], which makes the inherent frequency of SyncSW's gate drive circuit (including $C_{\rm gs2}$) much lower than the ringing frequency of displacement current I_{d2}. Besides, the existence of common source inductance could further reduce this inherent frequency (below 20 MHz) [11]. Therefore, without the need for considering the resonance between gate loop and displacement current, the impacts of circuit elements on false turn-on of Si devices are straightforward. In contrast to Si devices, most of the commercially available GaN transistors are free of common-source inductance and feature more than ten times smaller $C_{\rm iss}$ [23]. Hence, the gate-loop's resonant frequency is located at around 100 MHz, as plotted in Fig. 19. Since GaN transistor features fast switching speed and small $C_{\rm oss}$, the ringing frequency of its displacement current could lie in that region as well [see Fig. 19(b)], inducing resonance between the gate loop and displacement current. Consequently, the impacts of circuit parameters on the false turn-on of GaN transistor could be more complicated.

Based on the aforementioned analytical model, the maximum and minimum of the false triggering voltage can be obtained. Thus, the impacts of circuit parameters along with the optimum negative gate voltage supply can be studied. In the previous section, a 200 V input voltage is selected in most cases to reduce losses and avoid dangerous circuit conditions (e.g., shoot through). During the simulations in this part, a higher input voltage (300 V) is employed to explore the operating regions that are difficult to handle in measurement and extract more information about the false turn-on.

In order to deeply comprehend the mechanism of the simulated results, an impedance analysis is carried out. The equivalent circuit of SyncSW's gate drive circuit is illustrated in Fig. 19(a), where the transient current flowing through the network equals to the displacement current of $C_{\rm gd2}$. The impedance of the network is derived in (27), where H_0-H_3 and J_0-J_4 are presented in Appendix C from (C.1) to (C.9). Since the false triggering voltage could be denoted as (28), the portion of I_{d2} that flows into the gate drive circuit would be amplified when there exists resonance peak in Z

$$\frac{H_3s^3+H_2s^2+H_1s+H_0}{J_4s^4+J_3s^3+J_2s^2+J_1s+J_0} \tag{27}$$

$$V_{\rm gs2}(\omega)=\alpha I_{d2}(\omega)Z(\omega) \tag{28}$$

where α is the proportion of I_{d2} that flows into the gate drive network.

As shown in Table VI and Fig. 18, the impacts of the source-sense inductance $L_{\rm ss}$, the power-loop inductance $L_{\rm power}$, the external-added gate-to-source capacitance of SyncSW $C_{\rm gs2-ex}$, the physical placements of $C_{\rm gs-ex}$, and the turn-off resistance of SyncSW $R_{g2-\rm off}$) are investigated. Obvious differences could be found in circuit parameters' impacts between Si and GaN based bridge-leg circuits. The effects of $L_{\rm ss}$ are illustrated in Fig. 18(a). Because of the resonance between $L_{\rm ss1}$ and $C_{\rm iss}$ of CtrlSW during the turn-on process [37], the amplitude of I_{d2} along with the false triggering voltage increase in *Stage 1*. When $L_{\rm ss1}$ is larger than 17 nH, *Stage 2* commences where the impedance of $L_{\rm ss1}$ dominates and the maximum value of the false triggering voltage begins to step down.

The fast Fourier transform result of I_{d2} is depicted in Fig. 19(b). Since I_{d2} rises slowly before reaching its first peak P_1, the main frequency components of P_1 (below 100 MHz) are lower than those of the subsequent peaks (P_s around 160 MHz). As plotted in Fig. 19(c), with $L_{\rm ss2}$ being enlarged, the amplitude of gate-loop's resonance peak significantly increases. Although the resonance peak of gate drive circuit R_{p1} slowly moves downward, it always partially overlaps with frequency components

TABLE VI
IMPACTS OF CIRCUIT PARAMETERS ON THE MAXIMUM FALSE TRIGGERING VOLTAGE OF GAN AND SI BRIDGE-LEGS

Circuit Parameters	Gate-Loop Inductance of CtrlSW L_{g1} (L_{ss1})	Gate-Loop Inductance of SyncSW L_{g2} (L_{ss2})	Power-Loop Inductance L_{power}	External-Added Gate–Source Capacitance C_{gs2-ex}	Physical Placements of C_{gs1-ex} and C_{gs2-ex}	Turn-off Resistance of SyncSW Rg_{2-off}
Si Bridge-Leg	→	→	↑	↓	/	↑
GaN Bridge-Leg	*(a)*	↑	*(b)*	*(c)*	*(d)*	↑

Remarks: "CtrlSW" denotes the controlling switch in the bridge-leg; "SyncSW" denotes the synchronous switch in the bridge-leg;"→" denotes no obvious change; "↑" denotes increase with the increase of the considered parameter;"↓" denotes decrease with the increase of the considered parameter; "/" denotes that the parameter is not considered;"(a)," "(b)," "(c)," and "(d)" denote the variation trends displayed in Fig. 18(a), (b), (c), and (d).

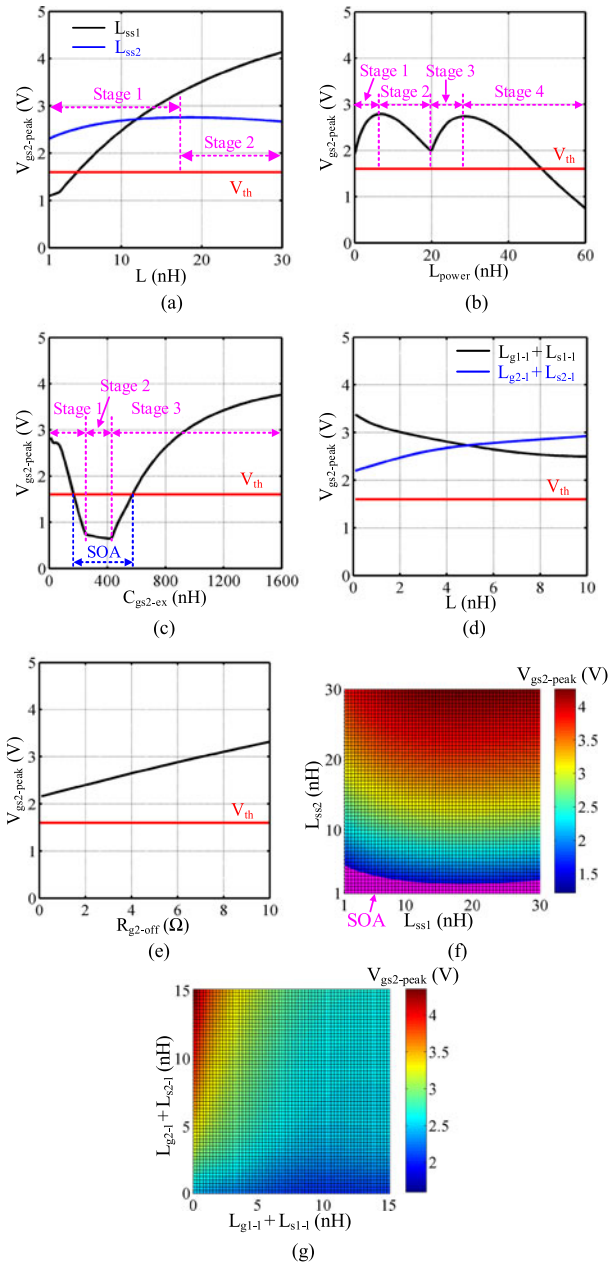

Fig. 18. Impacts of circuit parameters on the maximum values of false triggering voltage pulses under 300 V input voltage: (a) Source-sense inductance L_{ss1} and L_{ss2}; (b) power-loop inductance L_{power}; (c) external-added gate-to-source capacitance of SyncSW C_{gs2-ex}; (d) positions of external added capacitances; (e) turn-off resistance of SyncSW R_{g2-off}; (f) plane graph of the SS inductances; (g) plane graph of the positions of external added capacitances.

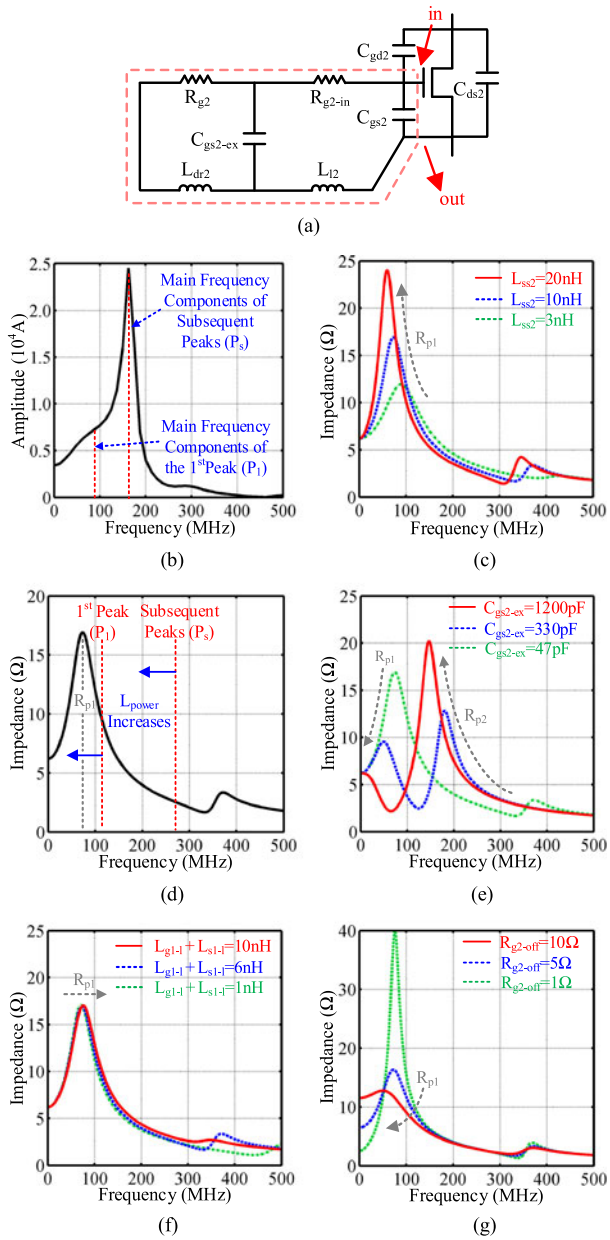

Fig. 19. Impedance analysis of gate drive circuit: (a) Equivalent circuit of SyncSW's gate drive scheme; (b) FFT result of I_{d2}; (c) impedance–frequency relationship under different L_{ss2}; (d) impedance–frequency relationship under different L_{power}; (e) impedance–frequency relationship under different C_{gs2-ex}; (f) impedance–frequency relationship under different physical placements of C_{gs2-ex}; (g) impedance–frequency relationship under different R_{g2-off}.

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2 notes

of P_1. Thus, L_{ss2} could play an important role in intensifying the false triggering voltage. Fig. 18(f) gives more information on the influences of SS inductances and provides an SOA for design consideration. However, once the negative gate voltage is applied in real applications, it is hard to reduce L_{ss2} to a low value (e.g., below 5 nH) since the SS terminal of GaN transistor is directly connected to gate voltage's reference point rather than the gate driver chip.

Fig. 18(b) illustrates the effects of power-loop inductance, which can be divided into four stages. As depicted in Fig. 19(c), the main frequency components of I_{d2} move downward with the enlargement of $L_{\rm power}$. In *Stages 1* and *2*, the resonance between P_1 and R_{p1} takes the leading position, and the critical point is reached when the main frequency of P_1 is consistent with R_{p1}. As $L_{\rm power}$ continues increasing, both the ringing frequency and the damping ratio of I_{d2} decrease. Consequently, the amplitudes of P_s are comparable to that of P_1, while the frequency components of P_s keeps approaching R_{p1}, leading to *Stage 3* and *4*. Similarly, the dividing point of *Stage 3* and *4* is attained when the frequency peak of P_s equals to R_{p1}.

The relationship between the false triggering voltage and $C_{\rm gs2-ex}$ is depicted in Fig. 18(c). As described in Section III, although a larger $C_{\rm gs2-ex}$ of $\rm SW_2$ could first damp the fluctuation on $V_{\rm gs2}$, the false triggering pulse would be intensified when $C_{\rm gs2-ex}$ keeps increasing. By looking into the impedance of $\rm SW_2$'s gate loop, this phenomenon could be further explained. Apart from the aforementioned resonance peak R_{p1}, we can find another small resonance peak R_{p2} in high-frequency region. When a greater $C_{\rm gs2-ex}$ is employed, both R_{p1} and R_{p2} will be shifted downward in frequency domain, which first attenuates the false triggering voltage. However, the amplitude of R_{p2} could be largely blown up when a large enough $C_{\rm gs2-ex}$ is used (e.g., larger than 600 pF). Such an effect could cause severe oscillation between gate loop and subsequent peaks of I_{d2}, as illustrated in *Stage 3* of Fig. 18(c). Despite the SOA provided, $C_{\rm gs2-ex}$ in the range of *Stage 2* is recommended, where the false triggering voltage would be minimized.

The impacts of physical placement of $C_{\rm gs-ex}$ could be investigated by enlarging $L_{g-l}+L_{s-l}$ and reducing $L_{\rm ss}$ simultaneously, to keep the total gate-loop inductance unchanged. The results are depicted in Fig. 18(d) and (g). Moving $C_{\rm gs1-ex}$ away from $\rm SW_1$ could partially decouple the gate-loop inductance so that the false triggering voltage would be slightly damped. Fig. 19(e) shows that moving $C_{\rm gs2-ex}$ away could mildly shift the R_{p1} toward the main frequency of P_1, resulting in slight increase in false triggering voltage.

The impacts of turn-off resistance of $\rm SW_2$ are illustrated in Figs. 18(e) and 19(g). When a small $R_{g2-\rm off}$ is applied, gate-loop's low-frequency response (below 50 MHz) could be damped, making the false triggering voltage rise slowly at the beginning of turn-on process. Thus, the maximum value of the false triggering voltage would decrease. However, owing to small $R_{g2-\rm off}$'s poor performance in suppressing the resonance peak, the minimum voltage would drop rapidly toward the negative gate limit of the GaN transistor.

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In summary, reducing $L_{\rm ss2}$ along with employing well-designed $C_{\rm gs2-ex}$ (*Stage 2*) and $L_{\rm power}$ (*Stage1 or 2*) exhibits effectiveness in mitigating the false triggering voltage, while relocating $C_{\rm gs-ex}$ and using proper $L_{\rm ss1}$ have limited impacts. Despite the effectiveness of $R_{g2-\rm off}$, there exists a penalty in a narrower negative safe margin of gate terminal.

Although the circuit parameters demonstrate their capability of mitigating the false turn-on, they still have limitations. For instance, when a higher switching speed is required, the false triggering voltage cannot be fully suppressed only by adjusting circuit parameters. Besides, in the applications where the circuit elements of CtrlSW and SyncSW are required to be symmetric (e.g., inverter applications), it is difficult to damp the fluctuation at gate terminal and retain high-voltage slew rate simultaneously. In Si-based bridge-leg, an efficient solution to false turn-on is to employ a large enough negative gate voltage supply (e.g., -5 V) for turn-off [38]. However, when a large negative gate bias is applied on GaN transistor, the minimum value of the false triggering voltage could approach gate terminal's negative limit.

In order to fully damp the false triggering voltage under various circuit conditions, it is essential to investigate into the proper negative gate voltage supplies as well as the ranges of circuit parameters, where the negative gate voltage could be employed to suppress the false turn-on without exceeding the negative gate voltage limit. Fig. 20 displays the upper and lower limits of the negative gate bias when the CtrlSW switches faster under 300 V input voltage ($R_{g1-\rm on}=2\,\Omega$, $dV_{\rm ds1}/dt=110\,\rm V/\,ns$). With negative gate voltage bias changing, the upper limit is reached when the maximum voltage of false triggering voltage pulse equals to $V_{\rm th}$, while the lower limit is attained when the minimum voltage meets the negative gate voltage limit of GaN transistor. The region where the upper limit is above the lower one indicates the ranges of circuit parameters, where it is possible to mitigate the false turn-on by employing a proper negative gate voltage bias. To prevent the false turn-on under fast switching circumstance with a properly designed negative gate voltage supply, $L_{\rm ss}$ should be designed according to Fig. 20 (b), while power-loop inductance smaller than 7 nH is required. With regard to external-added gate-to-source capacitance, the optimum region of $C_{\rm gs2-ex}$ still works, whereas relocating $C_{\rm gs-ex}$ is undependable. In addition, reducing turn-off resistance $R_{g2-\rm off}$ is unreliable neither, since the minimum value drops much faster than the maximum value of the false triggering voltage.

Compared with low-voltage devices, the high-voltage E-mode GaN transistor occupies more space on PCB, on account of relatively large package and heat dissipation requirement [39]. As a result, it is hard to reduce the power-loop inductance to a very low value (e.g., below 5 nH). Thus, general design procedures for GaN-based converters containing bridge-leg configuration circuit are as follows. First, we can start with optimizing the power loop and extracting its inductance. Then, based on the design guidelines obtained from the analytical model, the parameters of gate drive circuit of both CtrlSW and SyncSW can be selected, including $L_{\rm ss}$, $R_{\rm g-off}$, as well as the value and

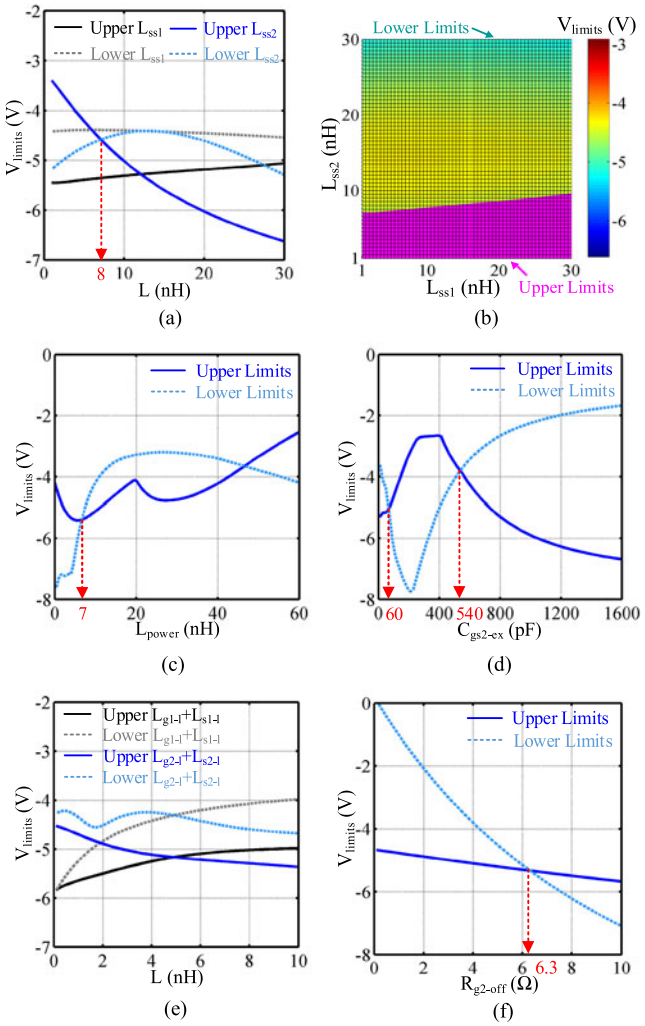

Fig. 20. Upper and lower limits of negative gate voltage bias under different circuit parameters: (a), (b) Source-sense inductance $L_{\rm ss1}$ and $L_{\rm ss2}$; (c) power-loop inductance $L_{\rm power}$; (d) external gate-to-source capacitance of $\rm SW_2$ $\rm C_{gs2-ex}$; (e) positions of $\rm C_{gs1-ex}$ and $\rm C_{gs2-ex}$; (f) turn-off resistance of $\rm SW_2$ $R_{g2-\rm off}$.

location of $C_{\rm gs-ex}$. At last, identifying the maximum and minimum values of the false triggering voltages under the selected circuit parameters, and designing the optimum negative gate voltage bias for turn-off, to simultaneously achieve fast switching speed and suppress the false turn-on.

V. Conclusion

In this paper, a continuous device/circuit analytical model is established to evaluate the false turn-on phenomenon of high-voltage E-mode GaN transistors in bridge-leg configuration. Device models are developed first, which take into account the nonlinear *I–V* and *C–V* characteristics of the high-voltage E-mode GaN transistor. Then, a circuit-level model, combining device behaviors with various circuit parameters, is established. Compared with the piecewise switching process model and PSpice simulation, the proposed model exhibits better performances. A testing circuit with a GaN-based bridge-leg is constructed to measure the critical waveforms with regard to false turn-on evaluation, including displacement current and false triggering voltage pulse. Agreements between experimental results and theoretical analysis validate the proposed model. Owing to the complexity of false turn-on in GaN-based bridge-leg, the impacts of different circuit parameters are investigated, on account of the resonance between the displacement current and gate drive circuit. In order to mitigate the false turn-on problem without compromising the switching speed or exceeding the negative gate voltage limit of GaN transistor, optimization of negative gate voltage bias for turn-off is studied. The results indicate that reducing the SS inductance of SyncSW, adding properly designed external gate–source capacitances, and optimizing the power-loop inductance, along with employing well-designed negative gate voltage bias for turn-off, are the effective methods to mitigate the false turn-on problem.

Appendix

A. Ranges of Parameters Employed in the Equations for Device Modeling

TABLE A (I)
Ranges of Parameters in *I–V* Equations (1)–(5)

F_1 for small-scale adjustment of the saturation region			
M_1, M_5	M_2, M_6	M_3, M_7	M_4, M_8
1–20	0.01–0.2	$-5\times10^{-4}\sim-10^{-4}$	10^{-5}–10^{-4}
F_2 for large-scale adjustment of the saturation region			
M_9	M_{10}	M_{11}	M_{12}
1–10	0.8–1.2	10–20	0.9–1.1
$I_{\rm base}$	F_3 for linear region correction		
β	M_{13}	M_{14}	M_{15}
1–10	0.1–0.5	$-10\sim-1$	1–10
$I_{\rm base}$	F_4 for transition zone adjustment		
λ	M_{16}	M_{17}	M_{18}
3×10^{-5}–10^{-4}	0.01–0.2	0.8–1.2	0.9–1.1

TABLE A (II)
Ranges of Parameters in (6)

n	N_0	$N_{1\rm n}$	$N_{2\rm n}$	$N_{3\rm n}$
3–5	$-0.5\sim0.5$	$-0.5\sim1$	10^{-3}–5×10^{-2}	$-50\sim100$

TABLE A (III)
Ranges of Parameters in C–$V_{\rm ds}$ (7)

Logarithm functions F_5			Base cap.
N	$A_{\rm n}$	$V_{\rm n}$	C_0
3–5	10–100	10–200	*
Gaussian distribution functions F_6			
M	$B_{\rm m}$	$V_{\rm m}$	$\sigma_{\rm m}$
5–15	1–10	–50~50	1–10

Remarks: The units of the modeling result is "pF";
"*" denotes the constant capacitance under high $V_{\rm ds}$.

TABLE A (IV)
RANGES OF PARAMETERS EMPLOYED IN $C_{\rm iss}$–$V_{\rm gs}$ (8)

P_0	F_7 for sharp rise around $V_{\rm th}$		Gaussian functions F_{10}	
P_0	P_1	P_2	k	$B_{\rm k}$
200–500	50–100	50–100	5–10	−10∼20
F_8 and F_9 for variation trend adjustment before and after $V_{\rm th}$				
P_3, P_8	P_4, P_6, P_9	P_5, P_7, P_{10}	$V_{\rm k}$	$\sigma_{\rm k}$
50–100	0.5–1	1–3	−1∼3	0.1–1

Remarks: The unit of the modeling result is "pF."

TABLE A (V)
RANGES OF PARAMETERS EMPLOYED IN (9)

Q_1	Q_2	Q_3	Q_4
−0.5∼0.5	−0.5∼1	10^{-3}–5×10^{-2}	−50∼100

B. Matrix for Iterative Computation

$$A = |AP_1\, AP_2| \tag{B.1}$$

where

$$AP_1 = \begin{vmatrix} A_1 & 0 & 0 & 0 & A_5 & 0 & A_7 & A_8 \\ 0 & \frac{-R_{g1-\rm in}}{L_{l1}} & 0 & \frac{-1}{L_{l1}} & 0 & \frac{1}{L_{l1}} & 0 & 0 \\ 0 & 0 & \frac{-R_{g1}}{L_{\rm dr1}} & 0 & 0 & \frac{-1}{L_{\rm dr1}} & 0 & 0 \\ B_1 & B_2 & 0 & 0 & 0 & 0 & B_7 & 0 \\ C_1 & C_2 & 0 & 0 & 0 & 0 & C_7 & 0 \\ 0 & \frac{-1}{C_{\rm gs1-ex}} & \frac{1}{C_{\rm gs1-ex}} & 0 & 0 & 0 & 0 & 0 \\ D_1 & 0 & 0 & 0 & D_5 & 0 & D_7 & D_8 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{\rm diode1}} & 0 \\ E_1 & 0 & 0 & 0 & E_5 & 0 & E_7 & E_8 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ H_1 & 0 & 0 & 0 & H_5 & 0 & H_7 & H_8 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{vmatrix}$$

$$AP_2 = \begin{vmatrix} A_9 & 0 & 0 & 0 & A_{13} & 0 & A_{15} & A_{16} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ D_9 & 0 & 0 & 0 & D_{13} & 0 & D_{15} & D_{16} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ E_9 & 0 & 0 & 0 & E_{13} & 0 & E_{15} & E_{16} \\ 0 & \frac{-R_{g2-\rm in}}{L_{l2}} & 0 & \frac{1}{L_{l2}} & 0 & \frac{-1}{L_{l1}} & 0 & 0 \\ 0 & 0 & \frac{-R_{g2}}{L_{\rm dr2}} & 0 & 0 & \frac{1}{L_{\rm dr2}} & 0 & 0 \\ F_9 & F_{10} & 0 & 0 & 0 & 0 & F_{15} & 0 \\ G_9 & G_{10} & 0 & 0 & 0 & 0 & G_{15} & 0 \\ 0 & \frac{1}{C_{\rm gs2-ex}} & \frac{-1}{C_{\rm gs2-ex}} & 0 & 0 & 0 & 0 & 0 \\ H_9 & 0 & 0 & 0 & H_{13} & 0 & H_{15} & H_{16} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{C_{\rm diode2}} & 0 \end{vmatrix}$$

$$B = \left[\frac{V_{\rm BUS}}{p_3} 0 \frac{V_{\rm dd1}}{L_{\rm dr1}}\ B_7 I_{\rm ch1} C_7 I_{\rm ch1} 0 \frac{V_{\rm BUS} p_1}{p_3(p_1+q_1)} 0 \right.$$
$$\left. \frac{V_{\rm BUS}}{p_3} 0 \frac{V_{\rm dd2}}{L_{\rm dr2}} 0 0 \frac{V_{\rm BUS} p_2}{p_3(p_2+q_2)} \frac{-I_f}{C_{\rm diode2}}\right]^T \tag{B.2}$$

$$A_1 = -R_1/p_3 \tag{B.3}$$
$$A_5 = -q_1/[p_3(p_1+q_1)] \tag{B.4}$$
$$A_7 = R_1/p_3 - p_1 R_3/[p_3(p_1+q_1)] \tag{B.5}$$
$$A_9 = -R_2/p_3 \tag{B.6}$$
$$A_8 = -p_1/p_3(p_1+q_1) \tag{B.7}$$
$$A_{13} = -q_2/[p_3(p_2+q_2)] \tag{B.8}$$
$$A_{15} = R_2/p_3 - p_2 R_4/[p_3(p_2+q_2)] \tag{B.9}$$
$$A_{16} = -p_2/[p_3(p_2+q_2)] \tag{B.10}$$
$$B_1 = C_{\rm gd1}/(C_{\rm gd1}C_{\rm gs1} + C_{\rm ds1}C_{\rm gd1} + C_{\rm ds1}C_{\rm gs1}) \tag{B.11}$$
$$B_2 = (C_{\rm gd1} + C_{\rm ds1})/(C_{\rm gd1}C_{\rm gs1} + C_{\rm ds1}C_{\rm gd1} + C_{\rm ds1}C_{\rm gs1}) \tag{B.12}$$
$$B_7 = -C_{\rm gd1}/(C_{\rm gd1}C_{\rm gs1} + C_{\rm ds1}C_{\rm gd1} + C_{\rm ds1}C_{\rm gs1}) \tag{B.13}$$
$$C_1 = (C_{\rm gd1} + C_{\rm gs1})/(C_{\rm gd1}C_{\rm gs1} + C_{\rm ds1}C_{\rm gd1} + C_{\rm ds1}C_{\rm gs1}) \tag{B.14}$$
$$C_2 = C_{\rm gd1}/(C_{\rm gd1}C_{\rm gs1} + C_{\rm ds1}C_{\rm gd1} + C_{\rm ds1}C_{\rm gs1}) \tag{B.15}$$
$$C_7 = -(C_{\rm gd1} + C_{\rm gs1})/(C_{\rm gd1}C_{\rm gs1} + C_{\rm ds1}C_{\rm gd1} + C_{\rm ds1}C_{\rm gs1}) \tag{B.16}$$
$$D_1 = -p_1 R_1/[p_3(p_1+q_1)] \tag{B.17}$$
$$D_5 = 1/(p_1+q_1) - p_1 q_1/[p_3(p_1+q_1)^2] \tag{B.18}$$
$$D_7 = \{-R_3 + p_1[R_1 - p_1 R_3/(p_1+q_1)]/p_3\}/(p_1+q_1) \tag{B.19}$$
$$D_8 = -1/(p_1+q_1) - p_1^2/[p_3(p_1+q_1)^2] \tag{B.20}$$
$$D_9 = -p_1 R_2/[p_3(p_1+q_1)] \tag{B.21}$$
$$D_{13} = -p_1 q_2/[p_3(p_1+q_1)(p_2+q_2)] \tag{B.22}$$
$$D_{15} = p_1[R_2 - p_2 R_4/(p_2+q_2)]/[p_3(p_1+q_1)] \tag{B.23}$$
$$D_{16} = -p_1 p_2/[p_3(p_1+q_1)(p_2+q_2)] \tag{B.24}$$
$$E_1 = -R_1/p_3 \tag{B.25}$$
$$E_5 = -q_1/[p_3(p_1+q_1)] \tag{B.26}$$
$$E_7 = R_1/p_3 - p_1 R_3/[p_3(p_1+q_1)] \tag{B.27}$$
$$E_8 = -p_1/[p_3(p_1+q_1)] \tag{B.28}$$
$$E_{13} = -q_2/[p_3(p_2+q_2)] \tag{B.29}$$
$$E_9 = -R_2/p_3 \tag{B.30}$$
$$E_{16} = -p_2/[p_3(p_2+q_2)] \tag{B.31}$$

$$E_{15} = R_2/p_3 - p_2R_4/[p_3(p_2+q_2)] \quad \text{(B.32)}$$

$$F_9 = C_{\rm gd2}/(C_{\rm gd2}C_{\rm gs2} + C_{\rm ds2}C_{\rm gd2} + C_{\rm ds2}C_{\rm gs2}) \quad \text{(B.33)}$$

$$F_{10} = -(C_{\rm gd2} + C_{\rm ds2})/(C_{\rm gd2}C_{\rm gs2} + C_{\rm ds2}C_{\rm gd2} + C_{\rm ds2}C_{\rm gs2}) \quad \text{(B.34)}$$

$$F_{15} = -C_{\rm gd2}/(C_{\rm gd2}C_{\rm gs2} + C_{\rm ds2}C_{\rm gd2} + C_{\rm ds2}C_{\rm gs2}) \quad \text{(B.35)}$$

$$G_9 = (C_{\rm gd2} + C_{\rm gs2})/(C_{\rm gd2}C_{\rm gs2} + C_{\rm ds2}C_{\rm gd2} + C_{\rm ds2}C_{\rm gs2}) \quad \text{(B.36)}$$

$$G_{10} = -C_{\rm gd2}/(C_{\rm gd2}C_{\rm gs2} + C_{\rm ds2}C_{\rm gd2} + C_{\rm ds2}C_{\rm gs2}) \quad \text{(B.37)}$$

$$G_{15} = -(C_{\rm gd2} + C_{\rm gs2})/(C_{\rm gd2}C_{\rm gs2} + C_{\rm ds2}C_{\rm gd2} + C_{\rm ds2}C_{\rm gs2}) \quad \text{(B.38)}$$

$$H_1 = -p_2R_1/[p_3(p_2+q_2)] \quad \text{(B.39)}$$

$$H_5 = -p_2q_1/[p_3(p_1+q_1)(p_2+q_2)] \quad \text{(B.40)}$$

$$H_7 = p_2[R_1 - p_1R_4/(p_1+q_1)]/[p_3(p_2+q_2)] \quad \text{(B.41)}$$

$$H_8 = -p_1p_2/[p_3(p_1+q_1)(p_2+q_2)] \quad \text{(B.42)}$$

$$H_9 = -p_2R_2/[p_3(p_2+q_2)] \quad \text{(B.43)}$$

$$H_{13} = \{1 - p_2q_2/[p_3(p_2+q_2)]\}/(p_2+q_2) \quad \text{(B.44)}$$

$$H_{15} = \{-R_4 + p_2[R_2 - p_2R_3/(p_2+q_2)]/p_3\}/(p_2+q_2) \quad \text{(B.45)}$$

$$H_{16} = \{-1 - p_2^2/[p_3(p_2+q_2)]\}/(p_2+q_2), \quad \text{(B.46)}$$

where

$$\begin{aligned}
L_{dr1} &= L_{g1} + L_{ss1};\\
L_{l1} &= L_{g1-l} + L_{s1-l} + L_{g1-\rm in} + L_{\rm ss1-in};\\
L_{\rm dr2} &= L_{g2} + L_{\rm ss2};\\
L_{l2} &= L_{g2-l} + L_{s2-l} + L_{g2-\rm in} + L_{\rm ss2-in};\\
p_1 &= L_{d1-\rm in} + L_{s1-\rm in};\\
p_2 &= L_{d2-\rm in} + L_{s2-\rm in};\\
q_1 &= L_{c1} + L_{a1};\\
q_2 &= L_{c2} + L_{a2};\\
p_3 &= \frac{p_1q_1}{p_1+q_1} + \frac{p_2q_2}{p_2+q_2} + L_{d1-\rm ex} + L_{s1-\rm ex}\\
&\quad + L_{d2-\rm ex} + L_{s2-\rm ex}.
\end{aligned}$$

C. Equations for Gate-Loop's Impedance

$$H_0 = R_{g2-\rm in} + R_{g2} \quad \text{(C.1)}$$

$$H_1 = L_{l2} + L_{\rm dr2} + R_{g2-\rm in}R_{g2}C_{\rm gs2-ex} \quad \text{(C.2)}$$

$$H_2 = (R_{g2}L_{l2} + R_{g2-\rm in}L_{\rm dr2})C_{\rm gs2-ex} \quad \text{(C.3)}$$

$$H_3 = L_{l2}L_{\rm dr2}C_{\rm gs2-ex} \quad \text{(C.4)}$$

$$J_0 = 1 \quad \text{(C.5)}$$

$$J_1 = R_{g2}C_{gs2} + R_{g2}C_{gs2-\rm ex} + R_{g2-\rm in}C_{\rm gs2} \quad \text{(C.6)}$$

$$J_2 = L_{\rm dr2}C_{\rm gs2} + L_{\rm dr2}C_{\rm gs2-ex} + R_{g2-\rm in}R_{g2}C_{gs2}C_{gs2-\rm ex} + L_{l2}C_{\rm gs2} \quad \text{(C.7)}$$

$$J_3 = R_{g2-\rm in}L_{\rm dr2}C_{\rm gs2}C_{\rm gs2-ex} + R_{g2-\rm in}L_{l2}C_{\rm gs2}C_{\rm gs2-ex} \quad \text{(C.8)}$$

$$J_4 = L_{l2}L_{\rm dr2}C_{\rm gs2}C_{\rm gs2-ex} \quad \text{(C.9)}$$

where

$$\begin{aligned}
L_{l2} &= L_{g2-l} + L_{s2-l} + L_{g2-\rm in} + L_{\rm ss2-in};\\
L_{\rm dr2} &= L_{g2} + L_{\rm ss2}.
\end{aligned}$$

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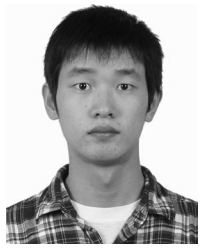

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An Analytical Model for False Turn-On Evaluation of High-Voltage Enhancement-Mode GaN Transistor in Bridge-Leg Configuration

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Thermal dirençleri dışında tüm karakteristiği bizimkiyle aynı

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Capacitance modelling

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Vgs'deki dalgalanmaların nasıl kontrol altına alınacağı hakkında

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