Comparing and Modeling Power GaN FETs for Switching Converter Applications

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Abstract

To use new wide bandgap power devices in power conversion applications, designers must integrate behavioral models that provide accurate representations of electrical characteristics into their designs. This work surveyed the electrical characteristics, and simulation models, as well as studying the switching performance of commercial and laboratory-fabricated GaN FETs. The results show that the commercial GaN FETs have superior switching performance, whereas the laboratory GaN FETs still have room for improvement.

Keywords: GaN FETs, E-mode, cascode, SPICE model

Introduction

Si is approaching its physical limitations, and wide bandgap devices consisting of gallium nitride (GaN) or silicon carbide (SiC) have superior material properties that make them the most suitable candidates to replace Si-based transistors [1]. Because using these new power devices in GaN-based switching converter applications may be challenging [2], building a compact model is necessary. Many GaN field-effect transistor (FET) manufacturers, such as EPC [3], GaN Systems [4], Panasonic [5], Transphorm [6], Texas Instruments [7], and VisIC [8], have published the device circuit models for their power transistors. This evidences that device models play an important role in circuit design and application. This work is a survey of commercially available GaN power transistors, their device models, and the gate drive circuit for driving their devices. Moreover, laboratory-fabricated GaN FETs and their compatible drives are presented for comparison, and double-pulse testers are used to evaluate the switching performance.

Power Transistor Characteristics, Device Models, and Gate Drive Circuits

A. Comparison of Device Parameters

The devices under consideration are GaN FETs. To compare switching performance, Cool MOSFETs with similar voltage ratings and R_{on} were chosen for comparison. Table I compares the device parameters for the commercial E-mode GaN (#1 [4], #2 [5]), cascode GaN FETs (#1 [6]), SiC, and Cool MOSFETs as well as the laboratory-fabricated cascode GaN FET. E-mode GaN devices have less parasitic inductance and capacitance because of the surface-mount package and material behavior. Moreover, the smaller R_{on} and gate charge afford them a superior figure of merit. However, their low threshold voltage (V_{TH}) and specific gate voltage rating limitations require more consideration in designing gate drives. Unlike E-mode GaN, cascode GaN FETs are compatible with existing gate drives for Si-based MOSFETs. Both E-mode and cascode GaN devices have better figures of merit than the other devices under comparison and can achieve faster switching and higher efficiency. The device under test, a laboratory-fabricated cascode GaN FET (#2 [9]), is shown in Fig. 1.

B. Device Model

GaN Systems [4], Panasonic [5], and Transphorm [6] have published their power transistor models. The device models for EPC, Texas Instruments, and VisIC are not under consideration because the Texas Instruments and VisIC models involve encryption, and the EPC device model is similar to that of GaN Systems with a voltage rating suited to low voltage applications. The main components and parameters of the device models proposed by these manufacturers are a voltage controlled current source (I_{DS}), nonlinear capacitors (C_{GD}, C_{GS}, and C_{DS}), parasitic package resistance (R_G, R_D, and R_S), and parasitic inductance (L_G, L_D, and L_S). Details are provided as follows.

a) Voltage-Controlled Current Source

A voltage-controlled current source is controlled by voltage V_{GS} and V_{DS}, which can be expressed by a MOSFET- or JFET-based model or nonlinear current represented by the analog behavior model of SPICE with the voltage-dependent shaping function. To take advantage of the behavioral modeling built into most modern SPICE simulators, GaN Systems provides models for its transistors, which represent the current source as

$$i_D = [k_2 - k_3(T-25)] \times \log(1+\exp((k_4 v(g,s) - k_5)/k_6)) \times [v(d,s)/(1+\max(k_7 + k_8 v(g,s), k_9) \times v(d,s))] \quad (1)$$

where k_i ($1 \leqq i \leqq 9$) represents constant parameters.

Panasonic uses the JFET model for describing the voltage-controlled current source [5], whereas Transphorm uses the Level-1 MOSFET model cascode with the JFET model [6]. The JFET equation in SPICE for the DC current is expressed as

Cutoff region : $V_{gs} \leq V_{TH}$,

$$I_d = 0 \quad (2a)$$

Linear region : $V_{ds} \leq V_{gs} - V_{TH}$,

$$I_d = \beta \times [2 \times (1 + \lambda \times V_{ds}) \times (V_{gs} - V_{TH}) \times V_{ds} - V_{ds}^2] \quad (2b)$$

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Saturation region : $0 < V_{gs} - V_{TH} < V_{ds}$,

$$I_d = \beta \times (1 + \lambda \times V_{ds}) \times (V_{gs} - V_{TH})^2 \quad (2c)$$

where β is the transconductance coefficient, and V_{TH} is the threshold voltage. The equation characterized by the Level-1 MOSFET model is identical to (2), with the exception that parameter β is replaced by 1/2 K_P, where K_P is the transduced value, and λ is the short-channel width-modulation slope coefficient in the saturated region.

b) Nonlinear Capacitors

The nonlinear capacitance characteristics [10] are modeled using semiempirical fits to obtain capacitance versus voltage data. Some methods are provided for defining the curves of nonlinear capacitors, which can be approximated as a linear combination of two exponential terms [12] or an arc tangent formula [13]. These functions provide a close fit to the data. GaN Systems implements a voltage-dependent charge source as the nonlinear capacitance:

$$Q = k_1 \log(1 + \exp((k_2 v(n_1, n_2) - k_3)/k_4)) + k_5 \log(1 + \exp((k_6 v(n_1, n_2) - k_7)/k_8)) \quad (3)$$

where k_i ($1 \leqq i \leqq 8$) denotes constant parameters, and n_i represents nodes of the gate, drain, or source.

Panasonic uses two individual paralleled JFET models to describe the nonlinear capacitance (C_{GS}, C_{GD}) and one diode to describe C_{DS}. Transphorm refers to the MOSFET model described in an application note [14], proposing a diode model for representing the voltage dependency of capacitance and combining three serial JFETs with different threshold voltages to describe the overall parasitic capacitance contour. The capacitance can be expressed as

$$C_{gs} = C_{gso} \cdot W \quad (4a)$$

$$C_{gs} = \frac{C_{gs}}{\left(1 - \frac{V_{gs}}{PB}\right)^{-M}} \quad (4b)$$

$$C_{gd} = \frac{C_{gd0}}{\left(1 - \frac{V_{ds}}{V_j}\right)^{-M}} \quad (4c)$$

$$C_{ds} = \frac{C_{ds0}}{\left(1 - \frac{V_{ds}}{V_j}\right)^{-M}} \quad (4d)$$

Table II summarizes the parasitic capacitance constructed in the GaN FET models. Test circuits [15] were used to evaluate the model provided by the manufacturer. The evaluated electrical characteristics include transfer characteristics (V_{GS} − I_{DS}), gate charge (Q_{GS} − V_{GS}), and parasitic capacitance (C_{iss} = C_{gs} + C_{gd}, C_{oss} = C_{gd} + C_{ds}, and C_{rss} = C_{gd}).

Results and Discussion

Fig. 2 shows the transfer characteristic curve (V_{GS}–I_{DS}) for the simulation and datasheet. The simulation results are in agreement with the datasheet, except that the curve of GaN Systems is lower for the simulation than for the datasheet, which can result in erroneous predictions of the plateau voltage (V_{PL}). The value of the plateau voltage can be determined from the device transfer characteristic graph. With a test drain-to-source current of 10 A and drain voltage of 100 V, the V_{PL} of CoolMOS is the highest (4.8 V), followed by the Transphorm (3.6 V), The laboratory-fabricated cascode GaN FET (2.9 V), and Panasonic (2.6 V). GaN Systems (2.3 V) has the lowest V_{PL}.

Fig. 3 shows the simulation results for Q_{GS} versus V_{GS} with a drain-to-source current of 10 A, and drain voltage of 100 V. The values of the plateau voltage are the same for all devices, as the transfer characteristic curve shows. Compared with the CoolMOS, GaN FETs require a lower total gate charge (Q_G) to charge and discharge the input capacitance (C_{iss}) of the transistors, which can enable faster switching.

Fig. 4 shows the measured parasitic capacitance. The laboratory-fabricated cascode GaN FET has the largest input parasitic capacitance (C_{iss}) compare to commercial E-mode GaN and CoolMOS. The input parasitic capacitance of the cascode LV MOSFET dominates the input parasitic capacitance value; therefore, the optimal LV MOSFET should be chosen. Nevertheless, it is still better than the CoolMOS when considering the Q_{GD} charge. Fig. 5 compares the Miller charge (Q_{GD}) of cascode GaN FET #1, cascode GaN FET #2, and CoolMOS. The Q_{GD} charge of cascode GaN FET #1 ($Q_{GD\_GaN\ FET\#1@100V}$ = 2.07 nC) is lower than cascode GaN FET #2 ($Q_{GD\_GaN\ FET\#2@100V}$ = 3.66 nC) and CoolMOS ($Q_{GD\_CoolMOS@100V}$ = 16.39 nC). Less Q_{GS} means that it has shorter current transition period, and less Miller charge shows that it has shorter voltage transition period.

Conclusions

This study surveyed the electrical characteristics, simulation models, as well as their switching performance. GaN FETs with lower parasitic capacitance performance have lower gate charge requirements, enabling faster switching. The laboratory-fabricated cascode GaN FET has the largest input parasitic capacitance (C_{iss}) should choose an optimal LV MOSFET to improve the switching performance.

References

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in *IEEE Transactions on Power Electronics, vol. 29, no. 5*, pp. 2155-2163, May 2014.

[2] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics* 4.3., pp. 707–719, 2016.

[3] EPC eGaN products, [Online]. Available: http://epc-co.com.

[4] GaN systems products GS66508T, [Online]. Available: http://www.gansystems.com/gs66508t.php.

[5] Panasonic GaN products PGA26E19BA, [Online]. Available: http://www.semicon.panasonic.co.jp.

[6] Transphorm GaN products TPH3006PS, [Online]. Available: www.transphormusa.com.

[7] Texas Instruments GaN products, [Online]. Available: http://www.ti.com/lit/ds/symlink/lmg3410.pdf.

[8] VisIC GaN products, [Online]. Available: http://visic-tech.com.

[9] P. C. Chou, and S. Cheng, "Performance characterization of gallium nitride HEMT cascode switch for power conditioning applications," *Materials Science and Engineering:B*, pp. 43–50, 2015.

[10] ON Semiconductor, "MOSFET Gate-Charge Origin and its Applications," AND9083/D Datasheet, Aug., 2014 – Rev. 1. [Online]. Available: www.onsemi.com.

[11] Infineon Cool MOS products IPP60R099C6, [Online].

Available: http://www.infineon.com.
[12] G. Di Capua and N. Femia. "A Versatile Method for MOSFETs Commutations Analysis in Switching Power Converters Design," *IEEE Transactions on Power Electronics*, *vol. 29, no. 2*, pp. 920–935, 2014.
[13] LTspice IV, M. MOSFET. Help Manual, Linear Technology Corporation, Milpitas, CA, USA, 1998–2013.
[14] "Description of the ON Semiconductor MOSFET Model," Application note AND9033, Semiconductor Components Industries, LLC, 2011. November, 2011 − Rev. 1. 1. [Online]. Available: www.intusoft.com.
[15] M. A. Broadmeadow, "Characterisation of the cascode gate drive of power MOSFETs in clamped inductive switching applications," Ph.D. dissertation, Dept. Elect. Eng., Queensland Univ., Brisbane, Australia, 2015.

TABLE I
COMPARISON OF DEVICE PARAMETERS: E-MODE GAN, CASCODE GAN, SIC, AND COOL MOSFET

	E-mode GaN		Cascode GaN		Cool
	#1 [4]	#2 [5]	#1 [6]	#2 [9]	MOS[11]
V_{DSS} (V)	650	600	600	600	650
R_{ON}(mΩ)	50	140	150	210	99
V_{TH} (V) Typ.	1.7	1.2	1.8	1.9	3
Max. V_{GS} rating(V)	7	4.5	18	18	20
Recommend V_{GS} (V)	6	3	8	8	12
Q_{gs} (nC)	2.2	0.7	2.1	12.5	14
Q_{gd} (nC)	1.8	2.6	2.2	5	61
FOM	145	413	487.5	1995	6732

TABLE II
COMPARISON OF NONLINEAR PARASITIC CAPACITANCE CONSTRUCTED IN DEVICE MODELS

	E-mode GaN		Cascode GaN	
	#1 [4]	#2 [5]	#1 [6]	#2 [9]
C_{GS}	voltage dependent charge source (3)	JFET internal capacitance (4b)	MOSFET internal capacitance connect with JFET internal Capacitance (4a)	
C_{GD}		JFET internal capacitance (4c)	diode internal capacitance connect with JFET internal Capacitance (4b)	
C_{DS}		diode internal capacitance (4d)	diode internal capacitance connect with JFET internal Capacitance (4d)	

Fig. 1 Laboratory-fabricated cascode GaN FET [9].

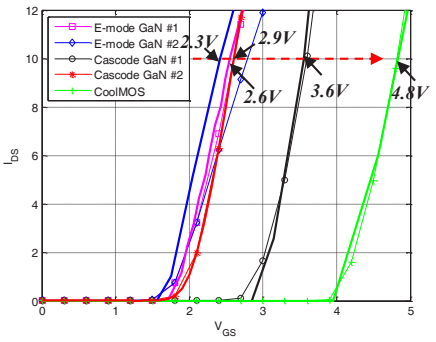

Fig. 2 Transfer characteristic curve (V_{GS}−I_{DS}) of GaN FET devices. (Symbols: simulation; solid lines: datasheet.)

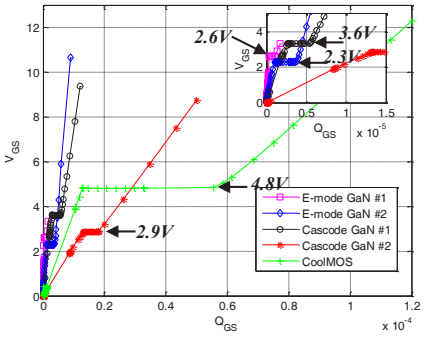

Fig. 3 Gate charge curve (Q_{GS}−V_{GS}) of GaN FET devices. (Symbols: simulation.)

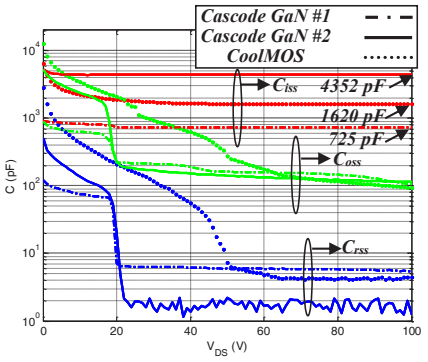

Fig. 4 Comparison of measured parasitic capacitance.

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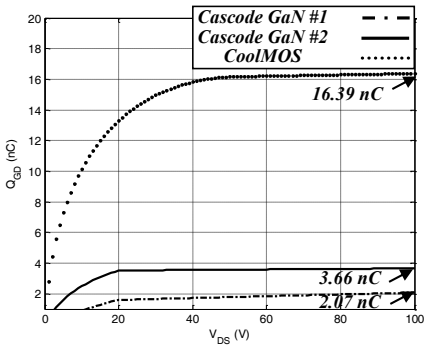

Fig. 5 Miller charge (Q_{GD}) comparison.