

Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic R_{ON} Characterization and Circuit Design Considerations

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Abstract—The systematic characterization of a 650-V/13-A enhancement-mode GaN power transistor with p-GaN gate is presented. Critical device parameters such as ON-resistance R_{ON} and threshold voltage V_{TH} are evaluated under both static and dynamic (i.e., switching) operating conditions. The dynamic R_{ON} is found to exhibit different dependence on the gate drive voltage V_{GS} from the static R_{ON} . While reasonably suppressed at higher V_{GS} of 5 and 6 V, the degradation in dynamic R_{ON} is significantly larger at lower V_{GS} of 3–4 V, which is attributed to the positive shift in V_{TH} under switching operations. In addition to characterization of discrete devices, a custom-designed double-pulse test circuit with 400-V, 10-A test capability is built to evaluate the transient switching performance of the p-GaN gate power transistors. Optimal gate drive conditions are proposed to: 1) provide sufficient gate over-drive to minimize the impact of the V_{TH} shift on the dynamic R_{ON} ; and 2) leave enough headroom to save the device from excessive gate stresses. Moreover, gate drive circuit design and board layout considerations are also discussed by taking into account the fast switching characteristics of GaN devices.

Index Terms—Design consideration, dynamic R_{ON} , p-GaN gate high-electron-mobility transistors (HEMTs), V_{TH} instability.

I. INTRODUCTION

ALGaN/GaN-ON-SI high-electron-mobility transistors (HEMTs), with the merit of low ON-resistance R_{ON} , fast switching speed, and high-temperature operation capabilities, are promising candidates for the next-generation power switches that enable power electronics systems with substantially increased efficiency and power density. However, they are intrinsically normally on devices because of the high-density 2-D electron gas (2DEG) induced by strong polarization effects. In practical applications, the enhancement-mode (E-mode) devices with positive threshold voltages V_{TH} are preferred over

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TABLE I
COMPARISON OF DEVICE PARAMETERS: STATE-OF-THE-ART SI POWER MOSFET, CASCODE GAN SWITCH, AND p-GaN GATE HEMT

Device technology	Si SJ MOSFET	Cascode GaN switch	p-GaN gate HEMT
Part #	IPP65R125C7	TPH3208PS	This work
Voltage rating (V)	650	650	650
R_{ON} (Ω)	0.125	0.11	0.125
Q_G (nC)	35	10	2
$C_{OSS,er}$ (pF)	53	82	38
$C_{OSS,tr}$ (pF)	579	132	60
Q_{rr} (nC)	7000	54	~ 0
V_{GS} limit (V)	± 20	± 18	$< \pm 10$
V_{TH} (V) @ $I_D = 1$ mA	4	2.1	1.2
I_{GSS} (μA) at $V_{DS} = 0$ V	< 0.1 at $V_{GS} = 20$ V	< 0.1 at $V_{GS} = 18$ V	< 100 at $V_{GS} = 7$ V

*All the devices are in the TO-220 package. Q_G , $C_{OSS,er}$, $C_{OSS,tr}$, and Q_{rr} are extracted with $V_{DS} = 400$ V.

the depletion-mode (D-mode) ones owing to their inherent fail-safe operation (i.e., normally off) and simpler gate control scheme.

To achieve normally-off operation, two different approaches are being deployed in commercially available GaN power transistors. A high-voltage D-mode GaN transistor can be combined with a low-voltage E-mode Si MOSFET to realize a two-chip cascode switch [1]–[3]. A single-chip E-mode GaN power transistor can be fabricated using p-GaN gate technique [3]–[7], gate recess [7]–[9] or plasma treatment [10]–[12]. Table I compares the device parameters of a cascode GaN switch [13] and a p-GaN gate HEMT. State-of-the-art Si superjunction (SJ) MOSFET [14] is also listed as reference. The cascode switch provides a major benefit of driving the Si MOSFET with existing gate drive ICs. While being a decent transitional solution at the early stage of GaN commercialization in power electronic applications, this two-chip configuration inevitably increases package complexity, and therefore cost. Moreover, the relatively large parasitic inductances and the charge mismatch issue not only limit the switching speed of cascode devices, but can lead to undesirable oscillations during switching transients, which will hurt the device reliability and increase switching losses [15], [16]. As another technique widely adopted by device manufacturers and research institutes, the p-GaN gate HEMT features

TABLE II
GATE CHARACTERISTICS OF DIFFERENT P-GAN DEVICES

Manufacturer	V_{TH} (V)	I_D/I_G at $V_{GS} = 6$ V	$V_{GS\min}/(V)$ $V_{GS\max}/(V)$	Gate drive voltage (V)
EPC [22]	1.4	$10^3 - 10^4$	-4/6	4 ~ 5
Panasonic [23]	1.2	$10^2 - 10^{3*}$	-10/4.5	3 ~ 5
GaN Systems [24]	1.3	$10^5 - 10^6$	-10/7	5 ~ 6.5
IMEC [7]	~2.0	$10^5 - 10^{10}$	-/12	-
FBH Berlin [6], [18], [25]	~1.0	$10^3 - 10^4$	-/~7	5

*Data obtained under $V_{GS} = 4.5$ V, the maximum allowable gate voltage for the Panasonic device.

a p-doped (Al)GaN layer on top of the AlGaN barrier to deplete the 2DEG channel at zero gate bias. Compared to cascode switches, these single-chip devices have significant less parasitic inductances and are able to deliver further improved $R_{ON} \cdot Q_G$ figure of merit.

Compared to cascode devices adopting a gate drive voltage of 10–12 V [17] (similar to Si power MOSFETs), the p-GaN devices are usually driven at much lower voltages because of their distinct gate characteristics. On one hand, only a small gate drive voltage is required to fully enhance their channel conductivity because of the relatively low V_{TH} and high transconductance (g_m), which is attributed to the high electron mobility (~ 2000 cm 2 /V·s) of the 2DEG channel. On the other hand, these devices have a tighter gate voltage limitation, as the gate leakage current would increase to a level that could degrade gate junction reliability or even lead to gate breakdown and device failure under large forward gate bias (e.g., > 10 V) [7], [18]–[21].

The gate characteristics (such as V_{TH} , V_{GS} limitation, and gate leakage current I_{GSS}) of p-GaN devices are closely related to the structure of the gate stack [19]–[21], [25], [26] (including the choice of gate metal, thickness and p-doping concentration of the p-GaN layer, as well as thickness and Al composition of the AlGaN barrier layer), and their processing conditions (e.g., metal deposition method, annealing conditions, etc.), all of which could vary with different manufacturers. Table II summarizes the critical parameters of several p-GaN gate HEMTs that have emerged in the market only in recent years. The eGaN FETs from EPC are usually driven at 4–5 V, considering a maximum gate voltage of 6 V [22], [27], [28]. GaN Systems recommends a gate drive voltage of 5–6.5 V for their devices, with an absolute limitation of 7 V at 25 °C [24], [29]. Meanwhile, a gate drive voltage of 4–5 V is used in most of the reported circuit demonstrations implementing Panasonic devices. An even lower V_{TH} of 3 V is adopted in some cases [30]–[33]. In general, for devices provided by different vendors, the suggested gate drive voltage varies accordingly within the range of 3–6.5 V. Yet a deeper understanding of their gate characteristics and a more generic guideline for selecting proper gate drive voltages for p-GaN devices, which is of significant importance to maximizing their performance advantages in power electronic circuits/systems, are still lacking to date.

Apart from the distinct gate characteristics under static conditions, critical parameters of currently available p-GaN devices are subject to the influence of various trapping effects

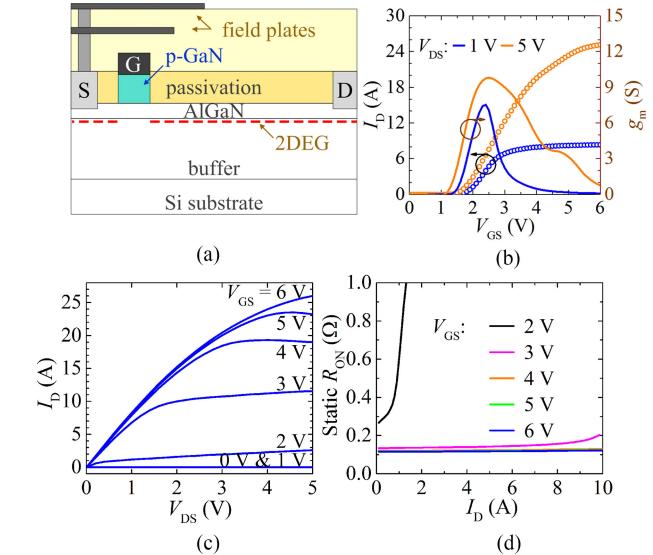


Fig. 1. (a) Cross-sectional schematic of the 650 V/13 A p-GaN gate HEMT. (b) Transfer curve of the p-GaN gate HEMT, (c) output curves, and (d) static R_{ON} versus I_D with different V_{GS} from 2 to 6 V at room temperature.

[6], [7], [18]–[20], [34], [35] under dynamic operation conditions. The resulting dynamic R_{ON} degradation and V_{TH} instability would further affect the circuit performance, and thus, must be taken into consideration when designing GaN-based power converters. While dynamic R_{ON} degradation induced by current collapse is being actively studied, the V_{TH} instability in p-GaN devices, as well as its impact on the dynamic R_{ON} , has seldom been discussed.

In this work, a 650-V/13-A p-GaN gate HEMT is characterized under static and dynamic operating conditions. The dynamic R_{ON} degradation is evaluated under different gate drive voltages by considering the influence of current collapse and V_{TH} instability. In addition to the device-level characterization (see Section II), a double-pulse test circuit is implemented to investigate its switching performance (see Section III). Aimed at fully leveraging the performance advantages of p-GaN devices and minimizing the influence of V_{TH} instability on circuit performance, guidelines for selecting the optimum gate drive voltages are presented, as well as other design considerations that facilitate their fast switching characteristics.

II. STATIC AND DYNAMIC DEVICE CHARACTERIZATION

Fig. 1(a) shows the schematic cross section of the 650 V/13 A p-GaN gate HEMT studied in this paper. Critical device parameters such as R_{ON} and V_{TH} are characterized in both static and dynamic conditions. The physical mechanism for the V_{TH} instability is revealed, and its impact on device dynamic R_{ON} is also discussed.

A. Static I–V Characteristics

Transfer and output characteristics of the device under test (DUT) [see Fig. 1(b) and (c)] are measured using the Agilent B1505A power device analyzer. The device features a V_{TH} of 1.23 V (at $I_D = 1$ mA, with $V_{GS} = V_{DS}$), and a static R_{ON} around 125 mΩ (at $V_{GS} = 6$ V, $V_{DS} = 1$ V). From Fig. 1(d)

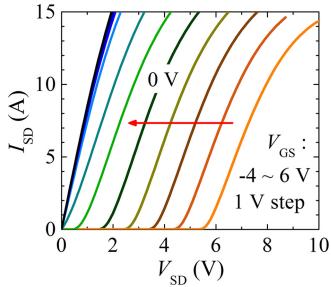


Fig. 2. $I-V$ characteristics of the DUT in reverse conduction mode.

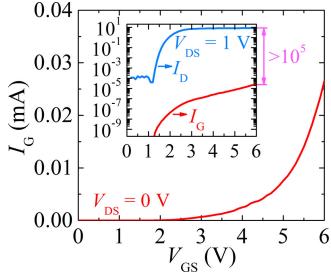


Fig. 3. Forward $I_G - V_{GS}$ characteristics of the DUT ($V_{DS} = 0$ V). Inset: semi-log plot of $I_G - V_{GS}$ ($V_{DS} = 0$ V) and $I_D - V_{GS}$ ($V_{DS} = 1$ V).

which plots the $R_{ON} - I_D$ relationship with V_{GS} ranging from 2 to 6 V, the static R_{ON} virtually saturates after V_{GS} reaches 4 V. According to the static characteristics, the device only needs a small gate drive voltage of 4 V (compared to 10–12 V for Si power MOSFETs, and 20 V for SiC MOSFETs) to fully enhance its channel conductivity and achieve minimum conduction loss.

In addition to forward $I-V$ characteristics, the reverse conduction performance of p-GaN gate HEMTs is also different from Si counterparts because of their distinct device structures. In contrast to vertical Si power MOSFETs, GaN power switches are lateral devices based on unintentionally doped AlGaN/GaN lateral heterojunctions, which conduct current through the high-mobility 2DEG channel. Consequently, they do not have the body diode resulting from the parasitic p-n junction in conventional Si power MOSFETs, which contributes to an extremely low (nearly zero) reverse recovery charge (Q_{rr}), a highly desirable feature in synchronous rectification or bidirectional conduction applications. In reverse conduction mode, the current flows from source to drain through the 2DEG channel when V_{GD} is larger than V_{TH} . Fig. 2 plots the reverse conduction characteristics of the DUT. With negative V_{GS} , the voltage drop on the switch is increased accordingly by an offset.

B. Gate Leakage Characteristics

Compared to Si power MOSFETs and cascode GaN switches, p-GaN devices are known to have a relatively vulnerable gate with rather tight gate voltage limitations (see Table I). As a result, their gate leakage characteristics, which often vary with different manufacturers, have substantial influence on the choice of gate drive voltages. Devices with larger I_G (such as those from Panasonic and EPC) tend to have tighter V_{GS} limitations and are driven with lower voltages, whereas those with smaller I_G (e.g., GaN Systems devices) usually allow a higher gate drive voltage and greater V_{GS} tolerance (see Table II). Fig. 3 plots the

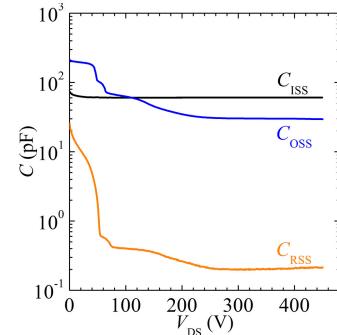


Fig. 4. $C-V$ characteristics of the device. $C_{ISS} = C_{GS} + C_{GD}$, $C_{OSS} = C_{DS} + C_{GD}$, and $C_{RSS} = C_{GD}$.

$I_G - V_{GS}$ curve of the DUT. At $V_{GS} = 6$ V, I_G is still more than five orders of magnitude lower than I_D , similar to devices from GaN Systems [24]. This I_G/I_D ratio is only $\sim 1\%$ of EPC devices [22]. Such a small gate leakage current suggests that the metal-p-GaN contact of the DUT is Schottky-like (rather than ohmic-like) [21], [26].

C. C-V Characteristics

$C-V$ characteristics of the DUT are measured using the Agilent B1505A power device analyzer. The three interelectrode capacitances C_{GS} , C_{GD} , and C_{DS} are measured, respectively, and then converted into C_{ISS} , C_{RSS} , and C_{OSS} , as shown in Fig. 4. Compared to state-of-the-art Si power MOSFETs [14], C_{ISS} of the p-GaN device is more than one order of magnitude lower, leading to substantially reduced Q_G . In addition, the extremely small C_{RSS} also facilitates faster switching speed of the device. Meanwhile, the extremely low Q_{OSS} compared to Si SJ MOSFETs (in Table I, $C_{OSS,tr}$ of the p-GaN device is ten times smaller than the Si counterpart) enables a much shorter dead-time in soft-switching applications [2].

D. Dynamic R_{ON} Degradation: Role of Current Collapse and V_{TH} Instability

Compared to the mature Si counterparts, the newly established GaN power devices still face the challenges of various reliability and stability issues induced by various trapping effects [6], [34], [35] under different bias conditions. In order to better understand (and further predict) device behavior in power switching circuits, it is necessary to characterize the device performance under dynamic operation conditions.

The dynamic R_{ON} of the DUT is measured using AMCAD 1000-V/30-A pulse IV system. Fig. 5(a) illustrates the soft-switching waveforms of the pulsed $I-V$ measurement. The measurement starts directly with OFF-ON soft-switching cycles (without long-time OFF-state prestress on the DUT). Within one cycle, the DUT is first stressed in the OFF-state (with $V_{GSQ} = 0$ V) with a drain bias (with V_{DSQ} varying from 0 up to 400 V), and then switched to the ON-state in the linear region with its dynamic R_{ON} measured during this period. The pulse width (time for the ON-state) is 10 μ s, and the pulse period (one OFF-ON cycle) is 1 ms. For better measurement accuracy, multiple switching cycles are applied for each bias condition (as a result, it takes ~ 400 ms to take one measurement point),

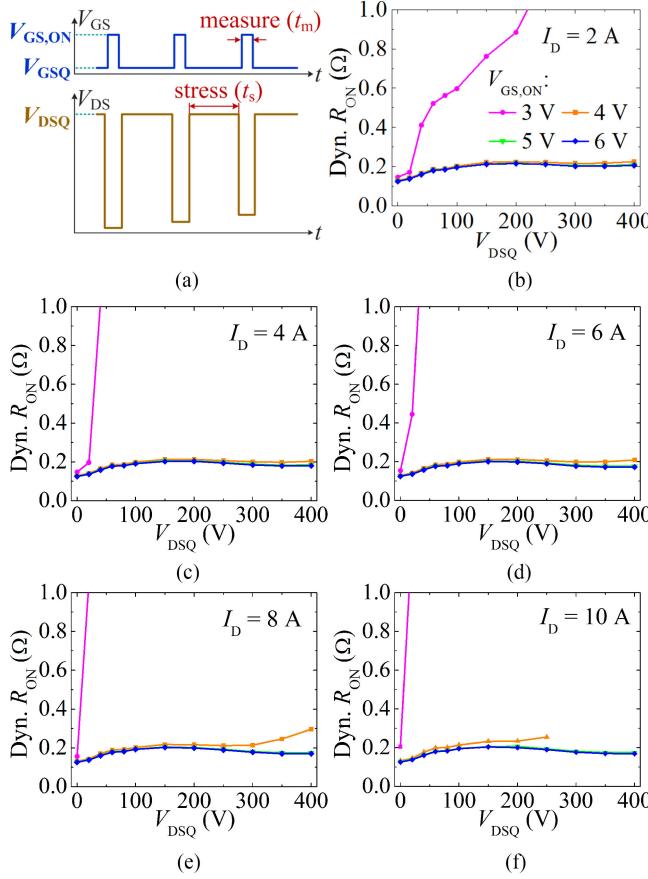


Fig. 5. (a) Illustration of the soft-switching waveforms for the pulsed I - V measurement. (b)–(f) Dynamic R_{ON} measured at different voltage and current levels up to 400 V, 10 A.

and device dynamic R_{ON} is measured by averaging data points obtained within 7–9.5 μs after it is turned on in each cycle. Small duty cycle of 1% assures that the self-heating effect is adequately suppressed in the measurement. Fig. 5(b)–(f) summarizes the measured dynamic R_{ON} under different voltage and current levels for $V_{GS,ON}$ of 3–6 V. In contrast to the static measurement results shown in Fig. 1(d), a strong dependence of the dynamic R_{ON} on $V_{GS,ON}$ is observed. While the dynamic R_{ON} is successfully kept below 200 m Ω for $V_{GS,ON}$ of 5 and 6 V over the entire tested range (400 V, 10 A), a significant degradation is observed for lower gate voltages of 3 and 4 V. Such distinct behavior of the dynamic R_{ON} degradation under different gate voltages implies the possibility of a V_{TH} shift under high-voltage switching operations, which has rarely been studied or reported for p-GaN devices.

In order to investigate the V_{TH} stability of the p-GaN device, dynamic transfer characteristics are measured using the same pulse conditions [see Fig. 6(a)]. As shown in Fig. 6(b), the V_{TH} shifts positively as V_{DSQ} increases. This positive V_{TH} shift, which is larger than 1 V under 400 V V_{DSQ} , results in a remarkable reduction in the drain current at lower gate voltages ($V_{GS,ON}$) of 3–4 V, and thus, a dramatic increase in the dynamic R_{ON} . Nevertheless, the impact of this positive V_{TH} shift on the drain current diminishes rapidly as $V_{GS,ON}$ increases. Under a $V_{GS,ON}$ of 5–6 V, the positive V_{TH} shift hardly has

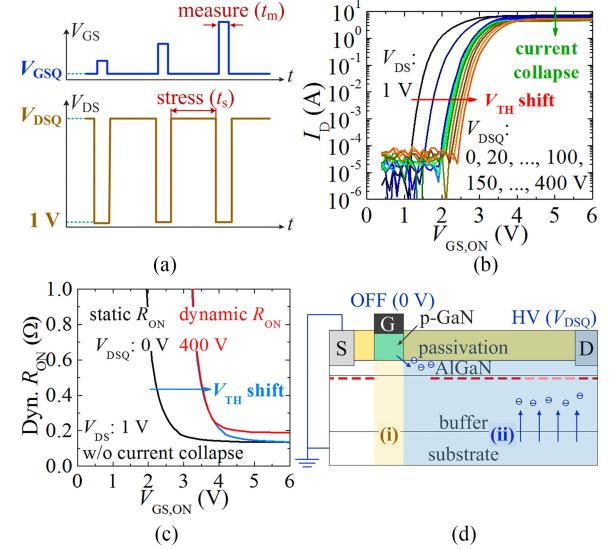


Fig. 6. (a) Pulse IV waveforms for the measurement of transfer characteristics. Quiescent biases V_{GSQ} and V_{DSQ} , as well as pulse width and pulse period are the same as in the dynamic R_{ON} measurement. (b) Transfer characteristics under dynamic switching operations with V_{DSQ} up to 400 V. (c) Dynamic R_{ON} versus $V_{GS,ON}$. Black line: measured static R_{ON} with $V_{DSQ} = 0 \text{ V}$. Red line: measured dynamic R_{ON} with $V_{DSQ} = 400 \text{ V}$. Blue line: calculated dynamic R_{ON} with $V_{DSQ} = 400 \text{ V}$ induced only by V_{TH} shift. The V_{TH} is positively shifted by 1.28 V (according to measurement results in Fig. 6(b)). (d) Schematic cross section of the DUT illustrating current collapse.

any influence on the dynamic R_{ON} [see Fig. 6(c)]. Therefore, the modest increase in the dynamic R_{ON} at V_{GS} of 5 and 6 V (see Fig. 5) is mainly due to current collapse induced by undesirable trapping effects in the gate-to-drain access region. As depicted in Fig. 6(d), at OFF-state with high drain bias, electrons can be injected: 1) from the gate electrode and trapped at the passivation/AlGaN-barrier interface or in the AlGaN barrier; and 2) from the substrate and trapped in the GaN buffer [34], [35]. When the device is switched ON, trapped electrons that cannot be emitted fast enough would partially deplete the 2DEG channel in the gate-to-drain access region and degrade the dynamic R_{ON} .

The positive shift in device V_{TH} suggests an increase of net negative charges (or equivalently, a decrease of net positive charges) in the gated region under reverse gate-to-drain bias V_{GD} . To further explore the V_{TH} stability under reverse gate bias, pulsed transfer characteristics are measured with negative V_{GSQ} (down to -17.5 V) and 0 V V_{DSQ} . Small V_{DSQ} of 0 V assures a symmetrical gate toward the source and the drain side by providing a uniform potential distribution along the 2DEG channel under the gate region. For $V_{GSQ} = -17.5 \text{ V}$, the transfer curve is measured with $V_{GS,ON}$ up to 2.5 V, limited by the 20 V voltage swing of the gate probe. Similarly, the transfer curve is measured up to 5 V when V_{GSQ} is -15 V. The measurement result plotted in Fig. 7(a) shows a similar positive shift in the V_{TH} when the gate is reverse biased.

To obtain insight into the observed V_{TH} instability, Fig. 8(a) and (b) illustrates the schematic cross section and corresponding energy band diagram of the gate stack of the p-GaN device at thermal equilibrium with $V_G = 0 \text{ V}$. Fig. 8(c) and (d) shows the

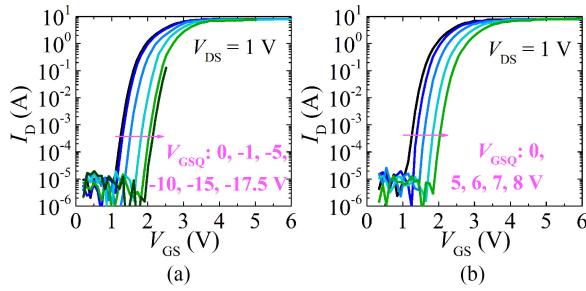


Fig. 7. Pulsed transfer characteristics of the DUT with (a) $V_{GSQ} < 0$, gate reverse biased, and (b) $V_{GSQ} > 0$, gate forward biased. The drain quiescent bias V_{DSQ} is 0 V. The pulse width and pulse period are the same as in previous measurements. A positive shift in the V_{TH} is observed in both cases.

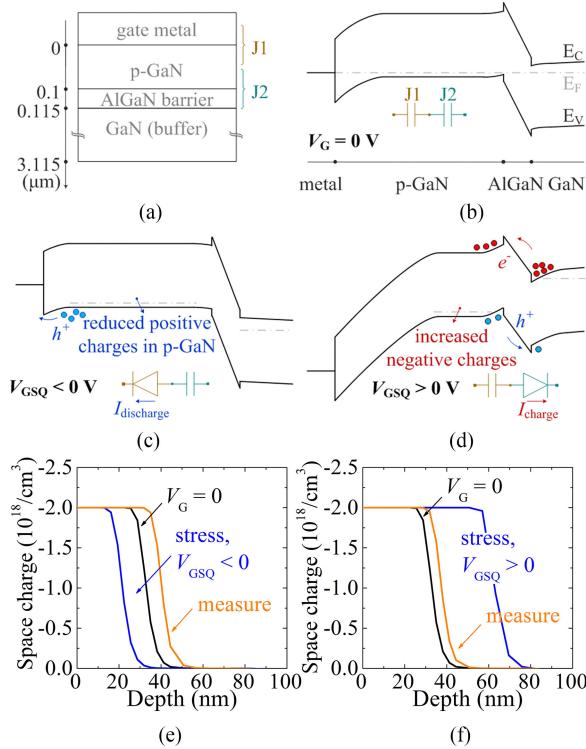


Fig. 8. (a) Schematic cross section of the metal/p-GaN/AlGaN/GaN gate stack. (b) Schematic energy band diagram along the depth of the gate stack at thermal equilibrium with $V_G = 0$ V. (c) Energy band diagram with negative V_{GSQ} . (d) Energy band diagram under relatively large positive V_{GSQ} . (e) and (f) Simulated space charge density within the p-GaN layer with a negative ($V_{GSQ} < 0$), and a positive ($V_{GSQ} > 0$) gate stress, respectively. At first, the device is at thermal equilibrium with $V_G = 0$ V (the black line). Then, the gate stress is applied for long enough time (the blue line) before it is removed at last (the orange line, corresponds to 10 μ s after the removal of the gate stress).

schematic energy band diagrams of the device under negative and positive gate stresses, respectively. TCAD simulations have also been carried out to reveal the change of the space charge density within the p-GaN layer corresponding to the two stress conditions qualitatively [see Fig. 8(e) and (f)]. The thickness of the p-GaN layer is set to be 100 nm, with a p-doping concentration (N_A) of $2 \times 10^{18} \text{ cm}^{-3}$, both of which are chosen based on the values typically used in p-GaN devices reported in the literature [19]–[21], [25], [26].

As illustrated in Fig. 8(a) and (b), the gate consists of two back-to-back junctions connected in series, namely, the metal-p-GaN Schottky junction (J1) and the p-GaN-AlGaN/GaN

heterojunction (J2). The potential of the floating p-GaN layer sandwiched in the middle can be modulated through charge injection/emission under different gate voltages, causing a shift in device V_{TH} . At reverse gate bias with $V_{GSQ} < 0$ V [see Fig. 8(c)], the Schottky diode J1 is forward biased, with a decreased depletion width in the p-GaN layer [see Fig. 8(e)]. As a result, holes in the p-GaN layer are emitted to the gate metal, discharging ($I_{discharge}$) the capacitor related to the reverse-biased heterojunction J2. When V_{GS} is switched back to positive levels, the reduced positive charges in the p-GaN layer cannot be restored immediately (considering the extremely low charging current of the J2 capacitor provided by the reverse-biased J1 diode), thus leading to a positive shift in the V_{TH} . This agrees well with the simulation results where the depletion width is increased after the stress, suggesting the existence of excessive negative charges in the p-GaN layer.

When a large positive voltage is applied to the gate [see Fig. 8(d)], the heterojunction diode J2 becomes forward biased, facilitating hole injection toward the GaN channel layer and electron “spill-over” into the p-GaN. As a result, the capacitor of the reverse-biased heterojunction J1 (with an increased depletion width, as shown in Fig. 8(f)) is charged up by the current flow, raising the voltage across it. When V_{GS} is switched back to lower levels (e.g., around V_{TH}), the excessive negative charges stored in the p-GaN layer cannot be pumped out instantaneously (as confirmed by the widened depletion region after the stress in the simulation). Instead, they can only be removed at a very slow speed (i.e., the discharging speed of the J1 capacitor) given the significantly lower current through the J2 diode at lower V_{GS} . Therefore, the V_{TH} would also shift toward the positive direction (within the measurement time scale of 10 μ s), which is consistent with the measurement results plotted in Fig. 7(b).

According to previous discussions, the positive V_{TH} shift (during the stress time t_s) and its recovery (during the measure time t_m) are dynamic processes defined by the charging/discharging time constants of the capacitors (which, again, are closely related to the gate structure of the device). Therefore, it should be noted that the V_{TH} shift shown in Figs. 6 and 7 could vary with different pulse conditions (e.g., t_s and t_m), and more detailed measurements need to be carried out in order to quantitatively characterize the V_{TH} shift over a broader time scale.

The characterization and analysis in this section show that for p-GaN devices, it is insufficient to perform the device characterization only under static conditions. When operated in switching mode, critical device parameters such as R_{ON} and V_{TH} could deviate from the static values, and therefore must be further evaluated under dynamic conditions. The investigation of dynamic R_{ON} degradation and V_{TH} instability suggests that a higher V_{GS} of 5–6 V would provide adequate gate over-drive to overcome the V_{TH} -shift-induced dynamic R_{ON} degradation in power switching applications.

III. SWITCHING PERFORMANCE EVALUATION AND CIRCUIT DESIGN CONSIDERATION

A. Double-Pulse Test Setup

The switching characteristics of the GaN device are evaluated using a double-pulse tester (DPT) circuit. Fig. 9 depicts the

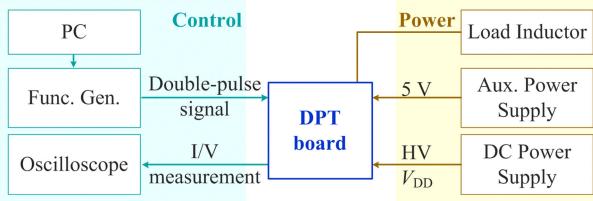


Fig. 9. Testing system setup for switching performance evaluation.

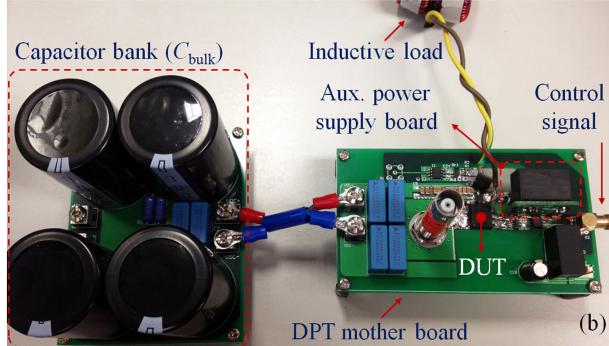
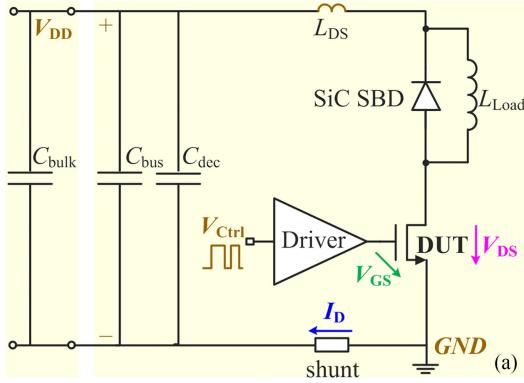


Fig. 10. (a) Circuit schematic, and (b) photograph of the DPT used for switching performance evaluation.

testing system setup. The double-pulse signals with adjustable pulse widths are generated from an arbitrary waveform generator which is controlled by a personal computer. The drain current is sensed using a $0.1\ \Omega$ coaxial shunt (SSDN-10) with small insertion impedance, and then monitored by an oscilloscope. Gate and drain voltages are measured by single-ended passive probes owing to their relatively high bandwidth. For more accurate measurement of the fast switching transients, probe-tip adaptors with minimized inductance [17] are used for voltage probe grounding instead of the standard 10-cm ground clips. Before measurement, it is critical that the voltage and current probes are deskewed to compensate their differences in the propagation delay, especially for high-speed GaN devices with greater sensitivity to timing misalignment. This is achieved by removing the inductive load and replacing the diode with a low inductance $100\text{-}\Omega$ resistor (i.e., essentially a resistive load circuit) [36], [37]. Fig. 10 shows the circuit schematic and photograph of the DPT. A 600-V SiC Schottky barrier diode is used

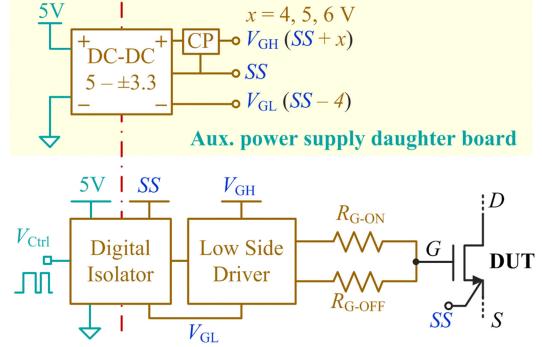


Fig. 11. Schematic of the gate drive circuit.

as the freewheeling diode of the inductive load to facilitate fast commutation processes. The bulk capacitor bank C_{bulk} with an equivalent capacitance of $680\ \mu\text{F}$ maintains a smooth dc-bus voltage.

B. Gate Drive Circuit Design

Given the distinct characteristics of p-GaN devices compared to Si counterparts, special considerations must be taken with respect to gate drive circuit design. First, instead of a voltage range of 10–12 V as in the case of Si power MOSFETs (and cascode GaN switches), the suggested gate drive voltages V_{GH} [6], [22]–[24], [27]–[32] of commercial p-GaN devices are much lower, ranging from 3 to 6.5 V. According to the device characterization described in Section II, the channel conductivity of the DUT is fully enhanced when V_{GS} is 4 V under static conditions. However, higher V_{GS} of 5 and 6 V is needed under switching operations considering the positive shift in the V_{TH} . At the same time, more aggressive gate drive voltages (e.g., $V_{\text{GH}} \geq 7\ \text{V}$) could accelerate the gate junction degradation or even lead to device failure considering the less robust gate junction with breakdown voltages slightly larger than 10 V in many cases (note that the gate voltage rating would always be smaller than the breakdown voltage out of reliability considerations) [7], [18]–[20]. Second, with a relatively low V_{TH} and a very high dv/dt rate, these devices are susceptible to false turn-on in phase-leg configurations. To address this issue, a negative gate voltage V_{GL} from -3 to $-5\ \text{V}$ is often employed in many circuit demonstrations [6], [17], [31]. Nevertheless, the adoption of negative V_{GL} also increases the voltage drop on the device in reverse conduction mode (see Fig. 2). An antiparallel diode could be used to reduce the reverse conduction loss when necessary. Third, the much faster switching speed of GaN power devices (i.e., dv/dt as much as 3–5 times that of the best Si power MOSFETs) greatly increases their sensitivity to parasitics, which requires delicate design of the gate drive circuit (i.e., driving method, component selection, board layout, etc.) to minimize parasitic inductance and capacitance.

Aimed at probing the optimal driving conditions for the E-mode GaN device studied in this work, a gate drive circuit is designed, as shown in Fig. 11. A low-side gate driver chip LM5114 with high driving current and low output impedance is selected to facilitate fast charging/discharging of the input

capacitances of the GaN power switch. Moreover, its independent source and sink outputs allow separate control of turn-on and turn-off speed. Digital isolator ISO721 is used to provide control signal isolation owing to its high common mode transient immunity (>150 V/ns with careful layout design) [38] enabled by the extremely low input-to-output capacitance (1 pF). Dual output isolated power supply (MEJ1D0503SC) with small isolation capacitance of 3 pF is used to power up the gate drive circuit. A charge pump chip with adjustable output voltage is employed to provide different turn-on gate voltages (i.e., $V_{GH} = 4, 5, 6$ V). The turn-off gate voltage (V_{GL}) is about -4 V.

C. Board Layout Considerations

The DPT is implemented on a four-layer printed circuit board (PCB). The layout is designed with every effort to minimize the parasitic inductances of both the gate loop and the power loop.

1) *Mounting of DUT*: Although several manufactures offer GaN power devices housed in various low-inductance leadless packages to fully liberate their advantageous performance, the leaded packages are still dominant in many applications because of their simplicity for PCB assembly and flexibility in thermal management design. In this work, the GaN device with the substrate connected to the source is packaged into TO-220 with a pin configuration of G-S-D. This arrangement effectively mitigates the coupling capacitance (C_{GD}) between the gate loop and the power loop (compared to conventional G-D-S configuration). To further reduce the common source inductance, Kelvin connection is adopted with the source lead being the “Kelvin source sense (SS).” Moreover, in order to reduce the lead inductance, a slot is created in the PCB for mounting the DUT with minimized lead length by “sinking” the device in the 1.6-mm thick PCB [see Fig. 12(a)], which also enables effective heat dissipation from the backside (compared to the case in Fig. 12(b)).

2) *Power Loop*: As phase-leg configuration is the most commonly used subcircuit in practical applications, the layout is designed assuming two GaN devices with antiparallel diodes in the commutation loop. The power supply rails (V_{DD} and GND) are established in a planar structure with four 220 nF film capacitors (C_{bus}) and 20 ceramic capacitors (2.2 nF each, C_{dec}) placed in the immediate vicinity of the power devices [see Fig. 12(c)], fully decoupling the external stray inductances along the dc bus.

3) *Gate Loop*: In order to minimize the gate loop inductance, vertically overlapped planar structure is employed in the layout design of auxiliary supply voltages (V_{GH} and V_{GL}) as well as the SS reference. Moreover, the parasitic capacitance across the isolation barrier is minimized by avoiding any overlap between primary and secondary sides of the digital isolator as well as the isolated power supply. This is critical for improving the dv/dt immunity of the gate drive circuit, especially for fast switching GaN power devices [38]. In addition, given the tight layout of the DPT mother board, the auxiliary power supply is implemented on separate daughter boards to reduce the distance (and so the stray inductance) between supply voltages and driver chips [see Fig. 12(d)]. Meanwhile, this perpendicular configuration also helps to minimize the coupling between the gate loop and the power loop.

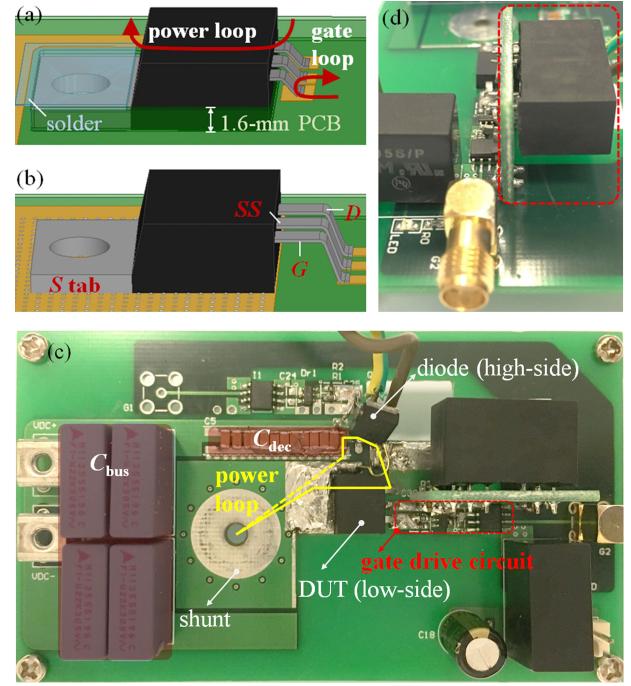


Fig. 12. (a) PCB slot is created for mounting the DUT with minimum lead length and effective heat dissipation. (b) Surface mounted DUT without the slot in PCB results in longer leads and thus larger lead inductances. The packaged device has a pin configuration of G-S-D. Kelvin connection with source lead being the “Kelvin SS” is adopted to decouple the gate loop and the power loop. (c) Top view of the DPT board. (d) Side view of the auxiliary power supply daughter board (outlined in red dash).

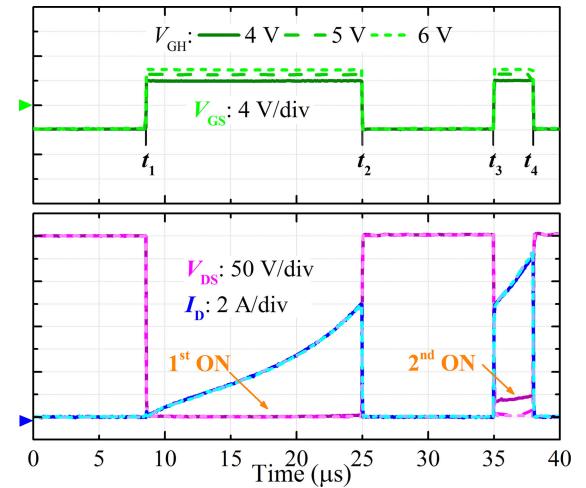


Fig. 13. Double-pulse waveforms with $V_{GH} = 4$ (solid line), 5 (dash), and 6 V (short dash) under 400 V, 10 A. $R_{G-ON}/R_{G-OFF} = 10 \Omega/1.5 \Omega$, the internal gate resistance is measured to be 1.8 Ω using the power device analyzer.

D. Dynamic R_{ON} Under Hard-Switching Operation

Double-pulse tests were performed up to 400 V, 10 A. For a given V_{DD} (e.g., 400 V), the tests were conducted under different current levels ranging from 2 to 10 A with a 2 A step. The DUT is biased in the OFF-state at the beginning (for about 1 min) and then turned on at t_1 . During the first ON-state pulse, the

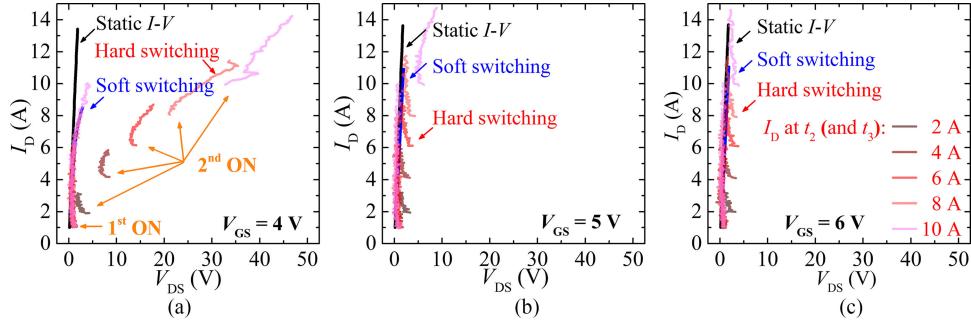


Fig. 14. $I_D - V_{DS}$ characteristics of the DUT under different operation conditions. Black line: static $I-V$ (with $V_{DSQ} = 0\text{ V}$); blue line: dynamic characteristics under soft-switching-pulsed $I-V$ measurement with $V_{DSQ} = 400\text{ V}$; red line: dynamic characteristics under double-pulse tests with $V_{DD} = 400\text{ V}$. The first pulse comes after the “soft turn-on” with zero current (t_1), while the second pulse follows the hard turn-on (t_3) with I_D increasing from 2, 4, 6, 8, and 10 A, respectively.

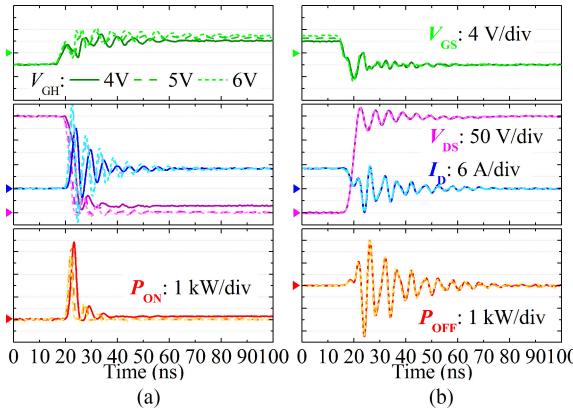


Fig. 15. (a) Turn-on and (b) turn-off waveforms (including: V_{GS} , V_{DS} , I_D , and instantaneous power) with different V_{GH} . $V_{DD} = 400\text{ V}$, $I_{Load} = 10\text{ A}$, $R_{G-ON}/R_{G-OFF} = 10\Omega/1.5\Omega$.

inductive load is charged up, increasing the current flowing through the DUT (I_D). When I_D reaches the desired value (e.g., 10 A), the DUT is turned off at t_2 . The width of the first pulse ($t_2 - t_1$) is determined by the target drain current I_D as well as the charging speed of the inductive load (V_{DD}/L). Then, after a short interval of 10 μs , the DUT is turned on again at t_3 and I_D continues to increase. The second ON-state pulse, which comes after two hard-switching transitions (i.e., at t_2 and t_3), lasts for 3 μs before its final turn-off at t_4 . Fig. 13 shows the waveforms of the DUT at 400 V, 10 A with V_{GH} equal to 4, 5, and 6 V. The first ON-state pulse lasts for 16.4 μs . When V_{GH} is 4 V, a significant voltage drop on the DUT is observed at the second ON-state, suggesting a dramatic increase in the dynamic R_{ON} during this period.

To further investigate the dynamic R_{ON} degradation under hard-switching operations in a more explicit way, $I_D - V_{DS}$ relationships are extracted from the double-pulse waveforms. Fig. 14 shows the $I_D - V_{DS}$ characteristics during the two ON-state pulses under 400 V bus voltage (red line). The static $I-V$ (black line) and dynamic characteristics under soft-switching-pulsed $I-V$ measurements (blue line) are also plotted for comparison. $I_D - V_{DS}$ curves during the first pulse coincide with the soft-switching measurement results for V_{GH} of 4–6 V (i.e., the 1-min OFF-state prestress has negligible influence on

dynamic R_{ON} degradation of the DUT), whereas a more severe degradation in the dynamic R_{ON} is observed during the second pulse. The reason for such distinction is most likely related to different stresses on the DUT prior to two ON-state pulses. Before the first pulse, the DUT is biased in the OFF-state for a relatively long time and then turned on with zero current, similar to the soft-switching measurement in Fig. 5. While before the second pulse, the DUT goes through two hard-switching transitions during which the device is stressed at high current and high voltage levels simultaneously (especially for the turn-on transient). Nevertheless, the dynamic R_{ON} degradation during the second pulse resembles the soft-switching measurement results (see Fig. 5) with a clear dependence on the gate drive voltage, indicating larger V_{TH} shift under hard-switching operations. This is because during the high-power hard-switching transients, significant amount of hot electrons are generated in the channel. Some of them can be injected into the p-GaN layer in the gated region and result in further shift in the V_{TH} .

The double-pulse test result confirms the positive V_{TH} shift in the soft-switching-pulsed $I-V$ measurements (i.e., the first pulse), and reveals a further shift in the V_{TH} under hard-switching operations (i.e., the second pulse). The effect of this V_{TH} instability is twofold: 1) it aggravates the dynamic R_{ON} degradation (and therefore, device conduction loss) under relatively low V_{GH} . Therefore, a V_{GH} of at least 5 V is recommended for soft-switching applications, while a V_{GH} of 6 V should be employed under hard-switching operations, especially in high-power applications (i.e., 400 V, 10 A), so that the V_{TH} -shift-induced dynamic R_{ON} degradation is minimized; 2) the more positive V_{TH} enhances the false turn-on immunity of the p-GaN device, which enables a less negative or even zero V_{GL} in practical applications.

E. Switching Performance Evaluation

Fig. 15 shows the turn-on and turn-off switching transients of the DUT under 400 V, 10 A with V_{GH} equal to 4, 5, and 6 V. The turn-off characteristics are almost identical, while the turn-on waveforms vary with V_{GH} .

Fig. 16 compares the switching performance under different V_{GH} at 400 V bus voltage in terms of: 1) switching speed; 2) switching energy; and 3) voltage/current stresses on the DUT.

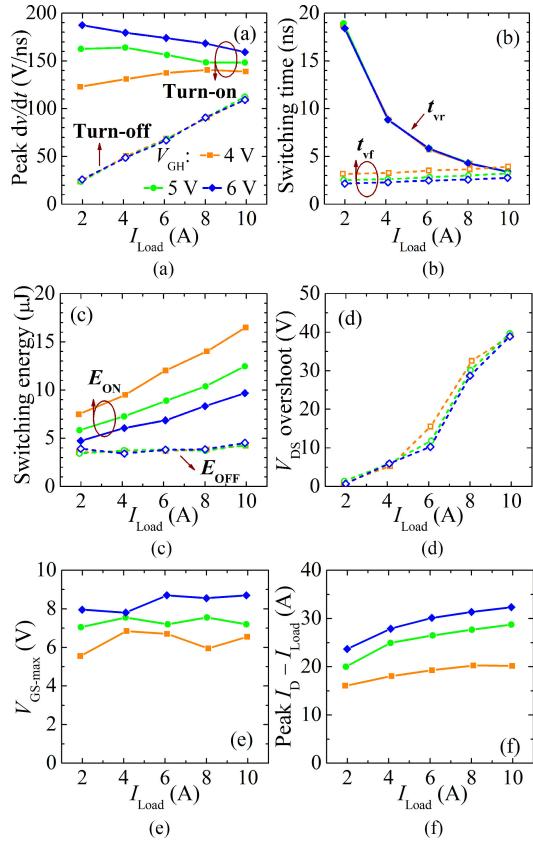


Fig. 16. (a) Peak dv/dt , (b) switching time (fall and rise time for V_{DS}), (c) switching energy (E_{ON} and E_{OFF}), (d) drain voltage overshoot during turn-off, (e) gate voltage overshoot during turn-on, and (f) drain current “overshoot” during turn-on. $V_{DD} = 400$ V. t_{vf} (and t_{vr}) is the time it takes for V_{DS} to fall from 90% to 10% (and to rise from 10% to 90%) of the bus voltage during the turn-on (and turn-off) transient. E_{ON} (and E_{OFF}) is the switching energy between the time when I_D (and V_{DS}) rises to 10% of the load current (bus voltage) and the time when V_{DS} (and I_D) falls to 10% of the bus voltage (and load current).

A fast switching (turn-on) speed with peak dv/dt larger than 150 V/ns and a voltage fall time t_{vf} less than 3.5 ns has been achieved with V_{GH} of 5 and 6 V. For the turn-on transient, the switching speed increases with V_{GH} , as witnessed by the larger dv/dt rate and shorter switching time (t_{vf}) at higher V_{GH} . This is because a larger gate drive voltage allows a higher channel current (DUT in saturation region, $I_{ch} = g_m(V_{GS} - V_{TH})$) during the voltage fall time, thus providing a larger displacement current that discharges/charges the output capacitances of the low- and high-side devices faster [see Fig. 16(f)]. The faster turn-on speed naturally leads to lower turn-on energy under higher V_{GH} , at the price of increased electromagnetic interference (EMI). The maximum voltage appearing at the gate (V_{GS_max}) is also measured. With R_{G_ON} equal to 10 Ω , V_{GS_max} could exceed 8.5 V when V_{GH} is 6 V. It should be noted that this is the externally measured V_{GS} including the voltage drop across the lead inductance of the TO-220 package (although it has been minimized in our design). Nevertheless, further increase in V_{GH} (accompanied by even larger V_{GS_max}) is not recommended since it could accelerate gate junction

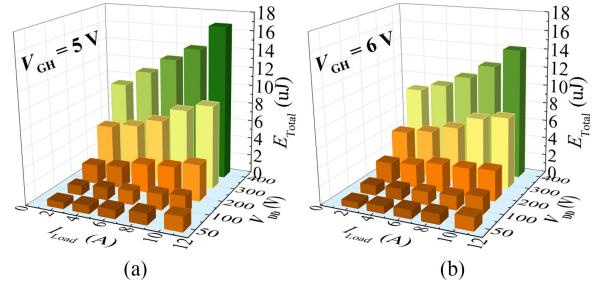


Fig. 17. E_{Total} of the DUT up to 400 V, 10 A with V_{GH} of: (a) 5 V, and (b) 6 V.

degradation and increase the risk of device failure considering a gate voltage limitation of no more than 10 V [7], [18]–[20].

The turn-off characteristics are almost the same under varying V_{GH} , given an identical V_{GL} of around -4 V in all cases. The linearly increased peak dv/dt and the clearly decreased voltage rise time (t_{vr}) at higher I_{load} indicate a turn-off process limited by the power loop, where all of the load current is used to charge/discharge C_{OSS} of the low-side switch and the junction capacitance of the high-side diode. Meanwhile, the faster turn-off speed (di/dt) also induces a larger V_{DS} overshoot across the power loop inductance under higher I_{Load} , which is around 16 nH (including the parasitic inductance of PCB trace, device package, and current shunt) derived from the turn-off ringing. Unlike E_{ON} which is positively correlated to I_{Load} , E_{OFF} presents a very weak I_{Load} dependence as the shorter turn-off time (which tends to reduce E_{OFF}) counterbalances the increase in the load current.

Total switching energy E_{Total} of the DUT under different voltage and current levels is evaluated and summarized in Fig. 17. The switching loss (at a given switching frequency) under a specific bus voltage and load current can be projected from E_{Total} (for nonsynchronous topologies). In parallel, the dynamic R_{ON} characteristics measured under soft/hard-switching conditions can be used for estimating device conduction loss. Depending on circuit topologies (hard or soft switching) and system specifications (i.e., output power, efficiency, power density, EMI, etc.), a V_{GH} of 5 or 6 V can be used for driving the p-GaN device while saving it from excessive gate stresses.

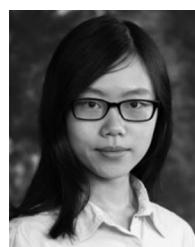
IV. CONCLUSION

Device characteristics of a commercial 650 V p-GaN gate power HEMT have been systematically investigated under static and dynamic operating conditions. With reference to the static I - V characteristics, the dynamic R_{ON} under different gate drive voltages has been evaluated by using both soft-switching-pulsed I - V measurements and inductive load hard-switching measurements (i.e., double-pulse tests). A strong dependence of dynamic R_{ON} degradation on the gate drive voltage has been observed. Although fairly suppressed under higher V_{GS} of 5–6 V, the dynamic R_{ON} is significantly larger (in comparison with the static R_{ON}) under lower V_{GS} of 3–4 V. Such a dynamic R_{ON} degradation is found to be the result of the positive V_{TH} shift under (soft/hard) switching operations. By

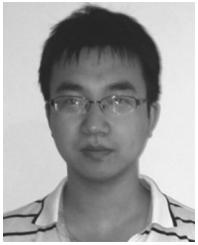
considering 1) V_{TH} -shift-induced dynamic R_{ON} degradation under switching operations; and 2) gate voltage limitation for reliable operations, an optimum gate drive voltage of 5–6 V has been identified that enables minimum R_{ON} degradation without sacrificing device long-term reliability by excessive gate stresses. In addition to the device-level characterization, switching performance of the p-GaN gate HEMT has been evaluated in a double-pulse test circuit up to 400 V, 10 A. Gate drive circuit design and board layout considerations have also been presented with full considerations given to the fast switching characteristics of GaN devices. Leveraging the performance advantages of GaN power transistors, especially p-GaN gate HEMTs, requires more than a simple drop-in replacement of Si-based counterparts. The device characterization and circuit design considerations presented in this paper provide valuable information for GaN-based converter design and loss projection.

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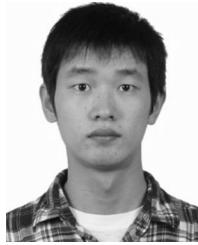
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