## Weekly Report – 26 Feb 2018

## PWM Generation using DSP

Digital Input / Output

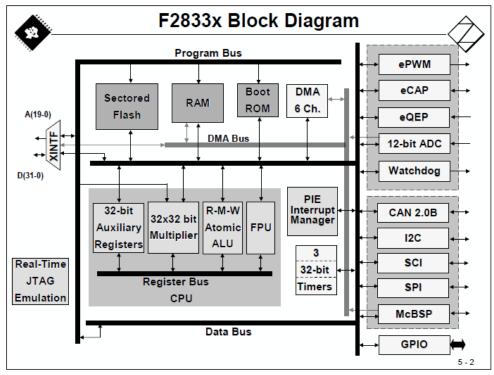


Figure 1: General Block Diagram of uP

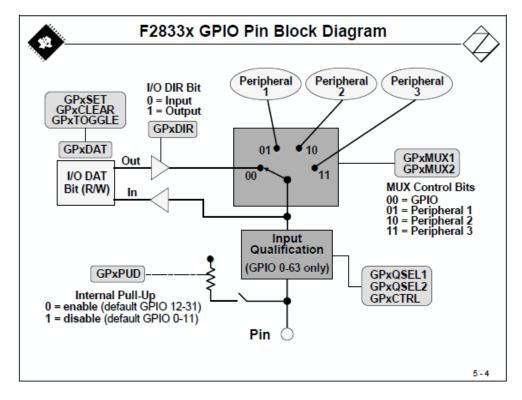


Figure 2: GPIO Pin Block Diagram

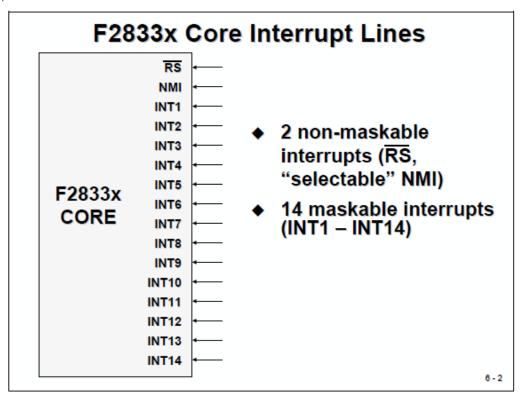


Figure 3: Interrupt Lines

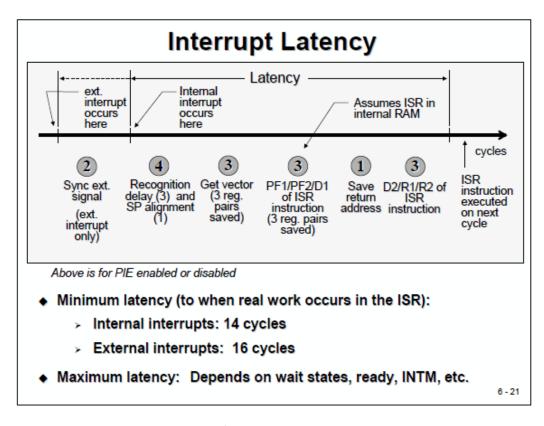


Figure 4: Interrupt Loop

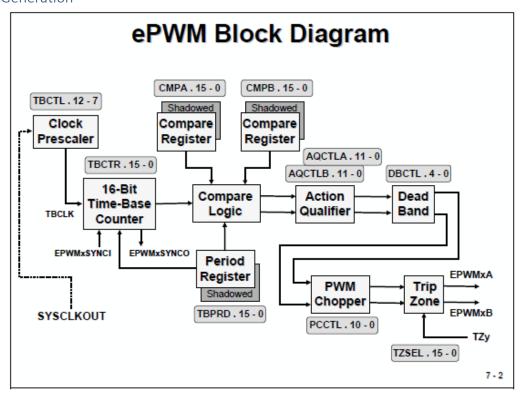


Figure 5: ePWM Block Diagram

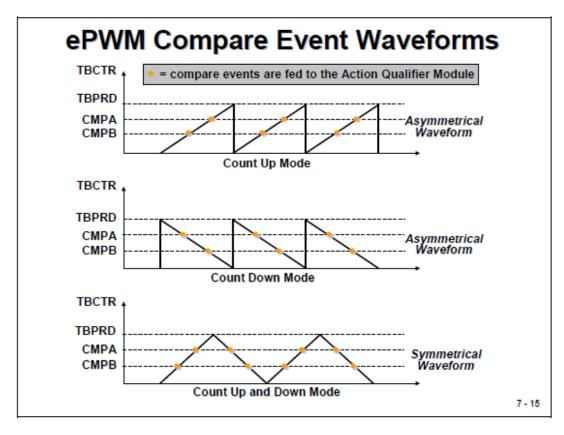


Figure 6: Timer Counter Modes

WM A	ction	Qualif	ier Ac	tions
Time-Base Counter equals:				EPWM Output
Zero	СМРА	СМРВ	TBPRD	Actions
Z X	CA X	CB X	PX	Do Nothing
Z ↓	CA →	CB ↓	<b>P</b> →	Clear Low
<b>Z</b> ↑	CA ↑	CB	<b>P</b> ↑	Set High
Z	CA T	CB	P	Toggle
	Tim Zero  Z X  Z ↓  Z  ↑	Time-Base Co  Zero CMPA  Z X  Z CA X  Z CA  ↓  CA ↑  CA ↑	Time-Base Counter equal Zero CMPA CMPB  Z CA CB X  Z CA CB CB	Zero CMPA CMPB TBPRD  Z X CA X CB Y X  Z CA CB P Y  Z CA CB P  Z CA CB P  Z CA CB P  T CA CB P  T CA CB P  T CA CB P

Figure 7: Action Qualifier

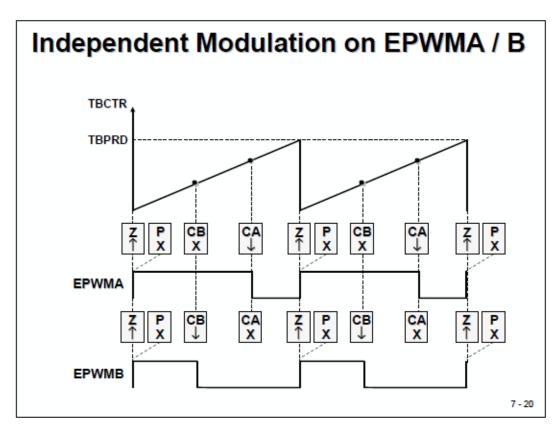


Figure 8: How action qualifier works

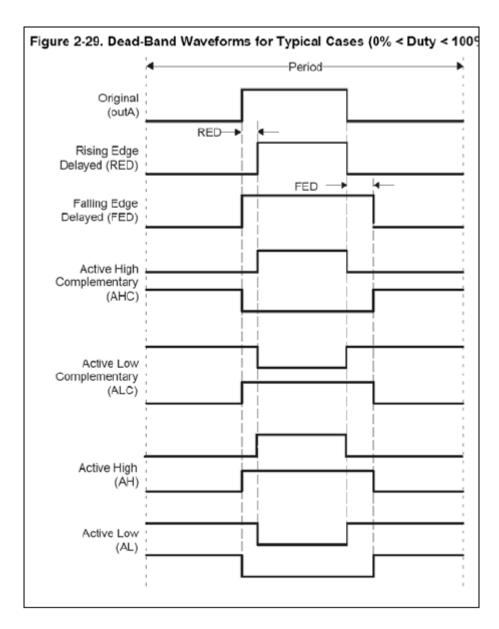


Figure 9: Dead Time

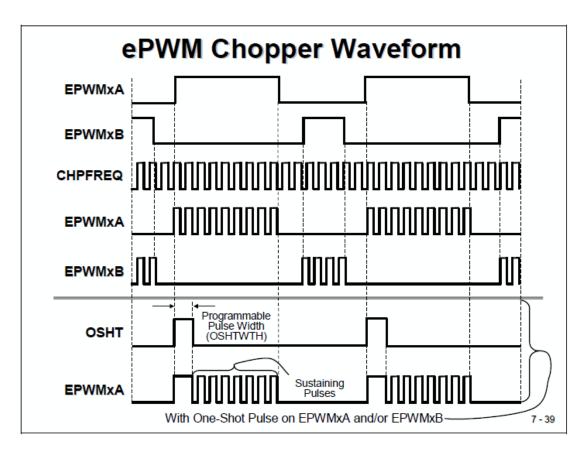
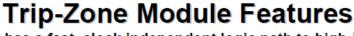


Figure 10: PWM Chopper



- Trip-Zone has a fast, clock independent logic path to high-impedance the EPWMxA/B output pins
- Interrupt latency may not protect hardware when responding to over current conditions or short-circuits through ISR software
- Supports: #1) one-shot trip for major short circuits or over current conditions
  - #2) cycle-by-cycle trip for current limiting operation

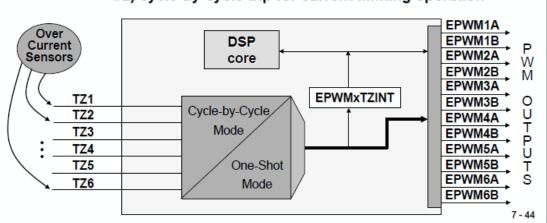


Figure 11: Trip Zone

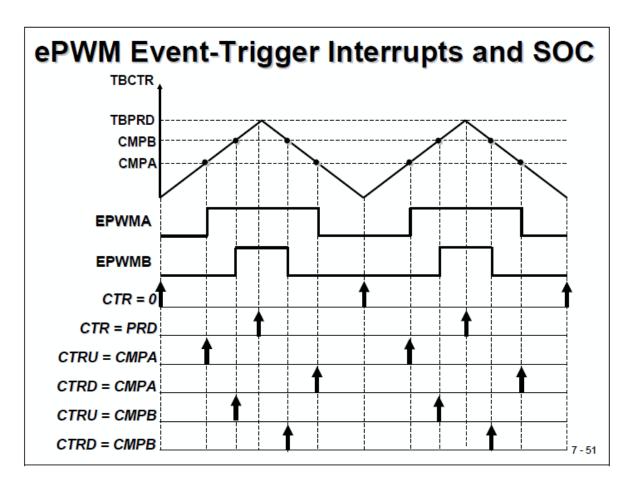


Figure 12: ePWM Interrupt

## **GaN Test**

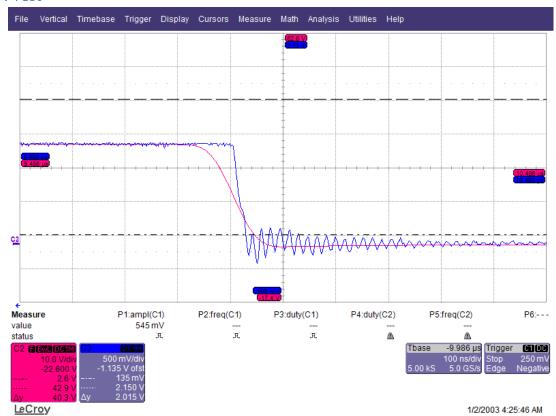


Figure 13: Blue and Red are both Vds of Bottom Switch

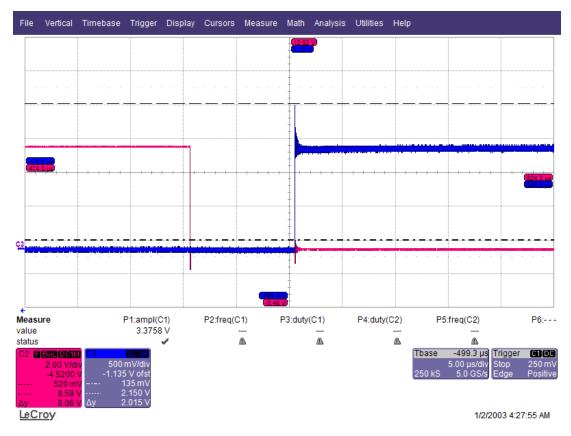


Figure 14: Dead Time View - Red -> Vgs, Blue -> Vds

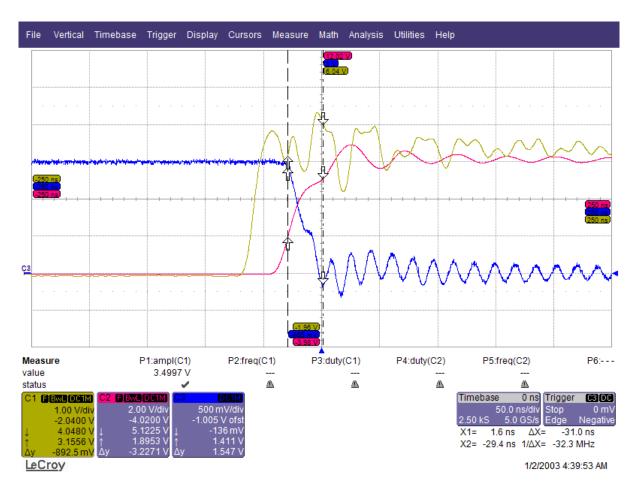


Figure 15: Blue > Vds, Red-> Vgs and Yellow -> Applied PWM