Weekly Report – 26 Feb 2018

PWM Generation using DSP

Digital Input / Output

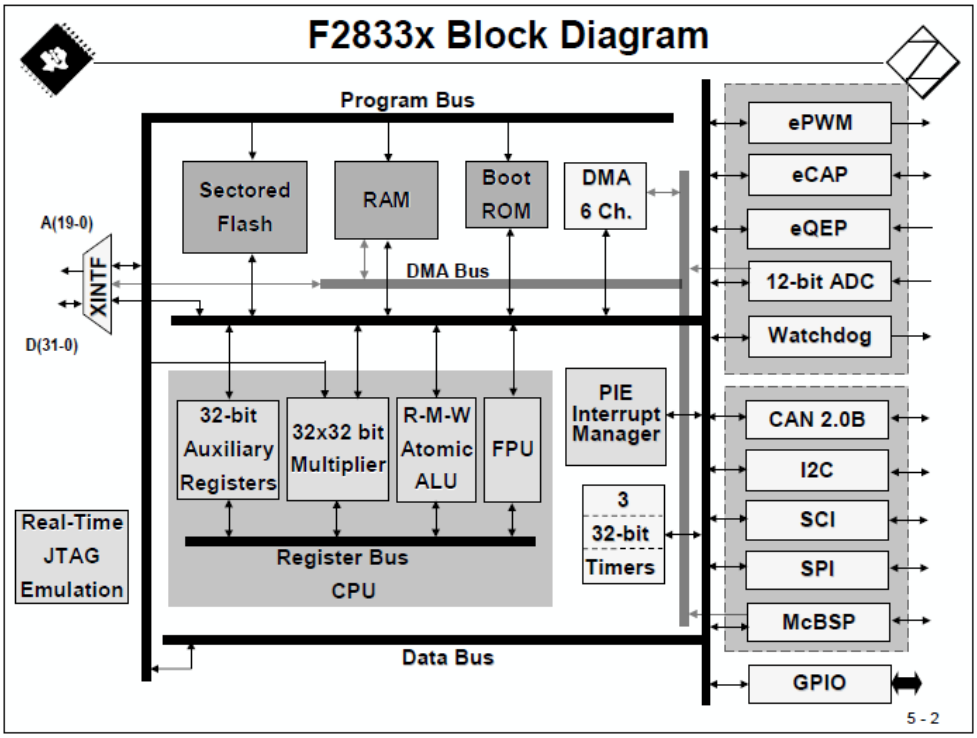

Figure 1: General Block Diagram of uP

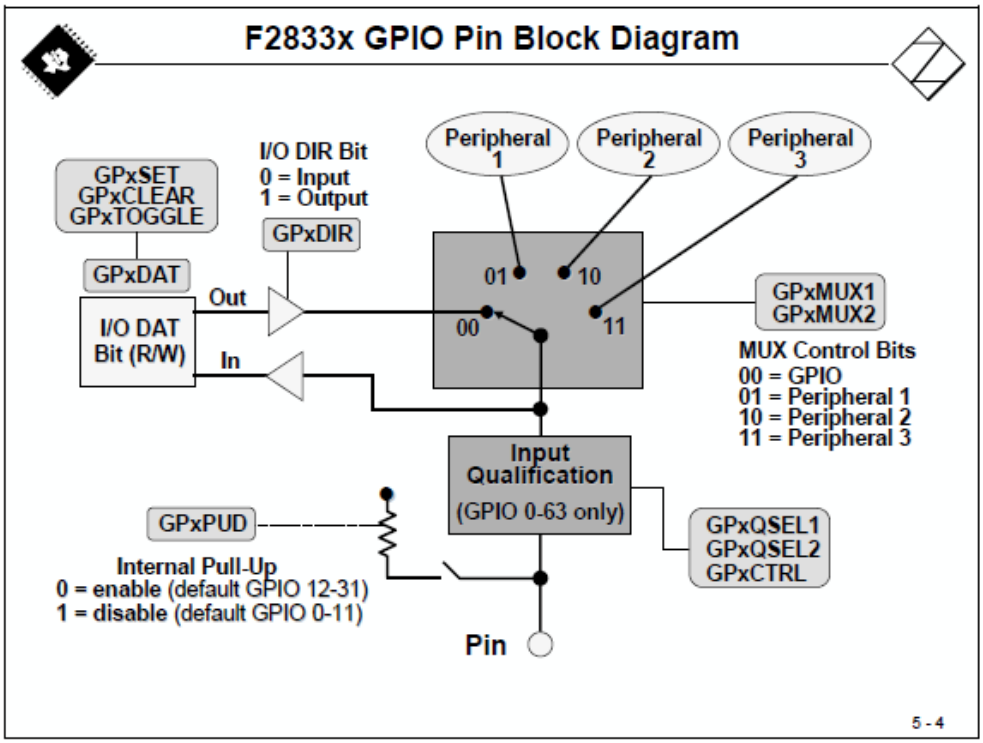

Figure 2: GPIO Pin Block Diagram

Interrupts

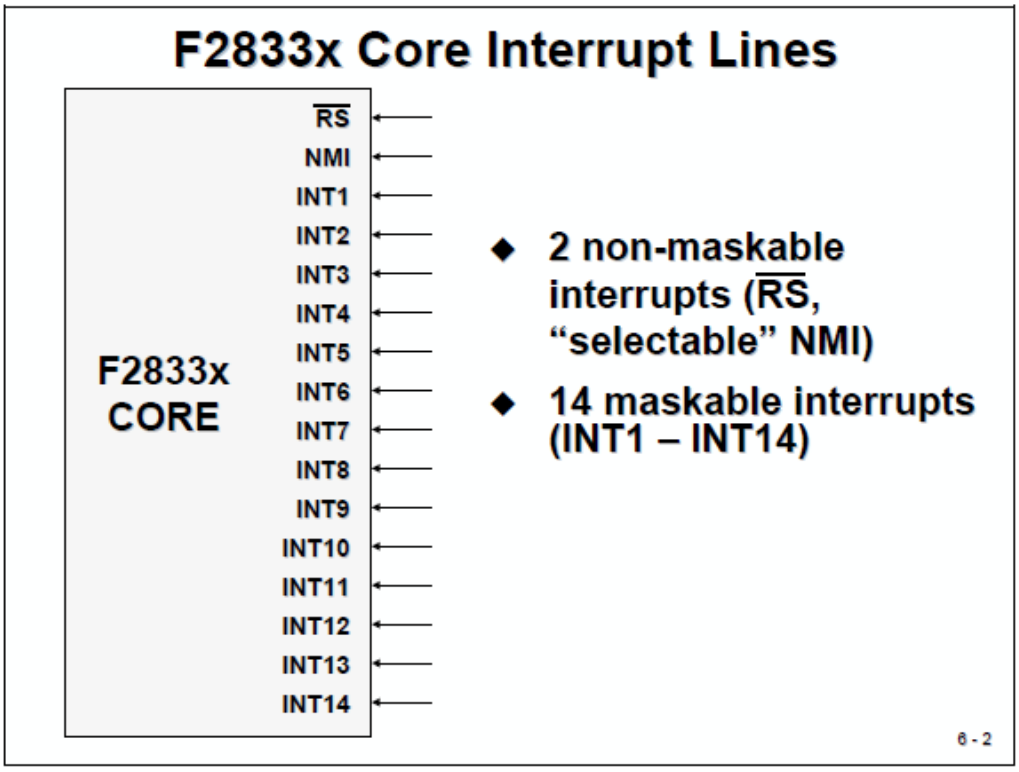

Figure 3: Interrupt Lines

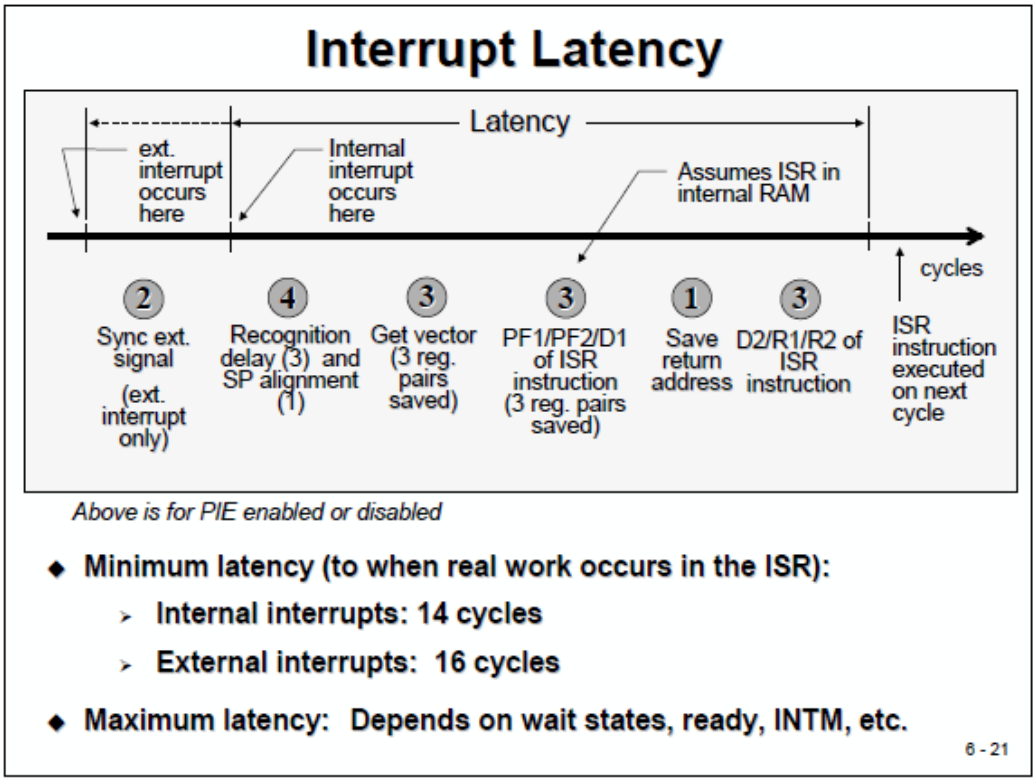

Figure 4: Interrupt Loop

PWM Generation

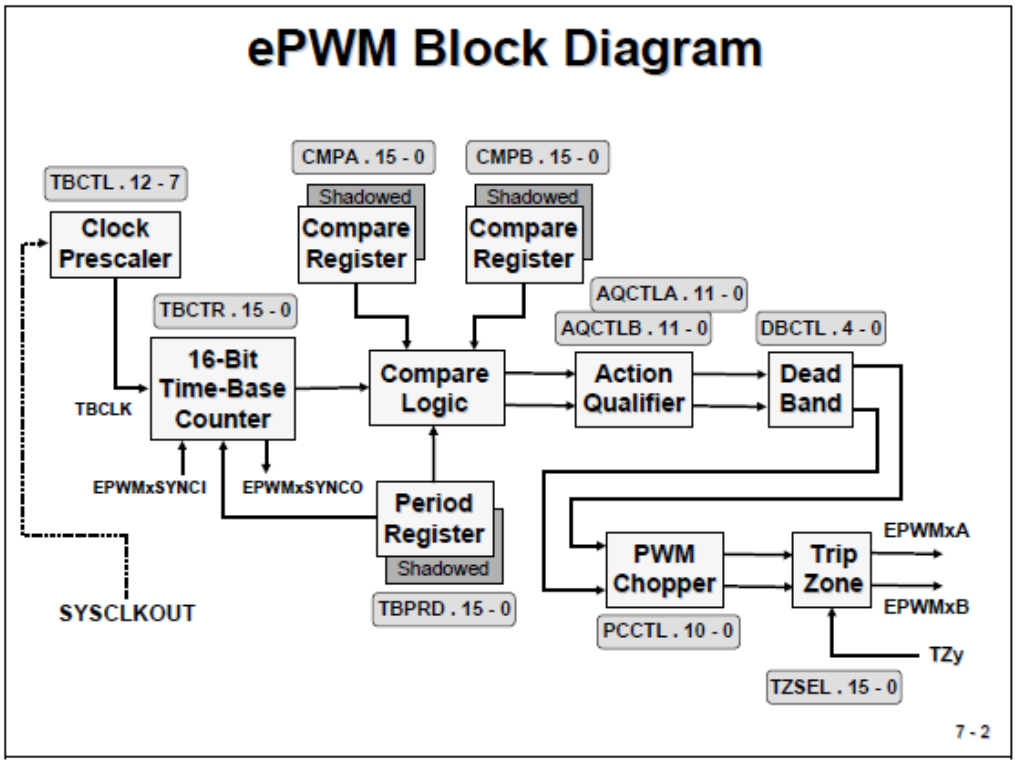

Figure 5: ePWM Block Diagram

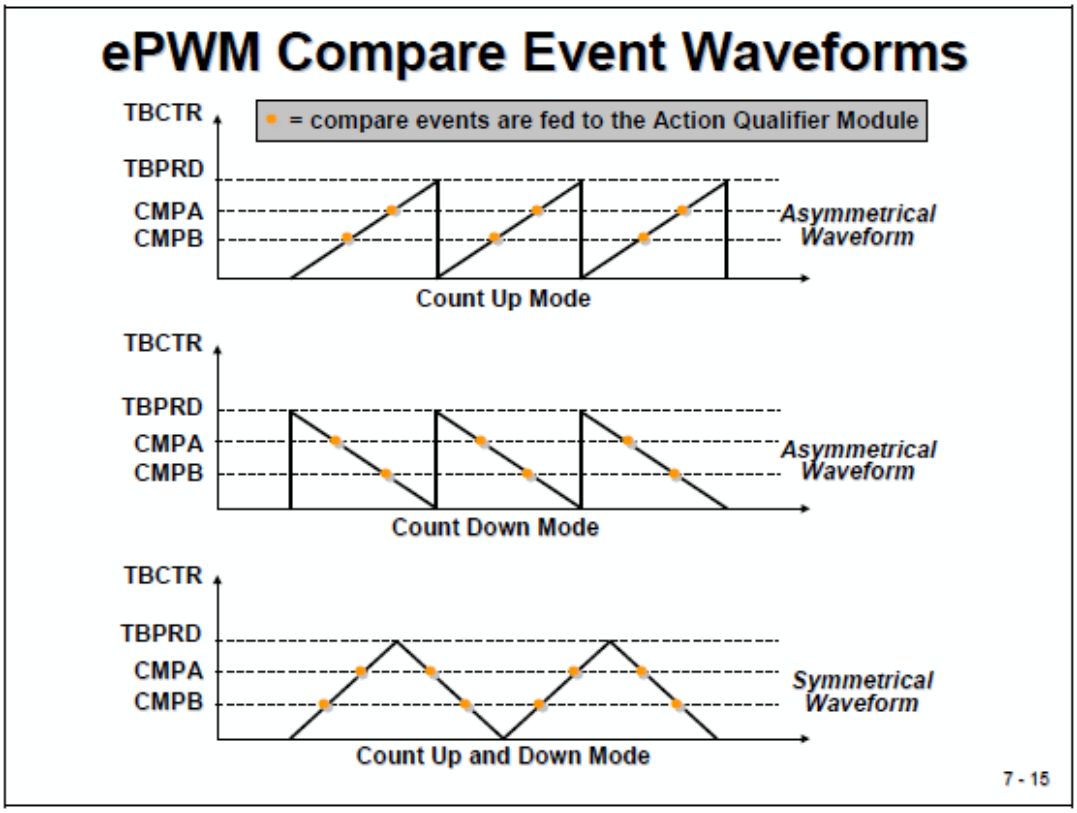

Figure 6: Timer Counter Modes

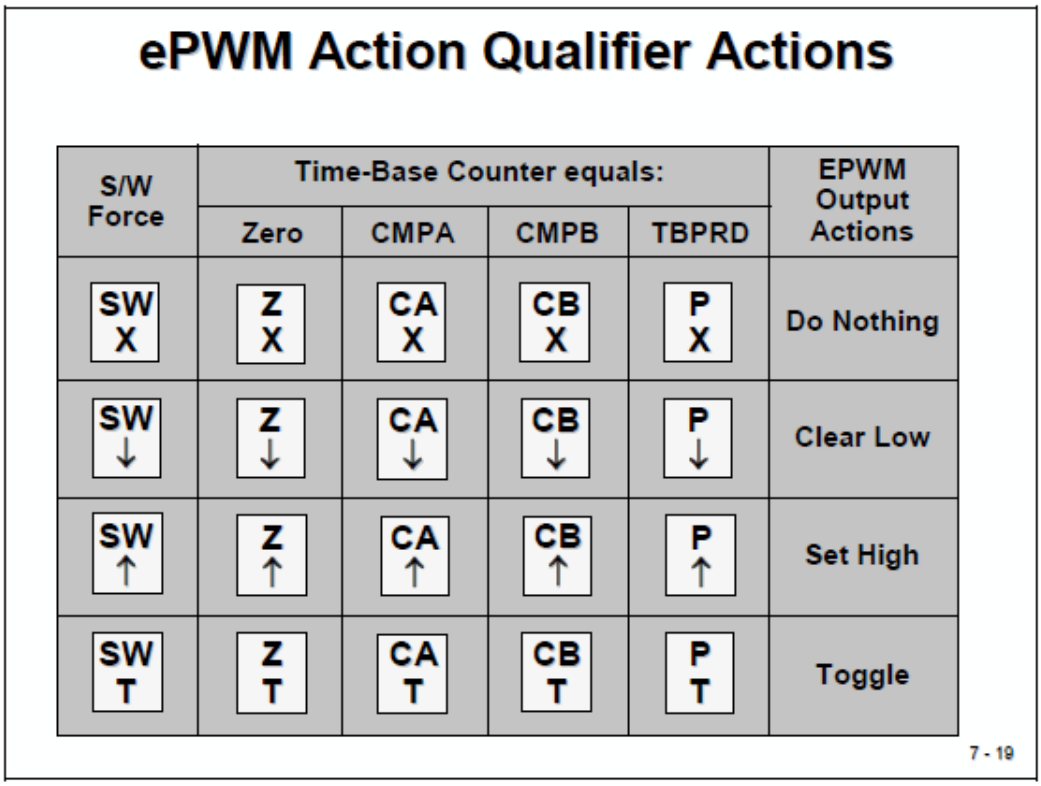

Figure 7: Action Qualifier

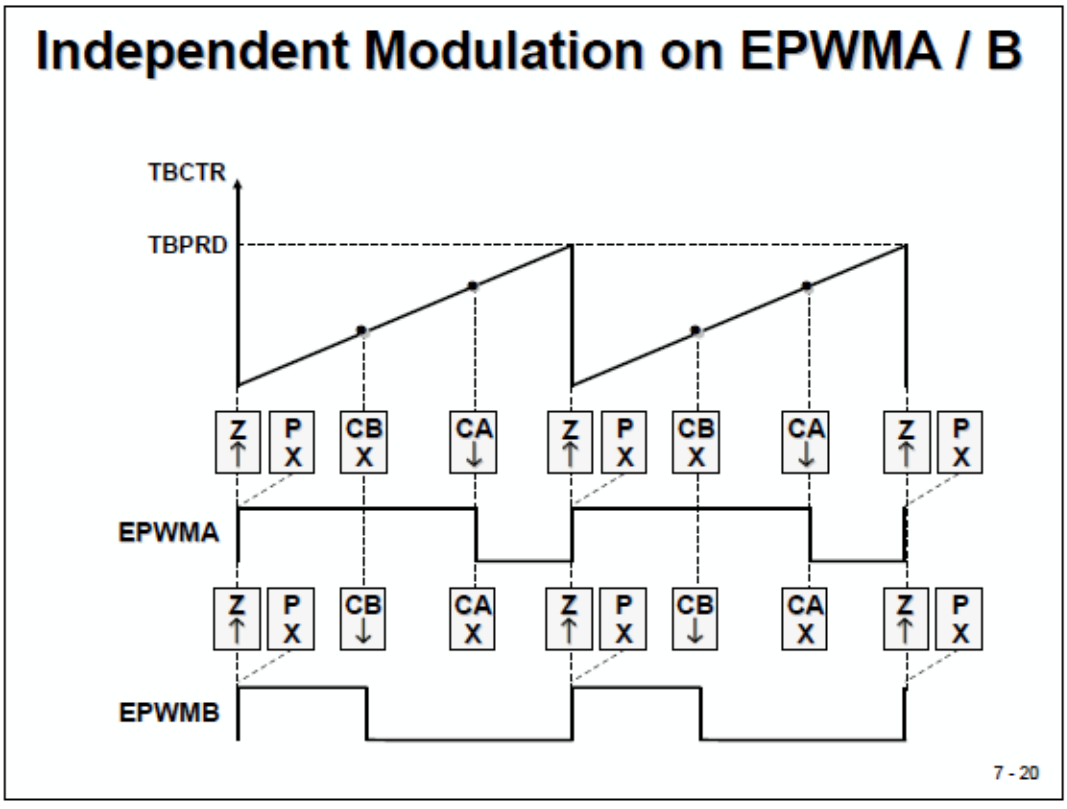

Figure 8: How action qualifier works

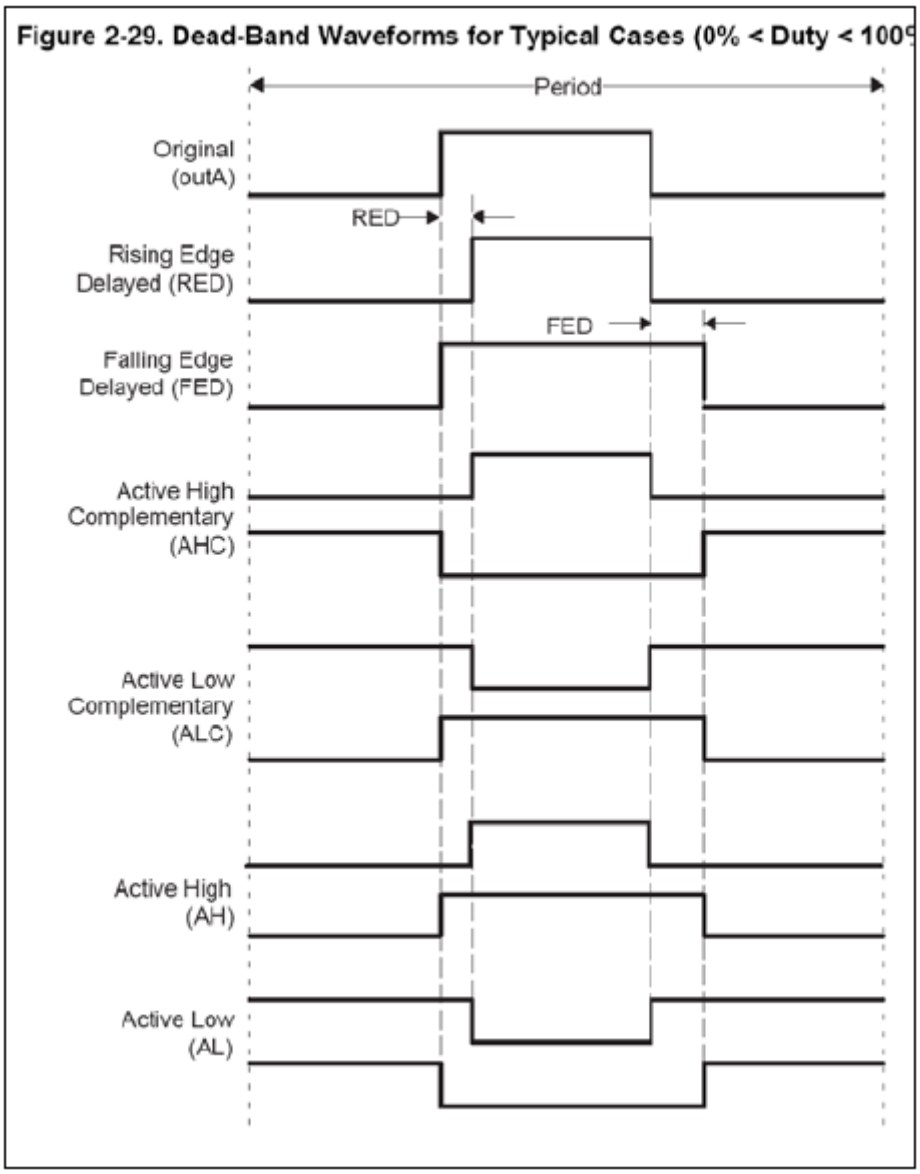

Figure 9: Dead Time

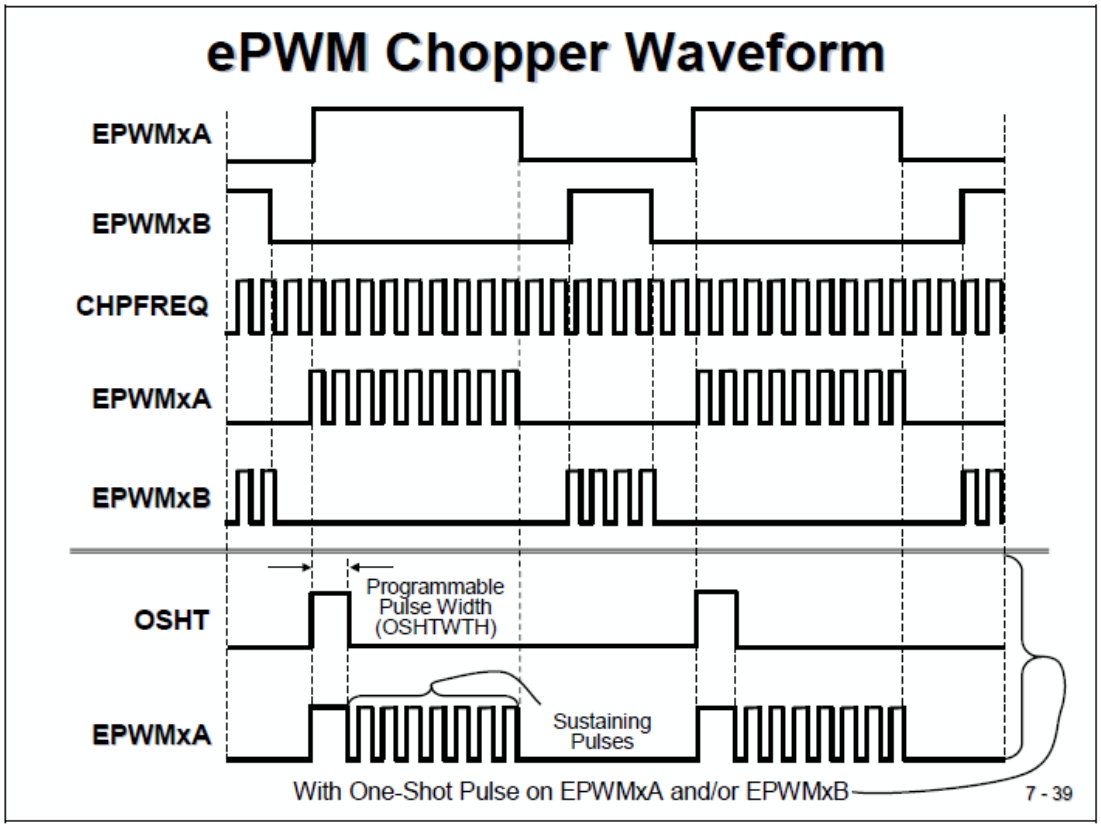

Figure 10: PWM Chopper

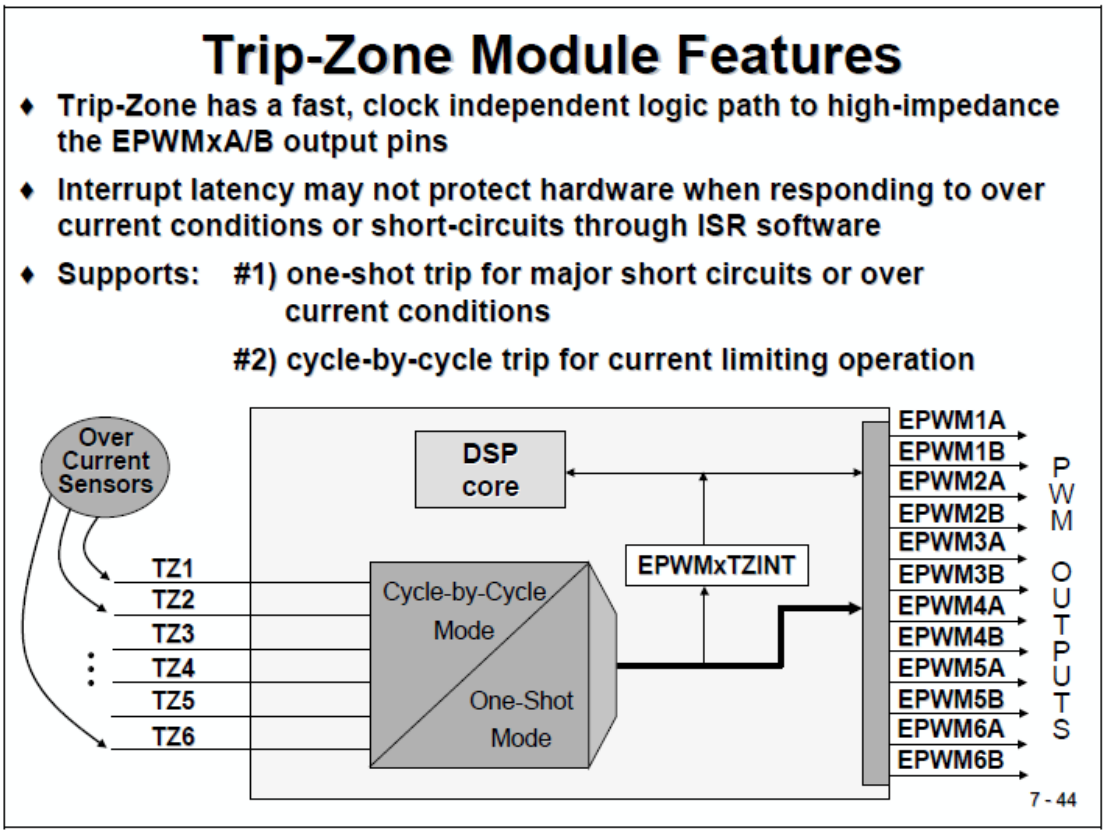

Figure 11: Trip Zone

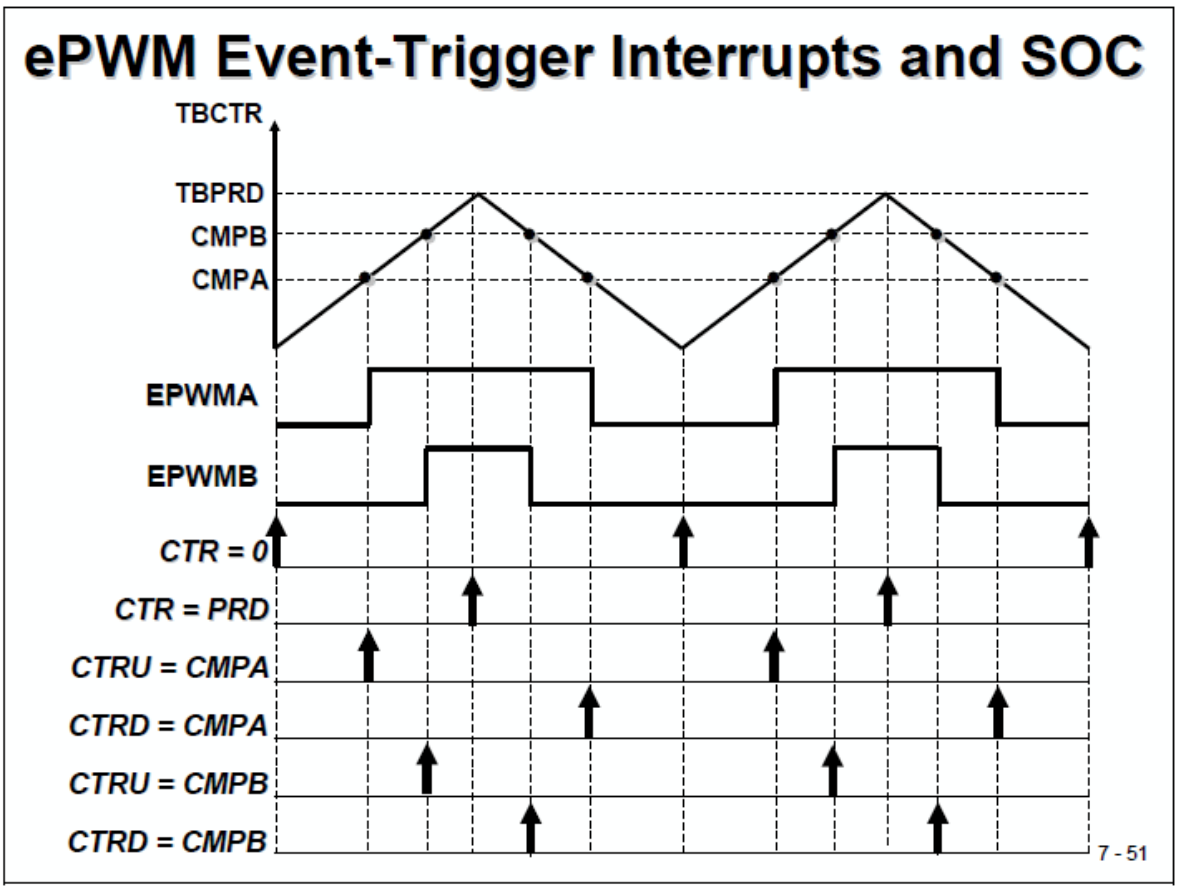

Figure 12: ePWM Interrupt

GaN Test

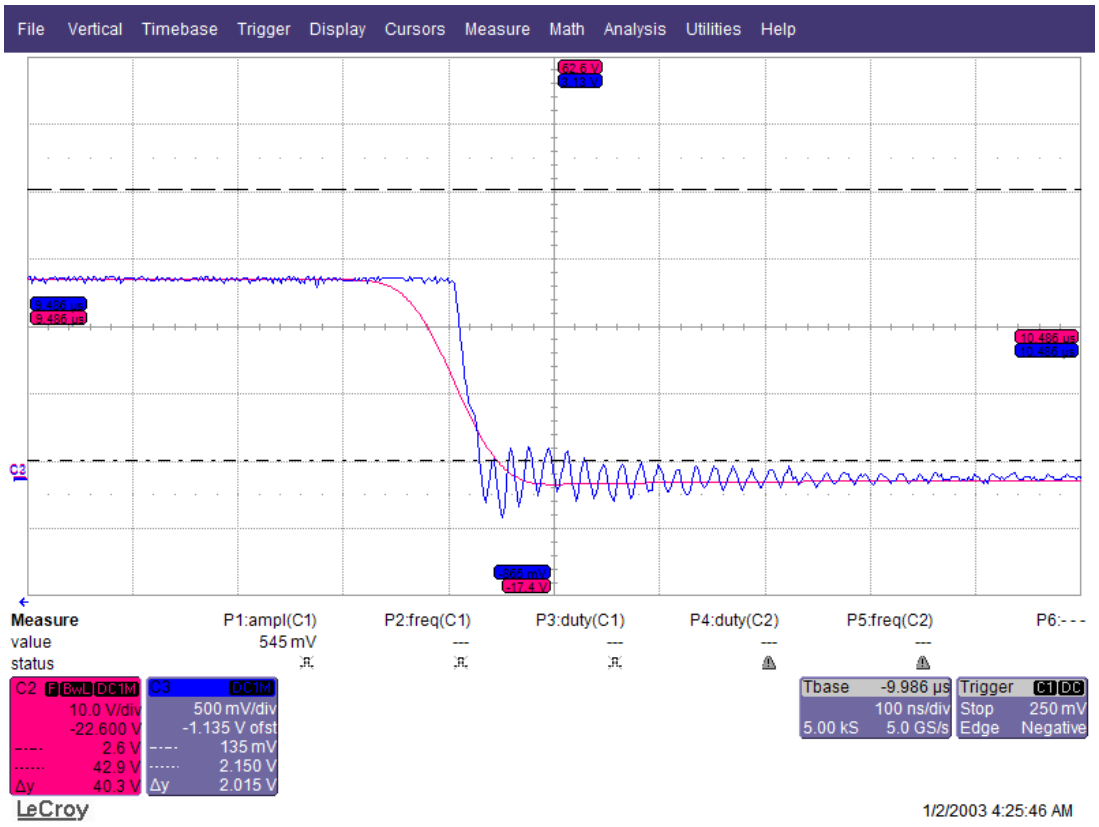

Figure 13: Blue and Red are both Vds of Bottom Switch

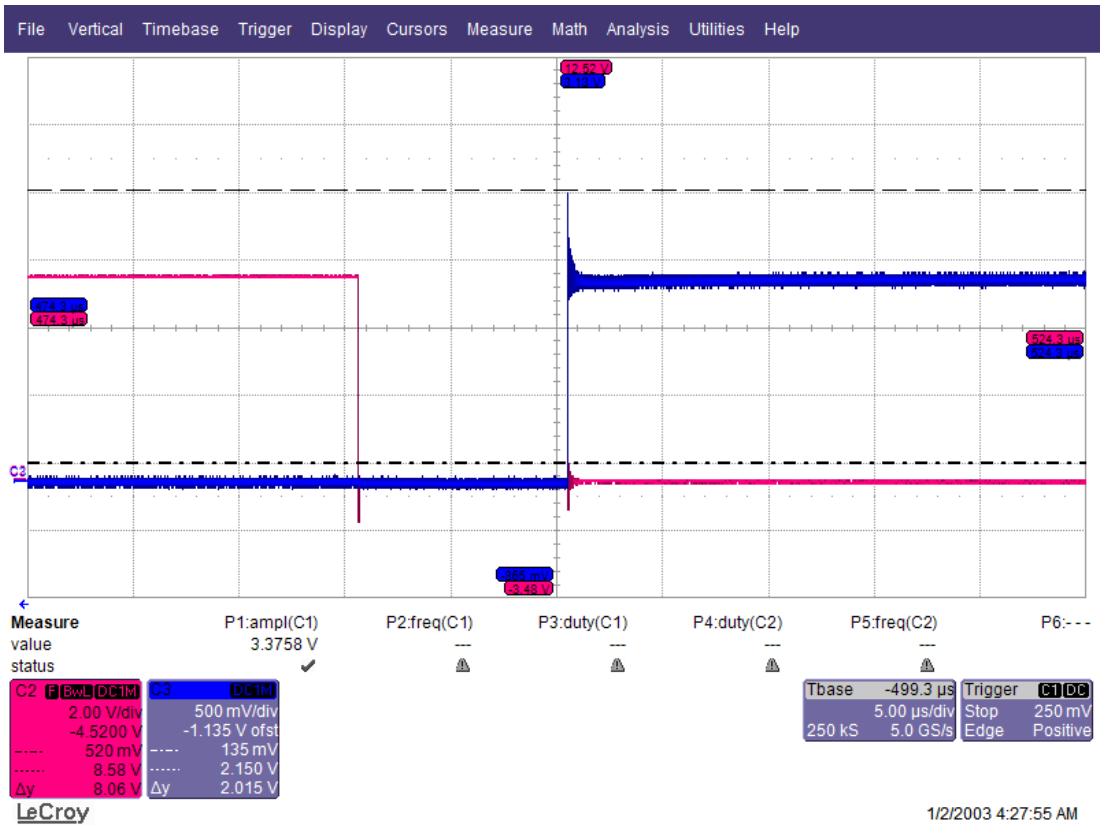

Figure 14: Dead Time View - Red -> Vgs, Blue -> Vds

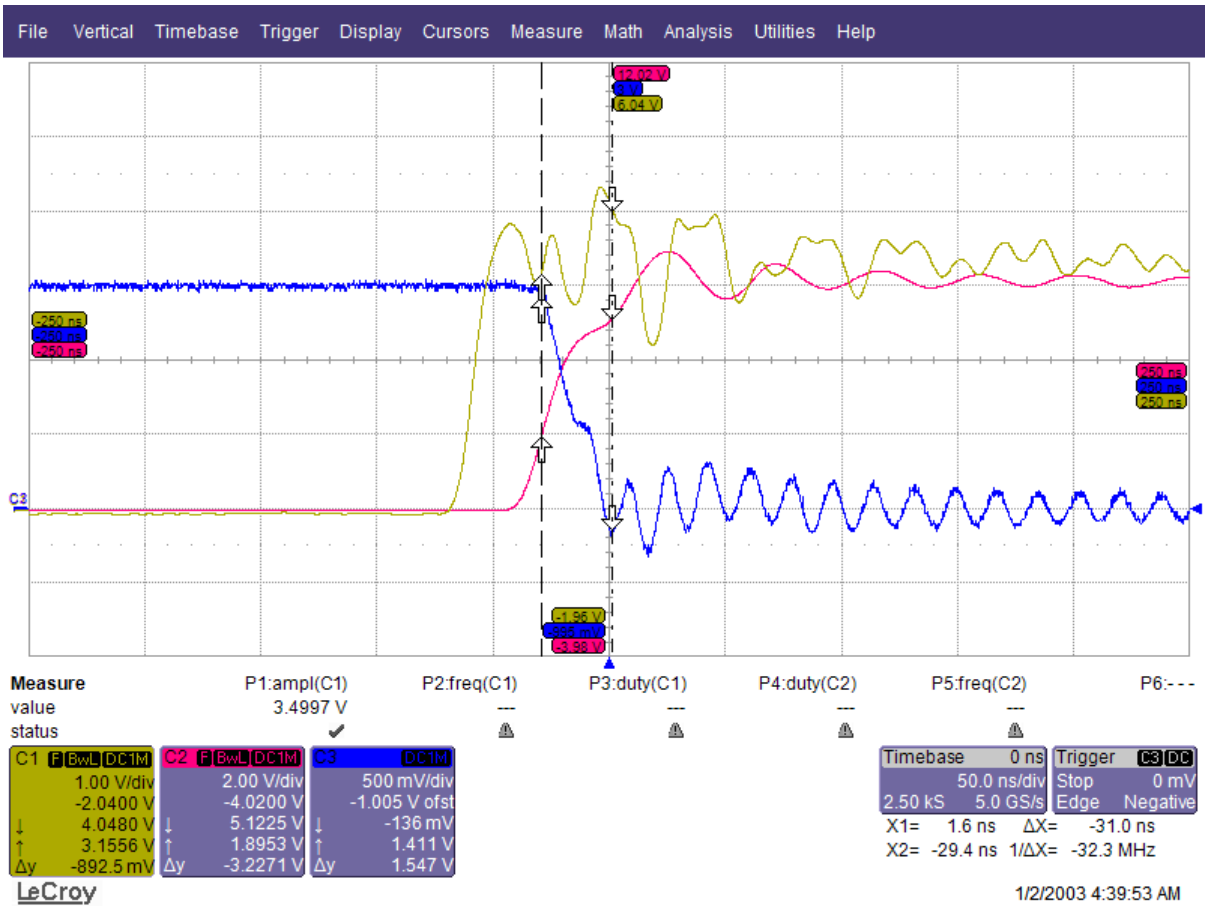

Figure 15: Blue > Vds, Red-> Vgs and Yellow -> Applied PWM