Comparison of Inverter Topologies Suited for Integrated Modular Motor Drive Applications

Topic number: TT01

***Abstract*-In this paper, various inverter topologies are compared for integrated modular motor drive (IMMD) applications. Two-level voltage source inverter (2L-VSI), three-level voltage source inverter (3L-VSI) and series/parallel combinations of these topologies with system level modularity are investigated in terms of motor side and DC link side voltage and current harmonic spectrum, passive component sizes and motor drive efficiency. New generation wide band-gap GaN power semiconductor devices are utilized in modular topologies and they are compared with a conventional motor drive utilizing IGBTs under the same system ratings. The effect of phase-shifting between the PWM carrier signals of parallel connected modules and its contribution to size reduction is investigated. IMMD structure has proven to have a superior efficiency performance over conventional motor drives, thanks to the utilization of GaNs. It has been shown that over 98% motor drive efficiency can be achieved for an IMMD with 8 kW output power by using a newly proposed topology where 2L-VSI converters are connected both in series and parallel on the DC link.**

I. INTRODUCTION

Electric motor drives use over 45% of the overall electricity consumption, which makes energy conversion efficiency quite important. Many of the electric motors are driven by variable frequency adjustable speed drives (ASDs) each day due to the need for precise speed or motion control. Power density plays a critical role in designing motor drives in several applications such as electric traction and aerospace.

Conventional ASDs are composed of motor drive inverter power electronics, passive components, cooling structures, control/communication interfaces and sensors for speed control. In integrated motor drives, the aforementioned drive components are integrated on the electric motor to reduce the system size, eliminate the connection cables for better EMI/EMC performance and eliminate the need for separate enclosures [1]. A more compact solution is dividing the system in modules which is called the Integrated Modular Motor Drive (IMMD) concept. A dedicated drive is integrated onto each motor segment in IMMDs. The advantages of using such an arrangement can be listed as: reduction of power semiconductor device and motor winding voltage and current stresses, improvement of fault tolerance capability, distribution of heat sources to get an easier thermal management and cost reduction in manufacturing, maintenance and repair [2].

In IMMD applications, with the introduction of modularity, the variety of available topologies suitable for motor drive increases significantly in IMMD applications. Three-phase voltage source inverter (VSI) topologies for different applications such as motor drive or grid-connected renewable energy converters have been proposed, evaluated, tested and reported thoroughly for many years. Most of these studies include two-level VSI (2L-VSI) and three-level VSI (3L-VSI), cascaded H-bridge (CHB) and modular multilevel converter (M2LC) for higher voltage ratings. On the other hand, different motor poles can be connected to separate and dedicated drive inverters in IMMDs which brings design flexibility in terms of motor drive topology selection [3].

To integrate the drive to the motor, significant size reduction should be achieved to fit all the drive components in a small volume [1]. The largest components in an average power converter are the passive components and heatsinks [4], therefore the size reduction challenge can be addressed by either minimization of the DC link capacitor or heat sink volume (or both) in an integrated drive. Considering the design flexibility, investigation of the most suitable motor drive topology in terms of DC link ripples, AC side harmonics and efficiency is mandatory.

There have been several studies in search for the most suitable motor drive arrangement for an IMMD design. The first integrated regenerative motor drive was proposed in 2002 for industry applications which was based on a matrix converter topology [5]. Another prototype based on matrix converters was built for a 30kW induction motor [6]. The aim of these studies was to eliminate the need for filtering elements. In [7], converter topologies on the rectifier front-end are evaluated for integrated motor drives, keeping the inverter side the same. An IMMD design with soft magnetic composite (SMC) core material for a five-phase machine is developed in [8], where each phase leg is composed of independent IGBT based half-bridges. A similar approach is used in [9] for a six-phase machine, grouping each three-phase with a common neutral point. This was the first IMMD prototype with dedicated controllers on each module to further increase the reliability and fault tolerance. A 50kW, 6-phase integrated fault tolerant permanent magnet motor drive is proposed in [10], where each phase of the drive is composed of a full-bridge converter, instead of half bridges. GaN FETs were firstly introduced into the IMMD designs in 2013 to reduce the DC link capacitor size as well as eliminate the heat sink by operating at high switching frequencies [11]. In this work, series connection of inverter modules is proposed to match the low voltage rating of GaNs to higher DC link voltages. Evaluation of the aforementioned conventional inverter topologies (2L-VSI, 3L-VSI and CHB) has been investigated by the authors of [2] and [3] for IMMDs, and compared with their proposed topology having series connected 2L-VSI

inverters in terms of number of components, flexibility in voltage levels, modularity and fault tolerance [12]. Gate signal interleaving has been applied to decrease the capacitor size [12]. Additional medium-voltage inverter topologies are mentioned in [3] where separate DC links are used for each inverter. Moreover, the series connected topology is further extended with replacing the 2L-VSI with 3L-VSI either in Neutral Point Clamped (NPC) or Flying Capacitor (FC) configuration [3]. Similar evaluation parameters are considered in these studies; however, these evaluations are generally conceptual rather than providing numerical comparisons.

In this paper, a detailed analysis is presented for the evaluation of selected inverter topologies suited for IMMD applications. A conventional 2L-VSI IGBT based inverter is considered in addition to the 2L-VSI and 3L-VSI GaN based IMMD inverters and their series and/or parallel connected derivations. Gate signal interleaving is applied in parallel connected converters to reduce the DC link capacitor size. Motor terminal voltage and line current, DC link voltage and capacitor current spectral analyses are performed using MATLAB/Simulink simulations. Furthermore, power semiconductor losses are analyzed for varying switching frequencies using numerical integration method applied to device waveforms obtained from MATLAB/Simulink simulations.

II. System Description

A. Integrated Modular Motor Drives

Several different ways of integration methods are proposed in the literature as listed in [1]. IMMD structure considered in this paper is called stator iron mount integration where each stator pole piece has its own drive module that consists of power electronics, and control electronics as shown in Fig. 1 [9]. In this study, an IMMD having a nominal output power of 8 kW is considered, the block diagram of which can be seen in Fig. 2. Depending on the number of machine poles, the topology and configuration of modular pole-drive modules can be arranged. The rated values of the system are shown in Table 1.

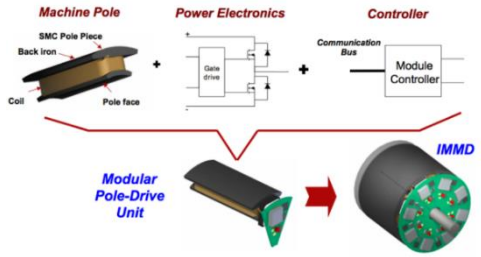


Fig. 1. An IMMD illustration with stator iron mount integration [9]

TABLE I
RATED VALUES OF THE SYSTEM

Parameter	Value
Drive total output power, P_{out}	8 kW
DC link voltage, V_{dc}	540 V
Number of phases in each module, m	3
Power factor, pf	0.9
Fundamental output frequency, f_0	50 Hz

B. Classification of Topologies

Five different IMMD topologies are compared and evaluated which are shown in Fig. 3. 2L-2S-VSI is the same as the one proposed in [12]. 2L-2S2P-VSI and 3L-2P-VSI are topologies derived from the series connected one. These are novel topologies presented in this study where both series and parallel connection are applied simultaneously. The 3-level topologies are in diode clamped (neutral point clamped) multilevel configuration.

Sinusoidal Pulse Width Modulation (SPWM) technique is applied for all topologies. Additionally, interleaving is applied for the topologies where parallel connected modules share the same module capacitor. In fact, the same technique can be applied to series connected modules; however, while decreasing the ripple voltage on the overall DC input, it does not affect the percent ripple on the individual module DC buses. The aim of restricting the percent ripple on the DC link is to make sure that the AC side voltage waveform quality is not affected by the DC link ripples, therefore it is meaningless to decrease the overall DC link voltage ripple. Consequently, interleaving has no net effect on voltage ripple for series connection.

C. Power Semiconductor Devices

In this study, a conventional motor drive topology (2L-VSI) is considered having IGBTs and anti-parallel diodes as power semiconductor devices. By doing so, it is possible to compare the power density and efficiency of IMMDs with a conventional motor drive. For the other topologies, a type of series connection is used purposefully, either directly connecting 2-level modules in series, or using 3-level inverters, to make the drive having an input of 540 VDC compatible with commercially available GAN FETs with the highest voltage rating. Two different GaNs having 650V blocking voltage rating are used from GaN Systems with suitable current ratings according to the having parallel connection or not. Finally, Silicon Carbide (SiC) Schottky diode from Wolfspeed is selected for the clamping diode of the 3-level topologies. All the selected devices and their basic parameters are shown in Table 2 [13], [14], [15].

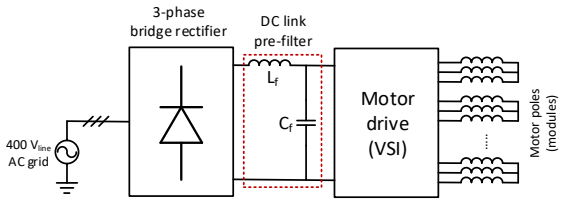


Fig. 2. Block diagram of the IMMD

TABLE II
SELECTED DEVICES AND THEIR PARAMETERS [13], [14], [15]

Device	FF50R12RT4	GS66508B	GS66516B	C5D50065D
Type	IGBT	GaN	GaN	SiC Diode
Voltage	1200 V	650 V	650 V	650 V
Current	50 A	30 A	60 A	50 A
$V_{ce,sat}$	2,15 V	-	-	-
$R_{ds,on}$	-	50 mΩ	25 mΩ	-
V_f (diode)	1.65 V	-	-	2.0 V

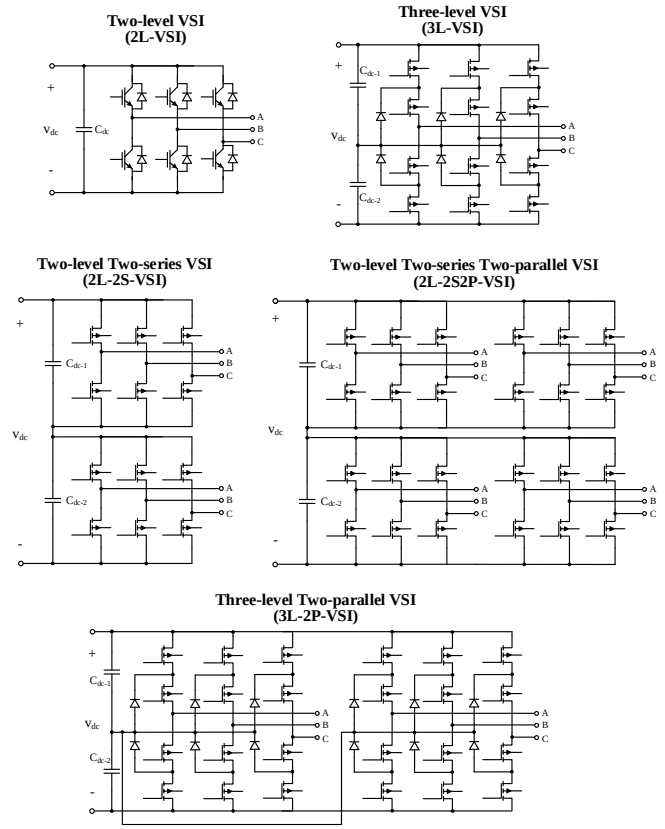
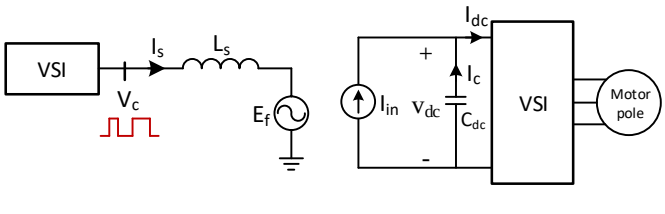


Fig. 3. The five motor drive topologies

III. EVALUATED PARAMETERS

A. *Motor side*

The motor is chosen as a permanent magnet synchronous motor (PMSM) with concentrated windings. The number of slots is kept constant and four stator poles are either connected in series, or connected to the drive modules separately, depending on the number of modules existing in the corresponding topology. The single phase equivalent of one module of the motor is shown in Fig. 4. The induced voltage (E_f) and phase inductance (L_s) are chosen from a pre-designed PMSM specific to this application. The corresponding inverter voltage (V_c) and load angle (δ) are calculated in the simulations. Modulation depth (m_a) of each inverter is kept constant at 0.9 for all topologies. Quality of the voltage and current waveforms are evaluated on the AC side by their harmonic spectrum and total harmonic distortion values for both voltage (THD_v) and current (THD_i), which are calculated as in (1) and (2).



(a) AC side model (b) DC link model

Fig. 4. Models used in the evaluation

$$THD_v = 100\ x \sqrt{\frac{\sum_{n=2}^{\infty} {V_n}^2}{{V_1}^2}} \quad (1)$$

$$THD_i = 100\ x \sqrt{\frac{\sum_{n=2}^{\infty} {I_n}^2}{{I_1}^2}} \quad (2)$$

B. *DC link*

The general model of the DC link is shown in Fig. 4. It is assumed that the DC bus pre-filter is good enough to suppress any low frequency ripples or disturbances coming from the grid side. The DC input is represented by an ideal pure DC current source (I_{in}), magnitude of which depends on the motor loading. Each VSI module draws a current (I_{dc}) which consists of both DC component and a high frequency ripple component, which is supplied by the module capacitor (I_c). The ripple current is directly related to the phase current of the motor pole (I_s) and is independent of the switching frequency (f_{sw}), as expressed in [16]. Ripple current handling capability of the capacitors is a critical design value directly affecting the selected capacitor size, hence power density. The only way to reduce the RMS value of this current for a given output power is to apply interleaving.

The voltage ripple ($V_{dc\text{-}r}$) is critical and should be restricted module-wise as it may introduce additional harmonics to the inverter output voltage. The constraint on the voltage ripple is usually limited by 1%, which is also applied here. The ripple voltage is related to capacitor ripple current, capacitance (C_{dc}) and switching frequency directly, as shown in (3). For a given ripple current (I_c), the ripple voltage constraint can be achieved by either increasing f_{sw} or increasing C_{dc}. Thus, smaller DC bus capacitors can be designed with high frequency operation to meet the size restrictions.

$$I_c \propto V_{dc-r}\ f_{sw}\ C_{dc} \quad (3)$$

Two different types of capacitors are utilized in the DC bus; electrolytic capacitors and metal film capacitors [16]. Electrolytic capacitors have higher capacitance per volume; however, their lifetime is limited and dependent to operating temperature. Therefore, film capacitors are more suitable for integrated motor drives where electronic components are subjected to high operating temperatures. Film capacitors are known for their high current handling capability, but their capacitance per volume rating is low which makes capacitance reduction more critical for an IMMD application. That being said, the spectral analysis of DC link voltage and currents, RMS current requirement and capacitance requirement in terms of switching frequency will be included in this comparison.

C. *Efficiency*

Efficiency is one of the most critical parameters in motor drive applications, especially for heavy duty industrial loads. In addition to this, cooling method and size of the heat sink directly depend on the motor drive efficiency. Remembering the fact that heat sink one of the largest components in the motor drive, minimization of this component is particularly

important for IMMDs. Optimal selection of switching frequency is required for such designs due to its trade-off between the DC link capacitor size and heat sink size due to switching losses. Although GaNs are known for their superior switching performance, the inverter topology still has great impact on the resultant power semiconductor devices losses, and hence efficiency.

The device losses are analyzed using numerical integration method applied to the time-domain voltage and current waveforms gathered from the motor drive simulations. A sample device waveform is shown in Fig. 5 to visualize the applied method for a full conduction cycle of one of the inverter switches. First, all the loss-related data from the device datasheets are converted to functions in MATLAB which are dependent to device currents, using curve fitting. During the integration process, the conduction, turn-on or turn-off losses are detected at each time instant. At each instant, the corresponding energy is calculated using the instantaneous current information, the related datasheet parameter value and simulation time step (Δt). From (4) to (8), the equations used in determining the conduction energy for IGBT, conduction (both forward and reverse) energy for GaN, conduction energy for diode, switching energy (turn-on, turn-off or C_{oss}) for GaN and IGBT, and reverse recovery energy for diode are shown respectively. At the end of the fundamental cycle, cumulative energy components are converted to power losses multiplying by fundamental frequency using (9).

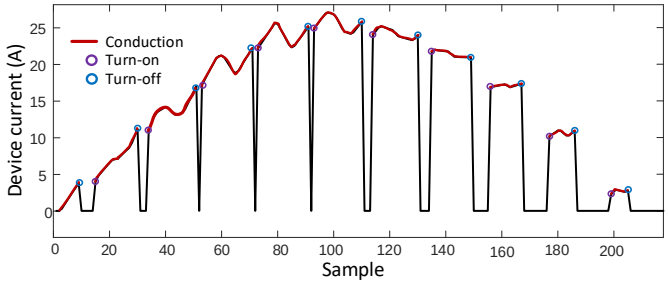


Fig. 5. Visualization of the device loss calculation method

$$E_{con}(t) = V_{ce-sat}[I(t)] \times I[t] \times \Delta t \quad \text{(IGBT)} \quad (4)$$

$$E_{con}(t) = R_{ds-on}[I(t)] \times I[t]^2 \times \Delta t \quad \text{(GaN)} \quad (5)$$

$$E_{con}(t) = V_f[I(t)] \times I[t] \times \Delta t \quad \text{(Diode)} \quad (6)$$

$$E_{sw}(t) = (E_{sw}[I(t)]) \quad \text{(IGBT / GaN)} \quad (7)$$

$$E_{rr}(t) = (E_{rr}[I(t)]) \quad \text{(Diode)} \quad (8)$$

$$P_{loss} = f_0 \times \int E_{loss}\, dt \quad (9)$$

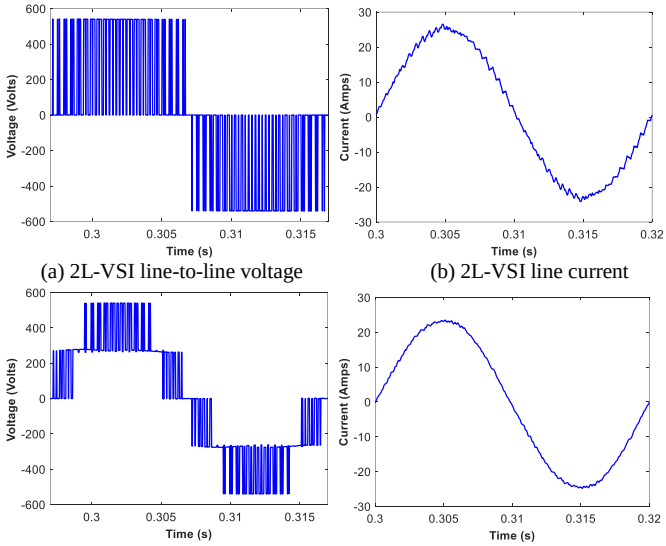
D. Other Considerations

Another crucial factor regarding the motor drive topology is the fault tolerance capability, which is also one of the major features separating IMMDs from conventional drives. Obviously, a single 2L-VSI or 3L-VSI do not have any fault tolerance capability. Although the motor poles are separately connected to distinct modules in series connection, it does not mean a fully fault tolerant operation is obtained. However, assuming the DC link input is unchanged, the motor may still be able to operate with reduced power rating even if one of the modules fail, if the voltage ratings of the remaining modules can withstand by the safety margin used during component selection. This is practical only for high number of series connected modules. Fault tolerance is achievable in real terms when modules are connected in parallel; i.e., if one of the modules fails, the operation can continue with reduced power output. Series and parallel connection also affect the voltage and current ratings of the devices which are also important factors due to two factors: size and cost. Height of a capacitor tends to get smaller as its voltage rating reduces. Moreover, using n devices with 1/n current ratings instead of a single device for a full rating will always result in higher cost. This in fact is the major factor that limits the maximum number of modules used.

IV. Topology Comparison

A. AC side characteristics

Voltage and current waveforms for 2L-VSI and 3L-VSI topologies are shown in Fig. 6. Waveforms for series or parallel connection are not included since only the magnitudes are changed. Moreover, the voltage and current spectra of each topology are shown in Fig. 7. Voltage THD is not affected by the switching frequency, therefore it is presented as a table for different topologies in Table 3. Moreover, current THD values obtained for single switching frequency (10 kHz for 2L-VSI, 50kHz for other topologies) are shown in Table 3 as well.



(a) 2L-VSI line-to-line voltage (b) 2L-VSI line current

(c) 3L-VSI line-to-line voltage (d) 3L-VSI line current

Fig. 6. AC side waveforms for 2L-VSI and 3L-VSI (f_{sw} = 2 kHz)

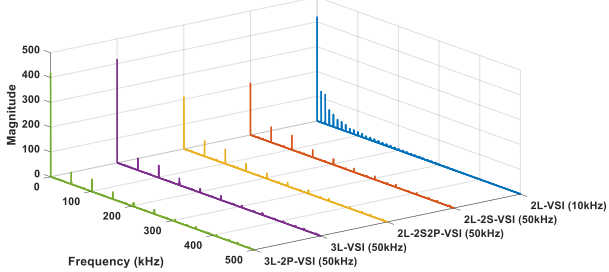


Fig. 7(a) Spectrum of phase voltage

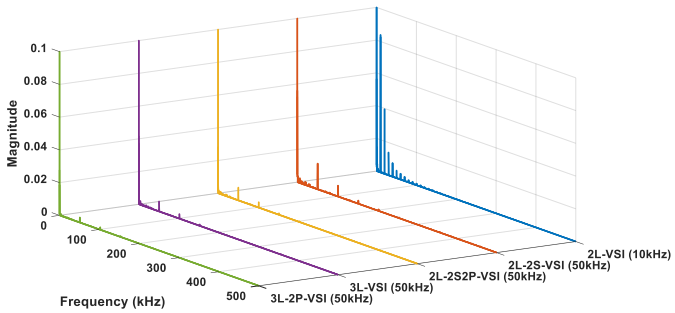


Fig. 7(b) Spectrum of line current

Fig. 7. AC side spectra (f_{sw} = 10 kHz for IGBT, f_{sw} = 50 kHz for GaN)

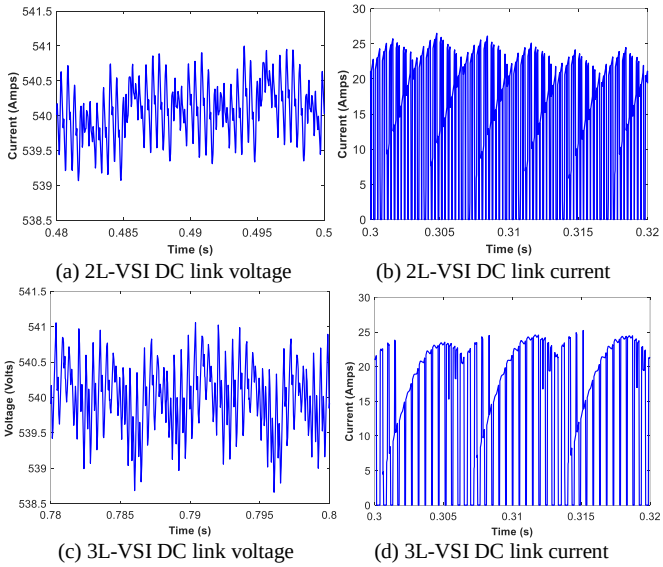
TABLE III

AC OUTPUT VOLTAGE THD AND DC LINK CAPACITOR RMS CURRENT

Topology	THD_v (%)	THD_i (%)	$I_{c\text{-}rms}$ (A)
2L-VSI	79.67	0.96	9.65
2L-2S-VSI	79.57	0.74	9.61
2L-2S2P-VSI	79.52	0.74	7.28
3L-VSI	39.60	0.43	8.49
3L-2P-VSI	39.58	0.43	4.48

B. *DC bus characteristics*

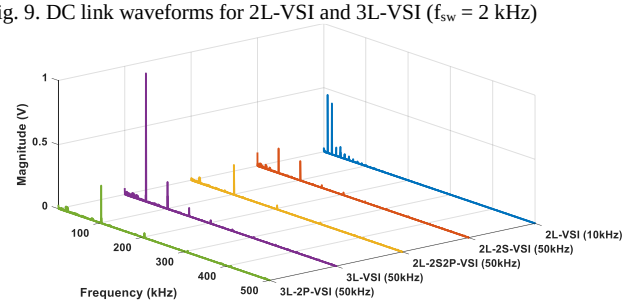
DC link voltage and current waveforms for 2L-VSI and 3L-VSI and effect of interleaving for parallel connected modules are shown in Fig. 9. Moreover, the voltage and current spectra of each topology are shown in Fig. 10. The variation of required capacitance with switching frequency can be seen in Fig. 11. The DC link capacitor RMS currents are listed in Table 3 for all topologies.



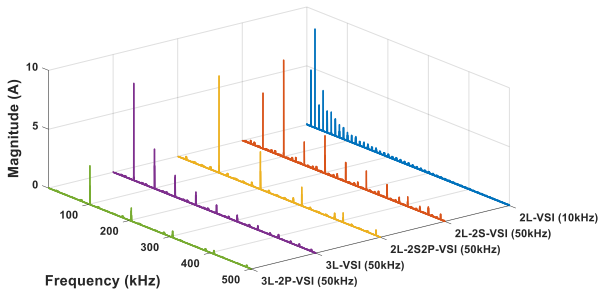
(a) 2L-VSI DC link voltage (b) 2L-VSI DC link current

(c) 3L-VSI DC link voltage (d) 3L-VSI DC link current

Fig. 9. DC link waveforms for 2L-VSI and 3L-VSI (f_{sw} = 2 kHz)



(a) Spectrum of DC link voltage



(b) Spectrum of DC link current

Fig. 10. DC side spectra (f_{sw} = 10 kHz for IGBT, f_{sw} = 50 kHz for GaN)

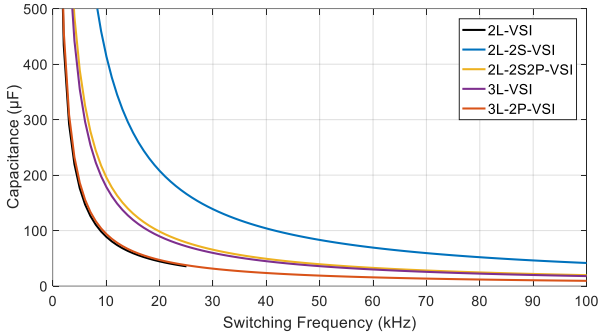


Fig. 11. Variation of required capacitance with switching frequency

C. *Efficiency evaluation*

Variation of motor drive efficiencies with switching frequency for the topologies at full-load are shown in Fig. 12. Since IGBT is used for conventional 2L-VSI motor drive topology, the applied switching frequency is limited to 25 kHz. Distribution of loss components for all topologies are shown in Fig 13.

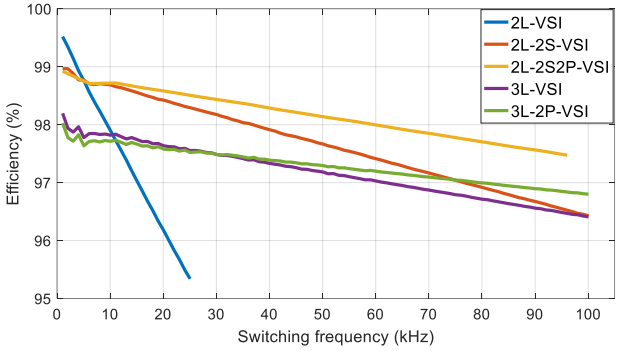


Fig. 12. Variation of motor drive efficiency with switching frequency

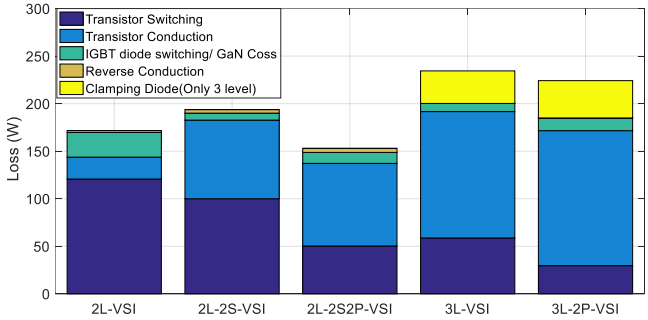


Fig.13. Distribution of loss components for different topologies (f_{sw} = 10 kHz for 2L-VSI, f_{sw} = 50 kHz for other topologies)

D. Discussions

On the motor side, 3L-VSI topologies have better waveform quality for both voltage and current compared to 2L-VSI topologies at the same frequency since the number of levels is higher. Series or parallel connection do not affect the voltage harmonic spectrum on the motor side. IMMD topologies with GaN FETs have the advantage of using higher switching frequencies such that the harmonic frequencies are much greater than the ones of conventional topology with IGBT. Because of this, the magnitude of the motor line current harmonics is also much lower as seen in Fig. 7. For the same switching frequency, THD of both voltage and current is lower for 3L-VSI topologies than 2L-VSI.

On the DC link, 3L-VSI has lower ripple RMS current than 2L-VSI. Apart from this, the only factor that changes the RMS current is the application of phase-shifting (interleaving) which is only applicable in parallel connected topologies. In overall, the best performance on the DC link RMS current is obtained for 3L-2P-VSI. The percent DC bus voltage ripple per module is kept at 1% for all topology simulations to obtain the required capacitance as shown in Fig. 11. The total capacitance variations show that, series connection of modules increase the capacitance requirement, therefore using 3L-VSI topologies instead of series connected 2L-VSI is more advantageous. Parallel connected topologies are also advantageous thanks to interleaving. 3L-2P-VSI and 2L-VSI conventional topology have the best performance on capacitance requirement, however the former can reach much higher switching frequencies, lowering the capacitance more.

According to the results shown in Fig. 12, 2L-2S2P-VSI is the most efficient topology for all frequencies higher than 10 kHz. It has been shown that using parallel connection in any of the topologies result in better efficiencies as the switching frequency gets larger. The 3L-VSI topologies have lower efficiency than 2L-VSI topologies for IMMDs where GAN FETs are used. The conventional 2L-VSI with IGBT have a very good efficiency for very low switching frequency values; however, its efficiency drops drastically since the switching losses get much more dominant. Efficiency values as high as 98% can be achieved below 60 kHz for 2L-2S2P-VSI. The advantages of decreasing the switching losses by using GaN transistors and eliminating all the diode losses introduced by either the transistor or the three level topology, combined with the loss decline brought by the parallel connection makes this topology ideal for high efficiency operation. Despite using a switching frequency 5 times the conventional case, the switching losses of the topologies with GAN FETs are lower. The 3L-VSI topologies has the disadvantage of additional clamping diode losses.

There are two aspects in terms of the fault tolerance of an IMMD system: fault tolerance of the motor; i.e., capability of the motor to operate under the fault of one of the motor windings, and fault tolerance of the drive; i.e., capability of the drive to supply the motor when one drive module is in fault. Motor fault tolerance directly depends on the number of independent motor modules making 2L-2S2P-VSI the most advantageous. Series connection of inverters does not directly imply drive fault tolerance, therefore 2L-2S2P-VSI and 3L-2P-VSI have better drive fault tolerance. In overall, a fully fault tolerant IMMD system can be achieved by using both series and parallel connected 2L-VSI modules.

V. Conclusions

In this paper, comparison of five different motor drive topologies suited for IMMDs is presented. The utilization of GaN devices in IMMDs shows promising performance over a conventional motor drive in all aspects. The improvement in motor drive efficiency to reduce the heat sink size, by using parallel connected modules is shown. Furthermore, size reduction in DC link capacitors is achieved by using gate signal interleaving in modular structure. It has been shown that, 98% efficiency can be obtained with very small DC bus capacitance for a newly proposed topology where 2-level modules are connected both in series and parallel configuration. Permitting the utilization of commercial GaN FETs with series connection, this topology has also increased fault tolerance capability in terms of both motor and drive inverters.

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