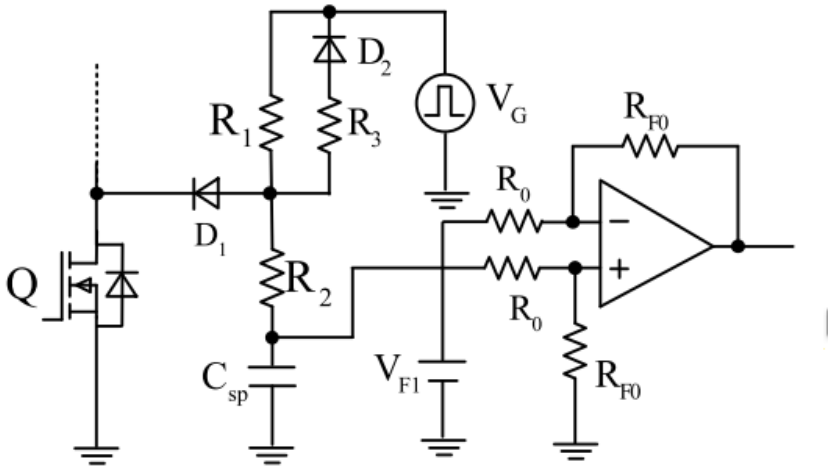
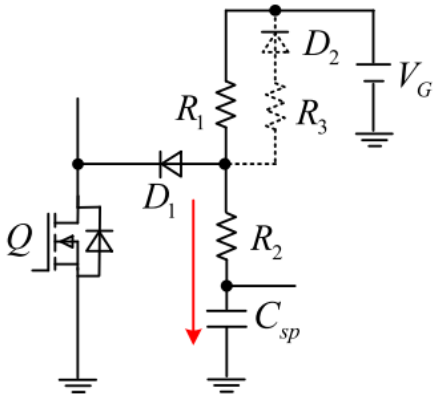
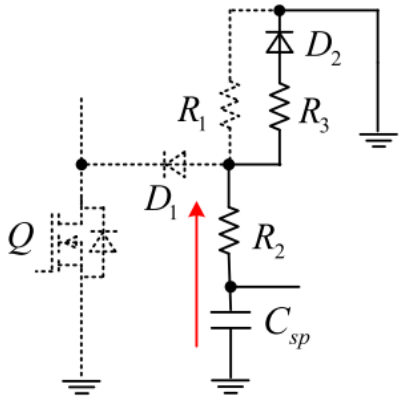


Fig. 4. Schematic diagram of sampling circuit

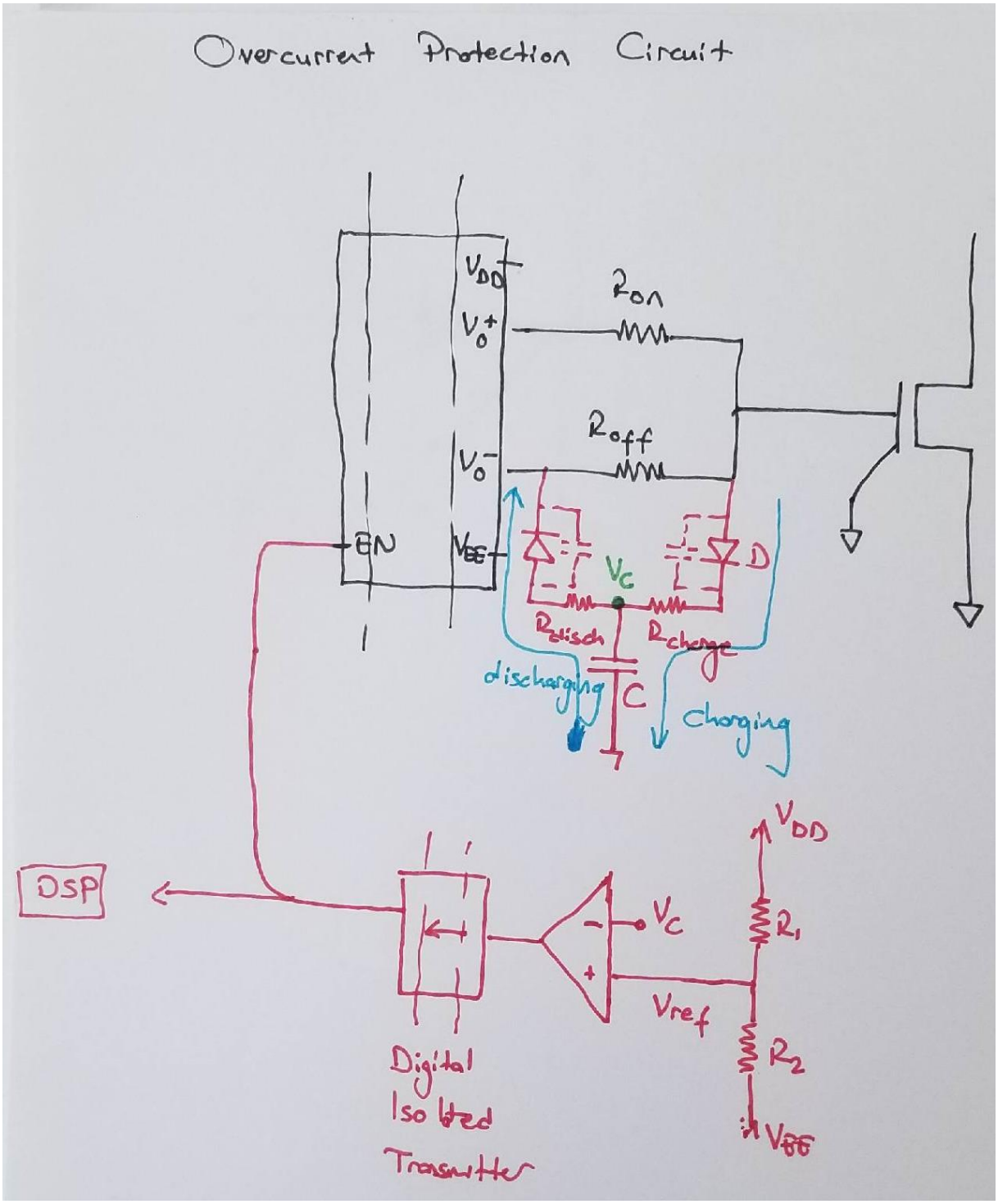


(a) On-state condition



(b) Off-state condition

Fig. 5. Operating principle of the sampling circuit


Overcurrent Protection Circuit
V_{DD}
V_o^+
V_o^-
EN
V_{EE}
R_{on}
R_{off}
V_C
D
R_{disch}
R_{charge}
discharging
C
charging
DSP
Digital
Isolated
Transmitter
V_{DD}
R_1
V_C
V_{ref}
R_2
V_{EE}