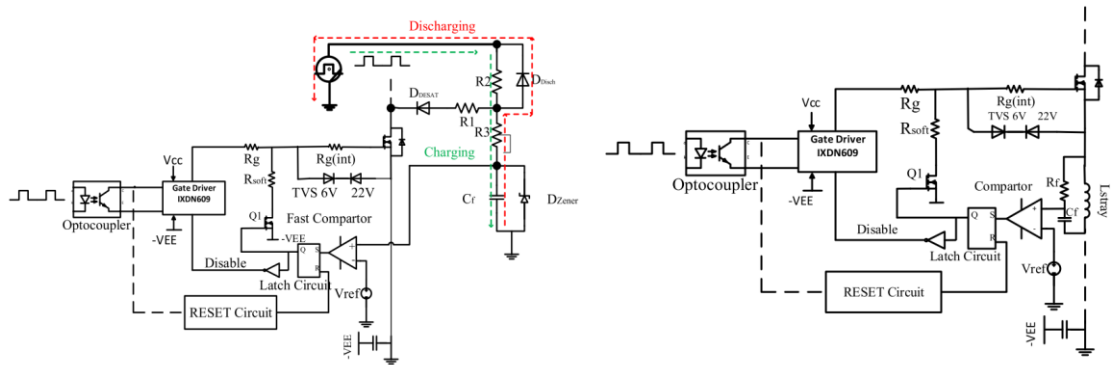
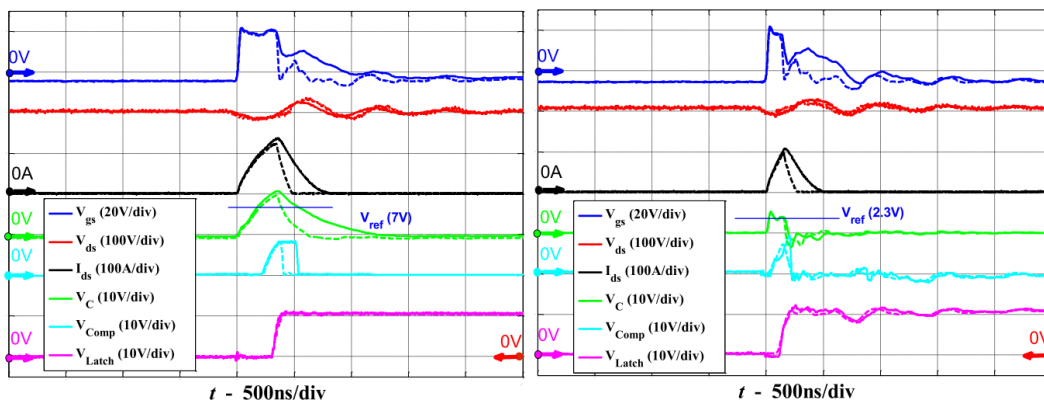


Protection Techniques



a- Desaturation Technique

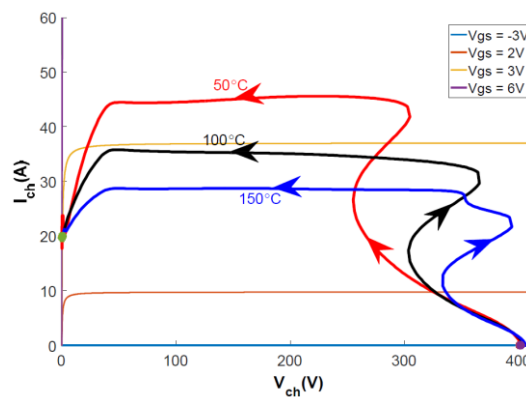
b- Parasitic Inductance Technique



(a) Desaturation Technique

(b) Parasitic Inductance Technique

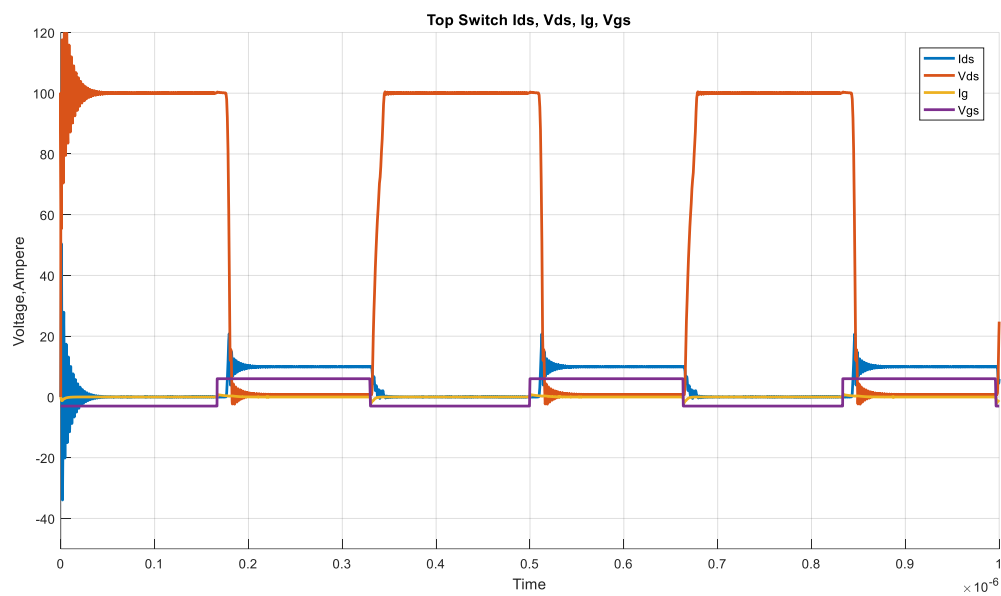
- Parasitic inductance technique detects fault 2 times faster
- Desaturation technique requires fast and low C_{oss} diodes
- The current can be limited in lower level with parasitic inductance technique
- Desaturation technique has less distorted node voltages



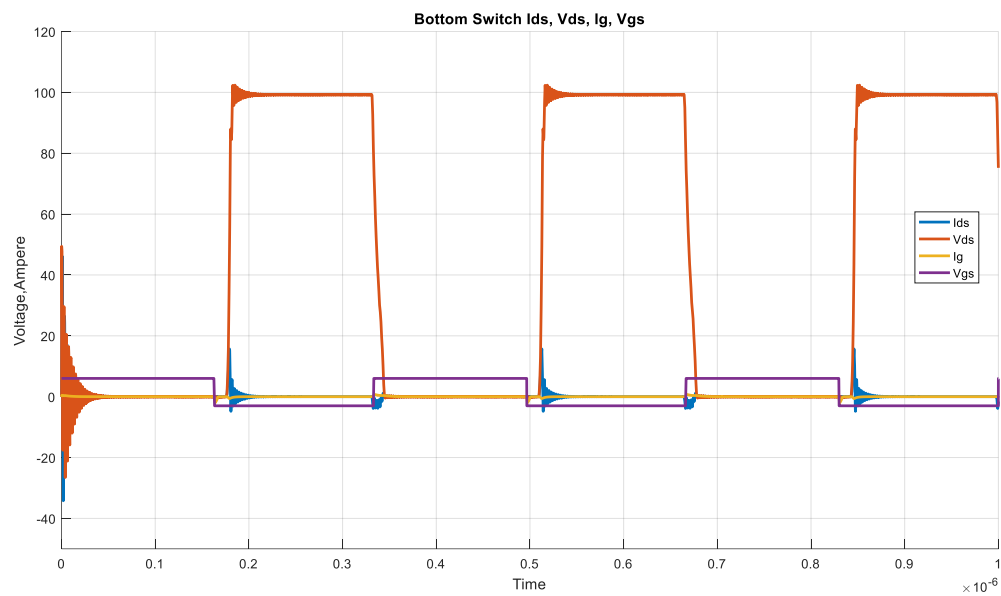
For GaN transistor with loop inductance of 7 nH

- @ 150°C - di/dt is nearly 8.6 A/ns
- @ 100°C - di/dt is nearly 12.8 A/ns
- @ 50°C - di/dt is nearly 21.4 A/ns

State Space Simulations



Top Switch Waveforms



Bottom Switch Waveforms

ODE Solvers

```
tspan = [0 400e-6];  
x0 = zeros(4,1);  
[tout,xout] = ode45(@GaN, tspan, x0);
```

Elapsed time decreased from 2.65 secs to 1.57 secs.

Minimum time-step can be limited.

Solver selection is critical.

