Instability Analysis and Oscillation Suppression of Enhancement-Mode GaN Devices in Half-Bridge Circuits

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***Abstract*—This paper analyzes the problem of instability in enhancement-mode gallium nitride (GaN) transistors based half-bridge circuits. The instability may cause sustained oscillation, resulting in overvoltage, excessive electromagnetic interference (EMI), and even device breakdown. GaN devices operate in the saturation region when they conduct reversely during the dead time. Under the influence of parasitic parameters, the GaN-based half-bridge circuit exhibits positive feedback under certain conditions, thus resulting in sustained oscillation. A small-signal model is proposed to study this positive feedback phenomenon. Like the second-order under-damped system, damping ratio is defined to determine the system's stability. Based on the model, the influence of circuit parameters on instability is investigated and guidelines to suppress the oscillation are given. Reducing the common-source inductance, increasing the gate resistance of the inactive switch or connecting a diode in parallel to the inactive switch are some effective ways to suppress the oscillation. Finally, the analyses are verified by both simulation and experiment.**

***Index Terms*—Gallium nitride (GaN), sustained oscillation, positive feedback, parasitic, reverse conduction.**

I. Introduction

In recent years, gallium nitride (GaN) transistors are gaining increased attention in high efficiency and high power-density converters [1], [2]. Compared with silicon devices, GaN devices have a smaller figure of merit [3], and thus are capable of working at a higher switching frequency while maintaining high efficiency. As the switching frequency increases, the power density of the converter can be increased due to the reduction in the size of the passive components [4]–[10]. However, higher switching speed can lead to more serious overvoltage and parasitic ringing, and lower on-resistance and capacitances can result in a smaller damping ratio. This can lead to more severe instability problems for GaN-based power circuits [11]–[14].

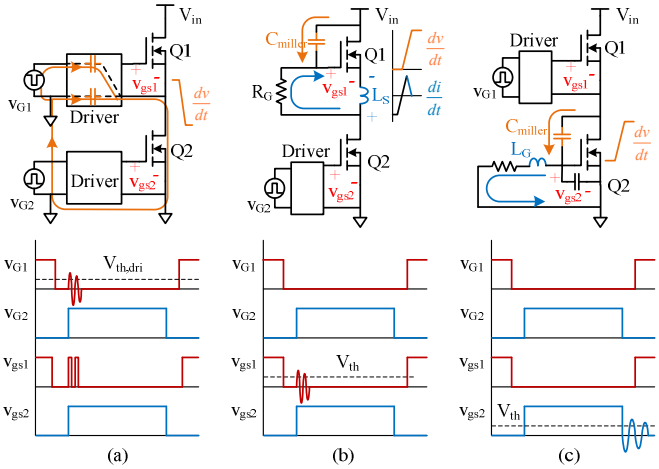

Fig. 1. Equivalent circuit and typical waveforms of the common instability problems. V_{G1} and V_{G2} are the PWM signals; V_{gs1} and V_{gs2} are the gate-source voltages. (a) PWM signal noise, related to high *dv/dt* and parasitic capacitance between power circuit and signal circuit. (b) Turn-on gate oscillation, related to high *dv/dt*, high *di/dt*, miller capacitance and common-source inductance. (c) Turn-off gate oscillation, related to high *dv/dt* and large gate inductance.

Research work has been conducted to study the instability problem. Fig. 1 shows the three common problems of instability. One of the problems is the PWM signal distortion caused by high *dv/dt* [11], [15]. High *dv/dt* can distort the PWM signal through the parasitic capacitance between signal circuit and power circuit. The distorted PWM signal may trigger the switch to falsely turn on or turn off. The second common problem is the turn-on gate oscillation induced by high *dv/dt* and high d*i*/d*t* [12], [16]–[18]. In a half-bridge circuit, when the active switch turns on, the drain-source voltage of inactive device increases sharply. The displacement current flows through the miller capacitance of the inactive switch to its gate node, which may cause the gate-source voltage to exceed the threshold voltage. Meanwhile, a voltage is generated across the common-source inductance under the effect of *di/dt*. The voltage worsens the gate-source voltage of the inactive switch through the driver loop. In worse cases, this problem could lead to sustained oscillation. The third problem of the instability is turn-off gate oscillation caused by the large gate inductance and

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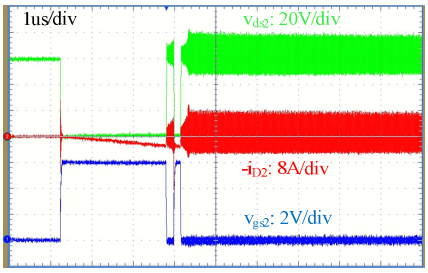

Fig. 2. Measured sustained oscillation waveforms in the GaN-based half-bridge circuit.

high *dv*/*dt*. During the active switch turn-off process, the current through miller capacitance caused by high *dv*/*dt* must be sunk though the gate inductance, and thus energy is stored in gate inductance. Then under the effect of gate inductance and input capacitance, the gate voltage of active switch rings back and may exceed the threshold voltage, thus resulting in false turn-on and even sustained oscillations. The papers [13], [19] established a model using negative resistance theory and successfully explained the instability of a SiC-based circuit. Another problem is observed in cascode GaN devices under high-current turn-off condition [14]. The cascode GaN device is normally off by using a low-voltage Si MOSFET connected in series with a depletion-mode GaN device. The capacitance mismatch between GaN device and Si MOSFET may result in the oscillation. Adding a proper capacitor in parallel with Si MOSFET can solve the problem.

Besides the above problems, there is another problem observed in enhancement-mode GaN devices based half-bridge circuit. Fig. 2 shows the measured waveforms and Fig. 3 is the GaN-based half-bridge circuit. The oscillation occurs when the active switch is off and the inactive switch conducts reversely. Note that the gate-source voltage of the active device is normal. The oscillations are related to the unique reverse conduction characteristics of the GaN devices, which does not occur in silicon or silicon carbide MOSFETs based circuit because of their different reverse conduction characteristics from GaN devices.

This paper presents a theoretical treatment of the sustained oscillation problem in enhancement-mode GaN devices based half-bridge circuits. The GaN devices work in the saturation region due to their unique reverse conduction characteristics when conducting reversely during dead-time. And a feedback system is formed if the parasitic parameters are considered. The feedback may become positive under some conditions, resulting in sustained oscillations. A small-signal model is proposed to describe the feedback system. Then the stability criterion is proposed to determine the stability of the system. Based on the stability criterion, the effect of circuit parameters on the oscillation is investigated and guidelines to suppress the oscillation are presented. Spice simulation is performed to verify the analysis and provides detailed insight into the problem. Finally, a GaN-based half-bridge prototype is built and the experiment results show a good agreement with the analyses.

The paper is organized as follows. Section II proposes a model to describe the problem of instability. Section III investigates the influence of circuit parameters on instability and presents guidelines to suppress the oscillation. Section IV and V are simulation and experiment verifications. Section VI concludes the paper.

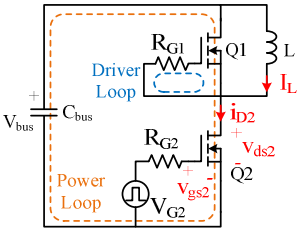

Fig. 3. A half-bridge circuit with inductive load. Q1 is the inactive device and Q2 is the active device.

TABLE I
LIST OF SYMBOLS

Symbol	Description
g_m	Reverse transconductance
R_{loop}	High-frequency power loop resistance
R_{Gint}	Internal gate resistance of Q1
R_{G1}	External added gate resistance of Q1
R_G	Total gate resistance, sum of R_{Gint} and R_{G1}
L_S	Common-source inductance of Q1
L_G	Gate inductance of Q1
L_D	Drain inductance
C_{gs}	Gate-source capacitance of Q1
C_{ds}	Drain-source capacitance of Q1
C_{gd}	Gate-drain capacitance of Q1
C_{oss2}	Output capacitance of Q2
C_{ext}	External capacitance paralleled with C_{oss2}
i_{ch}	Channel current of Q1
i_{D2}	Drain current of Q2
v_{gd}	Gate-drain voltage of Q1
v_{ds2}	Drain-source voltage of Q2
v_{gs2}	Gate-source voltage of Q2

II. CIRCUIT MODELING AND STABILITY CRITERION

A half-bridge circuit with an inductive load in Fig. 3 is chosen to study the instability problem. The top switch Q1 works as a synchronous device, which is called inactive device. The bottom switch Q2 is an active device driven by double pulse signals. The switching of the active switch causes current commutation with the external circuits while the switching of the inactive switch only causes current commutation within the switch. The inactive switch is also called 'synchronous FET'. After Q2 turns off, the inductor current I_L flows through Q1 from its source to drain. In this case, the sustained oscillation may occur due to the reverse conduction characteristics of GaN devices and parasitic parameters. Table I lists the symbols used in this paper.

A. Reverse Conduction Characteristics of GaN Devices

The reverse conduction characteristics of GaN devices are quite different from that of Si or SiC MOSFETs. Si or SiC MOSFETs have body diodes to conduct the reverse current. As for GaN devices, there is no body diode existing in them. When the gate-source voltage V_{gs} or gate-drain voltage V_{gd} is greater

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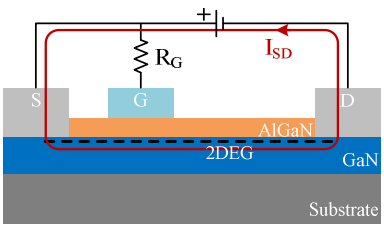

Fig. 4. Simplified structure of GaN devices when conducting reverse current. 2DEG in the channel starts to conduct when $V_{gd} > V_{gd,th}$.

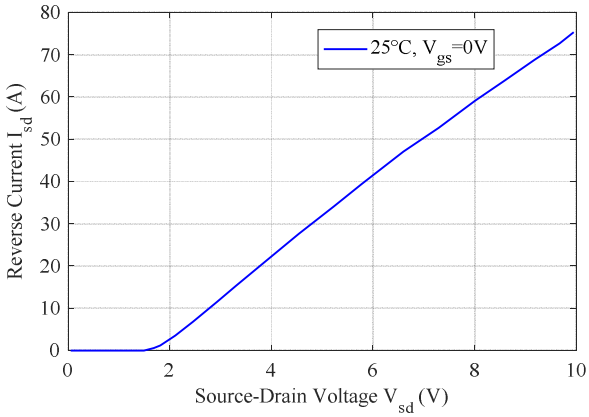

Fig. 5. Reverse conduction characteristics of a 650 V GaN device [21].

than the threshold voltage, the electrons are attracted to the aluminum gallium nitride (AlGaN) and GaN heterostructure interface so that the two-dimensional electron gas (2DEG) is reestablished, and thus the GaN devices can conduct current [3], [20]. The conditions that GaN devices can conduct current are

$$V_{gd} > V_{gd,th} \text{ or } V_{gs} > V_{gs,th} \tag{1}$$

where $V_{gd,th}$ is gate-drain threshold voltage and $V_{gs,th}$ is gate-source threshold voltage.

Fig. 4 shows a simplified structure of GaN devices when conducting reversely. The gate-source voltage V_{gs} equals 0 V because the gate leakage current is negligible. In other words, $V_{gd} = V_{sd}$. After Q2 turns off, inductor current charges the output capacitance of Q1 reversely, resulting in the increase of V_{sd}. Q1 starts to conduct until V_{sd} exceeds the threshold voltage $V_{gd,th}$. Q1 works in saturation region because

$$V_{sd} > V_{gd} - V_{gd,th}. \tag{2}$$

The channel current I_{ch} is now controlled primarily by the gate-drain voltage V_{gd}.

Fig. 5 shows the reverse conduction characteristics of a 650 V GaN device. The curve is measured at steady-state, so the current I_{sd} equals the channel current I_{ch}. Meanwhile, V_{gd} equals V_{sd} when V_{gs} is 0 V. Therefore, the I_{sd} - V_{sd} curve is also the I_{ch} - V_{gd} curve and the following relationship can be obtained:

$$I_{ch} = f(V_{gd}) \tag{3}$$

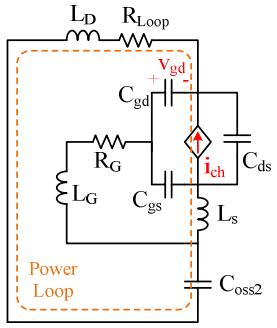

Fig. 6. Small-signal circuit of the half-bridge circuit.

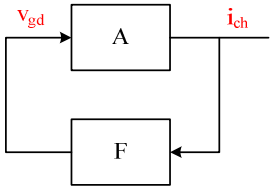

Fig. 7. Block diagram of the feedback system.

Equation (3) shows that the GaN device's channel can be equivalent to a voltage-controlled current source.

B. *Small-Signal Model*

Because the transconductance and capacitance of switching device are nonlinear, it is difficult to directly establish a model to determine the stability of the circuits. With the linearized small-signal model, the stability theory of linear system can be used. The small-signal circuit in Fig. 6 is derived from the circuit in Fig. 3. The bus capacitor C_{bus} is shorted and the inductor L is opened. Q2 is replaced by its the output capacitance C_{oss2} because it has been turned off. Q1 is replaced by a voltage-controlled current source combining with three capacitors. Gate resistance R_G consists of Q1's inner gate resistance R_{Gint} and external gate resistance R_{G1}. The common-source inductance L_S is the inductance shared by the driver loop and the power loop. The gate inductance L_G is defined as the driver loop inductance minus the common-source inductance. The drain inductance L_D is defined as the power loop inductance minus the common-source inductance. R_{loop} is the high-frequency power loop resistance.

The small-signal circuit can be described by a feedback system. Fig. 7 shows the block diagram of the feedback system. A is the amplified gain. F is the feedback transfer function.

According to (3), A is derived as

$$A(s) = \frac{i_{ch}(s)}{v_{gd}(s)} = g_m \tag{4}$$

where i_{ch} is a small change of the channel current, v_{gd} is a small change of gate-drain voltage, and g_m is the transconductance.

Next is to derive the feedback transfer function F. Fig. 6 is redrawn as shown in Fig. 8(a). The impedances Z_1, Z_2, and Z_3 form a star connection. The star connection can be changed into delta connection by using the following formulas:

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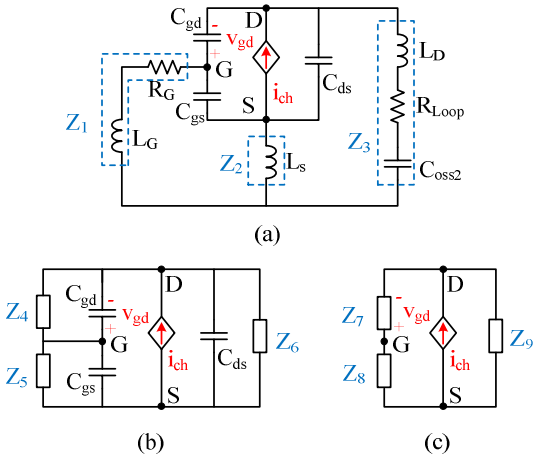

Fig. 8. Circuit simplification processes for deriving the feedback transfer function *F*.

$$Z_4 = \frac{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}{Z_2} \tag{5}$$

$$Z_5 = \frac{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}{Z_3} \tag{6}$$

$$Z_6 = \frac{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}{Z_1} \tag{7}$$

where $Z_1=R_G+sL_G$, $Z_2=sL_S$, and $Z_3=R_{loop}+sL_D+1/sC_{oss2}$. The circuit is further simplified in Fig. 8(c), where $Z_7=Z_4//(1/sC_{gd})$, $Z_8=Z_5//(1/sC_{gs})$, and $Z_9=Z_6//(1/sC_{ds})$. Then we could obtain the feedback transfer function:

$$F(s) = \frac{v_{gd}(s)}{i_{ch}(s)} = -\frac{Z_7Z_9}{Z_7 + Z_8 + Z_9} \tag{8}$$

Then, the loop gain *G* is expressed as:

$$G(s) = A(s)\cdot F(s) = -\frac{g_m}{s}\frac{a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0}{b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \tag{9}$$

where b_i and a_i (i=0, 1, 2, 3, 4) are coefficients listed in Appendix. It should be noted that this is a fifth-order system. There are seven dynamic elements, a loop formed by C_{gd}, C_{gs}, and C_{ds}, and a cut set formed by L_S, L_G, and L_D. The order of the system is the number that the dynamic elements minus the number of loops formed by capacitors and the number of cut sets formed by inductors.

The well-known Barkhausen stability criterion states that for any feedback system to attain stable oscillation, the loop gain is equal to unity [22]:

$$G(j\omega_0) = 1 \tag{10}$$

where ω_0 is oscillation frequency. However, little information about the stability can be acquired from (10). In order to have a deeper insight into the system, the block diagram is modified by adding a disturbance signal *d*, as shown in Fig. 9.

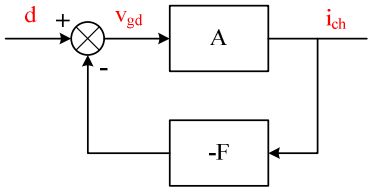

Fig. 9. Modified block diagram of the feedback system. *d* is the disturbance.

TABLE II
CIRCUIT PARAMETERS

Symbol	Value	Symbol	Value
g_m	10 S	L_D	7 nH
R_{loop}	0.22 Ω	C_{gs}	240 pF
R_G	1.3 Ω	C_{ds}	440 pF
L_S	0.2 nH	C_{gd}	60 pF
L_G	5.2 nH	C_{oss2}	65 pF – 500 pF

According to Fig. 9, the closed-loop transfer function $T(s)$ is derived as:

$$T(s) = \frac{i_{ch}(s)}{d(s)} = \frac{A(s)}{1 - G(s)} \tag{11}$$

Submitting (4) and (9) into (11), it yields (12):

$$T(s) = \frac{g_m s(b_4s^4 + b_3s^3 + b_2s^2 + b_1s^1 + b_0)}{c_5s^5 + c_4s^4 + c_3s^3 + c_2s^2 + c_1s + c_0} \tag{12}$$

The poles of $T(s)$ determines the stability of the system. The system is unstable if the real part of any pole is positive. All poles can be solved easily with the help of mathematical tools if the circuit parameters are known.

The circuit parameters are obtained based on the experimental prototype. Parasitic inductance is extracted through Ansys Q3D extractor software according to the PCB layout. The transconductance and capacitances are taken from the device's datasheet. Their values are chosen at the DC operating point which is determined by inductor current and bus voltage. The DC operating point selected for linearization is when Q2 has turned off and Q1 is reversely conducting. At this operating condition, C_{oss2} is the value when Q2 is biased at the bus voltage and g_m is the slope of the I_{sd} - V_{sd} curve where the current equals the inductor current. The capacitance C_{oss2} varies from 500 pF to 65 pF when the bus voltage increases from 0 V to 500 V. Table II lists the circuit parameters.

C. *Stability Criterion*

With the purpose of illustrating the stability of the system, the pole-zero map of $T(s)$ is plotted in Fig. 10(a). There are 5 poles, a real pole p_3 and two pairs of complex conjugate poles p_1 and p_2. The real pole p_3 is negative and located far from the imaginary axis, therefore has no effect on the instability of the

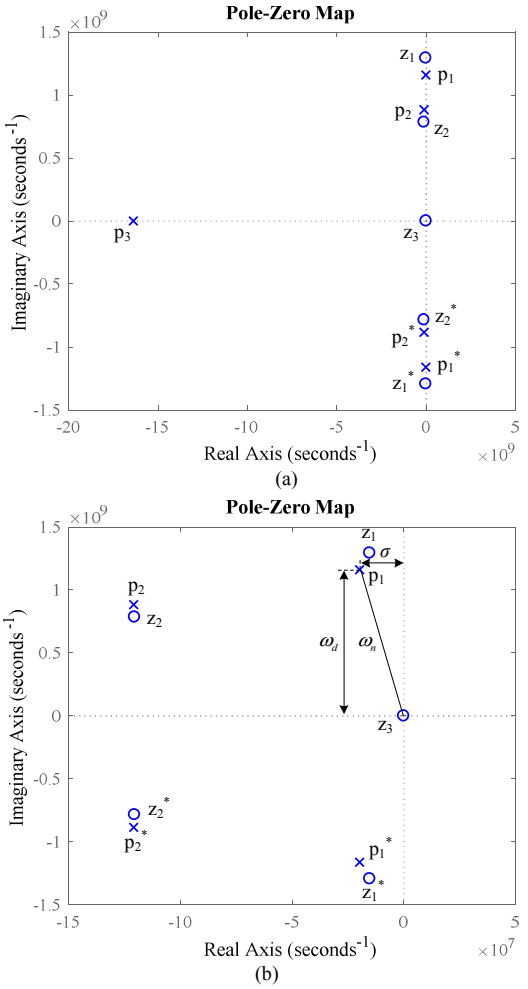

Fig. 10. (a) Pole-zero map of closed-loop transfer function $T(s)$. (b) Enlarged pole-zero map. (L_D = 7 nH; C_{oss2} = 100 pF; R_{loop} = 0.22 Ω; R_G = 1.3 Ω; L_G = 5.2 nH; C_{gs} = 240 pF; L_S = 0.2 nH; C_{ds} = 440 pF; g_m = 10 S; C_{gd} = 60 pF).

system. Fig. 10(b) is the enlarged view and it shows that p_1 is much closer to the imaginary axis than p_2. Therefore, p_1 is the dominant pole and determines the system's stability.

The complex pole p_1 can be defined in terms of their real and imaginary parts:

$$p_1 = -\sigma + j\omega_d \tag{13}$$

Similar to the second-order system, the damping ratio is defined as [23]:

$$\varsigma = \frac{\sigma}{|p_1|} = \frac{\sigma}{\sqrt{\sigma^2 + \omega_d{}^2}} = \frac{\sigma}{\omega_n} \tag{14}$$

The damping ratio ζ can be used to reflect the stability of the system. When $\zeta = 0$, the amplitude of the oscillation remains constant over time and the oscillation frequency is ω_d. When $\zeta > 0$, the pole has a negative real part so the system is stable. The greater the damping ratio ζ is, the faster the oscillation damps. When $\zeta < 0$, the pole has a positive real part so the system is

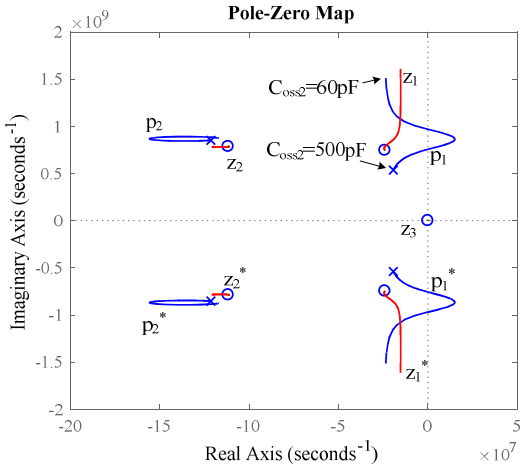

Fig. 11. Pole-zero locus of $T(s)$ when C_{oss2} changes from 60 pF to 500 pF.

unstable and the oscillation amplitude increases with time. Note that the oscillation will eventually turn into a steady state because of the nonlinearity of the switching devices. Fig. 2 clearly shows the process that the oscillation changes from an increased state to a steady state.

Because p_1 is very close to the imaginary axis, the oscillation frequency can be approximately calculated:

$$f \approx \frac{\omega_d}{2\pi} \tag{15}$$

Fig. 11 shows the pole-zero locus of $T(s)$ when C_{oss2} changes from 60 pF to 500 pF. It is reasonable to use p_1 as the dominant pole because p_1 is always much closer to the imaginary axis than p_2. Fig. 11 also shows that p_1 enters the right half plane when C_{oss2} is in a certain range. Because C_{oss2} is nonlinear and decreases as the drain-source voltage increases, the system is unstable in a certain range of bus voltage.

III. Influence of Circuit Parameters on Instability

The oscillations can cause many problems: overvoltage, excessive EMI, or even device breakdown. To avoid the sustained oscillation and suppress the oscillation rapidly, the influence of the parameters on the instability are studied and the guidelines are developed.

A. Influence of Circuit Parameters on Instability

Fig. 12 - Fig. 21 illustrate the damping ratio variation by sweeping different circuit parameters to investigate their influence on stability. The plotting procedures of each curve are as follows. First, the bus voltage is divided into a number of discrete values from 10 V to 500 V and the value of C_{oss2} corresponding to each bus voltage is obtained according to the C_{oss} - V_{ds} curve. Then, the poles are solved after substituting C_{oss2} and other parameter values into (12). Finally, the damping ratios at the corresponding bus voltage are obtained by using (14). The circuit parameters are listed in Table II.

The damping ratio changes significantly when the bus voltage is below 200 V since C_{oss2} reduces rapidly with the

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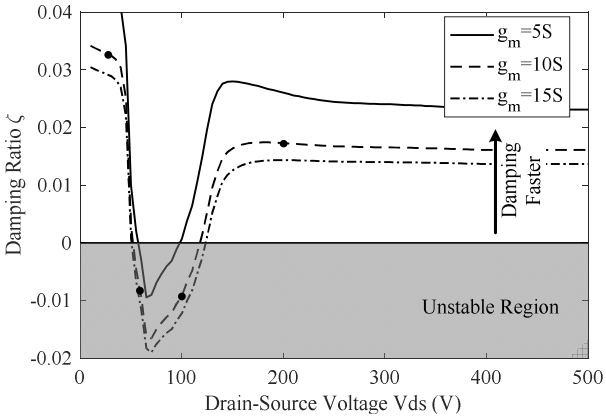

Fig. 12. Damping ratio ζ vs. transconductance g_m.

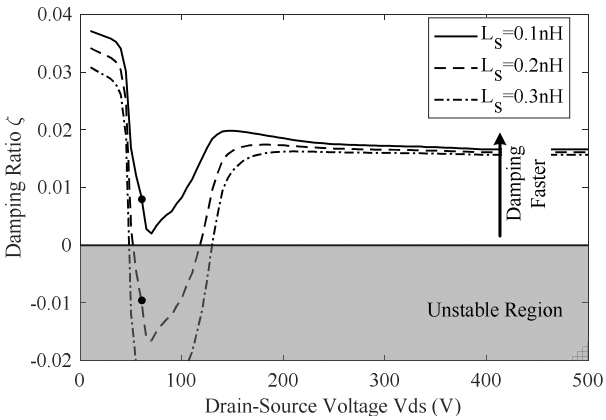

Fig. 13. Damping ratio ζ vs. common-source inductance L_S.

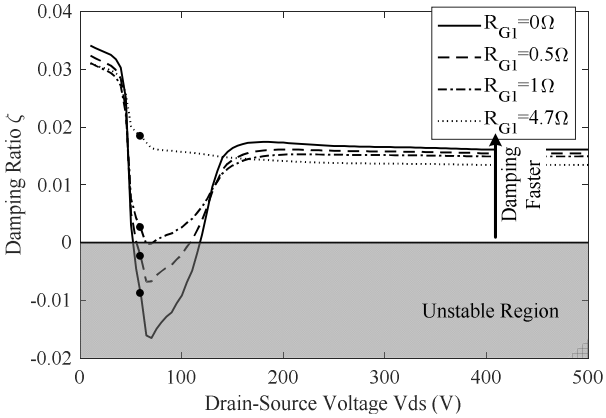

Fig. 14. Damping ratio ζ vs. external gate resistance R_{G1}.

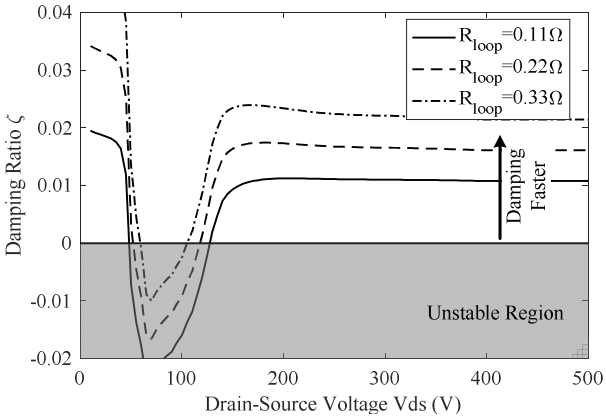

Fig. 15. Damping ratio ζ vs. power loop resistance R_{loop}.

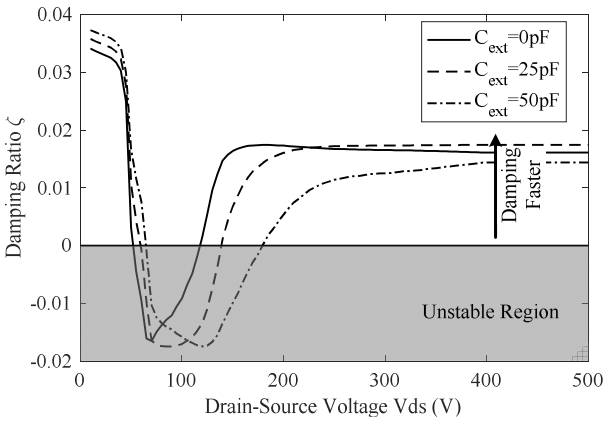

Fig. 16. Damping ratio ζ vs. external capacitance C_{ext} paralleled with C_{oss2}.

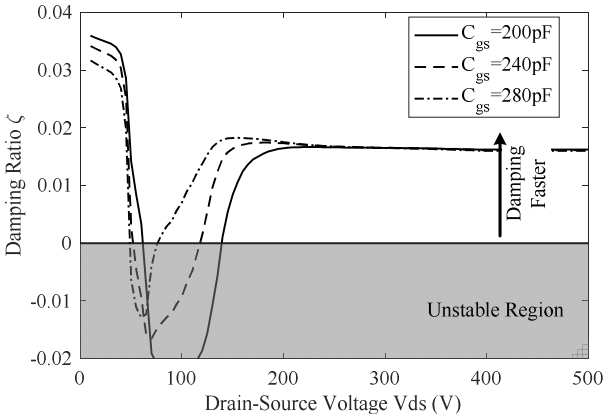

Fig. 17. Damping ratio ζ vs. gate-source capacitance C_{gs}.

increase of the bus voltage. When the bus voltage is above 200 V, the damping ratio is nearly constant because the change of C_{oss2} is small. According to the figures, it can be concluded that: the damping ratio increases with an increase of R_{loop}, or increases with a decrease of g_m and L_S; the system tends to be more stable with larger R_g and C_{gs}; the unstable region moves to a lower voltage region with a decrease of L_D or an increase of L_G; an increase in C_{oss2} enlarges the unstable region; C_{gd} and C_{ds} have little influence on the damping ratio.

Further analyses are conducted to gain a better understanding of the instability. Fig. 22 shows the bode diagram of power loop impedance Z_{Power} (defined as $R_{loop}+s(L_D+L_S)+1/sC_{oss2}$) and loop gain G. The oscillation frequency is located where the phase of the loop gain G is near zero, which is close to the resonant frequency of Z_{Power}. Since Z_{Power} is very low at the oscillation frequency, most of the oscillation current should flow through the power loop. When the large oscillation current flows through L_S, a large voltage is generated in L_S, and then could have a significant impact on v_{gd} through the driver circuit. The smaller L_G tends to allow more voltage generated in L_S to be fed back into v_{gd}, resulting in worse oscillation. Because $L_S \ll L_G$, $Z_6 \approx Z_{Power}$. As shown in Fig. 8(b), C_{ds} is connected in paralleled with Z_6. The impedance of C_{ds} is much larger than Z_6 at the oscillation frequency, which is satisfied in most cases, so the role of C_{ds} is negligible.

In addition, the junction temperature of the device also has

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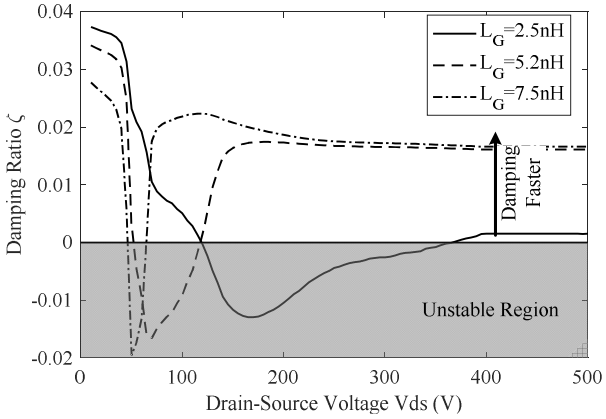

Fig. 18. Damping ratio ζ vs. gate inductance L_G.

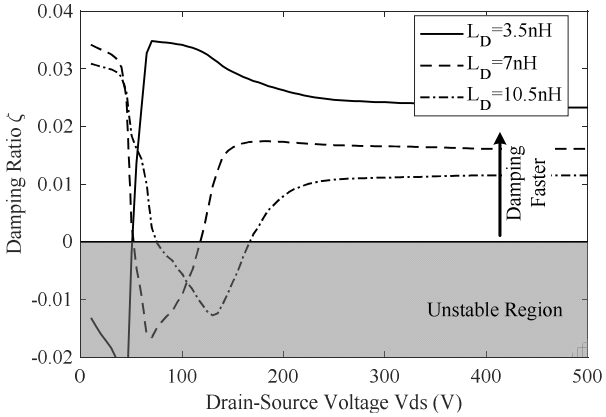

Fig. 19. Damping ratio ζ vs. drain inductance L_D.

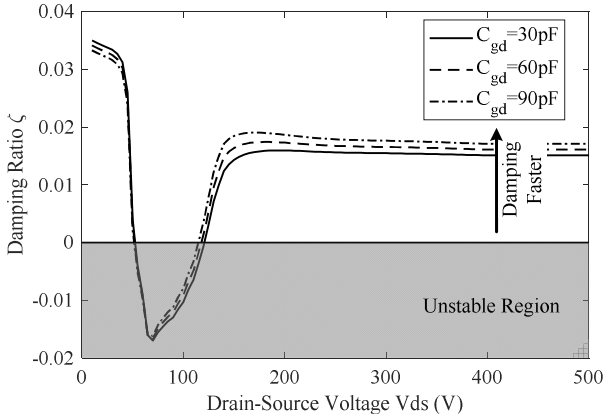

Fig. 20. Damping ratio ζ vs. gate-drain capacitance C_{gd}.

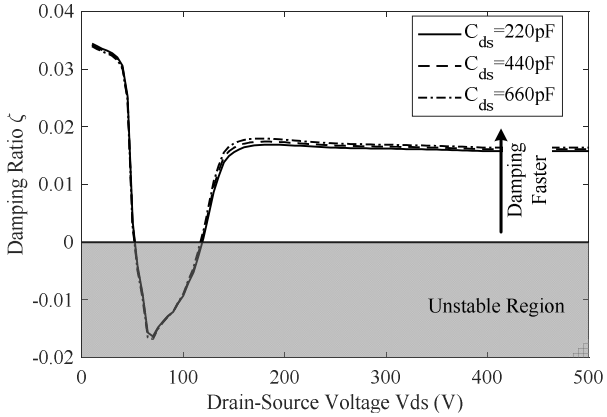

Fig. 21. Damping ratio ζ vs. drain-source capacitance C_{ds}.

an effect on the oscillation. R_{loop} increases as the junction temperature increases due to the increased on-resistance of the device. Meanwhile, g_m decreases as junction temperature increases. So the damping ratio increases and the system tends to be more stable at higher junction temperature.

B. Guidelines to Suppress Oscillation

According to the above analysis, the guidelines to suppress the oscillation are summarized. The first option is to reduce the parasitic parameters such as L_D, C_{ext}, and especially L_S by optimizing the layout. Another benefit of reducing L_D, L_S, and C_{ext} is that the switching losses are reduced accordingly [24]–[26]. The second method is to increase the gate resistance R_G. This is the simplest and easiest way. However, larger R_G increases the risk of false turn-on problem [17]. In addition, paralleling a diode with Q1 is also an effective way. After Q2 turns off, the reverse current is bypassed by the diode and Q1 no longer operates in the saturation region. So the unstable phenomenon does not occur. Another benefit is that the reverse conduction loss can be reduced because the reverse conduction voltage of the diode is smaller than that of the GaN device [27]. The disadvantage is that the switching losses are increased due to the junction capacitance and the reverse recovery charge of the diode.

It is not recommended to improve the stability by increasing L_G because the large L_G will cause the gate voltage oscillation. Besides, an external paralleled C_{gs} may not be effective because of the presence of L_S and R_{Gint}. It should be noted that reducing the switching speed of the active device doesn't help to reduce the risk of sustained oscillation.

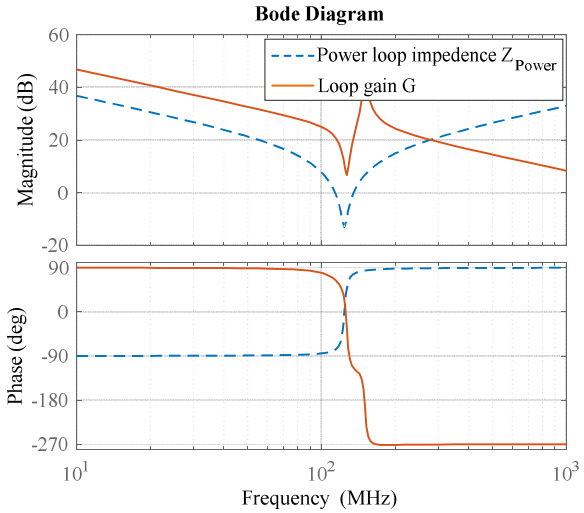

Fig. 22. Bode diagram of the power loop impedance Z_{Power} and loop gain G.

IV. Simulation Verifications

Simulation is conducted to verify the analysis using LTspice software. The simulation circuit is a half-bridge circuit and parasitic parameters are taken into account. The GaN device uses a spice model provided by the manufacturer. The device

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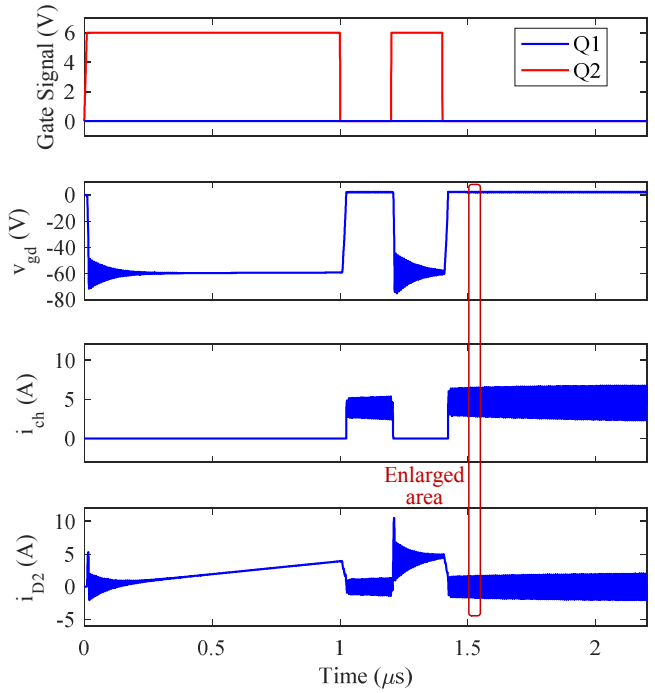

Fig. 23. Simulated waveforms.

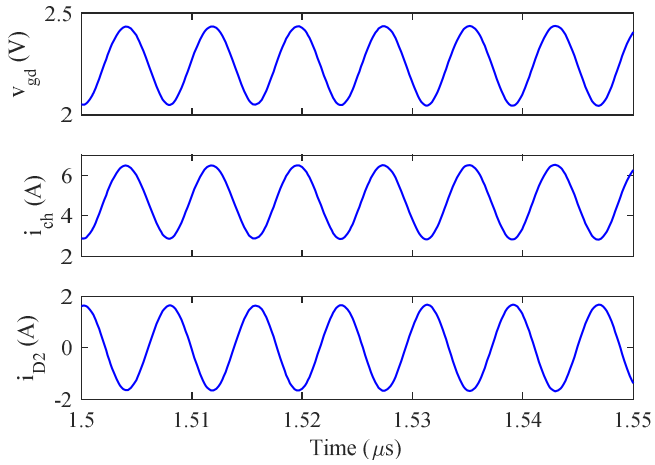

Fig. 24. Enlarged view of the simulated waveforms.

model is modified so that we can observe the channel current and the gate-drain voltage inside the device. The bus voltage is 60 V and the current is about 5 A when Q2 turns off. Other circuit parameters are listed in Table II. Q2 is driven by a double pulse signal. Fig. 23 shows the simulated waveforms. The sustained oscillation is observed after Q2 turns off, which is predicted in Fig. 12.

The waveforms are zoomed in to present more details in Fig. 24. The waveforms of v_{gd} and i_{ch} have the same shape and the same phase, which confirms the relationship between i_{ch} and v_{gd} expressed in (4) and also indicates that Q1 works in the saturation region.

Fig. 25 shows the waveforms when gate signal of Q1 is added. When gate signal of Q1 is high, Q1 operates in the ohmic region instead of saturation region. The channel current is no longer controlled by v_{gd}. The circuit becomes stable because there exists no closed-loop system. The power loop

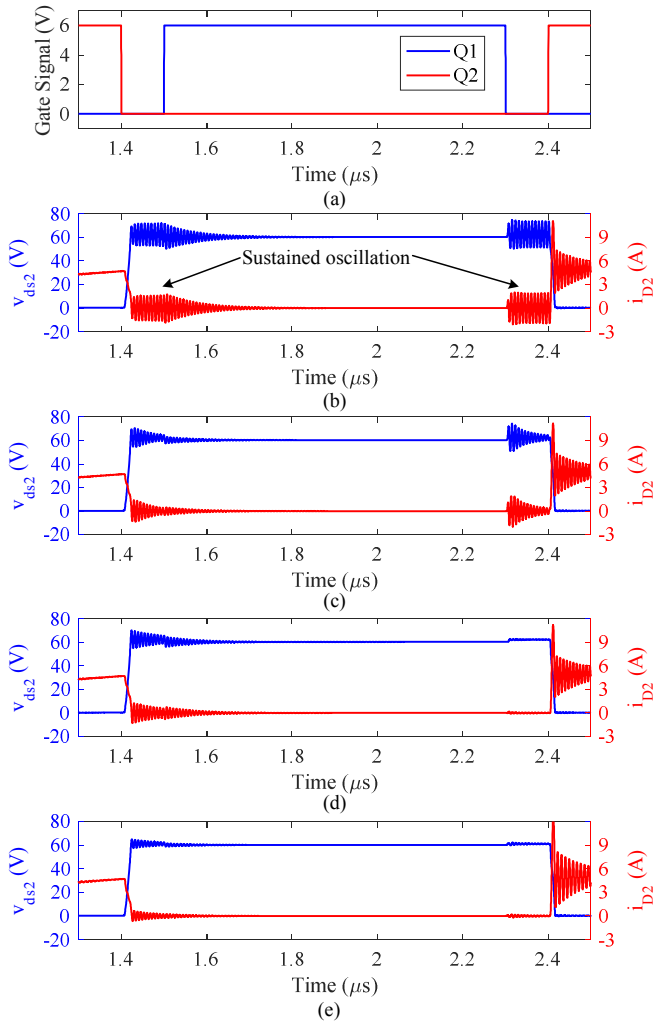

Fig. 25. Simulated waveforms. (a) Gate signals. (b) R_{G1} = 0 Ω and L_S = 0.2 nH. (c) R_{G1} = 0 Ω and L_S = 0.1 nH. (d) R_{G1} = 4.7 Ω and L_S = 0.2 nH. (e) R_{G1} = 0 Ω, L_S = 0.2 nH, and Q1 is paralleled with a diode.

inductance, output capacitance of Q2, and high-frequency power loop resistance form a second-order under-damped circuit, and thus the oscillation damps down. After the Q1's drive signal changes from high to low, Q1 again works in the saturation region. The system is unstable and sustained oscillation occurs again. The oscillation is attenuated when the common-source inductance L_S is reduced to 0.1 nH as shown in Fig. 25(c). In Fig. 25(d), the oscillation damps when the Q1's external gate resistance R_{G1} increases to 4.7 Ω. Fig. 25(e) shows that paralleling a diode with Q1 also has a good effect on suppressing oscillation. The damping ratios calculated by (14) are highlighted in Fig. 13 and Fig. 14. The instability predicted by the damping ratios are consistent with the simulation results.

V. Experiment Results and Discussions

A. Experimental Prototype

Fig. 26 shows a prototype of the half-bridge circuit with an inductive load. The switching devices are GS66508P (650 V enhancement-mode GaN devices) produced by GaN Systems Inc. The internal gate resistance R_{Gint} of GaN device is 1.3 Ω. The driver is LM5114. The current shunt is SSDN-414, which

TABLE III
PROTOTYPE PARAMETERS

Symbol	Description	Value
V_{bus}	Bus voltage	30 - 200 V
I_L	Inductor current	5 A
R_S	Current shunt resistance	0.1 Ω
R_{Gint}	Internal gate resistance of GaN devices	1.3 Ω
V_G	Driver voltage	6 V
R_{G2}	Q2's gate on (off) resistor	20 Ω (10 Ω)

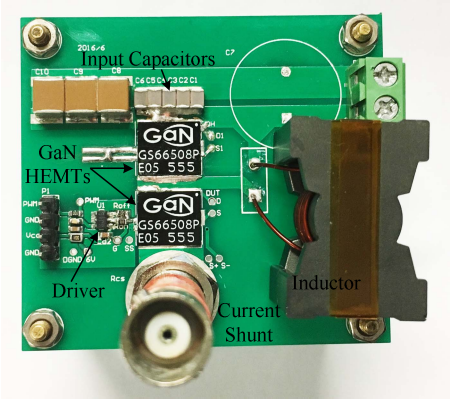

Fig. 26. Experimental prototype of the half-bridge circuit with inductive load.

has a resistance of 0.1Ω and a bandwidth of 2 GHz. The probe is P6139A with a bandwidth of 500 MHz. The parameters of the prototype are shown in Table III. The other parameters are listed in Table II.

B. Experimental Verifications

1) Influence of bus voltage on stability

Fig. 27 shows the measured waveforms under different bus voltages. When the bus voltage is 30 V or 200 V, the oscillation is damped quickly. When the bus voltage is 60 V or 100 V, the oscillation is undamped. The instability is also predicted by the damping ratios highlighted in Fig. 12. When the bus voltage is 60 V or 100 V, the damping ratio is less than zero, thus predicting the system is unstable; when the bus voltage is 30 V or 200 V, the damping ratio is greater than zero, thus predicting the system is stable. The experiment results show a good agreement with the predicted results.

2) Influence of inductor current on stability

Fig. 28 shows the measured waveforms with different inductor current. The inductor current has little influence on the stability due to its small impact on the circuit parameters when it changes from 2 A to 15 A. In addition, the switching speed varies with inductor current, which indicates that the switching speed has no effect on such instability to some extent.

3) Oscillation frequency

The predicted oscillation frequency is calculated using (15). The oscillation frequency varies with V_{bus} since the output capacitance C_{oss2} is a function of the drain-source voltage. Fig. 29 shows that the measured results agree well with the predicted results. In addition, the resonant frequency of the power loop impedance Z_{loop}, namely $1/(2\pi((L_D+L_S)C_{oss2})^{0.5})$, is close to the predicted and experimental results, which can be used to easily estimate the oscillation frequency.

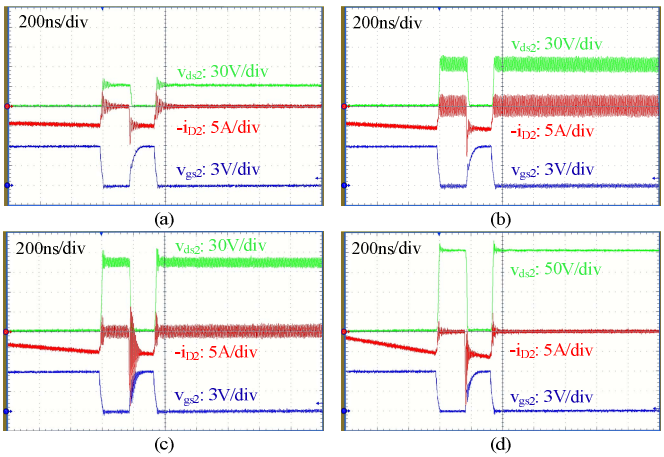

Fig. 27. Measured waveforms under different bus voltages where R_{G1} = 0 Ω. (a) V_{bus} = 30 V. (b) V_{bus} = 60 V. (c) V_{bus} = 100 V. (d) V_{bus} = 200 V.

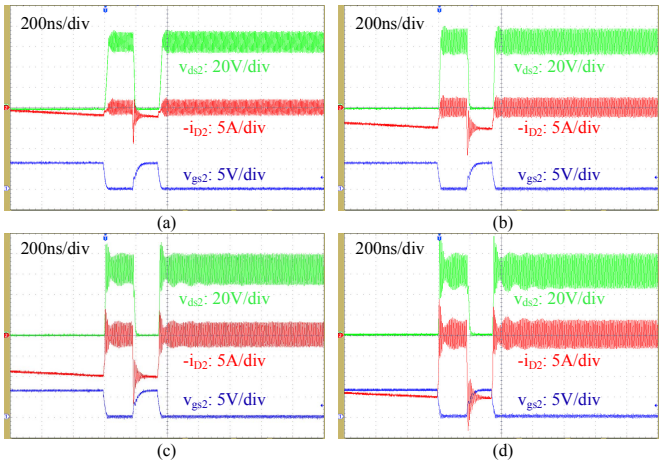

Fig. 28. Measured waveforms under different inductor currents. (a) I_L = 2 A. (b) I_L = 5 A. (c) I_L = 10 A. (d) I_L = 15 A.

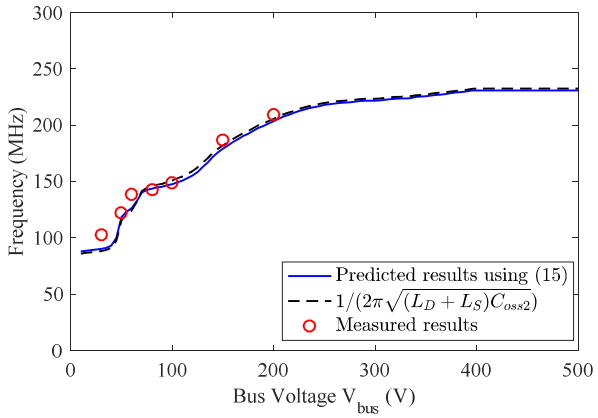

Fig. 29. Oscillation frequency.

C. Guidelines to Suppress Oscillation

1) Reducing common-source inductance to suppress oscillation

Two experiments with different L_S are performed. The GaN device GS66508P has a source sense pin connected with the source inside the package in order to reduce L_S. At the first experiment, the driver ground of inactive device is connected to the source sense pin and the resulted L_S is about 0.2 nH. The

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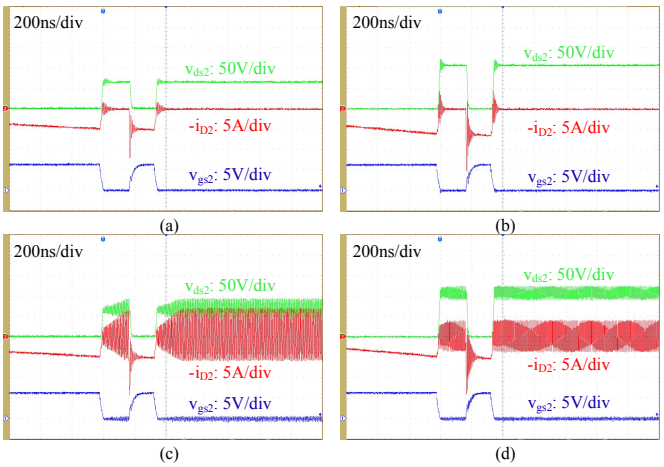


Fig. 30. Measured waveforms under different common-source inductance where R_{G1} = 1 Ω. (a) L_S = 0.2 nH at V_{bus} = 60 V. (b) L_S = 0.2 nH at V_{bus} = 100 V. (c) L_S = 0.5 nH at V_{bus} = 60 V. (d) L_S = 0.5 nH at V_{bus} = 100 V.

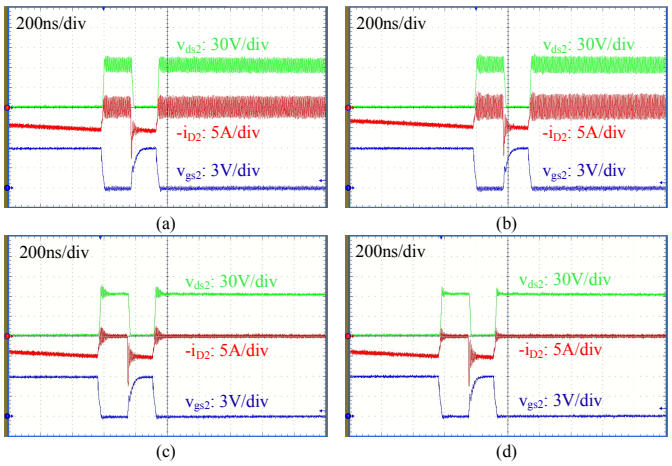


Fig. 31. Measured waveforms under different external gate resistors at V_{bus} = 60 V. (a) R_{G1} = 0 Ω. (b) R_{G1} = 0.5 Ω. (c) R_{G1} = 1 Ω. (d) R_{G1} = 4.7 Ω.

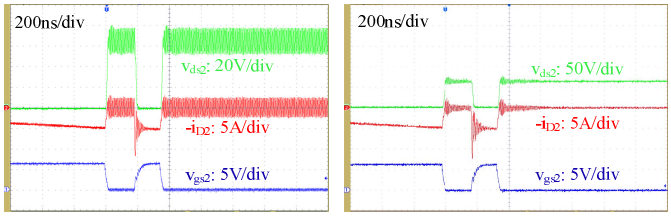


Fig. 32. Measured waveforms. (a) Without diode. (b) A SiC diode is paralleled across the drain and source of the inactive switch.

circuit is stable when bus voltage is 60 V or 100 V by increasing R_{G1} to 1 Ω as shown in Fig. 30(a) and (b). At the second experiment, the driver ground is disconnected from the source sense pin and then connected to the source. L_S is thus increased to about 0.5 nH. It is a reasonable approach to connect the driver ground to the source because some GaN devices do not have the source sense pin. Under the experimental conditions, sustained oscillations are observed as shown in Fig. 30(c) and (d). The experimental results show that reducing L_S can effectively suppress the oscillation.

2) *Increasing gate resistance to suppress oscillation*

Fig. 31 shows the measured waveforms under different external gate resistors R_{G1} at V_{bus} = 60 V. When R_{G1} is very small, such as 0 Ω and 0.5 Ω, the oscillation is undamped. When R_{G1} =1 Ω, the oscillation is damped slowly. When R_{G1} is increased to 4.7 Ω, the oscillation is damped quickly. The experimental results show that increasing the gate resistance can significantly suppress the oscillation.

The instability is also predicted by the damping ratios highlighted in Fig. 14. The damping ratio increases with the increase of R_{G1}. When R_{G1} is 0 Ω and 0.5 Ω, the damping ratio is less than zero, thus predicting the system is unstable. When R_{G1} is 1 Ω and 4.7 Ω, the damping ratio is greater than zero, thus predicting the system is unstable. Because the damping ratio at R_{G1} = 1 Ω is smaller than that at R_{G1} = 4.7 Ω, the oscillation decays more slowly at R_{G1} = 1 Ω. The predicted results obtained from the proposed model are consistent with the experiment results.

3) *Paralleling a diode across the drain and source of the inactive switch to suppress oscillation*

A 600 V SiC diode [28] is paralleled across the drain and source of the inactive switch to suppress the oscillation. The junction capacitance of the SiC diode leads to increase in C_{ds}, which has little effect on the stability because the increased C_{ds} has little effect on the damping ratio, as shown in Fig. 21. As a comparison, the circuit works in an unstable state without the diode and sustained oscillation is observed in Fig. 32(a). After the diode is paralleled, the sustained oscillation is suppressed as shown in Fig. 32(b). However, the oscillation does not decay quickly at the beginning due to the presence of the diode's parasitic inductance. Efforts should be made to reduce the parasitic inductance to achieve better suppression effect.

VI. Conclusion

Theoretical treatment of an instability problem observed in GaN-based half-bridge circuits has been presented in this paper. The observed problem is found to be related to the unique reverse conduction characteristics of GaN devices and parasitic parameters. A model has been proposed to determine the stability of the system. Further, the effect of various parameters on stability has been investigated. Finally, the proposed model has been validated by simulation and experiment results. Based on the analyses in this paper, the guidelines to suppress the oscillation have been presented. It has been shown that the oscillations in GaN-based half-bridge circuits can be significantly reduced by minimizing the common-source inductance, by increasing the gate resistance of inactive switch, and by connecting a diode in parallel with the inactive switch. It has been noted that reducing the switching speed of the active device doesn't help to reduce the risk of sustained oscillation.

Appendix

The coefficients in (9) and (12) are as follows:

$$a_4 = C_{gs}C_{oss2}(L_DL_G + L_DL_S + L_GL_S)$$

$$a_3 = C_{gs}C_{oss2}(L_DR_G + L_SR_G + L_GR_{loop} + L_SR_{loop})$$

$$a_2 = C_{gs}L_G + C_{oss2}L_D + C_{gs}L_S + C_{gs}C_{oss2}R_GR_{loop}$$

$$a_1 = C_{gs}R_G + C_{oss2}R_{loop}$$

$$a_0 = 1$$
$$b_4 = C_{oss2}(C_{ds}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{gs})(L_D L_G + L_D L_S + L_G L_S)$$
$$b_3 = C_{oss2}(C_{ds}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{gs})(L_D R_G + L_S R_G + L_G R_{loop} + L_S R_{loop})$$
$$b_2 = (C_{ds}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{gs})(L_G + L_S + C_{oss2}R_G R_{loop}) + C_{oss2}(C_{ds}(L_D + L_S) + C_{gd}(L_D + L_G) + C_{gs}(L_S + L_G))$$
$$b_1 = (C_{ds}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{gs})R_G + (C_{gd} + C_{gs})C_{oss2}R_G + (C_{ds} + C_{gd})C_{oss2}R_{loop}$$
$$b_0 = C_{ds} + C_{gd} + C_{oss2}$$
$$c_5 = b_4$$
$$c_4 = g_m a_4 + b_3$$
$$c_3 = g_m a_3 + b_2$$
$$c_2 = g_m a_2 + b_1$$
$$c_1 = g_m a_1 + b_0$$
$$c_0 = g_m a_0$$

REFERENCES

[1] F. C. Lee and Q. Li, "High-Frequency Integrated Point-of-Load Converters: Overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127-4136, Sep. 2013.

[2] D. Reusch and J. Strydom, "Evaluation of Gallium Nitride Transistors in High Frequency Resonant and Soft-Switching DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151-5158, Sep. 2015.

[3] A. Lidow, J. Strydom, M. d. Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion*, 2nd ed. Efficient Power Conversion Corporation: Wiley Press, 2015.

[4] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert and B. J. Blalock, "Investigation of Gallium Nitride Devices in High-Frequency LLC Resonant Converters," *IEEE Trans. on Power Electron.*, vol. 32, no. 1, pp. 571-583, Jan. 2017.

[5] W. Liang, L. Raymond, L. Gu, and J. Rivas, "27.12MHz GaN resonant power converter with PCB embedded resonant air core inductors and capacitors," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 4251-4256.

[6] A. Hariya, K. Matsuura, H. Yanagi, S. Tomioka, Y. Ishizuka, and T. Ninomiya, "Five-Megahertz PWM-Controlled Current-Mode Resonant DC-DC Step-Down Converter Using GaN-HEMTs," *IEEE Trans. Ind. Applicat.,* vol. 51, no. 4, pp. 3263-3272, July-Aug. 2015.

[7] F. Gamand, M. D. Li, and C. Gaquiere, "A 10-MHz GaN HEMT DC/DC Boost Converter for Power Amplifier Applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 59, no. 11, pp. 776-779, Nov. 2012.

[8] A. Hariya, T. Koga, K. Matsuura, H. Yanagi, S. Tomioka, Y. Ishizuka*, et al.*, "Circuit Design Techniques for Reducing the Effects of Magnetic Flux on GaN-HEMTs in 5 MHz - 100 W High Power-Density LLC Resonant DC-DC Converters," *IEEE Trans. Power Electron.,* to be published.

[9] Y. Zhang, M. Rodriguez, and D. Maksimovic, "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers," *IEEE Trans. Power Electron.,* vol. 31, no. 11, pp. 7926-7942, Nov. 2016.

[10] X. Huang, F. C. Lee, Q. Li, and W. Du, "High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor," *IEEE Trans. Power Electron.,* vol. 31, no. 6, pp. 4343-4352, Jun. 2016.

[11] W. Zhang, X. Huang, F. C. Lee, and Q. Li, "Gate drive design considerations for high voltage cascode GaN HEMT," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 1484-1489.

[12] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Cross conduction analysis for enhancement-mode 650-V GaN HFETs in a phase-leg topology," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, 2015, pp. 98-103.

[13] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in Half-Bridge Circuits Switched With Wide Band-Gap Transistors," *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2380-2392, May 2014.

[14] X. Huang, W. Du, F. C. Lee, Q. Li, and W. Zhang, "Avoiding Divergent Oscillation of a Cascode GaN Device Under High-Current Turn-Off Condition," *IEEE Trans. Power Electron.,* vol. 32, no. 1, pp. 593-601, Jan. 2017.

[15] Analog Devices Inc. (2012). *Design Fundamentals of Implementing an Isolated Half-Bridge Gate Driver*. [Online]. Available: www.analog.com

[16] T. Yanagi, H. Otake, and K. Nakahara, "The mechanism of parasitic oscillation in a half bridge circuit including wide band-gap semiconductor devices," in *Proc. IMFEDK*, 2014, pp. 1-2.

[17] J. Wang and H. Shu-Hung Chung, "Impact of Parasitic Elements on the Spurious Triggering Pulse in Synchronous Buck Converter," *IEEE Trans. Power Electron.,* vol. 29, no. 12, pp. 6672-6685, Dec. 2014.

[18] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration," *IEEE Trans. Power Electron.,* vol. 29, no. 4, pp. 1986-1997, Apr. 2014.

[19] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability Considerations for Silicon Carbide Field-Effect Transistors," *IEEE Trans. Power Electron.,* vol. 28, no. 10, pp. 4453-4459, Oct. 2013.

[20] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 3, pp. 707-719, Sep. 2016.

[21] GaN Systems Inc. (2015). *GS66508P*. [Online]. Available: www.gansystems.com

[22] G. Gonzalez, "Theory of Oscillators," in *Foundations of oscillator circuit design*, 1st ed USA: Artech House Inc., 2007, pp. 1-51.

[23] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback control of dynamic systems*, 6th ed. USA: Pearson Education, 2009.

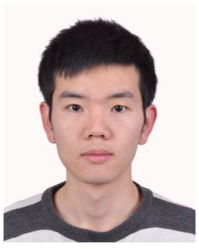
[24] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DC–DC Converter," *IEEE Trans. Power Electron.,* vol. 32, no. 6, pp. 4728-4740, Jun. 2017.

[25] D. Reusch and J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter," *IEEE Trans. Power Electron.,* vol. 29, no. 4, pp. 2008-2015, Apr. 2014.

[26] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An Analytical Switching Process Model of Low-Voltage eGaN HEMTs for Loss Calculation," *IEEE Trans. Power Electron.,* vol. 31, no. 1, pp. 635-647, Jan. 2016.

[27] H. Di and B. Sarlioglu, "Deadtime Effect on GaN-Based Synchronous Boost Converter and Analytical Model for Optimal Deadtime Selection," *IEEE Trans. Power Electron.,* vol. 31, no. 1, pp. 601-612, Jan. 2016.

[28] Cree Inc. (2015). *C3D10060A*. [Online]. Available: www.wolfspeed.com/



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Dr. Jain has supervised and guided almost 100 graduate students, postdoctoral fellows, and power electronics engineers who are well placed in industry and academia. He has published over 500 papers and holds 100 patents (granted and pending). Among his many awards and honors are the Queen's Prize for Excellence in Research, the IEEE William Newell Power Electronics Award, the Engineering Medal of the Professional Engineers of Ontario, the IEEE IAS Distinguished Lecturer, Fellow of the IEEE, Fellow of the Royal Society of Canada, Fellow of the Engineering Institute of Canada, and Fellow of the Canadian Academy of Engineering.