Comparison of Inverter Topologies Suited for Integrated Modular Motor Drive Applications

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***Abstract*— In this paper, various inverter topologies are compared for integrated modular motor drive (IMMD) applications. Two-level voltage source inverter (2L-VSI), three-level voltage source inverter (3L-VSI) and series/parallel combinations of these topologies with system level modularity are compared in terms of voltage and current harmonic spectrum, passive component sizes and motor drive efficiency. New generation wide band-gap GaN power semiconductor devices are utilized in modular topologies and they are compared with a conventional IGBT motor drive. The effect of phase-shifting between the PWM carrier signals of parallel connected modules and its contribution to size reduction is investigated. IMMD structure has proven to have a superior efficiency compared to conventional motor drives, thanks to the utilization of GaNs. It has been shown that over 98% motor drive efficiency can be achieved for 8kW IMMD by using a newly proposed topology where 2L-VSI converters are connected both in series and parallel on the DC link.**

Keywords—motor drive efficiency, voltage source inverter, integrated motor drive, modular motor drive topologies, gallium nitride

I. INTRODUCTION

Electric motor drives use over 45% of the overall electricity consumption, nowadays makes energy conversion efficiency quite important. Many of these electric motors are driven by variable frequency adjustable speed drives (ASDs) due to the need for precise speed or position control. Power density is a critical factor in designing motor drives in several applications such as electric traction and aerospace.

Conventional ASDs are composed of motor drive inverter power electronics, passive components, cooling structures, control/communication interfaces and sensors for speed control. In integrated motor drives, the aforementioned drive components are integrated on the electric motor to reduce the system size, eliminate the connection cables for better EMI/EMC performance and eliminate the need for separate enclosures [1]. A more compact solution is dividing the system in modules which is called the Integrated Modular Motor Drive (IMMD) concept. A dedicated drive is integrated onto each motor segment in IMMDs. The advantages of using such an arrangement can be listed as: reduction of voltage and current stress on power semiconductor devices and motor windings, improvement of fault tolerance capability, distribution of heat sources to achieve an easier thermal management and cost reduction in manufacturing, maintenance and repair [2].

Three-phase voltage source inverter (VSI) topologies for different applications such as motor drive or grid-connected renewable energy converters have been proposed, evaluated, tested and reported thoroughly. Most of these studies include two-level VSI (2L-VSI), three-level VSI (3L-VSI), cascaded H-bridge (CHB) and modular multilevel converter (M2LC) for higher voltage ratings. In IMMD applications, with the introduction of modularity, the variety of available topologies suitable for motor drive increases significantly. Different poles of the modular stator can be connected to different and dedicated drive inverters in IMMDs which brings design flexibility in terms of motor drive topology [3].

Significant size reduction should be achieved to fit all the drive components in a small volume in order to integrate the drive to the motor [1]. The largest components in an average power converter are the passive components and the heatsinks [4], therefore the size reduction challenge can be addressed by minimization of the DC link capacitor or heat sink volume in an integrated drive. Considering the design flexibility, investigation of the most suitable motor drive topology in terms of DC link ripples, AC side harmonics and efficiency is required.

There have been several studies in search for the most suitable motor drive arrangement for an IMMD design. The first integrated regenerative motor drive was proposed in 2002 for industry applications which was based on a matrix converter topology [5]. Another prototype based on matrix converters was built for a 30kW induction motor [6]. The aim of these studies was to eliminate the need for filtering elements. In [7], converter topologies on the rectifier front-end are evaluated for integrated motor drives, keeping the inverter side the same. An IMMD design with soft magnetic composite (SMC) core material for a five-phase machine is developed in [8], where each phase leg is composed of independent IGBT based half-bridges. A similar approach is used in [9] for a six-phase machine, grouping each three-phase with a common neutral point. This was the first IMMD prototype with dedicated controllers on each module to further increase the reliability and fault tolerance. A 50kW, 6-phase integrated fault tolerant permanent magnet motor drive is proposed in [10], where each phase of the drive is composed of a full-bridge converter, instead of half bridges. GaN FETs were firstly introduced into the IMMD designs in 2013 to reduce the DC link capacitor size as well as eliminate the heat sink by operating at high switching frequencies [11]. In this work, series connection of inverter modules is proposed to match the low voltage rating of GaNs to higher DC link voltages. Evaluation of the aforementioned conventional inverter topologies (2L-VSI, 3L-VSI and CHB) has been investigated by the authors of [2] and [3] for IMMDs, and compared with their proposed topology having series connected 2L-VSI inverters in terms of number of components, flexibility in voltage levels, modularity and fault tolerance [12]. Gate signal interleaving has been applied to decrease the capacitor size [12]. Additional medium-voltage inverter topologies are

mentioned in [3] where separate DC links are used for each inverter. Moreover, the series connected topology is further extended with replacing the 2L-VSI with 3L-VSI either in Neutral Point Clamped (NPC) or Flying Capacitor (FC) configurations [3]. Similar evaluation parameters are considered in these studies; however, these evaluations are generally conceptual rather than providing numerical comparisons.

In this paper, a detailed analysis is presented for the evaluation of selected inverter topologies suited for IMMD applications. A conventional 2L-VSI IGBT based inverter is considered in addition to the 2L-VSI and 3L-VSI GaN based IMMD inverters and their series and/or parallel connected derivations. Gate signal interleaving is applied in parallel connected converters to reduce the DC link capacitor size. Motor terminal voltage and line current, DC link voltage and capacitor current spectral analyses are performed using MATLAB/Simulink simulations. Furthermore, power semiconductor losses are analyzed for varying switching frequencies using numerical integration method applied to device waveforms obtained from MATLAB/Simulink simulations.

II. System Description

A. Integrated Modular Motor Drives

Several different ways of integration methods are proposed in the literature as listed in [1]. IMMD structure considered in this paper is called stator iron mount integration where each stator pole piece has its own drive module that consists of power electronics, and control electronics as shown in Fig. 1 [9]. In this study, an IMMD having a nominal output power of 8 kW is considered, the block diagram of which can be seen in Fig. 2. Depending on the number of machine poles, the topology and configuration of the pole-drive modules can be arranged. The rated values of the system are shown in Table 1.

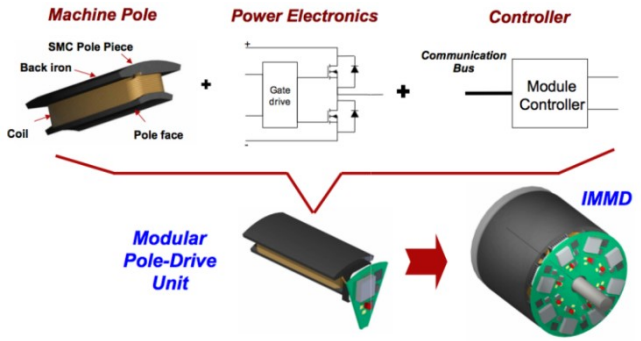


Fig. 1. An IMMD illustration with stator iron mount integration [9]

TABLE I. Specifications of the Proposed System

Parameter	Value
Drive total output power, P_{out}	8 kW
DC link voltage, V_{dc}	540 V
Number of phases in each module, m	3
Power factor, pf	0.9
Fundamental output frequency, f_0	50 Hz

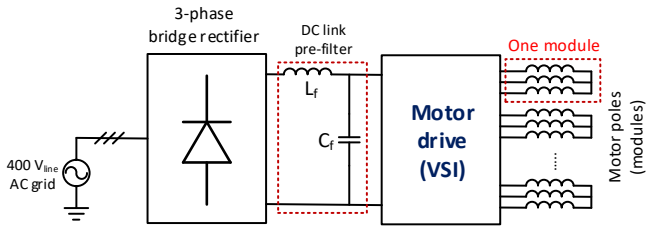


Fig. 2. Block diagram of the IMMD

B. Classification of Topologies

Five different IMMD topologies, which are shown in Fig. 3, are compared and evaluated. The topology of 2L-2S-VSI is the same as the one proposed in [12]. The topologies, 2L-2S2P-VSI and 3L-2P-VSI, are derived from the series connected one. These are novel topologies presented in this study where both series and parallel connection are applied simultaneously. For better visualization, the connection diagram of 2L-2S2P-VSI topology is shown in Fig. 4. The 3-level topologies are in diode clamped (neutral point clamped) multilevel configuration.

Sinusoidal Pulse Width Modulation (SPWM) technique is applied for all topologies. Level shifted SPWM is utilized for the modules having three-level configuration. Additionally, gate signal interleaving is applied for the topologies where parallel modules are fed from the same module capacitor. In fact, the same technique can be applied to series connected modules; however, while decreasing the ripple voltage on the overall DC input, it does not affect the percent ripple on the individual module DC buses. The aim of restricting the percent ripple on the DC link is to make sure that the AC side voltage waveform quality is not affected by the DC link ripples, therefore it is meaningless to decrease the overall DC link voltage ripple. Consequently, interleaving has no net effect on voltage ripple for the series connection modules.

C. Power Semiconductor Devices

In this study, a conventional motor drive topology (2L-VSI) with IGBTs and anti-parallel diodes is included in the comparison. For the other topologies, a type of series connection is used purposefully, either directly connecting 2-level modules in series, or using 3-level inverters, to make the drive having an input of 540 VDC compatible with commercially available GaN FETs with the highest voltage rating. Two different GaNs having 650 V blocking voltage rating are used from GaN Systems with suitable current ratings depending on whether there is a parallel connection or not. Finally, Silicon Carbide (SiC) Schottky diode from Wolfspeed is selected for the clamping diode of the 3-level topologies. All selected devices and their parameters are presented in Table 2 [13], [14], [15]. The switching frequency for 2L-VSI is limited to 25 kHz in the simulations and parameter evaluation due to the practical limitations of IGBTs, while the switching frequency applied to the topologies with GaN devices can go up to 100 kHz.

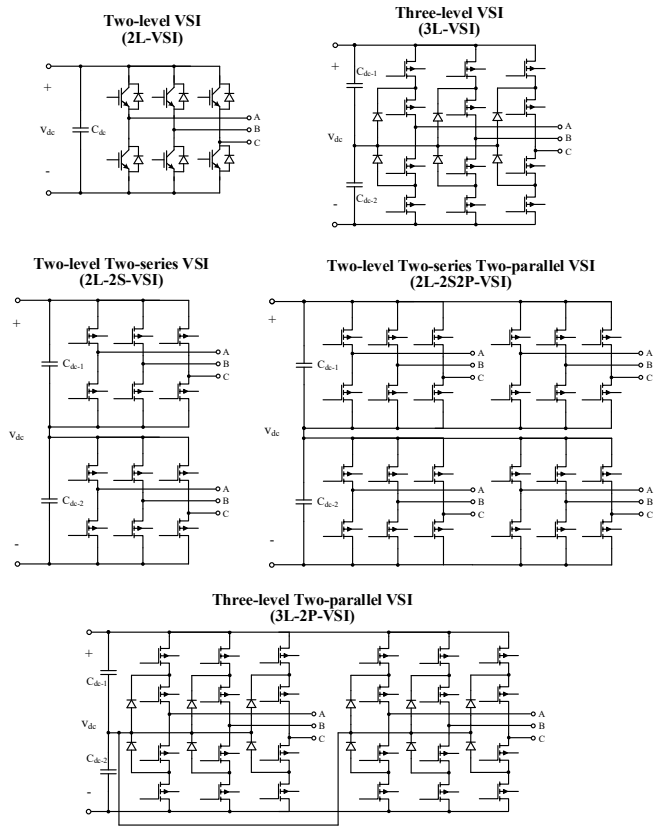


Fig. 3. Circuit digram of the five different motor drive topologies

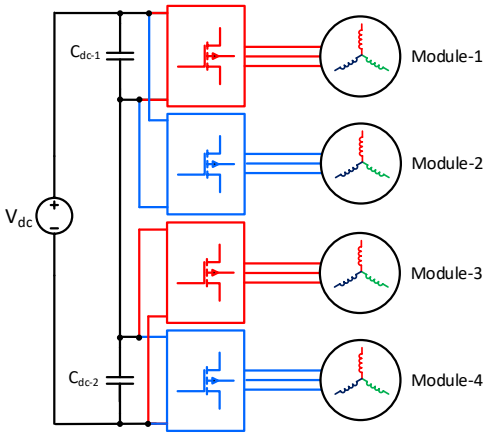


Fig. 4. Connection diagram of the 2L-2S2P-VSI topology

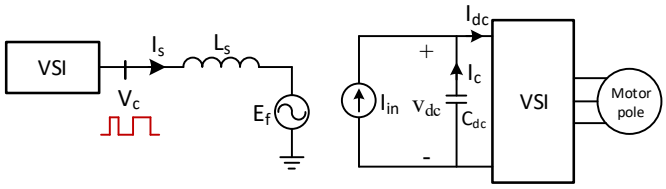
TABLE II. SELECTED DEVICES AND THEIR PARAMETERS [13], [14], [15]

Device	FF50R12RT4	GS66508B	GS66516B	C5D50065D
Type	IGBT	GaN	GaN	SiC Diode
Voltage	1200 V	650 V	650 V	650 V
Current	50 A	30 A	60 A	50 A
$V_{ce,sat}$	2,15 V	-	-	-
$R_{ds,on}$	-	50 mΩ	25 mΩ	-
V_f (diode)	1.65 V	-	-	2.0 V

III. EVALUATED PARAMETERS

A. AC Side Parameters

A permanent magnet synchronous motor (PMSM) with concentrated windings is designed specifically for this IMMD application. The number of slots is kept constant and four stator three-phase pole windings are either connected in series, or connected to the drive modules separately, depending on the number of modules existing in the corresponding topology. The parameters of the previously designed PMSM are listed in Table 3. Single phase equivalent circuit of one module of the motor is shown in Fig. 5(a). Induced voltage (E_f) and phase inductance (L_s) are obtained from the simulations applied to the designed motor. The corresponding inverter voltage (V_c) and load angle (δ) are calculated in the simulations. Modulation depth (m_a) of each inverter is kept constant at 0.9 at rated conditions for all topologies. Quality of the voltage and current waveforms are evaluated on the AC side by their harmonic spectrum and total harmonic distortion values for both voltage (THD_v) and current (THD_i), which are calculated as in (1) and (2).



(a) AC side model (b) DC link model

Fig. 5. Models used in the evaluation

TABLE III. PARAMETERS OF THE PRE-DESIGNED PMSM

Parameter	Value
Stator outer diameter, D_{os}	270 mm
Stator inner diameter, D_{is}	180 mm
Axial length, L_a	135 mm
Number of stator slots, Q_s	24
Number of rotor poles, p	20
Inductance of one stator pole winding, L_s	13.5 mH
Induced voltage of one stator pole winding, E_f	77 V_{rms}
Line current of one stator pole winding, I_s	8.7 A_{rms}

$$THD_v = 100 \text{ x} \sqrt{\frac{\sum_{n=2}^{\infty} {V_n}^2}{{V_1}^2}} \quad (1)$$

$$THD_i = 100 \text{ x} \sqrt{\frac{\sum_{n=2}^{\infty} {I_n}^2}{{I_1}^2}} \quad (2)$$

B. DC Link Parameters

The general model of the DC link of one module is shown in Fig. 5(b). It is assumed that the DC bus pre-filter sufficiently suppresses any low frequency ripples or disturbances from the grid side. The DC input is represented by an ideal pure DC current source (I_{in}), magnitude of which depends on the amount of motor loading. Each VSI module draws a current (I_{dc}) which consists of a pure DC component and a high frequency ripple component. This ripple current is supplied by the module capacitor (I_c). The ripple current (I_c) is directly related to the phase current of the corresponding stator module (I_s) and it is independent of the switching frequency (f_{sw}) by nature, as expressed in [16].

Ripple current handling capability of the capacitors is a critical design parameter directly affecting the selected

capacitor size, hence the motor drive power density. The only way to reduce the RMS value of the ripple current of a topology for a given output power is to utilize interleaving technique. The voltage ripple ($V_{dc\text{-}r}$) is also critical and should be restricted for each module as it may impose additional harmonics to the inverter output voltage. The constraint on the voltage ripple should be limited to 1% of the corresponding module DC link capacitor average voltage. As shown in the proportionality relation in (3), this ripple voltage is directly related to capacitor ripple current (I_c), capacitance (C_{dc}) and the switching frequency. Therefore, for a given ripple current, the ripple voltage constraint can be satisfied by either increasing f_{sw} or increasing C_{dc}. As a conclusion, smaller DC bus capacitors can be designed with only high frequency operation to meet the size restrictions.

$$I_c \propto V_{dc-r}\ f_{sw}\ C_{dc} \tag{3}$$

Two different types of capacitors are utilized in the DC bus; electrolytic capacitors and metal film capacitors [16]. Electrolytic capacitors have higher capacitance per volume; however, their lifetime is limited and dependent to operating temperature. Therefore, film capacitors are more suitable for integrated motor drives where electronic components are subjected to higher temperatures than conventional drives. Film capacitors are known for their high current handling capability, but their capacitance per volume rating is low which makes capacitance reduction more critical for an IMMD application. That being said, the spectral analysis of DC link voltage and currents, RMS current requirement and capacitance requirement in terms of switching frequency will be included in this comparison.

C. *Efficiency*

Efficiency is one of the most critical parameters in motor drive applications, especially for heavy duty industrial loads. In addition to this, cooling method and size of the heat sink directly depend on the motor drive efficiency. Remembering the fact that heat sink is one of the largest components in the motor drive, minimization of this component is particularly important. Optimal selection of switching frequency is required for such designs due to its trade-off between the DC link capacitor size and heat sink size due to the switching losses. Although GaNs are known for their superior switching performance, the inverter topology still has great impact on the resultant power semiconductor devices losses, and hence efficiency.

The device losses are analyzed using numerical integration method applied to the time-domain voltage and current waveforms gathered from the motor drive simulations. A sample device waveform is shown in Fig. 6 to visualize the applied method for a full conduction cycle of one of the inverter switches. First, all loss-related data from the device datasheets are converted to curve fitted functions in MATLAB which are dependent to device currents. During the integration process, the conduction, turn-on or turn-off losses are detected at each time instant. At each instant, the corresponding energy is calculated using the instantaneous current information, the related datasheet parameter value and simulation time step (Δt). From (4) to (8), the equations used in determining the conduction energy for IGBT, conduction (both forward and reverse) energy for GaN, conduction energy for diodes, switching energy (turn-on, turn-off or C_{oss}) for GaN and IGBT, and reverse recovery energy for diode are shown, respectively. At the end of the fundamental cycle, cumulative energy components are converted to power losses by multiplying with the fundamental frequency (f_0) using (9).

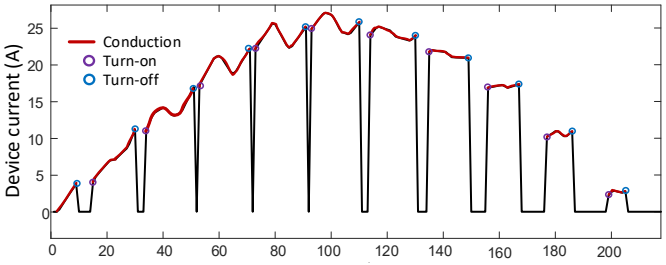


Fig. 6. Visualization of the device loss calculation method

$$E_{con}(t) = V_{ce-sat}[I(t)] \times I[t]\ \times \Delta t \qquad (IGBT) \tag{4}$$

$$E_{con}(t) = R_{ds-on}[I(t)] \times I[t]^2 \times \Delta t \qquad (GaN) \tag{5}$$

$$E_{con}(t) = V_f[I(t)] \times I[t]\ \times \Delta t \qquad (Diode) \tag{6}$$

$$E_{sw}(t) = (E_{sw}[I(t)]) \qquad (IGBT\,/\,GaN) \tag{7}$$

$$E_{rr}(t) = (E_{rr}[I(t)]) \qquad (Diode) \tag{8}$$

$$P_{loss} = f_0\ \times \int E_{loss}\, dt \tag{9}$$

D. *Other Considerations*

Another crucial factor regarding the motor drive topology is the fault tolerance capability, which is also a feature separating IMMDs from conventional drives. Obviously, a single 2L-VSI or 3L-VSI do not have any fault tolerance capability, neither on the motor side, nor on the drive side. Although the motor poles are separately connected to distinct modules in series connection, it does not mean a fully fault tolerant operation is obtained. However, assuming the DC link input is unchanged, the motor may still be able to operate with reduced power rating even if one of the modules fail, given that the voltage ratings of the remaining modules can withstand the DC link voltage. However, this is practical only for high number of series connected modules as the ratio of the module voltage to the total DC link input voltage gets lower. Fault tolerance is achievable in real terms for both motor windings and drive inverters when modules are connected in parallel; i.e., if one of the modules fails, the operation can continue with reduced power output.

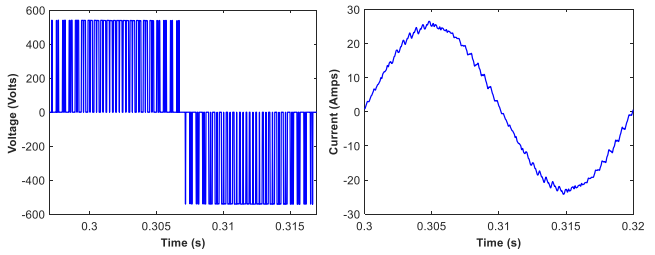
Series and parallel connection also affect the voltage and current ratings of the devices which are also important parameters due to two factors: size and cost. Height of a capacitor tends to get smaller as its voltage rating reduces. Therefore, having more series connection will result in shorter capacitor heights. However, the required number of capacitors will increase with increasing number of series connection. Moreover, using n devices with 1/n current rating instead of a single device with a full rating will always result in higher cost. This in fact is the major factor that limits the maximum number of modules used in the motor drive system.

IV. Topology Comparison

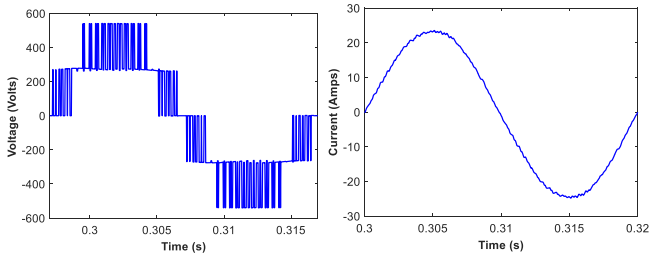
The topologies are compared depending on their AC side, DC bus and efficiency characteristics, as they are the key components of a drive circuit.

A. AC side characteristics

Voltage and current waveforms for 2L-VSI and 3L-VSI topologies are shown in Fig. 7. Waveforms for series or parallel connection are not included since only the magnitudes are varied. Moreover, the voltage and current spectra of each topology are shown in Fig. 8. Voltage THD is not affected by the switching frequency, therefore it is presented as a table for different topologies in Table 4. Current THD values obtained for single switching frequency (10 kHz for 2L-VSI, 50kHz for other topologies) are shown in Table 4, as well.

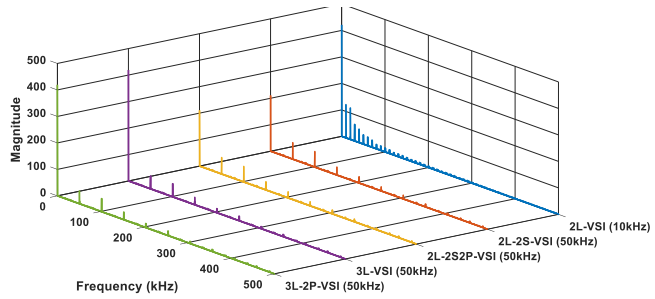


(a) 2L-VSI line-to-line voltage (b) 2L-VSI line current

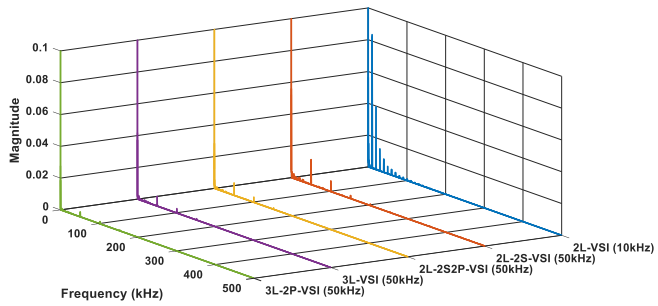


(c) 3L-VSI line-to-line voltage (d) 3L-VSI line current

Fig. 7. AC side waveforms for 2L-VSI and 3L-VSI (fsw = 2 kHz)



(a) Spectrum of phase voltage



(b) Spectrum of line current

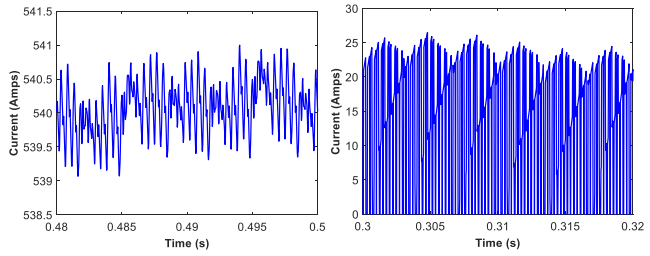
Fig. 8. AC side spectra (fsw = 10 kHz for IGBT, fsw = 50 kHz for GaN)

TABLE IV
AC Output Voltage THD and DC Link Capacitor RMS Current

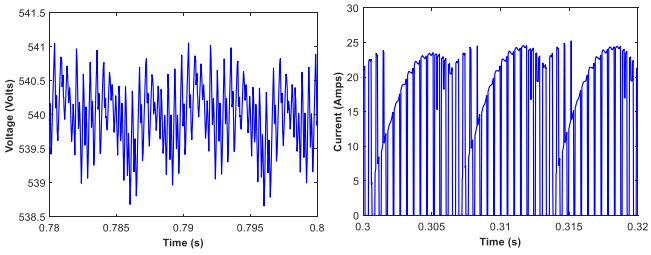
Topology	THD_v (%)	THD_i (%)	$I_{c\text{-}rms}$ (A)
2L-VSI	79.67	0.96	9.65
2L-2S-VSI	79.57	0.74	9.61
2L-2S2P-VSI	79.52	0.74	7.28
3L-VSI	39.60	0.43	8.49
3L-2P-VSI	39.58	0.43	4.48

B. DC Bus Characteristics

DC link voltage and current waveforms for 2L-VSI and 3L-VSI and effect of interleaving for parallel connected modules are shown in Fig. 9. Moreover, the voltage and current spectra of each topology are shown in Fig. 10. The variation of required capacitance with switching frequency can be seen in Fig. 11. The DC link capacitor RMS currents are also listed in Table 4 for all topologies.

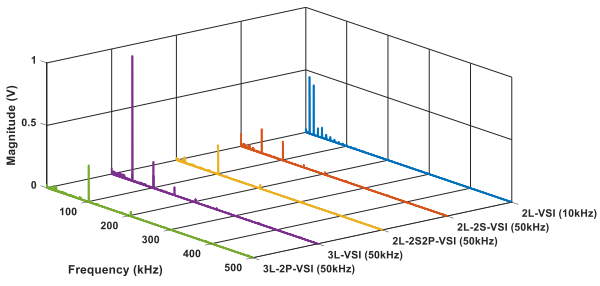


(a) 2L-VSI DC link voltage (b) 2L-VSI DC link current

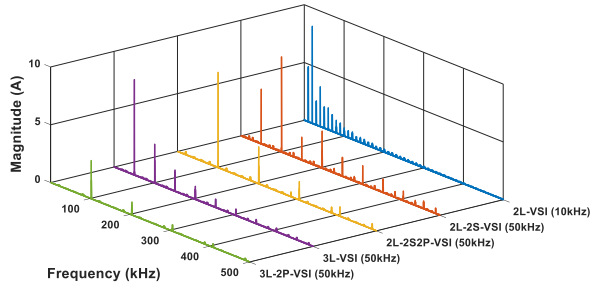


(c) 3L-VSI DC link voltage (d) 3L-VSI DC link current

Fig. 9. DC link waveforms for 2L-VSI and 3L-VSI (fsw = 2 kHz)



(a) Spectrum of DC link voltage



(b) Spectrum of DC link current

Fig. 10. DC side spectra (fsw = 10 kHz for IGBT, fsw = 50 kHz for GaN)

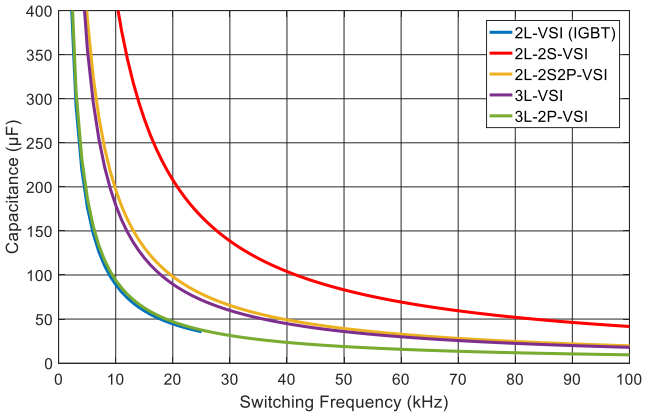


Fig. 11. Variation of required total capacitance with switching frequency

C. *Efficiency Evaluation*

Variation of motor drive efficiencies with switching frequency for the topologies at full-load are shown in Fig. 12. Since IGBT is used for conventional 2L-VSI motor drive topology, the applied switching frequency is limited to 25 kHz. Distribution of loss components for all topologies are shown in Fig 13. For selected switching frequencies, the variation of motor drive efficiencies for all topologies with varying load current is also shown in Fig. 14.

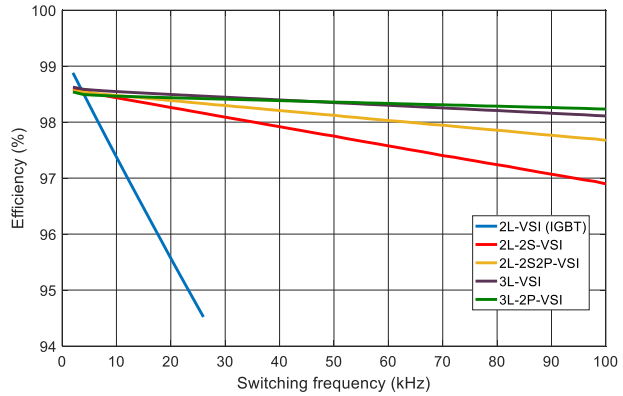


Fig. 12. Variation of motor drive efficiency with switching frequency

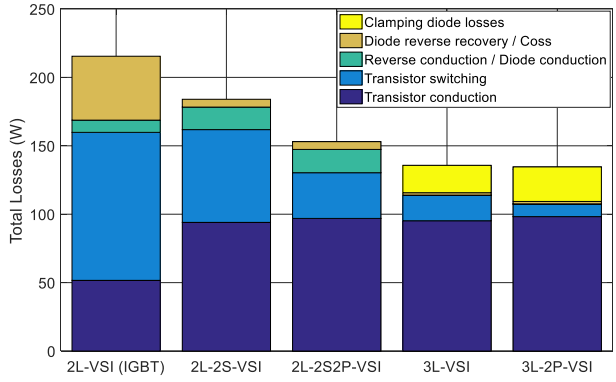


Fig. 13. Distribution of loss components for different topologies (fsw = 10 kHz for 2L-VSI, fsw = 50 kHz for other topologies)

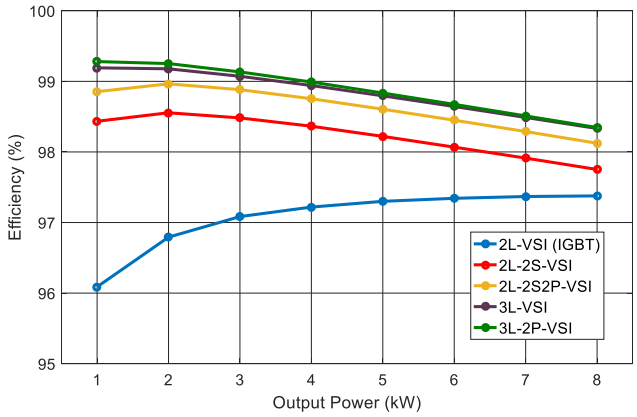


Fig. 14. Variation of motor drive efficiency with varying output power (load) (fsw = 10 kHz for 2L-VSI, fsw = 50 kHz for other topologies)

D. *Discussions*

On the motor side, 3L-VSI topologies have better waveform quality for both voltage and current compared to 2L-VSI topologies at the same switching frequency as a higher number of voltage levels is used. Series or parallel connection do not affect the voltage harmonic spectrum of the modules on the motor side. IMMD topologies with GaN FETs have the advantage of using higher switching frequencies such that the dominant harmonic frequencies are much greater than the ones of conventional topology with IGBT. Because of this, the magnitude of the motor line current harmonics is lower as seen in Fig. 8. For the same switching frequency, THD of both voltage and current is lower for three-level topologies than two-level.

On the DC link side, 3L-VSI has slightly lower ripple RMS current than 2L-VSI. Apart from this, the only factor that changes the RMS current is the application of phase-shifting (gate signal interleaving) which is only applicable in parallel connected topologies (2L-2S2P-VSI and 3L-2P-VSI). In overall, the best performance on the DC link RMS current is obtained for 3L-2P-VSI. The percent DC bus voltage ripple per module is kept at 1% for all topology simulations to obtain the required capacitance as shown in Fig. 11. The total capacitance variations show that, series connection of modules increase the capacitance requirement, therefore using 3L-VSI topologies instead of series connected 2L-VSI is more advantageous. Parallel connected topologies are also advantageous thanks to the effect of interleaving on the DC link voltage ripple. 3L-2P-VSI and 2L-VSI conventional topology have the best performance on capacitance requirement, however the former can reach much higher switching frequencies, lowering required the capacitance thanks to the utilization GaN devices.

It is clear from Fig. 13 that increasing the number of parallel connected modules decreases the switching losses since GaN transistors having lower current ratings tend to have much lower switching energies. However, parallel connection does not affect conduction losses significantly since the on-state resistance have direct proportionality with the current ratings. Therefore, as the switching frequency is increased, topologies having parallel connection results in better efficiencies compared to non-parallel variations. This result can be further improved by adding more parallel modules; however, the number of parallel connected modules is limited by the number of stator slots of the motor. Moreover,

the overall cost of the drive becomes an important issue as stated in the Section 3-D.

For the GaN semiconductors, conduction losses become more dominant compared to the switching losses. Therefore, the efficiency of the motor drive tends to decrease as the output power increases, as can be seen in Fig. 14. This trend is exactly the opposite for the IGBT based topology, as the switching losses are more dominant for the IGBT semiconductors. However, for all cases, even though the GaN based topologies are switched at much higher frequencies, their efficiency is always better than 2L-VSI topology above 5 kHz. For GaN based systems, efficiency is always larger than 97% for any of the cases while the efficiency of 2L-VSI after 22kHz drops below 95%. Apart from that, since the clamping diode losses is larger in 3L-2P-VSI, the overall efficiency difference between 3L-VSI and 3L-2P-VSI decreases at heavier loads.

According to the results shown in Fig. 12, 3L-VSI is the most efficient topology for switching frequencies between 10 and 46 kHz. Above 46 kHz, 3L-2P-VSI has the best efficiency. This change occurs due to the loss contribution of the clamping diodes. The efficiency difference between 2L-2S-VSI and 2L-2S2P-VSI is only a result of reduction of the switching losses due to the parallel connection.

It has been shown that using parallel connection in any of the topologies results in better efficiency as the switching frequency gets higher. The 3L-VSI topologies have better efficiency compared to the 2L-VSI topologies. Moreover, the voltage and THD values are lower for 3L-VSI topologies as well. The conventional 2L-VSI with IGBT have a very good efficiency for very low switching frequency values. However, its efficiency drops drastically since the switching losses get much more dominant. Efficiency values above 98% can be achieved with 2L-2S2P-VSI, 3L-VSI and 3L-2P-VSI topologies around 50 kHz. Even though the switching frequencies of the GaN based topologies are five times larger than the conventional IGBT case, the efficiency is always better for the GaN based topologies. One drawback of using three-level topologies is the imbalance of the transistor losses. The thermal design of the motor drive should be considered accordingly. This is not an issue for the 2L-VSI cases since the transistor losses are symmetrical for all topologies.

There are two aspects in terms of the fault tolerance of an IMMD system: fault tolerance of the motor; i.e., capability of the motor to operate under the fault of one of the motor pole windings, and fault tolerance of the drive; i.e., capability of the drive to supply the motor when one drive module is in fault. Motor fault tolerance directly depends on the number of independent motor modules making 2L-2S2P-VSI the most fault tolerant topology among the alternatives. Series connection of inverters does not directly imply drive motor fault tolerance, therefore 2L-2S2P-VSI and 3L-2P-VSI have better drive fault tolerance. In overall, a fully fault tolerant IMMD system can be achieved by using both series and parallel connected two-level VSI modules.

V. Conclusions

In this paper, comparison of five different motor drive topologies suited for IMMDs is presented. The utilization of GaN devices in IMMDs shows promising performance over a conventional motor drive in all aspects. The improvement in motor drive efficiency to reduce the heat sink size, by using parallel connected modules is shown. Furthermore, size reduction in DC link capacitors is achieved by using gate signal interleaving in modular structure. It has been shown that, 98% efficiency can be obtained with very small DC bus capacitance for a newly proposed topology where 2-level modules are connected both in series and parallel configuration. Permitting the utilization of commercial GaN FETs with series connection, this topology has also increased fault tolerance capability in terms of both motor and drive inverters.

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