Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors

Abstract: In this paper, turn-on and turn-off switching behavior of 650V enhancement-mode GaN power FETs are investigated. An analytical model is developed to analyze the current-voltage characteristics of the device during switching transients both with and without the effects of parasitic components.

I. Introduction

Wide band-gap power semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming more widespread, thanks to their superior efficiency and power density performance over Silicon (Si) based power semiconductor devices. Although current GaN devices are available at lower voltage (< 650V) and lower current (< 50A) ratings, they already became an attractive solution in several power converter applications. Several enhancement-mode (e-mode) GaN transistors are now commercially available up to 650 V ratings, which have better performance than cascode devices in terms of the switching speed, R_{ds-on} and reverse conduction. E-mode GaN FETs have low specific R_{ds-on} due to their high breakdown field as well as high electron mobility. They can be manufactured with smaller size so that the parasitic components due to packaging are lower resulting in faster switching [1]. Switching losses of these devices are much lower compared to their Si counterparts, which allows them to be used in high frequency applications, the size of passive components can be reduced.

Investigation of switching behavior of GaN power FETs is important for several reasons. First of all, high switching speed of GaNs make them more vulnerable to *di/dt* and *dv/dt* effects and parasitic components. Secondly, e-mode GaNs have reverse conduction capability without an intrinsic or external diode [2]. They act as a resistor just like MOSFETs in forward conduction; however, their behavior in reverse conduction is different than the forward conduction, varying with the applied gate-source (V_{gs}) voltage. Therefore, turn-on and turn-off characteristics are dependent on applied gate-source voltage. Usually in half bridge configurations, a negative gate voltage is required to avoid false turn-on, which results in a much higher on-state voltage when the device is not actively turn-on during dead-time [3]. Another reason for studying switching behavior of GaN is that their switching loss and reverse conduction loss model is not the same as Si MOSFETs. Although dead-time period and its effects on power loss calculations are usually ignored in other applications, it may affect the converter efficiency significantly in e-mode GaN applications [3].

Several recent studies have been published regarding e-mode GaN FET modeling. In [4], the I_{ds}-V_{ds}, I_{ds}-V_{gs} characteristics and dynamic R_{ds-on} behavior of e-mode GaNs are obtained using curve fitting from experimental data. An analytical model is applied with steady-state behavior with temperature dependency and dynamic response with varying input and output capacitances in [5]. A mode-by-mode analysis is investigated in [6] for estimating the switching losses under various parasitic effects using small-signal models. The false turn-on phenomenon and its relationship with the applied V_{gs} voltage are investigated in [3]. Several methods have been proposed for the minimization of the reverse conduction losses such as using a schottky diode in parallel with the synchronous GaN transistor [3]. In this paper, a hybrid model is proposed for the investigation of steady-state behavior and the switching transients of e-mode GaN power FETs. The state trajectories of the device during the turn-on and turn-off periods are obtained. The active turn-on and passive turn-on characteristics of the device are investigated on a synchronous buck converter. Also, the effect of varying device capacitances and parasitic inductances on these trajectories and their possible outcomes are studied.

II. GaN Modeling

In this study, a hybrid model is proposed as shown in Fig. 1(a). In this model, the drain-source characteristics is modeled by a dependent current source and a temperature dependent resistance which gives the steady state behavior of the device during forward and reverse conduction at different V_{gs} values. The blue branch in Fig. 1(a) indicates device channel and its current and voltage equals to $I_{ds} - V_{ds}$ in steady state. The analysis during the switching transients will be located onto this characteristics to show the regions that device operates during these transient periods. The equations used for steady-state models are shown in (1) and (2) for forward conduction and reverse conduction, respectively. These equations correspond to the I_{ds}-V_{ds} curves of the device and the dynamic R_{ds-on}, derived from the manufacturer's models. The logarithmic multiplier of the equations represents the trans-conductance of the device where V_{th} is the threshold voltage. The fractional multiplier represents the region in which the device is operating; i.e., active region or ohmic region. R_t represents the temperature dependency of R_{ds-on} in the model given in Fig. 1(a). Using this model, both steady-state and transient behavior of the conduction paths are obtained. The model is used in MATLAB/Simulink with a single-leg converter (synchronous rectifier) to investigate the switching behavior as shown in Fig. 1(b). The nominal values of this test circuit used for the simulations are listed in Table 1.
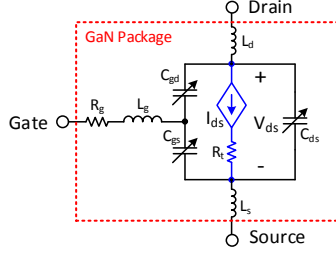
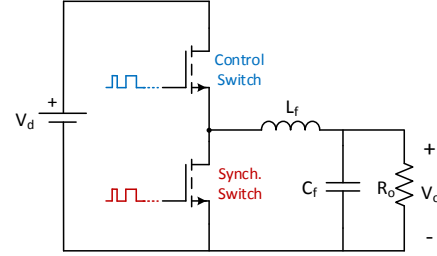Fig.1(a) Proposed hybrid model of e-mode GaN power FET   Fig. 1(b) The synchronous buck converter used for the analysis

$$I_{ds} = K_1 * ln\left[1 + e^{\left(\frac{V_{gs}-V_{th}}{K_2}\right)}\right] * \frac{V_{ds}}{1 + max(K_4 + K_5 * (V_{gs} + K_6), K_7) * V_{ds}} , K_i \ are \ constant \tag{1}$$

$$I_{ds} = -K_1 * ln\left[1 + e^{\left(\frac{V_{gd}-V_{th}}{K_8}\right)}\right] * \frac{V_{sd}}{1 + max(K_4 + K_5 * (V_{gd} + K_9), K_7) * V_{sd}} , K_i \ are \ constant \tag{2}$$

To show the accuracy of the steady state models, I_{ds}-V_{ds} characteristics of the selected device (GS66508B from GaN Systems) with varying V_{gs} is obtained in both forward and reverse conduction regions at 25 ^{0}C, and plotted side-by-side with the actual characteristics given in the datasheet of the selected device in Fig. 2 [7]. As shown, the reverse conduction behavior is highly dependent on the applied gate voltage, and shows a different behavior at negative gate voltage. In free-wheeling modes, this should make no difference since the applied gate voltage is positive. However, during dead-time periods, a negative gate voltage is applied increasing the reverse conduction loss, which makes the optimization of the negative gate voltage and dead-time duration very critical.
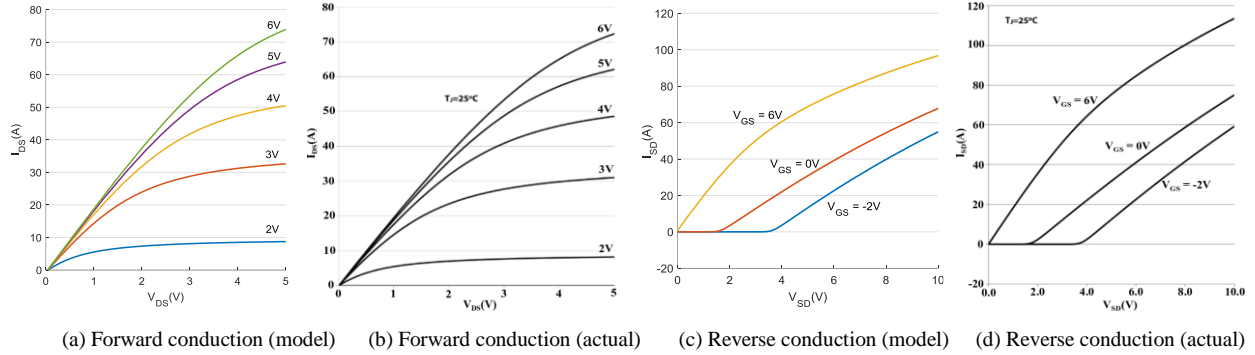
(a) Forward conduction (model)   (b) Forward conduction (actual)   (c) Reverse conduction (model)   (d) Reverse conduction (actual)

Fig.2. Steady-state characteristics of GS66508B obtained by the proposed model and the actual characteristics [7]

The second critical part of the model includes the capacitances which determine the transient behavior of the device during the switching operation as shown in Fig. 1. Although the values of these capacitances are usually given in the datasheets as constant at rated voltages, that kind of a model will not be accurate as they are actually dependent on V_{ds} voltage. Therefore, it may change the behavior of the device during turn-on and turn-off periods, and should be taken into account. In this study, these variable capacitances are modeled using curve fitting obtained from the datasheet, and the resulting characteristics is shown in Fig. 3 [7].
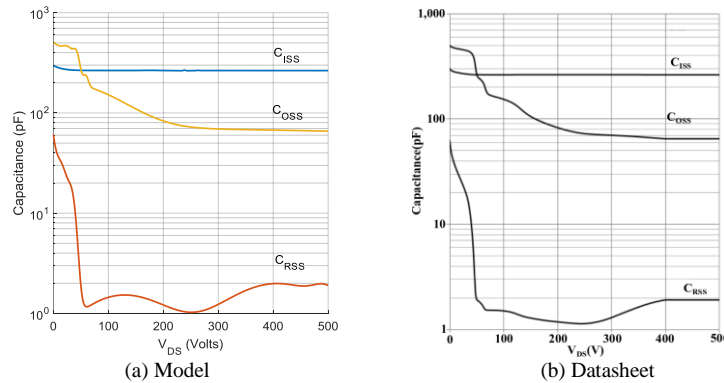
(a) Model   (b) Datasheet

Fig.3. Modeling of the capacitances using curve fitting

III. Switching Behavior of GaN

For better understanding of the switching behavior of e-mode GaNs, the turn-on and turn-off behavior of the selected device is investigated with a synchronous buck converter step-by-step using three models: the simplest model with constant capacitances and without parasitic inductances, the model with variable capacitances but without parasitic inductances, the most comprehensive model with variable capacitances and with parasitic inductances.

Table 1. The parameters used for the test circuit in MATLAB/Simulink [3, 7]

Input voltage (V_d)	400 V	Gate parasitic inductance (L_g)	1.0 nH	Dead-time (t_{dead})	10 ns
Output voltage (V_o)	200 V	Internal gate resistance (R_g)	1.5 Ω	Filter inductance (L_f)	10 µH
Output power (P_o)	3 kW	Turn-on gate resistance (R_{G-ON})	20 Ω	Filter capacitance (C_f)	220 nF
Applied gate voltage (V_{gs})	-3V/+6V	Turn-off gate resistance (R_{G-OFF})	5 Ω	Drain/source inductances (L_d/L_s)	0.9 nH

a) Model 1: The simplest model with constant capacitances and without parasitic inductances

For simplicity, the control switch is going to be labeled as "Top Switch" and the synchronous switch is going to be labeled as "Bottom Switch" from now on, in the synchronous buck converter. For Model 1 described above, turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. 4.

(a) Top switch turn-on   (b) Top switch turn-off   (c) Bottom switch turn-off   (d) Bottom switch turn-on
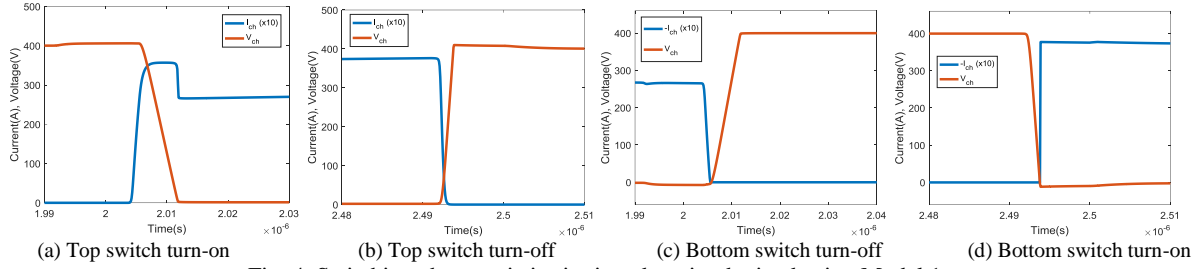
Fig. 4. Switching characteristics in time domain obtained using Model 1

Rather than giving the drain-source current, the channel current is preferred to clearly show the device characteristics better. For transient periods, since the parasitic capacitors' voltages increase or decrease, their currents affect the drain-source current which overshadows the device characteristics. As shown in Model 1, Figure 4(a), when the Top Switch is being turned on, the channel current makes an overshoot for two reasons. Firstly, since the Bottom Switch stops conducting, C_{OSS} (=C_{gd} +C_{ds}) of the Bottom Switch requires to be charged. Secondly, since C_{OSS} of the Top Switch is discharged, it causes current flow through the channel of the Top Switch. Additionally, even though it seems like soft switching is applied on Bottom Switch, actually it is not the case because C_{OSS} of the Bottom Switch is charged or discharged during transient periods and it would be observed if the current was I_{ds} instead of the channel current. One should note that the main characteristics observed in Model 1 are important to understand GaN behavior because even though these characteristics exist in complicated models, it might be hard to catch them with the presence of oscillations due to parasitic inductances and capacitances.

b) Model 2: The model with variable capacitances but without parasitic inductances

In this step, the capacitance values, which were kept constant previously, are treated as variable capacitances using the capacitance models presented in Section II. As shown in Figure 3, the capacitances change with respect to the applied drain-source voltage. Although C_{ISS} does not vary too much with varying V_{ds}, there is significant variation in C_{OSS} and C_{RSS}. The turn-on and turn-off characteristics of the top and the bottom switches are obtained against time and can be seen in Fig. 5.

(a) Top switch turn-on   (b) Top switch turn-off   (c) Bottom switch turn-off   (d) Bottom switch turn-on
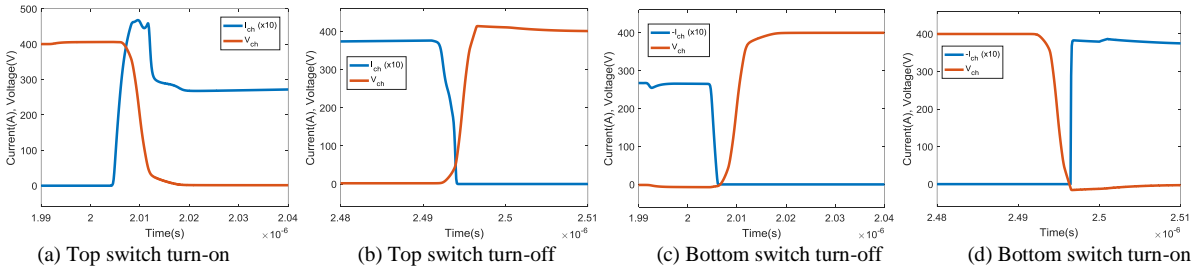
Fig. 5. Switching characteristics in time domain obtained using Model 2

In Model 2, it is observed that the overshoot in the Top Switch channel current increased because C_{OSS} is greater for lower drain-source voltages, which results in higher current flow under similar voltage change in time. Moreover, for

all transient periods given in Figure 5, it is observed that the voltage changes are smoother, which makes the model more realistic. Plus, those different change rates of voltage affect the channel current and that is why small dips and peaks are observed on the current waveforms.

c) Model 3: The most comprehensive model with variable capacitances and with parasitic inductances

(a) Top switch turn-on   (b) Top switch turn-off   (c) Bottom switch turn-off   (d) Bottom switch turn-on
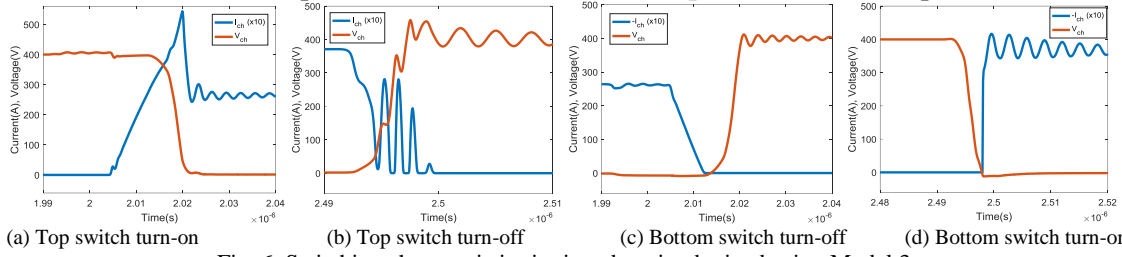
Fig. 6. Switching characteristics in time domain obtained using Model 3

Finally, to see the effect of the oscillations created by the LC resonance paths, the parasitic inductances are added to the model which are caused by packaging, busbar, conducting parts on the DC side and Capacitor ESLs. In Model 3, in which all the parasitic effects are included, as shown in Fig. 6, the oscillations started to emerge due to energy transfer between parasitic capacitances and inductors. During the turn-on period for the Top Switch, the channel current increases continuously, because C_{OSS} of the Top Switch is being discharged. With the parasitic inductors, the rate of change of the voltage on the C_{OSS} is not constant which results inconstant current flow through the channel on the contrary of variable-capacitance model. On the other hand, during the turn-off period for the Top Switch, huge oscillations are observed on channel current due to the Top Switch's C_{OSS} charging and discharging. Note that those oscillations observed on I_{ds} are not as high as channel current because the charging and discharging current flows are not reflected directly on drain-source current. That is why these oscillations are not observed on oscilloscopes. However, it is more expressive to investigate the channel current in such models to follow device states closely.

d) State Trajectories

In order to show these transients better, the I_{ch}, V_{ch} *paths*, which the Top and the Bottom switches follow during turn-on and turn-off periods, are also obtained as state trajectories and given in Fig.7. These trajectories are plotted on the device steady state current-voltage characteristic as given in Fig.2

(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off
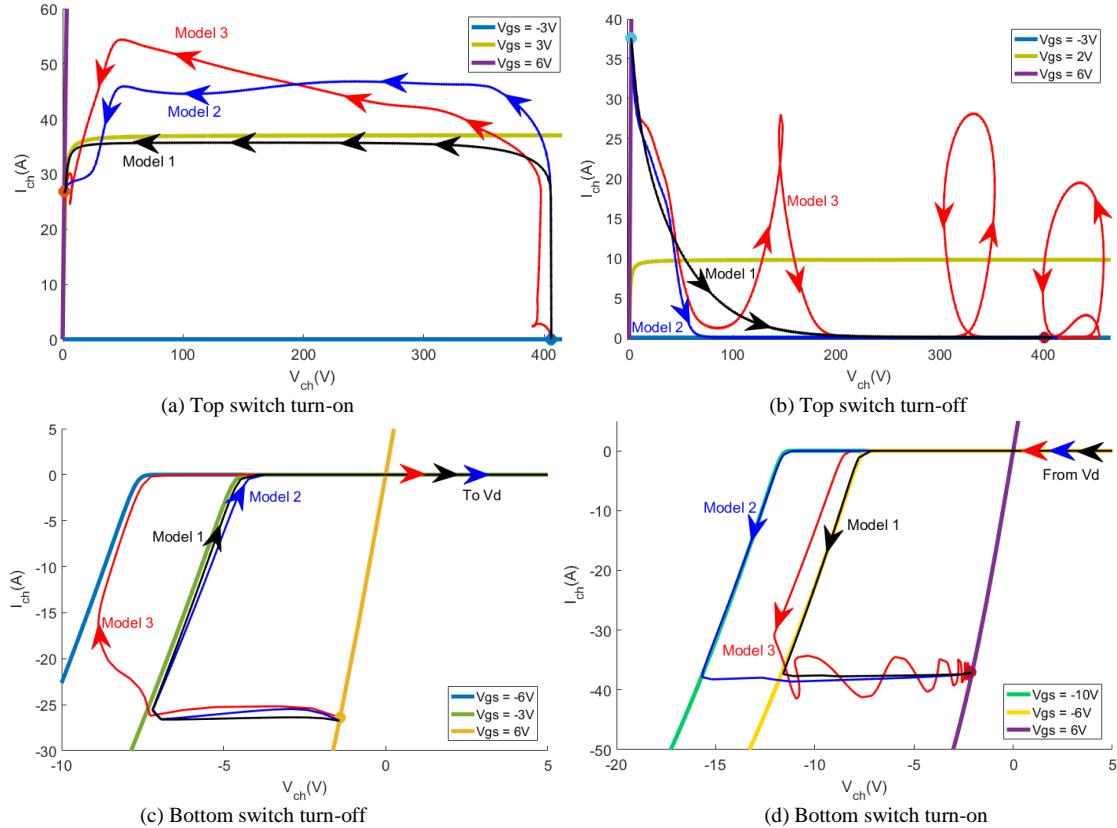
(d) Bottom switch turn-on

Fig 7. Switching characteristics as state trajectories (obtained using all the models)

When we look at the trajectory for the turn-on period of the Top Switch, Fig.7 (a), it is easy to see the Miller Plateau where the voltage drops and current stays constant ideally. During the turn-off period of the Top Switch, the oscillations on current are also observed on trajectory. As seen on the graph, actually the gate-source voltage also oscillates during that period. Moreover, an interesting result seen on the Bottom Switch turn-on trajectories is that when the inductors are not modeled but the capacitances are variable, the gate-source voltage drops until -10 Volts, which is the limit of the minimum gate-source voltage. However, when the inductors are included too, the result is more realistic and it is seen that gate-source voltage does not reach risky values. On the contrary, for turn-off trajectories of the Bottom Switch, the gate-source voltage drops to nearly -6V for Model 3. As a result, including inductors in model is critical to evaluate operation's safety.

Furthermore, focusing on the trajectories given on the Bottom Switch turn-off graph, it is seen that the load current completely flows through the channel of the Bottom Switch before positive gate-source voltage is applied. This conduction period is also called as dead-time. In IGBTs or MOSFETs, current flows through the anti-parallel diode or body diode during the reverse conduction which is not the case for GaN. In GANFETs, body diode or anti-parallel diode does not exist and the reverse current flows through the device channel. Therefore, when the top switch is being turned off, the constant load current flows through the channel of the Bottom Switch in reverse direction in the dead-time period. The positive gate-source voltage is applied just to minimize V_{sd} to obtain minimum loss. Thus, it can be deduced that applied gate-source voltage is not important for turning on the Bottom Switch and it is being turned on when the Top Switch stops conducting. To simplify the issue and to make the concept more understandable, the rise of the current in the Bottom Switch channel can be called as **active turn-on** and applying positive gate-source voltage is called as **passive turn-on**. The key difference is that in active turn-on device starts to conduct load current and in passive turn-on the current is not changed but the loss is decreased. This distinction is not required for IGBTs or MOSFETs because current flows through the anti-parallel diode or body diode during the dead-time and when the gate-source voltage is applied the current commutates from body diode to channel for MOSFETs. However, it is important for GaN devices because they have no body diode or anti-parallel diode and applying positive gate-source voltage changes nothing about current for reverse conduction. Similarly, for the turn-off period of the Bottom Switch, in the dead-time negative gate-source voltage is applied, which does not affect the channel current. The channel current starts to decrease when the top switch is turned on. Therefore, applying negative gate-source voltage should be called as **passive turn-off** and actual current decrease in the channel should be called as **active turn-off**.

IV.   Conclusions

In this paper, turn-on and turn-off characteristics of GaN devices are investigated step by step including different parasitic effects. Understanding the effect of the parasitics on turn-on and turn-off characteristics of GaN is important to understand GaN behavior and operating safely. For this purpose, a GaN device is modeled and the model is verified by comparing simulation results with datasheet results. Then, the channel current and channel voltage, which represent device characteristic better, are investigated on a synchronous buck converter circuit using accurately modeled GaN device. The simulation results belonging to channel current and voltage waveforms are presented and as a novel approach, their trajectories are represented on the steady state $I_{ds} - V_{ds}$ graphs in order to make the characteristics clearer. Moreover, in order to emphasize and express the unique conduction characteristics of GaN better, important definitions, active/passive turn on/off, are explained in Section III.

In the final paper, those results will be enriched with more simulation results and will be verified with experimental results. In experimental results, GS66508B-EVBDB daughter board will be used. By means of the experimental results, it is aimed to give more detailed explanation for turn-on and turn-off characteristics of GaN in the finalized paper.

V.   References

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