Investigation of Dynamic Performance and Switching Loss Accuracy of Enhancement-Mode GaN Power Transistor Computer Models

Abstract: In this paper, voltage and current transients and resulting switching loss performance of three different computer models for 650V enhancement- mode GaN power FETs are investigated. Importance of parasitics on the dynamic performance of GaN transistors are discussed and their effects on turn-on & turn-off switching loss is showed.

I. Introduction

II. GaN Modelling and Test Circuit

A model for a transistor includes two behavioral aspects that are steady-state and dynamic actions. In this study, the steady-state behavior of the GaN power FET is modeled with a voltage-dependent current source, which is the channel of the device, and temperature dependent resistances. The equations for voltage-dependent channel current are provided in (1) and (2). Those equations imply that there is an exponential relation between channel current and gate-source voltage. On the other hand, those equations show that an ohmic region occurs for low drain-source voltages where channel current changes with a constant ratio, $R_{ds\text{-}on}$, as given in Figure X. The constant channel resistance, $R_{ds\text{-}on}$, is important for conduction loss. Conversely, when the drain-source voltage is high, the GaN power FET operates in saturation region; that is, the channel current is constant. In order to improve the steady-state model so that the dynamic behavior is included, it is required to add parasitic capacitances and inductances also. The resulting model of GaN power FET is shown in Fig. 1(a). Note that, the parasitic capacitances are voltage-dependent and importance of the modeling voltage-dependent capacitances on the switching transients is discussed in Section III. Furthermore, the steady-state characteristic of GaN power FET model at 25 ^{o}C is given in Fig. X. Comparing to manufacturer provided results, it is seen that the steady-state behavior of the model is accurate.

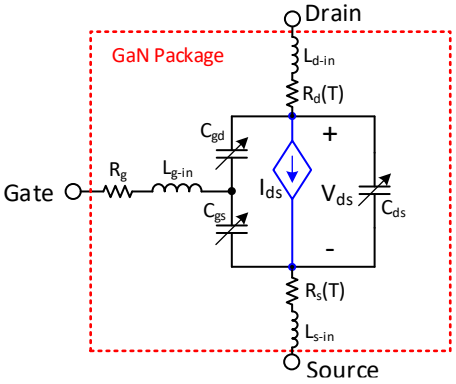


Fig.1(a) Proposed hybrid model of e-mode GaN power FET

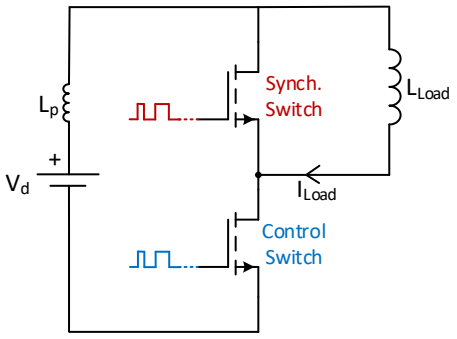
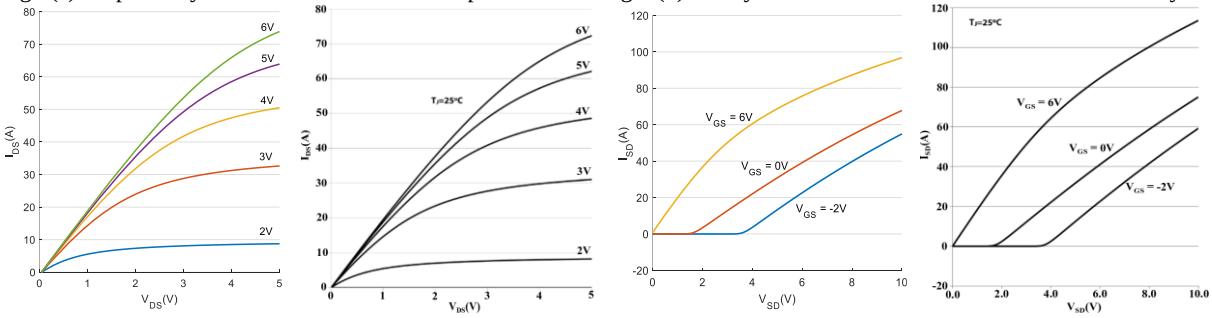


Fig. 1(b) The synchronous buck converter used for the analysis

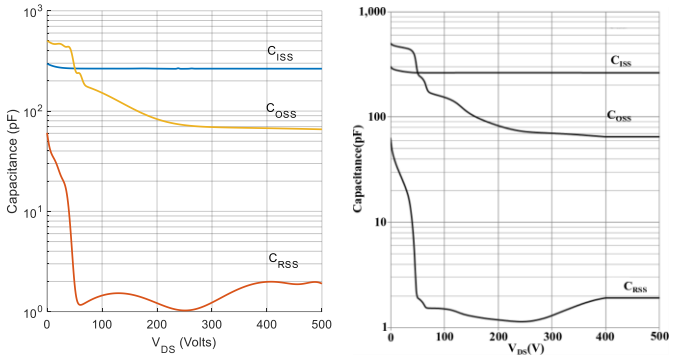


(a) Forward conduction (model) (b) Forward conduction (actual) (c) Reverse conduction (model) (d) Reverse conduction (actual)

Fig.2. Steady-state characteristics of GS66508B obtained by the proposed model and the actual characteristics

Secondly, the voltage-dependent parasitic capacitances are modeled using curve fitting obtained from datasheet and reference. The resultant curves are given in Fig. X and Fig. Y. The manufacturer provides the curve for parasitic capacitances with respect to the drain-source voltage and it is seen that C_{ISS} is constant. However, the C_{ISS} changes significantly with varying gate-source voltage and the model should be constructed by identifying gate charge. Therefore, in this paper, to model dynamic performance accurately C_{ISS}-V_{GS} curve is obtained from the reference graph given in [X].

Moreover, the resultant MATLAB/Simulink GaN power FET model is used on Double-Pulse-Test(DPT) circuit, Fig. X, to analyze transient performance of GaN power FET. DPT circuit is selected to have the same test circuit with the manufacturer. The nominal values of this test circuit, which are obtained from manufacturer model and test setup, are listed in Table X.



(a) Model (b) Datasheet

Fig.X. Modeling of the capacitances using curve fitting

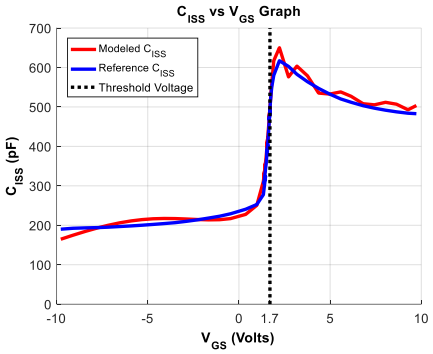


Fig. X: Modelling of C_{ISS}

Table X. The parameters used for the test circuit in MATLAB/Simulink [X]

Input voltage (V_d)	400 V	Gate loop inductance ($L_{g\text{-}ex}$)	3.0 nH	Dead-time (t_{dead})	10 ns
Load Inductance (L_o)	480 µH	Internal gate resistance (R_g)	1.5 Ω	Gate parasitic inductance ($L_{g\text{-}in}$)	0.65 nH
Applied gate voltage (V_{gs})	-3V/+6V	Turn-on gate resistance ($R_{G\text{-}ON}$)	10 Ω	Drain parasitic inductance($L_{d\text{-}in}$)	0.062 nH
Power loop inductance(L_p)	3.0 nH	Turn-off gate resistance ($R_{G\text{-}OFF}$)	2 Ω	Source parasitic inductance($L_{s\text{-}in}$)	0.45 nH

III. Dynamic Performance and Loss Accuracy of the Models

The loss analysis is conducted on three different model types to see the magnitude of the effects of the parasitics on analysis. In the first model, the parasitic capacitances are kept constant at datasheet nominal values and the internal parasitic inductances of the GaN power FETs are excluded from model. In the second model, the parasitic capacitances are variable but the inductances are excluded again. In the third model, the parasitic capacitances are variable and the internal parasitic inductances are included. Note that, the steady-state characteristics of both models are the same and gives accurate results as expected.

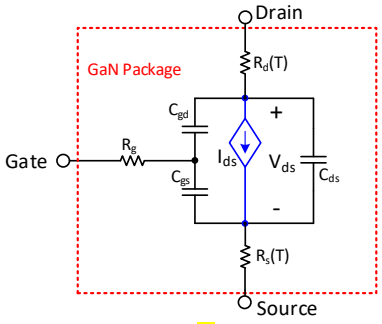


Fig.X(a) Model I

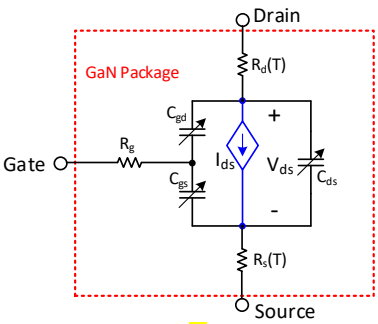


Fig.X(a) Model II

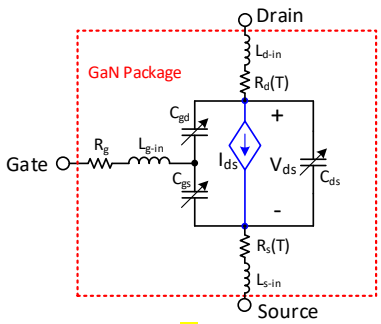


Fig.X(a) Model III

For each model, turn-on and turn-off losses of the Control Switch are obtained from simulation results for different load current ratings and they are given in Fig.X and Fig.Y. Then, the total switching losses of the models are compared with the experimental results, which are provided by manufacturer[X], as shown in Fig.X. The comparison tells that the dynamic performance of the Model 1 is not accurate. On

the other hand, switching energy losses of the Model 2 and the Model 3 are closer to each other and experimental results. As a result, having the parasitic inductances in model has a minor effect in comparison with the variable parasitic capacitances. Therefore, for a model to have an accurate dynamic characteristic the capacitances should be modeled correctly.

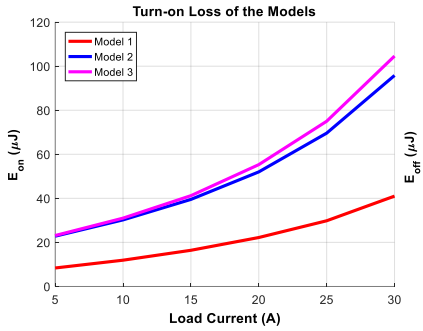


Fig.X(a) Turn-On Losses

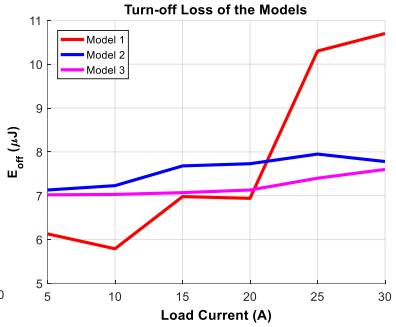


Fig.X(a) Turn-Off Losses

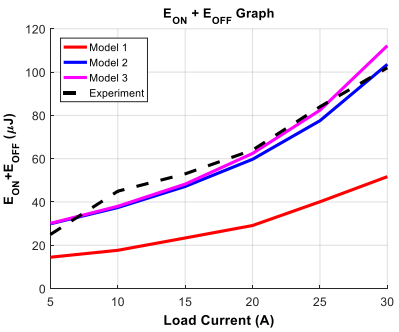


Fig.X(a) Total Switching Loss

Moreover, it can be deduced from the Fig. X, the model, which gives the most accurate results, is the Model 3 with all parasitics. Now, to visualize the switching waveforms, the turn-on and turn-off waveforms of the Model 3 are given in Fig.Y where the load current is 30 Amperes. At the starting moment of the turn-on switching period, a dip is seen on the drain-source voltage waveform. That dip is caused by the power loop inductance; that is, when the loop current changes from zero to load current immediately, there occurs a voltage drop on the loop inductance. In addition, it is seen that, the drain-source current makes an overshoot when the switch turns-on. This happens because the C_{OSS} of the Synch. Switch is being discharged and since its gate-source voltage is set to -3V, its channel cannot conduct the current, which results in an overshoot on the channel current of the Control Switch. The amount of overshoot depends on the input voltage and switching speed.

Further, an interesting switching waveform is observed during the turn-off period of Control Switch; that is, the drain-source current and the drain-source voltage change simultaneously, so it is inaccurate to use commonly preferred switching waveform which says the voltage rises first and then current falls to zero. This phenomenon belongs to only GaN power FETs because they have no body diode and they conduct current reversely using their channel. When the current of the Control Switch starts to fall as seen in the Fig. X, since the load current is continuous, the remaining amount of current has to flow through the Synch. Switch reversely. However, a problem rises here over the reverse conduction of the Synch. Switch, which is that a GaN power FET cannot conduct current reversely through its channel, when the drain-source voltage is positive. As seen on Fig. X, even though the current decreased in the duration t_1-t_2, the drain-source voltage of the Control Switch could not rise up to the input voltage which means the drain-source voltage of the Synch. Switch is still positive but it has to conduct reversely. Therefore, here the parasitic capacitances play a significant role; that is, when the drain-source current of the Control Switch starts decreasing, the reverse current does not flow through the channel of Synch. Switch but it flows through the parasitic capacitances of Synch. Switch so that the parasitic capacitances can be discharged. The discharging maintains until the drain-source voltage of Synch. Switch becomes negative. When the drain-source voltage has a negative value, the channel of the Synch. Switch starts conducting reversely. Because of this phenomenon, the drain-source current and voltages of Control Switch change simultaneously during turn-off period, so the current fall time is definitely equal to the voltage rise time during this period.

The voltage and current changing times are given in Fig. X for each model. For the turn-on period, the t_1-t_3 period is called as current rise time (t_{cr}) and the t_2-t_4 period is called as voltage fall time (t_{vf}). Similarly, for the turn-off period, the t_1-t_2 period is called as current fall time (t_{cf}) and voltage rise time (t_{vr}). As explained above, current fall time is strictly equal to voltage rise time.

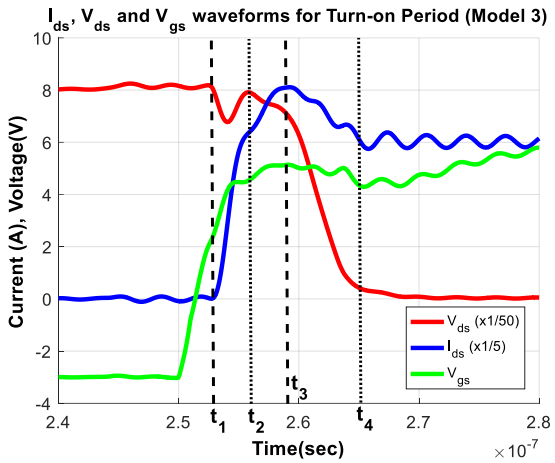


Fig.X(a) Turn-On Waveforms

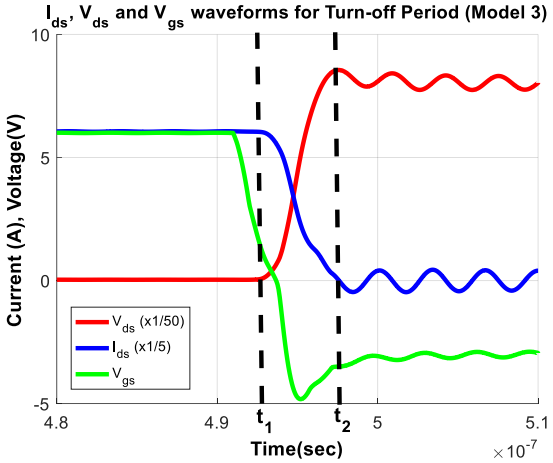


Fig.X(a) Turn-Off Waveforms

Similar to turn-on and turn-off loss results, for the current and voltage transient durations, the Model 1 behaves divergently and the results obtained from simulation of the Model 1 are not correct. On the other hand, it is observed there is a similarity between the Model 2 and the Model 3 that verifies the deduction made before; that is, the impact of the modelling of the parasitic capacitances is higher than the impact of including parasitic inductances on the dynamic characteristic of GaN power FET.

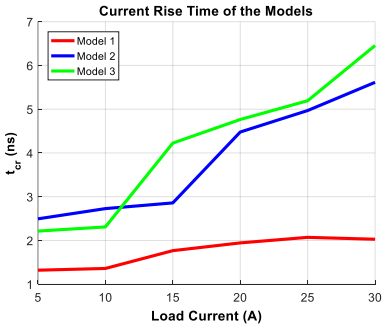


Fig.X(a) Current Rise Time

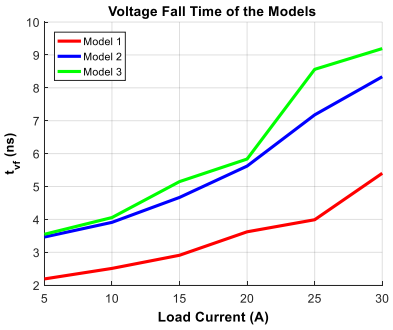


Fig.X(a) Voltage Fall Time

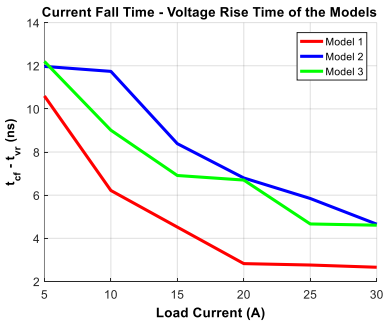


Fig.X(a) Current Fall /Voltage Rise Time

As observed in turn-off switching waveforms, again the trend of the current fall time (or voltage rise time) graph is different. In other words, even though the voltage fall time and current rise time increase with increasing load current, the voltage rise time decreases. Actually, it is a result of same phenomenon. As explained above, for the Synch. Switch to conduct reversely, the parasitic capacitances should be discharged and these capacitances are discharged with load current, which flows through them in reverse direction. Thus, higher load current means faster discharging, so the voltage rise time decreases with the increasing load current.

IV. Conclusions

In this paper, the dynamic behaviors and loss accuracy of the different models e-mode GaN power FETs is discussed. Three different model is proposed and for each model, corresponding turn on and turn off loss results are given for different current ratings. The simulation results are compared with the experimental results, which are provided by manufacturer. In addition, the impacts of the parasitics on the dynamic behavior are compared and the significance of voltage-dependent parasitic capacitance modelling is remarked. Moreover, the turn-off characteristics of the GaN power FET is investigated in Section III and it is shown that GaN power FET has a turn-off mechanism which is definitely different from other transistors.

In the final paper, the simulation results will be enriched with the instantaneous power dissipation results and the results will be compared with the experimental results, which will be conducted by the

researcher. In experimental results, GS66508B-EVBDB daughter board will be used. It is aimed to express the effect of the different parameters on dynamic behavior in the finalized paper.

V. Reference