Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors

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Abstract

In this paper, turn-on and turn-off switching behaviour of 650V enhancement-mode GaN power FETs are investigated. An analytical model is developed to analyse the current-voltage characteristics of the device during switching transients both with and without the effects of parasitic components. In addition, the effect of the temperature and circuit parameters on the switching characteristics are investigated.

GaN Modeling

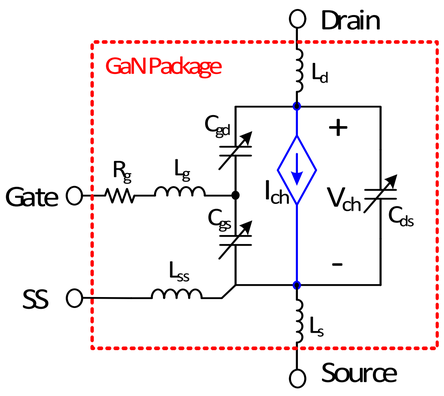
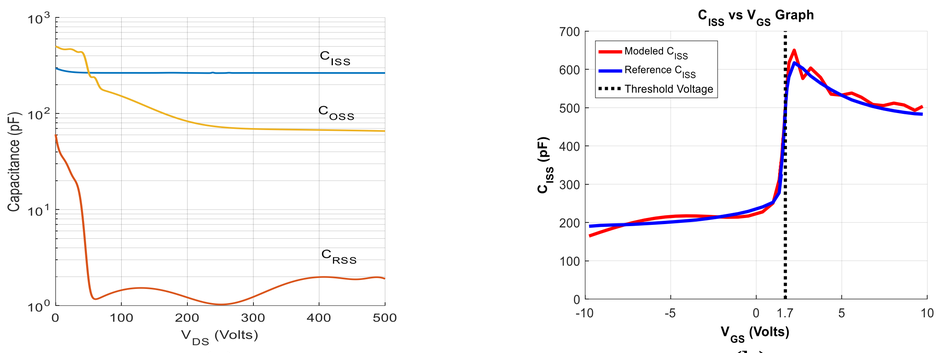


Fig. 1: The hybrid model of e-mode GaN power FET

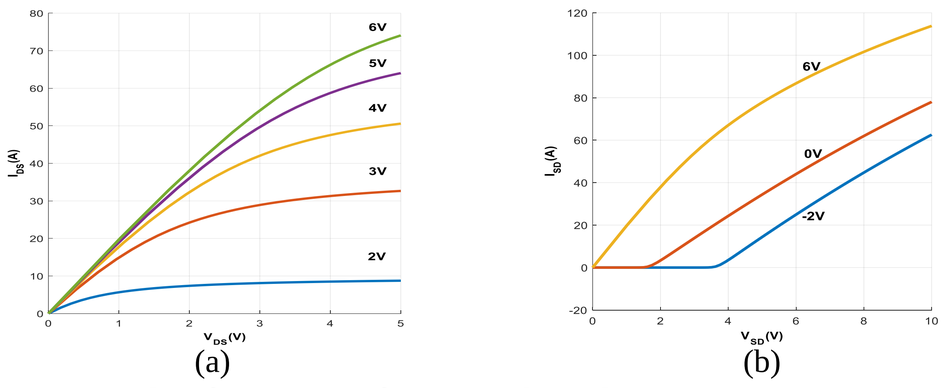
- Blue branch indicates the device channel
- The parasitic capacitances are highly dependent on the electrical field between drain-source terminals.
- Kelvin Source (SS) pin is used to eliminate Common Source Inductance (CSI) which might cause the device failure.



(a) (b)

Fig. 2: Parasitic capacitances vs Drain-Source Voltage plot (a) & Input Capacitance vs Gate-Source Voltage plot (b)

Even though manufacturer provides the Ciss as constant with respect to drain-source voltage, it changes significantly with varying gate-source voltage. Implementing this feature in the model is important to obtain accurate dynamic/switching characteristics.



(a) (b)

Fig. 3: Static Results of GS66508B for Forward Conduction (a) & Reverse Conduction (b)

The reverse conduction behaviour is highly dependent on the applied gate voltage. **A negative gate bias increases the reverse conduction loss**. Therefore, the negative gate bias level and dead-time duration optimization is very critical for especially high frequency switching applications.

- Junction temperature is a key factor which affects the trans-conductance of the device
- The trans-conductance is nearly halved for every 75ºC increase in junction temperature

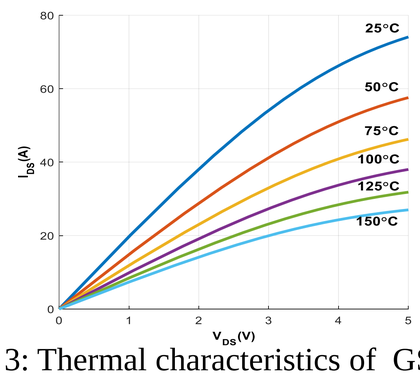


Fig. 3: Thermal characteristics of GS66508B obtained by the model for forward conduction at 6V gate-source voltage

Switching Test Circuit Configurations

A Double Pulse Test circuit is implemented in MATLAB / Simulink® platform to investigate switching transients.

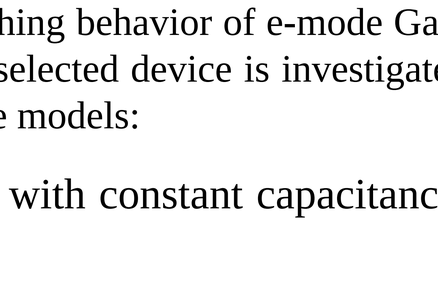


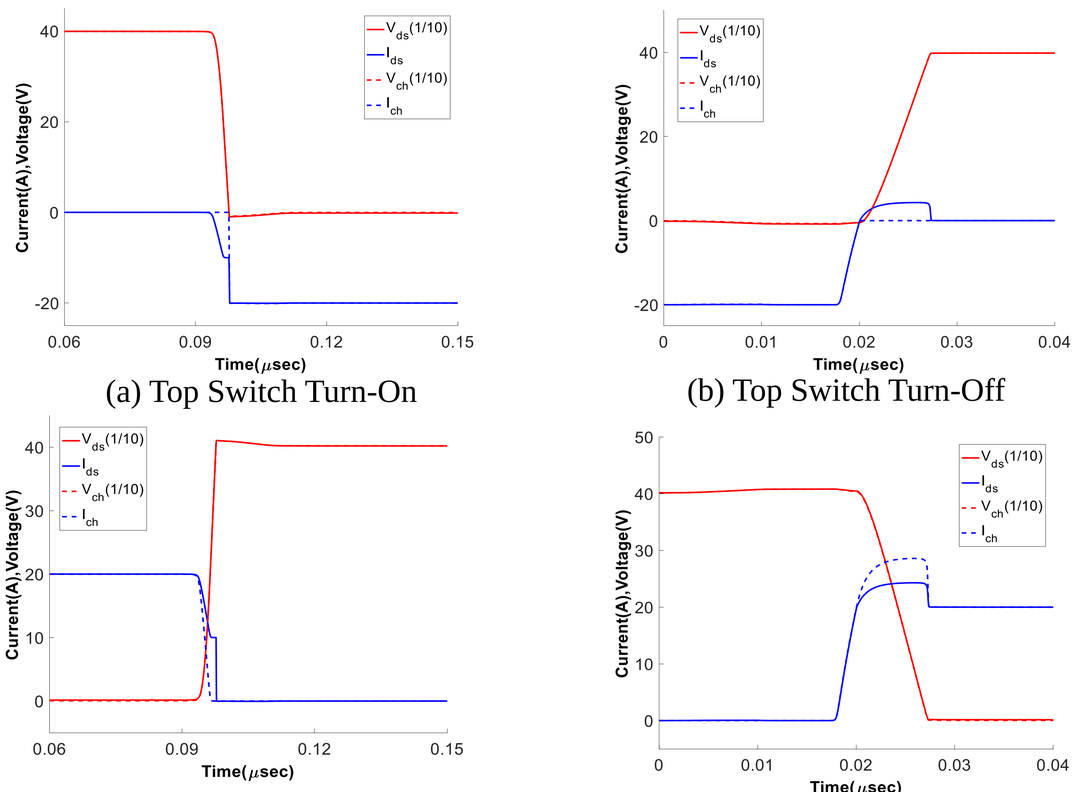
Fig. 4: Double Pulse Test (DPT) Circuit Configuration

Table 1: The parameters used for the test circuit in MATLAB / Simulink ®

Input voltage (V_d)	400 V	Internal gate resistance (R_g)	1.5 Ω	Gate parasitic inductance (L_g)	3.0 nH
Output Current (I_{LOAD})	20 A	Drain/source inductances (L_s)	0.9 nH	Power loop inductance (L_p)	7.0 nH
Load inductance (L_{LOAD})	35 mH	Turn-on gate resistance ($R_{G\text{-}ON}$)	10 Ω	Junction Temperature (T_J)	125 ^{0}C
Applied gate voltage (V_{gs})	-3V/+6V	Turn-off gate resistance ($R_{G\text{-}OFF}$)	1 Ω	Dead-time (t_{dead})	20 ns

For better understanding of the switching behavior of e-mode GaNs, the turn-on and turn-off behavior of the selected device is investigated with a DPT circuit step-by-step using three models:

❖ **Model 1:** The simplest model with constant capacitances and without parasitic inductances



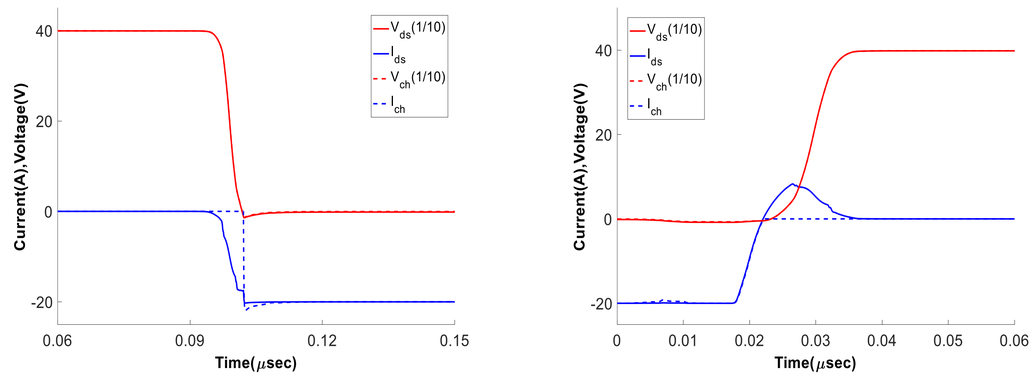
(a) Top Switch Turn-On (b) Top Switch Turn-Off

(c) Bottom Switch Turn-Off (d) Bottom Switch Turn-On

Fig. 5: Switching characteristics in time domain obtained using Model 1

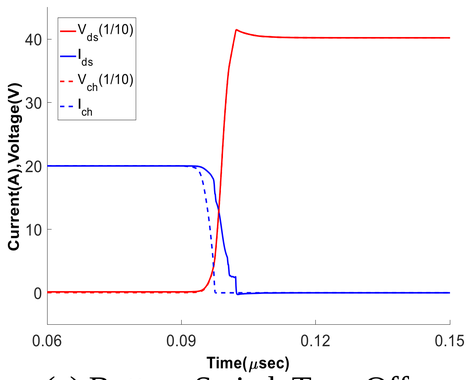
- No oscillations since the inductances are not included in the model
- Drain current and channel current are different due to the charging & discharging of switches' output capacitances
- The main characteristics can be observed in Model 1 easily

❖ **Model 2:** The model with variable capacitances but without parasitic inductances

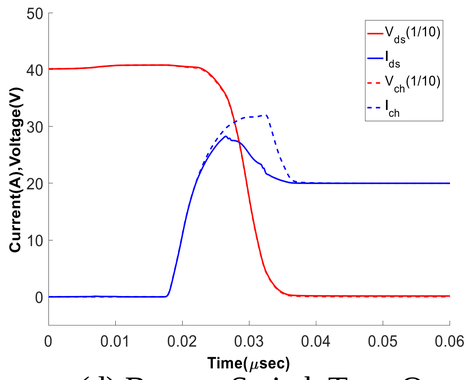


(a) Top Switch Turn-On (b) Top Switch Turn-Off

- Part II -



(c) Bottom Switch Turn-Off

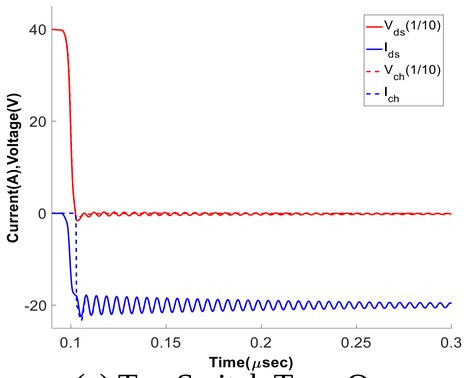


(d) Bottom Switch Turn-On

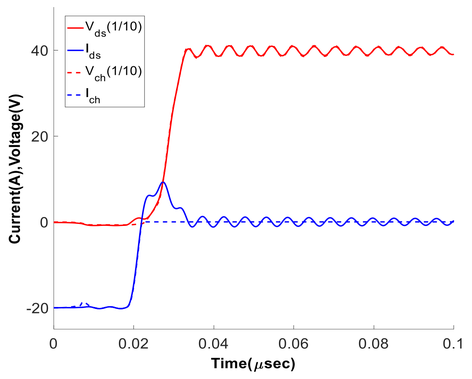
Fig. 6: Switching characteristics in time domain obtained using Model 2

- Amplitude of the overshoot in currents increased because for lower voltages now the Coss is greater than the Coss in Model 1, so the charging and discharging currents are required to be higher
- The transients are more smooth which is more realistic

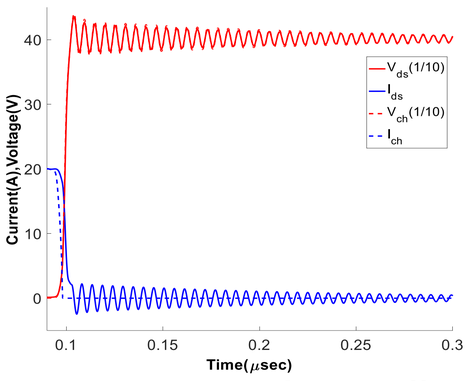
❖ **Model 3:** The most comprehensive model with variable capacitances and with parasitic inductances



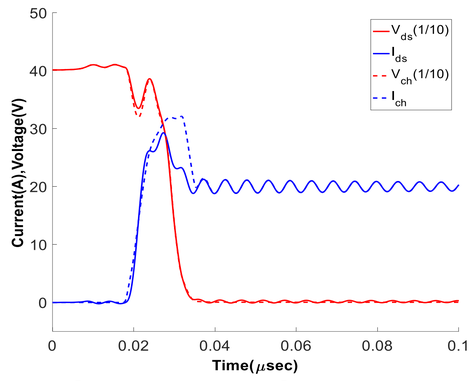
(a) Top Switch Turn-On



(b) Top Switch Turn-Off



(c) Bottom Switch Turn-Off

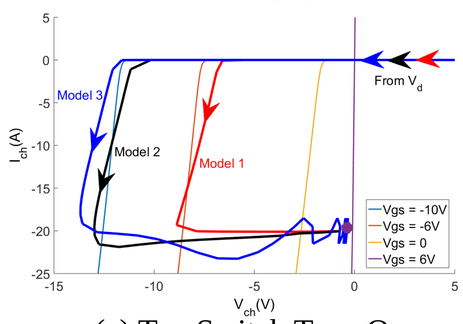


(d) Bottom Switch Turn-On

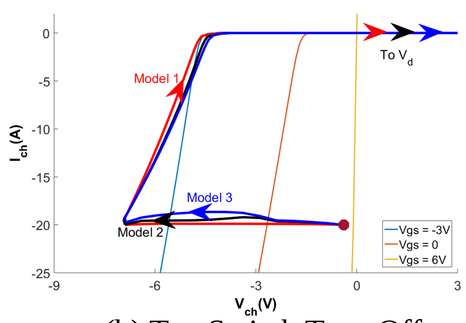
Fig. 7: Switching characteristics in time domain obtained using Model 3

- The parasitic inductances are added to the model, which are caused by packaging, busbar, conducting parts on the DC side and Capacitor ESLs
- A large dip is observed during bottom switch turn-off transient due to the loop inductance.
- The damping duration is dependent on the C_{OSS}, loop inductance and drain/source parasitic inductances and trans-conductance [8]

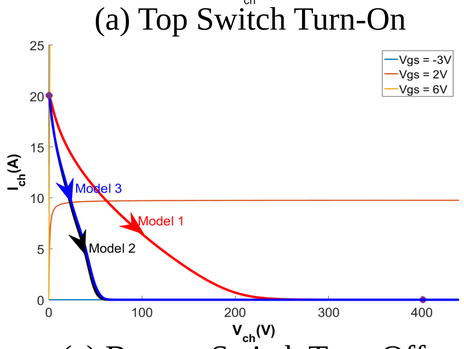
State Trajectories



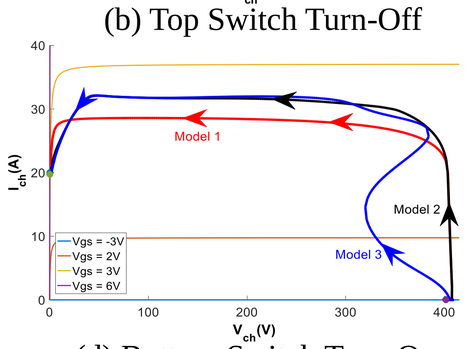
(a) Top Switch Turn-On



(b) Top Switch Turn-Off



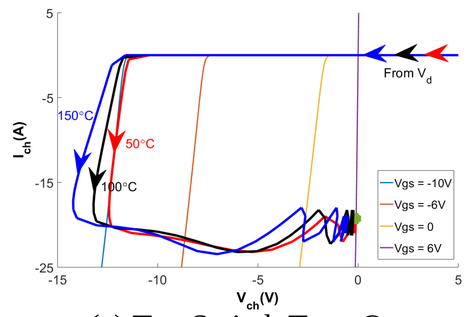
(c) Bottom Switch Turn-Off



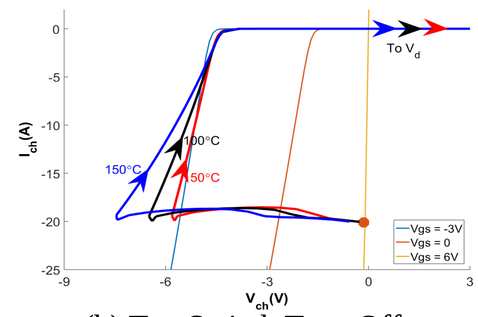
(d) Bottom Switch Turn-On

Fig. 8: Switching characteristics as state trajectories (obtained using all the models)

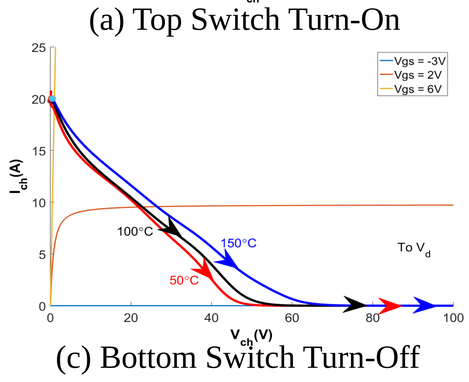
- The miller plateu where the current stays constant and voltage drops ideally can be seen in Fig. 8(d) easily.
- The third quadrant behavior of the GaN FETs are unique because the channel is able to conduct in reverse direction with any gate-source bias level. Therefore, the channel can conduct reversely without a positive gate bias and similarly channel might not stop conduction even a negative gate bias is applied.
- To make it more clear, active and passive turn-on/off concepts are proposed. **An active turn-on/off** means the channel starts or stops conduction whatever gate bias level is applied and **a passive turn-on/off** means the gate bias is changed but the channel continues its conducting or nonconducting state.



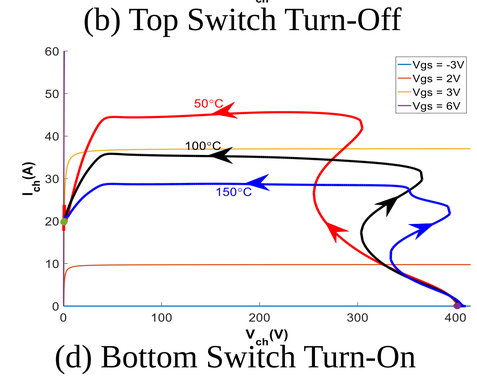
(a) Top Switch Turn-On



(b) Top Switch Turn-Off



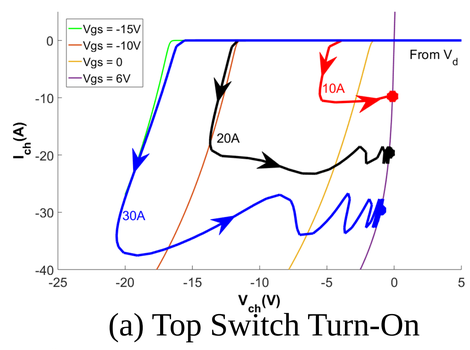
(c) Bottom Switch Turn-Off



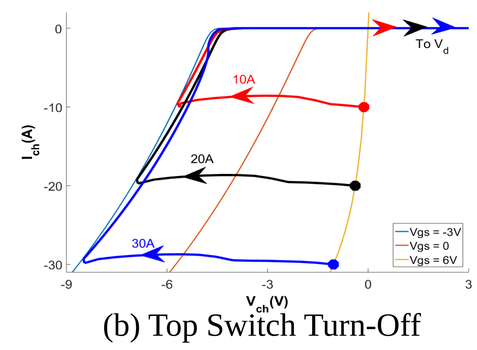
(d) Bottom Switch Turn-On

Fig. 9: Switching characteristics as state trajectories for different temperatures (Model 3)

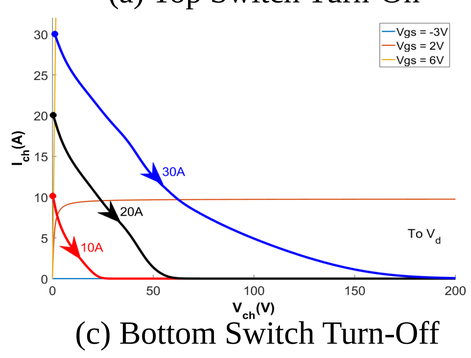
- Overshoot amplitude and voltage dip is decreased with temperature as seen in (d) due to lower transition speed
- The trans-conductance decreases with temperature; thus, for the same amount of current the drain-source voltage level increases



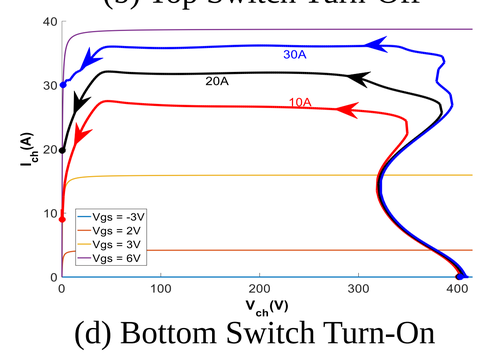
(a) Top Switch Turn-On



(b) Top Switch Turn-Off



(c) Bottom Switch Turn-Off

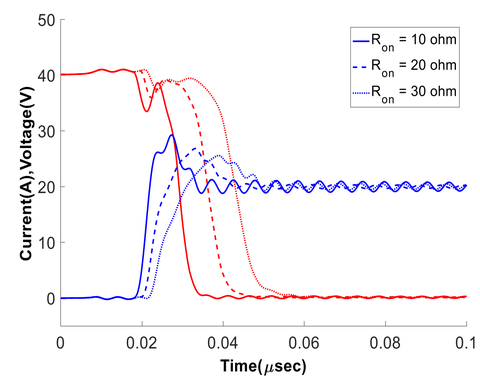


(d) Bottom Switch Turn-On

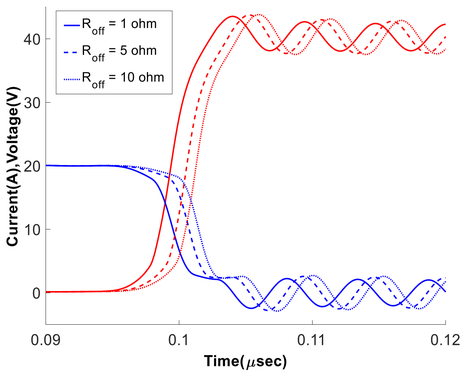
Fig. 10: Switching characteristics as state trajectories for different load currents (Model 3)

- The gate-voltage level changes dramatically with current level as seen in (a)
- As shown in (d), the voltage dip level is the same for all current levels because the transition speed is the same for all conditions

Effect of turn-on and turn-off resistances



(a) Turn-On



(b) Turn-Off

Fig. 11: Switching characteristics for different turn-on and turn-off resistances (Model 3)

Conclusion

In this study, a GaN device is modeled. The simulation results are presented as state-trajectories on the steady state I_{ds} – V_{ds} graph to discuss characteristics better. In order to express the unique conduction characteristics of GaN better, active/passive turn-on/off, are explained. Furthermore, it is shown that increasing operation temperature reduces trans-conductance significantly. Additionally, it is shown that the transient gate-source voltage is affected by the current whereas the switching speed is not changed as expected.

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