Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors

Abstract: In this paper, turn-on and turn-off switching behavior of 650V enhancement-mode GaN power FETs are investigated. An analytical model is developed to analyze the current-voltage characteristics of the device during switching transients both with and without the effects of parasitic components.

I. Introduction

Wide band-gap power semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming more widespread each day, thanks to their superior efficiency and power density performance over Silicon (Si) based power semiconductor devices. Although current GaN devices are available at lower voltage (< 650V) and lower current (< 50A) ratings, they have become an attractive solution in several power converter applications. Several enhancement-mode (e-mode) GaN transistors are now commercially available up to 650 V ratings, which have better performance than cascode devices in terms of switching speed, $R_{ds\text{-}on}$ and reverse conduction. E-mode GaN FETs have low specific $R_{ds\text{-}on}$ due to their high breakdown field as well as high electron mobility. They can be manufactured with smaller size so that the parasitic components due to packaging are lower resulting in faster switching [1]. Switching losses of these devices are much lower compared to their Si counterparts, and this allows them to be used in high frequency applications where passive components can be made smaller.

Investigation of switching behavior of GaN power FETs is important for several reasons. First of all, high switching speed of GaNs make them more vulnerable to *di/dt* and *dv/dt* effects and parasitic components. Second, e-mode GaNs have reverse conduction capability without an intrinsic or external diode [2]. They act as a resistor just like MOSFETs in forward conduction; however, their behavior in reverse conduction is different than forward conduction, varying with the applied gate-source (V_{gs}) voltage. Therefore, turn-on and turn-off characteristics are dependent on applied gate-source voltage. Usually, a negative gate voltage is required to avoid false turn-on which results in a much higher on-state voltage when the device is not actively turn-on during dead-time [3]. Another reason is that, their switching loss and reverse conduction loss model is not the same as Si MOSFETs. Although dead-time period and its effects on power loss calculations are usually ignored in other applications, it may affect the converter efficiency significantly in e-mode GaN applications [3].

Several recent studies have been published regarding e-mode GaN FET modeling. In [4], the I_{ds}-V_{ds}, I_{ds}-V_{gs} characteristics and dynamic $R_{ds\text{-}on}$ behavior of e-mode GaNs are obtained using curve fitting from experimental data. An analytical model is applied with steady-state behavior with temperature dependency and dynamic response with varying input and output capacitances in [5]. A mode-by-mode analysis is investigated in [6] for estimating the switching losses under various parasitic effects using small-signal models. The false turn-on phenomenon its relationship with the applied V_{gs} voltage are investigated in [3]. Several methods have been proposed for the minimization of the reverse conduction losses such as using a schottky diode in parallel with the synchronous GaN transistor [3]. In this paper, a hybrid model is proposed for the investigation of steady-state dynamic behavior and the switching transients of e-mode GaN power FETs. The state trajectories of the device during the turn-on and turn-off periods are obtained. the active turn-on and passive turn-on characteristics of the device are investigated on a synchronous buck converter. the effect of varying device capacitances and parasitic inductances on these trajectories and their possible outcomes are studied.

II. GaN Modeling

There are several modeling techniques applied to power semiconductor devices as mentioned before. In this study, a hybrid model is proposed which is shown in Fig. 1. In this model, the drain-source characteristics is modeled by a dependent current source and a temperature dependent resistance which gives the steady state behavior of the device during forward and reverse conduction at different V_{gs} values. The analysis during switching transients will be located onto $I_{ds} - V_{ds}$ characteristics to show the regions where the device operates during these transient periods. The equations used for steady-state models are shown in Eqn. (1) and (2) for forward conduction and reverse conduction, respectively. These equations correspond to the I_{ds}-V_{ds} curves of the device and the dynamic $R_{ds\text{-}on}$, derived from the manufacturer's models. The first multiplier of the equations represents the trans-conductance of the device where V_{th} is the threshold voltage. The second multiplier represents the region in which the device is operating; i.e., active region or ohmic region. R_t represents the temperature dependency of $R_{ds\text{-}on}$ in the model given in Fig. 1. Using this model, both steady-state and transient behavior of the conduction path are obtained. The model is used in MATLAB/Simulink with a single-leg converter (synchronous rectifier) to investigate the switching behavior as shown in Fig. 1. The nominal values of this test circuit used for the simulations are listed in Table 1.

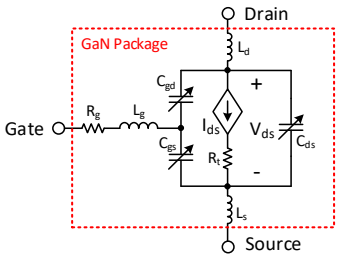


Fig.1(a) Proposed hybrid model of e-mode GaN power FET

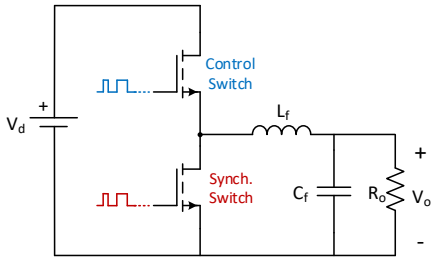
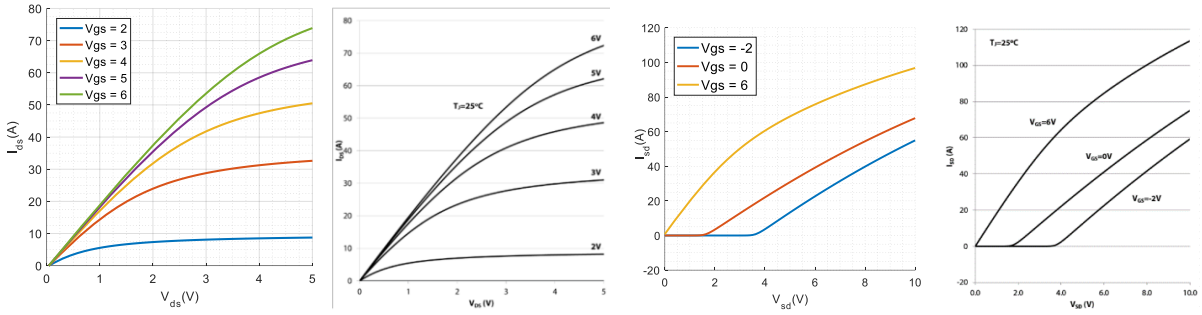


Fig. 1(b) The single leg converter used for the analysis

$$I_{ds} = K_1 * ln\left[1 + e^{\left(\frac{V_{gs}-V_{th}}{K_2}\right)}\right] * \frac{V_{ds}}{1 + \max\left(K_4 + K_5 * \left(V_{gs} + K_6\right), K_7\right) * V_{ds}} \quad (1)$$

$$I_{ds} = -K_1 * ln\left[1 + e^{\left(\frac{V_{gd}-V_{th}}{K_8}\right)}\right] * \frac{V_{sd}}{1 + \max\left(K_4 + K_5 * \left(V_{gd} + K_9\right), K_7\right) * V_{sd}} \quad (2)$$

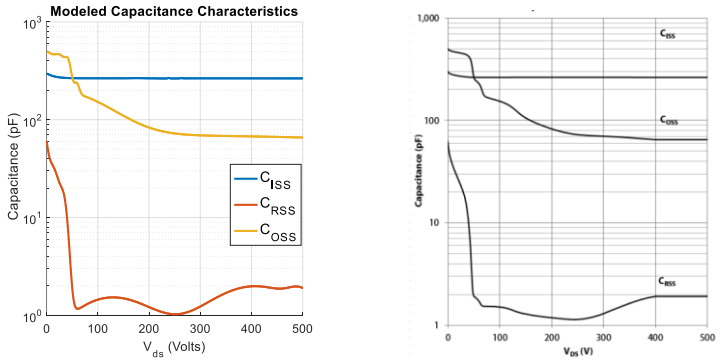
To show the accuracy of the steady state models, I_{ds}-V_{ds} characteristics of the selected device (GS66508B from GaN Systems) at different applied V_{gs} is obtained in both forward and reverse conduction regions at 25 ^{0}C, and plotted side-by-side with the actual characteristics given in the datasheet of the selected device [7] in Fig. 2. As shown, the reverse conduction behavior is highly dependent on the applied gate voltage, and shows a different behavior at negative gate voltage. In free-wheeling modes, this should make no difference since the applied gate voltage is positive. However, during dead-time periods, a negative gate voltage is applied increasing the loss, which makes the optimization of the negative gate voltage and dead-time duration very critical.



(a) Forward conduction (model) (b) Forward conduction (actual) (c) Reverse conduction (model) (d) Reverse conduction (actual)

Fig.2. Steady-state characteristics of GS66508B obtained by the proposed model and the actual characteristics [7]

The second critical part of the model includes the capacitances which determine the transient behavior of the device during switching operation as shown in Fig. 1. Although the values of these capacitances are usually given in the datasheets at rated voltages, that kind of a model will not be accurate as they are dependent on voltage. Therefore, it may change the behavior of the device during turn-on and turn-off periods, and should be taken into account. In this study, these variable capacitances are modeled using curve fitting obtained from the datasheet, and the resulting characteristics is shown in Fig. 3 [7].



(a) Model (b) Datasheet

Fig.3. Modeling of the capacitances using curve fitting

III. Switching Behavior of GaN

For better understanding of the switching behavior of e-mode GaNs, the turn-on and turn-off behavior of the selected device is investigated step-by-step using three models:

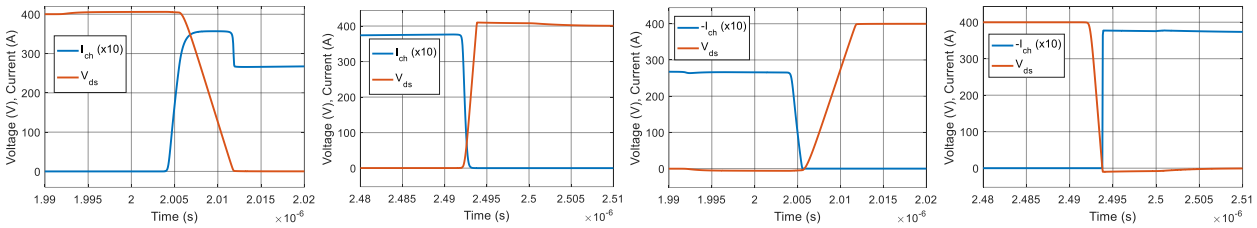
1) The simplest model with constant capacitances and without parasitic inductances,
2) The model with variable capacitances and without parasitic inductances,
3) The most practical model with variable capacitances and without parasitic inductances.

The nominal values of this test circuit used for the simulations are listed in Table 1, along with the device datasheet parameters used.

Table 1. The parameters used for the test circuit in MATLAB/Simulink

Input voltage (V_d)	400 V	Gate parasitic inductance (L_g)	1.0 nH	Dead-time (t_{dead})	10 ns
Output voltage (V_o)	200 V	Internal gate resistance (R_g)	1.5 Ω	Filter inductance (L_f)	10 µH
Output power (P_o)	3 kW	Turn-on gate resistance ($R_{G\text{-}ON}$)	20 Ω	Filter capacitance (C_f)	220 nF
Applied gate voltage (V_{gs})	-3V/+6V	Turn-off gate resistance ($R_{G\text{-}OFF}$)	5 Ω	Drain/source inductances (L_d/L_s)	0.9 nH

For simplicity, the control switch is going to be labeled as "Top Switch" and the synchronous switch is going to be labeled as "Bottom Switch" from now on, in the synchronous buck converter. For the simplest model described above, turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. 5.

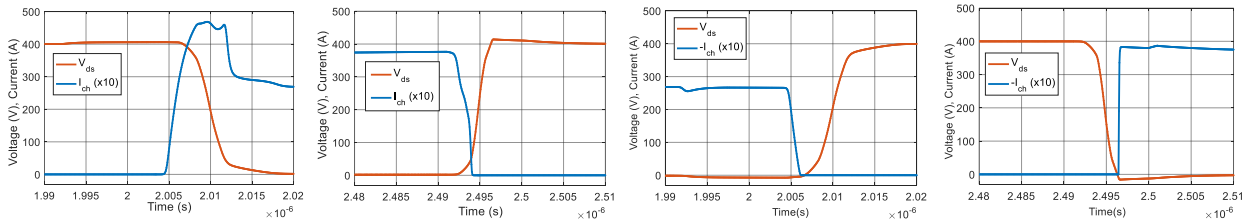


(a) Top switch turn-on (b) Top switch turn-off (c) Bottom switch turn-off (d) Bottom switch turn-on

Fig. 4. Switching characteristics in time domain obtained using the simplest model

Rather than giving the drain-source current, the channel current is preferred to show the device characteristic better. For transient periods, since the parasitic capacitors' voltages increase or decrease, their currents affect the drain-source current which overshadows device characteristic. As shown in simplest model, Figure 4(a), when the Top Switch is being turned on, the channel current makes an overshoot for two reasons. One of them is that since Bottom Switch stops conducting, C_{OSS} (=C_{gd} +C_{ds}) of the Bottom Switch requires to be charged and secondly, since C_{OSS} of the Top Switch is discharged, it causes current flow through the channel of Top Switch. Additionally, even though it seems soft switching is applied on Bottom Switch, actually it is not because C_{OSS} of the Bottom Switch is charged or discharged during transient periods and it would be seen if the current was I_{DS} instead of channel current. Note that the main characteristics observed in simplest model are important to understand GaN behavior because in complicated models even though these characteristics exist it might be hard to catch them among the oscillations.

In the next step, the capacitances values which were kept constant at their rated values previously are treated as variable capacitances using the capacitance models presented in Section II. As shown in Figure 3, the capacitances change with respect to the applied drain-source voltage. Contrary to C_{ISS}, there are significant changes in C_{OSS} and C_{RSS}. The turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. 5.

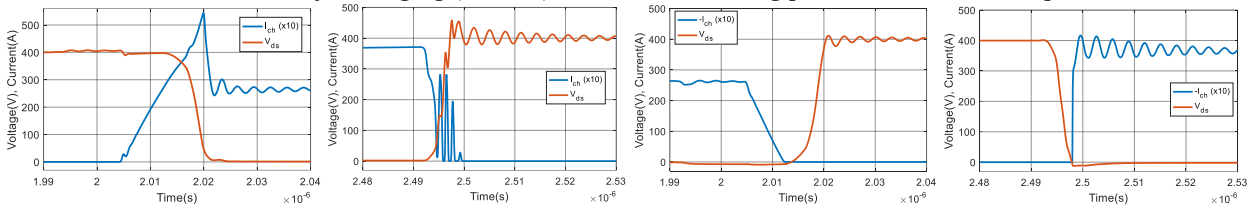


(a) Top switch turn-on (b) Top switch turn-off (c) Bottom switch turn-off (d) Bottom switch turn-on

Fig. 5. Switching characteristics in time domain obtained using variable capacitance model

In the variable-capacitance model it is observed that the overshoot in Top Switch channel current increased because for lower drain-source voltages, C_{OSS} is greater which results in higher current flow under similar voltage change in time. Moreover, for all transient periods given in Figure 5, it is observed that the voltage changes are smoother which makes the model more realistic. Plus, those different change rates of voltage affect the channel current and that is why small dips and peaks are observed on current waveforms.

Finally, to see the effect of the oscillations created by the LC resonance paths, the parasitic inductances are added to the model which are caused by Packaging (internal), Busbars, conducting parts on the Dc side, Capacitor ESLs etc…

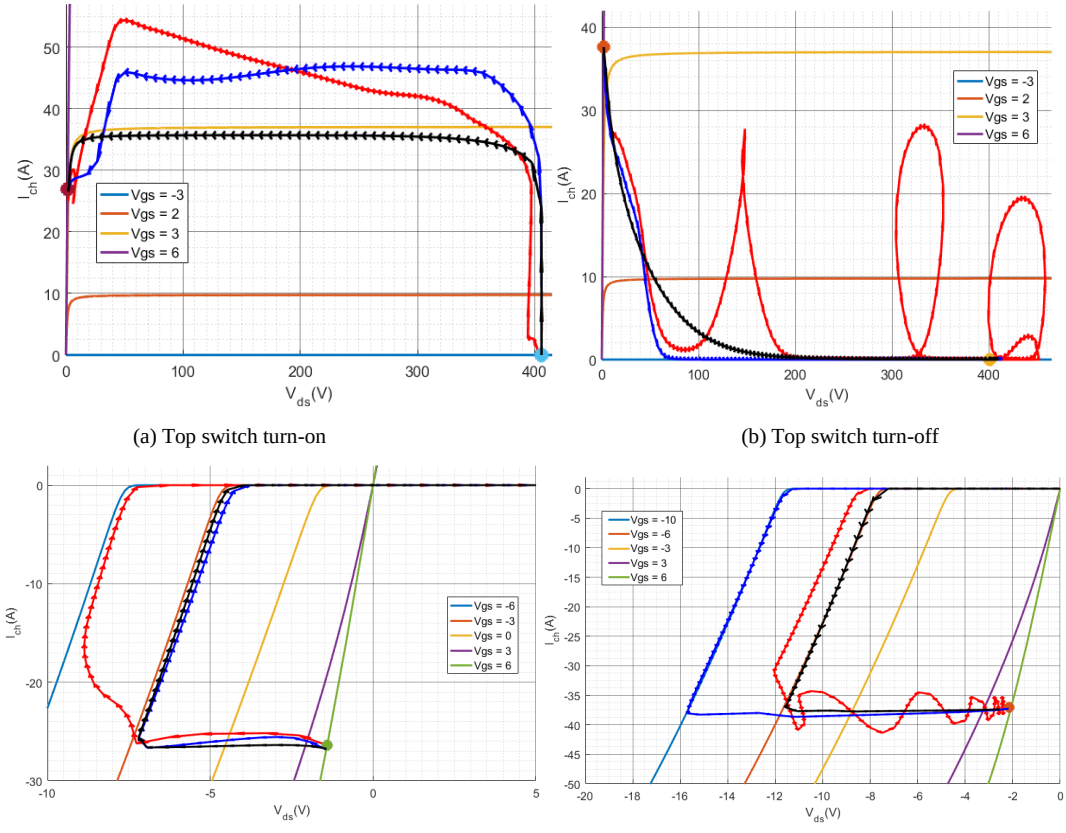


(a) Top switch turn-on (b) Top switch turn-off (c) Bottom switch turn-off (d) Bottom switch turn-on

Fig. 6. Switching characteristics in time domain obtained using the model with parasitics

In the most complicated model in which all parasitic effects are included, the oscillations started to be observed due to energy transfer between parasitic capacitances and inductors. During the turn-on period for Top Switch, the channel current increases continuously because C_{OSS} of the Top Switch is being discharged. With the parasitic inductors the change rate of the voltage on the C_{OSS} is not constant which is resulting inconstant current flow through the channel on the contrary of variable-capacitance model. On the other hand, during the turn-off period for Top Switch, huge oscillations are observed on channel current due to again Top Switch's C_{OSS} charging and discharging. Note that those oscillations observed on I_{DS} are not high as much as channel current because the charging and discharging current flows are not reflected directly on drain-source current, that is why those oscillations are not observed on oscilloscopes. However, to follow device state closely, the channel current needs to be investigated.

For a better visualization of these transients, the I_{ch}, V_{ds} paths that the top and bottom switches follow during turn-on and turn-off times are also obtained as state trajectories and shown in Fig.6. These trajectories are plotted on the device steady state current-voltage characteristic as given in Fig.2



(a) Top switch turn-on (b) Top switch turn-off

(c) Bottom switch turn-off (d) Bottom switch turn-on

Fig 7. Switching characteristics as state trajectories (obtained using all the models)

Each trajectory on the graphs represents a model. Black, blue and red trajectories show the simplest model, variable-capacitance model and the most practical model trajectory respectively in all graphs in Figure 7. When we look at the trajectory plotted during the turn-on period of Top Switch, it is easy to see the Miller Plateau where the voltage drops and current stays constant ideally. During the turn-off period of Top Switch, the oscillations on current are also observed on trajectory and as seen on the graph, actually the gate-source voltage also oscillates during that period. Moreover, an interesting result seen on the trajectories on Bottom Switch turn-on graph which is when the inductors are not modeled but the capacitances are variable the gate-source voltage drops until -10 Volts which is the limit of minimum gate-source voltage. However, when the inductors are included too, it gives more realistic results and it is seen that gate-source voltage does not reach risky values. On the contrary, for turn-off trajectories of Bottom Switch, the gate-source voltage drops to nearly -6V for most practical model. As a result, including inductors in model important to investigate operation's safety.

Furthermore, focusing on the trajectories given in Bottom Switch turn-off graph, it is seen that the load current completely flows through the channel of Bottom Switch before positive gate-source voltage is applied. This conduction period is called as dead-time as known. In IGBT and MOSFETs, during the reverse conduction current flows through the body diode which is not the case for GaN. In GaN, body diode does not exist and the reverse current flows through the device channel. Therefore, when the top switch is being turned off, the constant load current flows through the channel of the Bottom Switch in reverse direction in dead-time period. The positive gate-source voltage is applied just to minimize V_{SD} to obtain minimum loss. Thus, it can be deduced that applied gate-source voltage is not important for turning on the Bottom Switch and it is being turned on when the Top Switch stops conducting. To simplify the issue and to make the concept more understandable, the rise of the current in Bottom Switch channel is called as active turn-on and applying positive gate-source voltage is called as passive turn-on. The key difference is that in active turn-on device starts to conduct load current and in passive turn-on the current is not changed but the loss is decreased. This distinction is not required for IGBTs and MOSFETs because during dead-time current flows through the body diode and when the gate-source voltage is applied the current commutates from diode to channel. However, it is important for GaN devices because it has no diode and applying positive gate-source voltage changes nothing about current in reverse conduction. Similarly, for the turn-off period of Bottom Switch, in dead-time negative gate-source voltage is applied which does not affect current. The current starts to decrease when the top switch is turned on. Therefore, applying negative gate-source voltage should be called as passive turn-off and the device is actually turned-off actively when the top current starts conducting.

IV. Conclusions

In this paper, turn-on and turn-off characteristics of GaN device are investigated step by step including different parasitic effects. Understanding the effect of the parasitics on turn-on and turn-off characteristics of GaN is important to understand GaN behavior and operating safely. For this purpose, the channel current and channel voltage, which represent device characteristic better, are investigated on a synchronous buck converter circuit using accurately modeled GaN device. The simulation results belonging to channel current and voltage waveforms are shared and their trajectories are represented on the steady state $I_{DS} - V_{DS}$ graphs in order to make the characteristics clearer.

In the final paper, those results will be enriched with more simulation results and will be verified with experimental results. In experimental results, GS66508B-EVBDB daughter board will be used. In finalized paper it is aimed to give more detailed explanation of turn-on and turn-off characteristics of GaN.

V. References

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