Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors

Abstract: In this paper, turn-on and turn-off switching behavior of 650V enhancement-mode GaN power FETs are investigated. A developed model is used dedicated to GS66508B device of GaN Systems. Using this model, the current-voltage characteristics of the device during switching transients are analyzed both with and without the effects of parasitic components.

I. Introduction

Wide band-gap power semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming more widespread each day, thanks to their superior efficiency and power density performance over Silicon (Si) based power semiconductor devices. Although current GaN devices are available at lower voltage ($< 650V$) and lower current ($< 50A$) ratings compared to SiC, they have become an attractive solution in several power converter applications. Several enhancement-mode (e-mode) GaN transistors are now commercially available up to 650 V ratings, which are normally-off devices suitable for voltage source converter (VSC) applications and have better performance than cascade devices in terms of switching speed, $R_{ds\text{-}on}$ and reverse conduction behavior. The most common e-mode devices are EPC's GaN's with ratings up to 100V and 30A, and GaN Systems' GaNs with ratings up to 650V and 60 A [1]. E-mode GaN FETs have low specific on-state resistance due to their high breakdown field resulting in thinner drift regions as well as high electron mobility. They can be manufactured with smaller size so that the parasitic capacitances and inductances due to packaging are lower resulting in faster switching performance [1]. Switching losses of these devices are much lower compared to their Si counterparts, and this allows them to be used in high frequency applications where passive filter components such as inductors and capacitors can be made smaller.

Investigation of switching behavior of GaN power FETs is important for several reasons. First of all, high switching speed of GaNs make them more vulnerable to *di/dt* and *dv/dt* effects and parasitic components on not only the power stage, but also gate drive circuit layout. Second, e-mode GaNs have reverse conduction ability without an intrinsic or external diode, called self-commutated reverse conduction (SCRC) [2]. They act as a resistor just like MOSFETs in forward conduction; however, their behavior in reverse conduction is somewhat different than forward conduction, varying with the applied gate-source voltage. Therefore, turn-on and turn-off characteristics are dependent on applied gate-source voltage. Usually, a negative gate voltage is required due to dv/dt effect which may trigger false turn-on and eventually short circuit of the converter [3], which results in a much higher on-state voltage when the device is not actively turn-on during dead-band periods. Another reason is that, their switching loss and reverse conduction loss model is not the same as Si MOSFETs, and should be paid attention especially very high frequency converter applications. Although dead-band period and its effects on power loss calculations are usually ignored in other applications, it may affect the converter efficiency significantly in e-mode GaN applications [3].

Several studies have been published regarding e-mode GaN FET modeling, especially in the last few years. In [4], the I_{ds}-V_{ds}, I_{ds}-V_{gs} characteristics and dynamic $R_{ds\text{-}on}$ behavior of e-mode GaNs are obtained using curve fitting from experimental data and without an analytical model. 100V devices from EPC are used in a model which includes steady-state behavior with temperature dependency and dynamic response with varying input and output capacitance models using analytical models in [5]. A mode-by-mode analysis in the time-domain is investigated in [6] for estimating the switching losses under various parasitic effects using the small-signal model in each time interval. Several power semiconductor device modeling methods are discussed and the most suitable type for power electronics studies is presented in [7], using an inverter application. The false turn-on phenomenon its relationship with the applied V_{gs} voltage are investigated in [3]. Several methods haven been proposed for the minimization of the reverse conduction losses such as using a schottky diode in parallel with the synchronous GaN transistor [3], [8]. A frequency domain analysis is applied for modeling the effects of parasitic components during switching transients and methods have been proposed for minimizing the high frequency oscillations due to these parasitics [9].

In this paper, a hybrid model is proposed for the investigation of steady-state dynamic behavior and the switching transients of e-mode GaN power FETs. The state trajectories of the device during the turn-on and turn-off periods are obtained. the active turn-on and passive turn-on characteristics of the device are investigated on a synchronous buck converter. the effect of varying device capacitances and parasitic inductances on these trajectories and their possible outcomes are studied.

II. GaN Modeling

There are several modeling techniques applied to power semiconductor devices as mentioned before. In this study, a hybrid model is proposed which is shown in Fig. 1. In this model, the drain-source characteristics is modeled by a dependent current source and a temperature dependent resistance which gives the steady state behavior of the device during forward and reverse conduction at different gate-to-source voltages (V_{gs}). The analysis during switching transients will be located onto this drain-to-source current (I_{ds}) – drain-to-source voltage (V_{ds}) characteristics to show the regions where the device operates during these transient periods.

The equations used for steady-state models are shown in (1) and (2) for forward conduction and reverse conduction, respectively. These equations correspond to the I_{ds}-V_{ds} curves of the device and the dynamic R_{ds-on}, derived from the manufacturer's models. The first part of the analytical model represents the trans conductance of the device where V_{th} is the threshold voltage. the second part represents the region in which the device is operating; i.e., linear region or ohmic region. The resistance, R_t represents the temperature dependency of the dynamic R_{ds-on} in the model given in Fig. 1. Using this model, both steady-state and transient behavior of the drain-source conduction path are modeled.
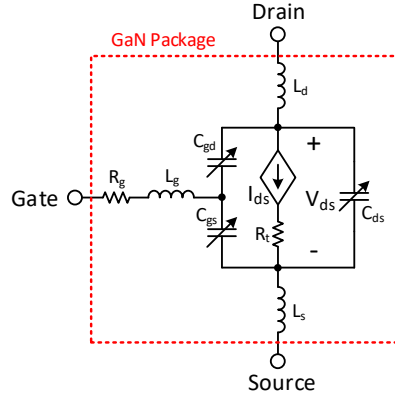

Fig.1. Proposed hybrid model of e-mode GaN power FET

$$I_{ds} = K_1 * ln\left[1 + e^{\left(\frac{V_{gs}-V_{th}}{K_2}\right)}\right] * \frac{V_{ds}}{1 + max\left(K_4 + K_5 * \left(V_{gs} + K_6\right), K_7\right) * V_{ds}} \tag{1}$$

$$I_{ds} = -K_1 * ln\left[1 + e^{\left(\frac{V_{gd}-V_{th}}{K_8}\right)}\right] * \frac{V_{sd}}{1 + max\left(K_4 + K_5 * \left(V_{gd} + K_9\right), K_7\right) * V_{sd}} \tag{2}$$

To show the accuracy of the steady state models, I_{ds}-V_{ds} characteristics of the selected device (GS66508B from GaN Systems) at different applied V_{gs} is obtained in both forward and reverse conduction regions at 25 ^{0}C, and plotted side-by-side with the actual characteristics given in the datasheet of the selected device [10] in Fig. 2. As shown, the reverse conduction behavior is highly dependent on the applied gate voltage, and shows a diode-like behavior rather than a fully-resistive behavior when a negative V_{gs} is applied. In free-wheeling modes, this should make no difference as the applied gate voltage is positive. On the other hand, during dead-time periods, a negative voltage is usually applied increasing the loss, which makes the optimization of the negative gate voltage and dead-time duration very critical.

(a) Forward conduction (model)　　(b) Forward conduction (actual)　　(c) Reverse conduction (model)　　(d) Reverse conduction (actual)
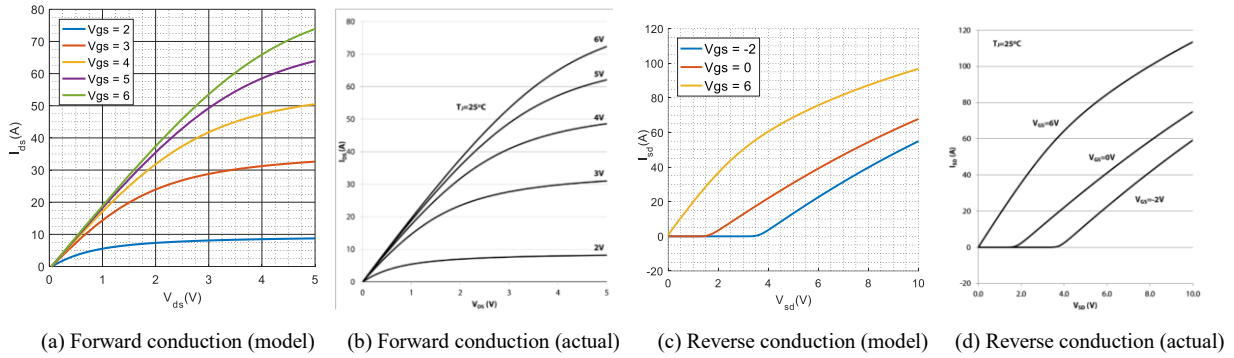
Fig.2. Steady-state characteristics of GS66508B obtained by the proposed model and the actual characteristics [10]

The second critical part of the model includes the capacitances which determine the transient behavior of the device during switching operation as shown in Fig. 1. These capacitances are gate-to-source capacitance (C_{gs}) which determines the xxx time, gate-drain capacitance (C_{gd}) which is effective during miller-pleatau region, and drain-to-source capacitance (Cds) which determines the xxx time. Although the values of these capacitances are usually given in the datasheets at rated voltages, that kind of a model will not be accurate as they are dependent on voltage, especially C_{ds}. Therefore, although in some kinds of analysis, such as loss characterization, this effect may not be significant, it may change the behavior of the device during turn-on and turn-off periods, and should be taken into account. In this study, these variable capacitances are modeled using curve fitting obtained from the datasheet, and the resulting characteristics is shown in Fig. 3.
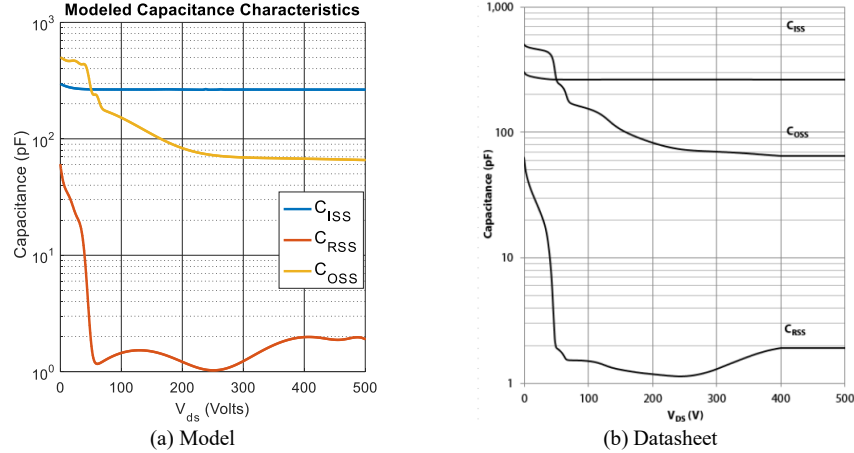
(a) Model   (b) Datasheet
Fig.3. Modeling of the capacitances using curve fitting

III.   Switching Behavior of GaN

For better understanding of the switching behavior of e-mode GaNs, the turn-on and turn-off behavior of the selected device is investigated step-by-step using three models:

- The simplest model with constant capacitances and without parasitic inductances,
- The model with variable capacitances and without parasitic inductances,
- The most practical model with variable capacitances and without parasitic inductances.

All these models are used in MATLAB/Simulink simulation environment. A single-leg converter (a half-bridge module, or a synchronous rectifier) is utilized for the switching behavior analysis, with an LC output filter and a resistive load as shown in Fig. 4. The nominal values of this test circuit used for the simulations are listed in Table 1, along with the device datasheet parameters used.
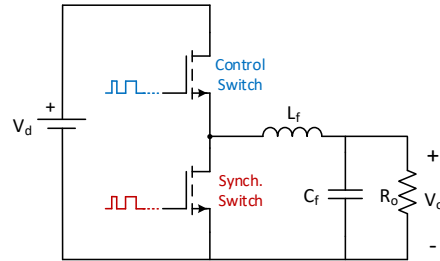

Fig. 4. The single leg converter used for the analysis

Table 1. The parameters used for the test circuit in MATLAB/Simulink

Input voltage (V_d)	X V	Applied gate voltage (V_{gs})	-3V/+6V	Deadtime (t_{dead})	X ns
Output voltage (V_o)	X V	Internal gate resistance (R_g)	X Ω	Filter inductance (L_f)	X mH
Output power (P_o)	X W	Turn-on gate resistance (R_{G-ON})	X Ω	Filter capacitance (R_f)	X mF
Internal gate resistance (R_g)	X Ω	Turn-off gate resistance (R_{G-OFF})	X Ω	??	

For simplicity, the control switch is going to be labeled as "Top Switch" and the synchronous switch is going to be labeled as "Bottom Switch" from now on, in the synchronous buck converter. For the simplest model described above, turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. 5.
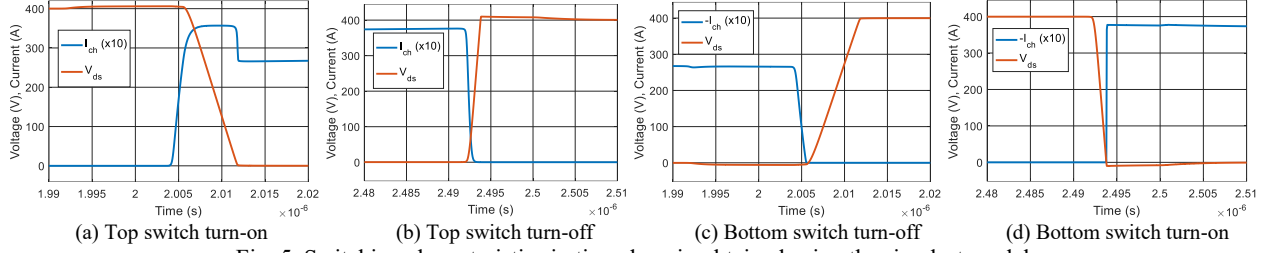

(a) Top switch turn-on   (b) Top switch turn-off   (c) Bottom switch turn-off   (d) Bottom switch turn-on

Fig. 5. Switching characteristics in time domain obtained using the simplest model

For a better visualization of these transients, the I_{ds}, V_{ds} paths that the top and bottom switches follow during turn-on and turn-off times are also obtained as state trajectories and shown in Fig.6.

(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off

(d) bottom switch turn-off
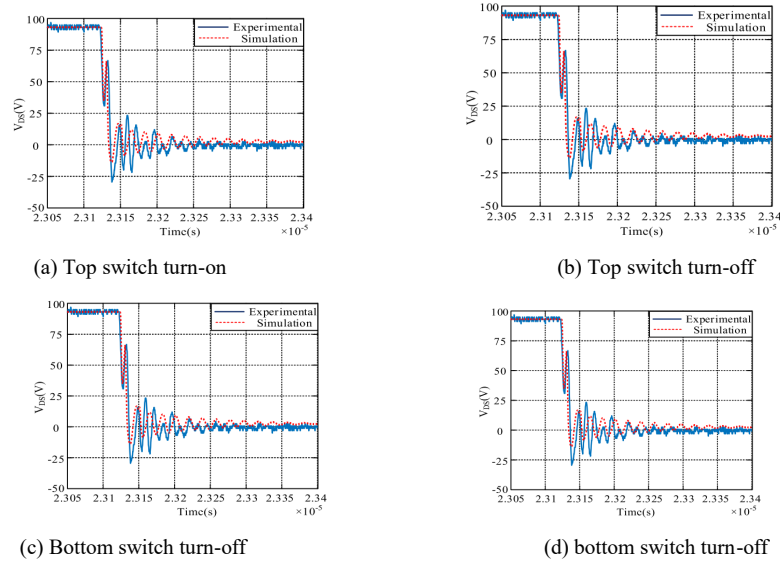
Fig Z. Switching characteristics as state trajectories (obtained using the simplest model)

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IV. Effect of Parasitic Elements

In the next step, the capacitances values which were kept constant at their rated values previously are treated as variable capacitances using the capacitance models presented in Section II. Hangi kapasitör daha etkili ve ne kadar değişiyor bahset. The turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. Y:
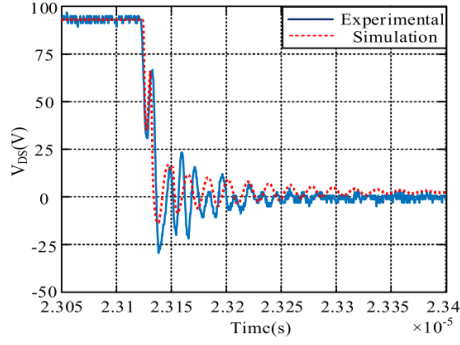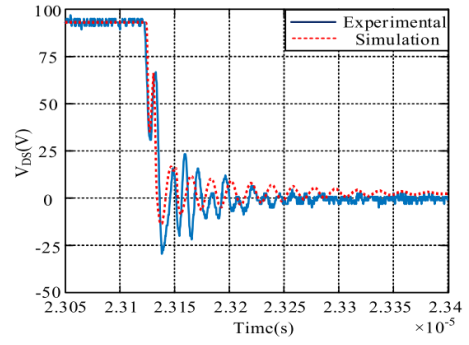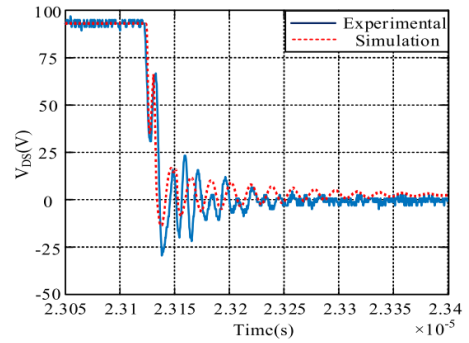
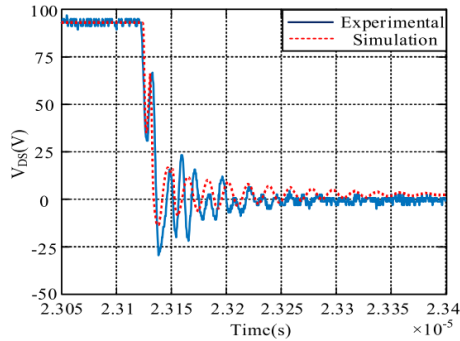(a) Top switch turn-on

(b) Top switch turn-off
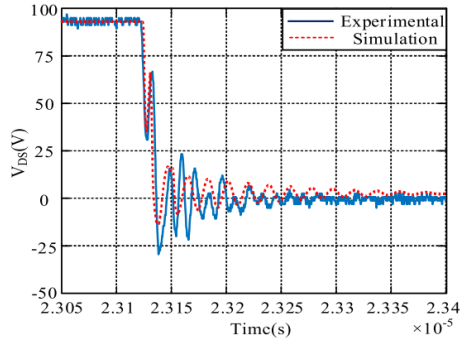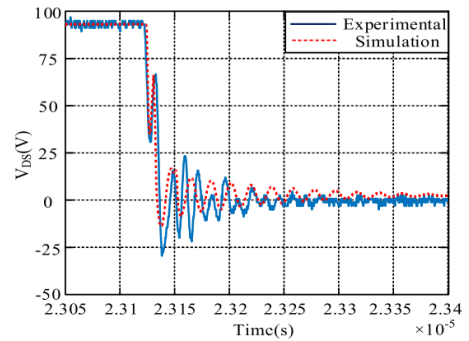

(c) Bottom switch turn-off

(d) bottom switch turn-off

Fig. Y. Switching characteristics against time (obtained using variable capacitance model)
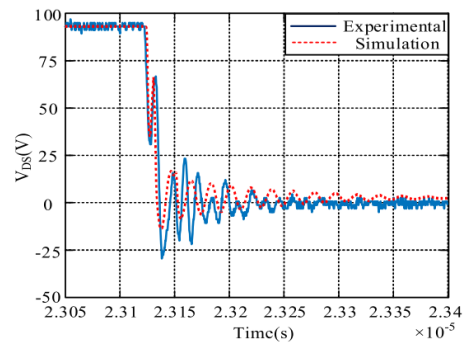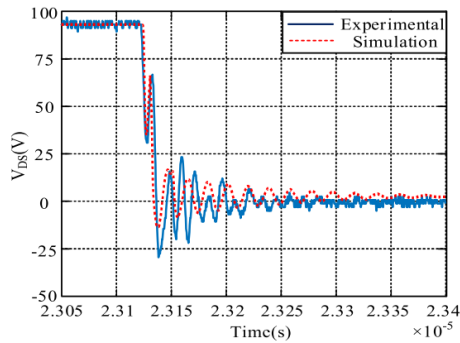
For a better visualization of these transients, the Ids, Vds paths that the top and bottom switches follow during turn-on and turn-off times are also obtained as state trajectories and shown in Fig. Z.

(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off   (d) bottom switch turn-off

Fig Z. Switching characteristics as state trajectories (obtained using variable capacitance model)

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Finally, to see the effect of the oscillations created by the LC resonance paths, the parasitic inductances are added to the model which are caused by:

- Packaging (internal)
- Busbars, conducting parts on the Dc side
- Capacitor ESLs etc…
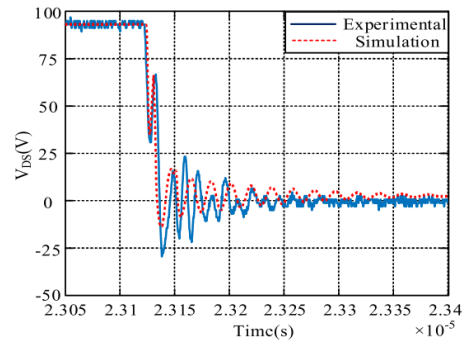
The investigation of these effects is important because:

- Buraya 3-5 madde sırf L'den gelebilecek sıkıntıları ekleyelim (overvoltage gibi)….

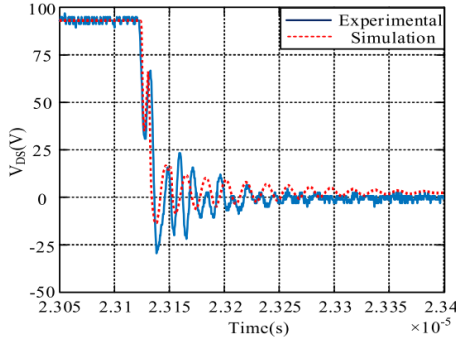The values are taken from the datasheet values [ref].

The turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. Y:
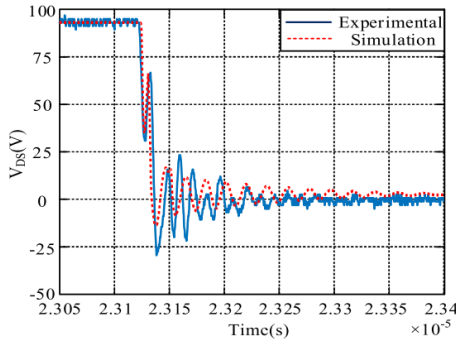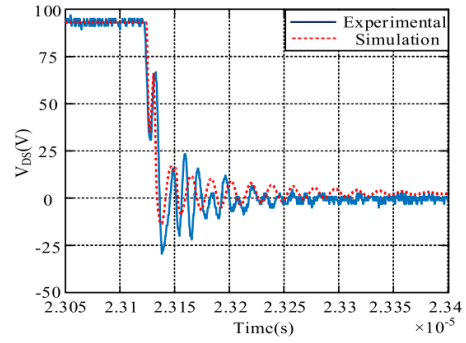

(a) Top switch turn-on   (b) Top switch turn-off
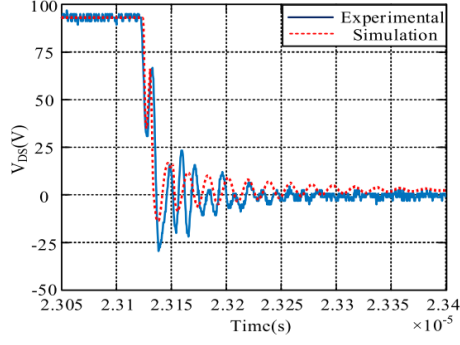

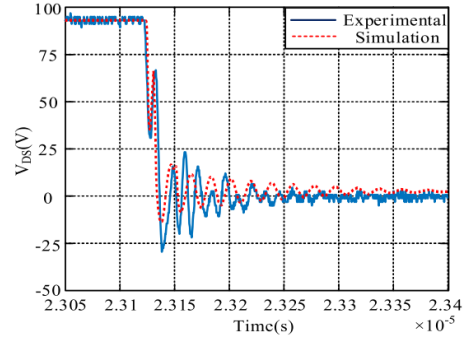(c) Bottom switch turn-off   (d) bottom switch turn-off

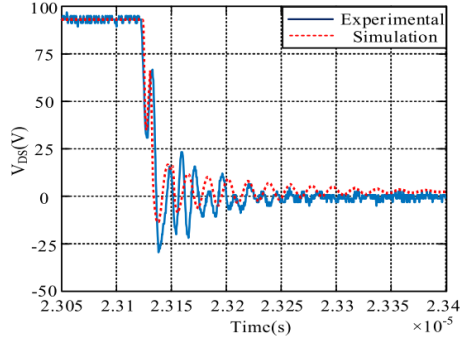Fig. Y. Switching characteristics against time (obtained using practical model)

For a better visualization of these transients, the Ids, Vds paths that the top and bottom switches follow during turn-on and turn-off times are also obtained as state trajectories and shown in Fig. Z.
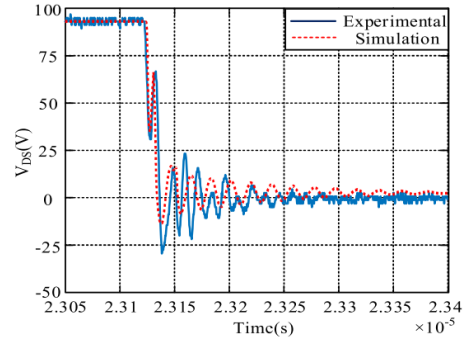
(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off

(d) bottom switch turn-off

Fig Z. Switching characteristics as state trajectories (obtained using practical model)

Yorumla

V. Conclusions

Hepsini toplayalım

Konu, objective

Problem, motivasyon

Çözüm, method

Beklentiler, çıktılar, çıkarımlar

In the final paper (çok yer kalmadı ama…..)

VI. References

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